4. Theory of Operation

4.1 Logic Section

4.1.1 DC Distribution and Regulation Part

Energizing the battery and pressing "END" key on the phone screen of the display shorts "VBATT" and "ON_SW", and U811 and U808 "+2.8V" regulator are enabled through D801, resulting in supplying power for U802 MSM main system processor and other digital circuits. At the same time, the reset output of U811, is applied to Q812 which are (Power On) reset circuits and "RESET/" and "RESIN/" signals are created to reset U802 processor, U804 memory. On the other hand, the battery voltage inputted as "ON_SW" turns ON Q801 to output "Low" to "ON_SW_SENSE/" port of MSM3000. MSM3000 receives this signal and recognizes that "END" (Power) key is pressed and maintains the power through D801 by outputting "High" through PS_HOLD signal.
U811 +2.8V power is used for MSM3000, U804 Memory, digital section on U503 IFR3000, U514 IFT3000, U807 PCM Audio Codec and other digital circuits.
U808 +2.8 AV power is supplied for Audio, the analog section on U807 STw5093, and other analog circuits. U502 supplies +2.8V power for RF Rx; U505 for VC-TXCO(System Timing Reference Clock), PLL, and VCO; U520 for RF Tx IF & Mixer. Power for RF Tx Power Amplifier is supplied directly from the battery.

4.1.2 Logic Part

4.1.2.1 Summary

The logic part is composed of MSM3000 ARM-7 processor core-combined CDMA ASIC, flash ROM & SRAM, and EEPROM. The MSM3000 is CDMA ASIC chipset which is implemented for system control and baseband digital signal processing on the terminal equipment. In order for MSM3000 to operate, CHIPx8, which is a signal transmitted from TCXO Clock and IFR3000, and external resonator are necessary. These generate the CPU clock built in MSM3000.

Major components used for the logic section are as follows:
1) MSM3000: U802, [ARM-7 processor core + CDMA signal processing + EVRC] ASIC
2) Flash ROM & SRAM: U804, 16 Mbit flash memory & 2 Mbit static RAM
3) EEPROM: U801, 256 kbit serial-interface EEPROM

4.1.2.2 Baseband Digital Signal Processing

MSM3000(Mobile Station Modem) is a core device for CDMA mode, containing ARM-7 CPU core. MSM3000 is composed of a single chip and of 196 pin PBGA package type, and the features and specifications of the clock are recapped as follows:
1) It interfaces IFR3000 & IFT3000 on RF section directly in CDMA mode.
2) It contains internal Vocoder which has even EVRC feature.
3) It is designed to interface RF section which makes power control circuit.
4) It has a built-in ARM-7 MicroProcessor Core.
5) It has a built-in watch dog timer.

6) It has a 64 byte FIFO(First Input First Output) serial data port.
7) It provides 31 GPIO(General Purpose Input Output) ports.
8) It provides 10 Interrupt Ports. (Of these, 5 ports are used to interface the key pad.)
9) It supports external DTMF ringer circuit.
10) It supports 8/16 bits external SRAM and EEPROM.
11) It has chip select feature for the external ROM, RAM, and EEPROM.
12) It provides A0-A19 address buses and AD0-Ad15 data buses.

The configuration by feature of the inside of MSM3000 is as follows:

1. Microprocessor Core

MSM3000 has a built-in ARM-7 MicroProcessor Core, and this MicroProcessor contains Interrupt Controller, Timer/Counter, and DMA Controller. In addition, 16 bit datapath is included, and addressing up to 1 Mbyte can be performed and I/O space can be extended up to 1Mbyte. Although it is necessary to provide Clock from the outside in order to operate MicroProcessor, this system provides Clock by using 27 MHz resonator.

2. Input Clock

1) CPU Clock(27 MHz):
This becomes the Clock needed for MicroProcessor built in MSM3000 to operate.

2) TCXO(19.68 MHz) Clock:
This is the reference clock for controlling EVRC Vocoder and SLEEP mode, and it is also the whole system reference clock.

3) CHIPx8(9.8304 MHz):
This is a Clock derived from 19.68 MHz TCXO Clock which is supported from IFR3000 of RF section and becomes the Timing Reference Clock for CDMA signal processing.

3. CDMA Core

This is the part for processing CDMA signals in CDMA mode, and it is composed of Demodulator, Modulator, and Decoder.

1) Demodulator:
This is composed of 4 demodulating fingers, 1 searcher engine, deinterleaver, time tracking part, and symbol combiner, and it implements such functions as forward link CDMA signal processing and timing acquisition.

2) Modulator:
This implements such functions as the encoding and interleaving of CDMA signal on reverse link, controlling the operation of IFT3000 on RF section in CDMA mode, and performing the automatic monitoring the status of IFT3000.

3) Decoder:

This implements Viterbi decoding on CDMA forward link.

CDMA Core and IFR3000/IFT3000 Interface

1) Transmitter:

8bit TX I and Q data are inputted in D/A converter inside IFT3000, and I data and Q data are stored in I DAC on rising edge of TX clock and Q DAC on falling edge of of TX clock, respectively.

TX_CLK+ and TX_CLK- become the reference clock for 8 bit D/A converter inside IFT3000 at TX.

2) Receiver:

Components such as analog I and Q baseband inside IFR3000 are converted to digital signals by the two and same 4 bit flash A/D converter. CDMA A/D converter is outputted as a new digital value at falling edge of CHIPx8(9.8304 MHz) which is the reference clock and inputted into MSM3000.

4. RF Interface

This interfaces RF section to control power amplifier, TxLO buffer amplifier, VC-TCXO, and AGC-end on the transmit/receive paths.

1) Transmitter Interface:

This sends TX_ADJ signal to TxAGC amplifier to adjust transmit power level; it sends PA_ON signal to control power amplifier.

2) Receiver Interface:

This sends RX_AGC_ADJ signal to Rx AGC Amplifier to adjust receive path gain; it sends TRK_LO_ADJ signal to RF section to control TCXO frequency automatically(AFC).

5. General Purpose ADC Support

This is connected to the inside of IFT3000 of RF section and accepts analog values of received signal level, battery level, and temperature level to monitor, recognize, and display them.

ADC_ENABLE signal needed for the operation of ADC inside IFT3000 is recognized at MSM3000, and ADC_CLK and ADC_DATA signal needed to control ADC are sent to MSM3000 from IFT3000.

6. UART(Universal Asynchronous Receiver & Transmitter) Interface with PDA System Main Processor

7. General Purpose Interface

This includes 31 GPIO(General Purpose Input Output) ports, 5 key sense ports, 2 PDM source ports, M/N counter, and 5 interrupt ports, and it is an I/O port for the controlling of external devices.

8. Vocoder Core

This implements EVRC function for aural signal on the basis of QCELP Vocoder Algorithm in CDMA mode. Vocoder Core interfaces the digital FM core and microProcessor inside MSM3000 and external CODEC.

Interface with external CODEC supports PCM_CLK(2.048MHz) and PCM_SYNC(8KHz) for CODEC. Voice PCM data inputted into PCM_DIN is compressed by QCELP Speech Algorithm in CDMA mode, while PCM data inputted into Vocoder Core from CDMA Core is outputted as PCM_DOUT.

9. Power Down Control Section

1) Idle Mode Control:

If IDEL/Signal changes to 'Low', transmitter section is disabled.

2) Sleep Mode Control:

If IDEL/ and SLEEP/ signals change to 'Low', all the sections except VC-TCXO circuit are disabled.

3) Receiver & Transmitter Mode Control:

If IDEL/ and SLEEP/ signals change to 'High', all the sections are enabled to implement the operation for transmission and reception.

Modes of Operation and Clock Availability

Mode	SLEEP/	IDLE/	CHIPX8	TCXO/4
SLEEP	L	X	Off	On
IDLE	H	L	On	On
RX/TX	H	H	On	On

4.1.2.3 Memory Part

Memory is composed of flash ROM & SRAM and EEPROM.

1. Flash ROM & Static RAM

Flash ROM and SRAM use a single IC, and the capacity of flash ROM is 16 Mbit(2 MByte). Main programs(Call Processing, User Interface, and Diagnostic Task) and additional programs(NAM Program and Test Program) are stored in this flash ROM. Consumers can download these programs through dealers even if their versions are upgraded in the future. SRAM's capacity is 2 Mbit(256 KByte) and stores system variables, stack of each task, data buffer.

2. EEPROM

The capacity of EEPROM is 256 KBit and stores ESN(Electronic Serial Number), NAM(Number Assignment Module) and other system parameters, phone numbers, audio levels, PDM to adjust transmit power levels, and its call processing related PDM values. In addition, Last PN Offset and PDM values in relation to RF temperature compensation are stored.

4.1.3 Speech Processor Part

1. Transmit Speech Processing

Aural signal inputted into the microphone is applied to PCM CODEC Filter via buffer-end inside CODEC IC. This PCM CODEC filter samples aural signals applied by receiving PCM_CLK(2.048 MHz) and PCM_SYNC(8 KHz) signals from MSM3000 and converts them to digital signals, and then applies them to PCM_DIN of MSM3000.

2. Receive Speech Processing

Digital signals outputted from PCM_DOUT of MSM3000 are converted to aural signals via D/A converter inside CODEC IC, subjected to volume adjustment though receiver filter, and then sent to audio amplifier. These aural signals are amplified by audio amplifier and outputted to receiver/speaker.

3. Ringer Sound Output to Buzzer

4.2 Radio Transceiver Section

4.2.1 DC Distribution and Regulation Part)

Battery voltage flows, in turn, to logic part and RF part via LDO(Low Drop-Out) regulators. In addition, this is designed to use several LDO regulators in order to supply power to each necessary part and to heighten efficiency. All parts use +2.8V.

+2.8V of U520 is used for transmitter part.

+2.8V of U502 is used for receiver part.

+2.8V of U505 is used for frequency synthesizer part and VC-TCXO.

4.2.2 Receiver Section

4.2.2.1 Summary

Receiver section occupies 869 MHz 894 MHz frequency band. It obtains IF frequency(85.38 MHz) from down converter which is 1st mixer. RF signal received from the antenna is applied to LNA through duplexer and amplified and applied to SAW filter, and then only necessary signals are sent to down converter which is 1st mixer. At this point, the down converter which is 1st mixer mixes RF signals with LO signals on frequency synthesizer part. The mixed 85.38 MHz IF signal is applied to SAW filter which is IF BPF, and only necessary signals are selected. 1st IF conversion gain is about 15dB. IF signal passes SAW filter which is IF BPF and then is induced to AGC amplifier, which is adjusted by PDM(Pulse Density Modulation) signal of MSM3000, according to the received signal strength level. This ACG amplifier is fitted to input sensitivity of IFR3000(Analog Baseband). The operation range of AGC is approximately 90dB(±45dB). Signal inputted to IFR3000 is downconverted at 2nd mixer to obtain baseband signal necessary for demodulation. 170.76 MHz VCO is oscillated to synthesize 2nd LO frequency and is demultiplied in two to apply 85.38 MHz 2nd LO. 2nd IF signal is divided into I and Q signals for baseband(Zero-IF, each of which is sent to A/D converter via Low Pass

Filter.

4.2.2.2 Receiver Part

1. Duplexer: F501

Duplexer is composed of Tx filter and Rx filter. It has an antenna port and is configured with dual structure for the division of transmission/reception paths. It also is composed of two filters; one is reception band filter that delivers signals received from the antenna, filtering it to 881.5±12.5 MHz frequency band and transmitting it to low noise amplifier; the other is transmission band filter that filters output signals of power amplifier to 836.5±12.5 MHz frequency band and transmits it to the antenna. The maximum insertion loss at reception band and transmission band is approximately 3dB, respectively.

2. LNA(Low Noise Amplifier): Q504

LNA minimizes noise of signals coming into the antenna feebly from the aerial antenna(base station) before amplifying them, and it has 1.5dB NF and 15dB gain.

3. RF BPF(Radio Frequency Band Pass Filter): F503

This filters only such signals with 881.5±12.5 MHz frequency band of reception frequency for cellular system terminal equipment and removes other signals and image components than reception frequency for terminal equipment. Insertion loss is maximum 3dB.

4. LO Buffer Amplifier: Q506

With Phase Lock being set between VCO and PLL IC, this amplifier inputs LO signal to LO port of Down Converter in optimal signal size and functions for Rx/Tx path isolation and VCO load isolation.

5. Down Converter(Mixer): U517

This down-converts RF signals amplified at LNA to 85.38 MHz IF signals. 85.38 MHz IF signals are made by the difference between band frequency of 881.5±12.5 MHz reception signal and band frequency of 1^{st} LO signal with 966.88±12.5 MHz. Conversion gain is 15dB.
And the CDMA/AMPS operation mode will be switched alternately corresponding to the logic status of the pin 7 of this IC applied from MSM3000 IC(U802). The operation mode is CDMA if this logic level is high, and the operation mode is AMPS if this logic level is low.

6. IF BPF(IF Band Pass Filter): F504 for CDMA, F502 for AMPS Mode

This reduces pressure of 85.38 MHz noise down-converted at 1^{st} mixer and extracts only essential signals corresponding to one channel. And also, it removes various kinds of image components generated at Down Converter. F504 has ±630 KHz pass bandwidth, and insertion loss is 11dB. F502 has ±15 KHz pass bandwidth, and insertion loss is 6dB.

7. IFR3000 = IF AGC + Rx 2^{nd} LO VCO + Analog Zero-IF Baseband + Digital Conversion

8. Thermistor: R504

As ambient environment or power amplifier temperature is changed, resistance value of thermistor also is changed, causing voltage distributed by R508, R509, and R504 to be changed. Temperature sensor is necessary to measure such changes by means of digital data and make soft compensation for change of RF analog circuit characteristics according to temperature. R508 and R509 are used in serial and parallel configuration in order to obtain linearity of temperature change by time.

4.2.3 Transmitter Section

4.2.3.1 Summary

Digital signal applied in 8 bit to IFT3000 uses TX_CLK+ and TX_CLK- as trigger and outputs I signal and Q signal sequentially, and each signal is sent to quadrature modulator via digital LPF. Quadrature modulator makes double-side band real spectrum that uses 130.38 MHz, in which complex signal of base bandwidth and 260.76 MHz VCO oscillant frequency are demultiplied in two, as carrier. MSM3000 counts from the received signal strength level(Open Loop Power Control) and generates PDM signals according to TX_AGC level suitable for the number of power control bit which does not conflict with Eb/No defined by the base station(Close Loop Power Control) and already calculated total sum of base station power. Its dynamic range is approximately 90dB. The said 130.38 MHx Tx IF signal is up-converted to UHF signal again. Signal converted into transmission frequency is filtered and amplified finally at power amplifier, and transmitted through the antenna via isolator duplexer.

4.2.3.2 Transmitter Part

1. IFT3000 = Analog Conversion + Analog I/Q Modulator + Tx IF LO PLL & VCO + IF AGC

2. IF AGC in IFT

This is used to increase/decrease or maintain transmit power level at optimum by request of the base station. Transmit AGC controls so that the received signal strength level and base station within cell maintain optimal Eb/No and transmit power of the mobile station does not exceed threshold power. Especially, AGC should have linearity and wide dynamic range. It changes attenuation of 130.38 MHz IF signal inputted from BBA and outputs it in appropriate size necessary for transmission. Its dynamic range is approximately 60dB. Minimum attenuation is 0dB, while maximum attenuation is 60dB.

3. IF BPF(IF Band Pass Filter): F507

This removes digital spurious except Tx IF, and insertion loss is 10dB.

4. Tx LO Buffer Amplifier: Q508

With Phase Lock being set between VCO and PLL IC, this amplifier inputs LO signal in size optimal for LO port of Up-Converting Mixer and functions for Rx/Tx path isolation and VCO load isolation.

5. IF Amplifier : Q510

6. Up-Converting Mixer: U516

This mixes 130.38 MHz signal amplified by IF Amp. with 966.88±12.5 MHz LO to up-convert the result to 836.5±12.5 MHz RF signal.

6. RF BPF(Radio Frequency Band Pass Filter): F506

This filters only such signals with 881.5±12.5 MHz frequency band of transmission frequency for cellular system terminal equipment and removes other signals and image components than transmission frequency for terminal equipment. Insertion loss is maximum 3dB.

7. Power Amp Module: U515

This is a power amplifier, which finally amplifies signals to sufficiently big size and transmits them through the antenna from the terminal equipment to the base station and has 28dB amplification factor and approximately 30% efficiency at 630mW(28dBm).

8. Isolator: U501

If other user's terminal equipment outputs very strong signal near your place(Weak current field area), such signal has the same frequency(CDMA: same frequency/different code in a cell) and accordingly may interfere with the power amplifier quite strongly through your terminal equipment's antenna and duplexer in reverse direction. The total sum of interfering power may be increased greatly if users are increased in the vicinity of your place. In this situation, limited linear range characteristic causes intermodulation at your power amplifier and increases noise spectrum of in-band and adjacent channel power, resulting in bad influence to spectral efficiency of the whole cellular system. Therefore, it is necessary to strengthen isolation in the reverse direction. In addition, your output signal may be mismatched due to environmental factor at the antenna(due to ambient radio wave interference, etc.) and your power amplifier may be damaged by reflected wave or power consumption may be increased. To improve such situation, isolator is installed at output-end of power amplifier.

9. Antenna: ANT 501

This is a device designed to transmit/receive radio wave at the aerial antenna.

4.2.4 Frequency Synthesizer Section

4.2.4.1 Summary

Frequency synthesizer part uses VC-TCXO(19.68MHz) as reference frequency. 19.68MHz of VC-TCXO is sent to frequency synthesizer part as reference input for UHF PLL IC and demultiplied equivalently to channel spacing by reference divider inside IC. VCO generates LO signal to be converted to transmit/receive carrier frequency. Each VCO output signal is inputted by LO buffer amplifier; one as local signal of down converter which is 1^{st} mixer; the other as local signal of up-converting mixer for transmission. Prescaler and variable frequency demultiplier inside UHF PLL IC demultiply pin 12 input

frequency according to channel frequency, and then phase detector compares reference frequency and phase. When PLL is combined, phase error is outputted to pin 10. Phase error signal is sent to VCO frequency control terminal via LPF. Digital data for determining channels of frequency synthesizer part is sent from logic part and composed of PLL_CLK, PLL_DATA, and PLL-EN signals in 3-line serial interface. Loop filter is composed of RC Lag Lead Filter and RC Low Pass Filter.

4.2.4.2 Frequency Synthesizer Part

1. VCO(Voltage Controlled Oscillator): U507

This generates 1st local frequency which is changed by voltage control and has 966MHz center frequency and ±12.5 MHz dynamic width. This signal is controlled by UHF PLL IC.

2. UHF PLL(Phase Locked Loop): U508

Reference frequency to be inputted is created at VC-TCXO, while signal to be divided is created at VCO. UHF PLL compares these two signals to detect them and varies VCO controlled voltage using pre-programmed counter to create LO signals needed for transmission and reception.

3. VC-TCXO(Voltage Controlled Temperature Compensated Crystal Oscillator): U509

This is mobile station system reference frequency source. Its frequency is 19.68MHz, and this frequency is applied to UHF PLL IC and MSM3000. For AFC of mobile station, PDM signal outputted from MSM3000 is controlled by smoothing voltage.

4.2.5 Supplemental Description for IFR3000 / IFT3000

4.2.5.1 Summary

IFR3000 / IFT3000 processes signals between RF part and digital circuitry and operates in direct connection to MSM3000. Its internal is composed of ADC, DAC, LPF, Divider, VCO, PLL, Mixer, and Logic Control Circuit.

4.2.5.2 IFR3000 ; Receive IF Signal Path

This is spread spectrally to 1.23MHz bandwidth at CDMA forward link as much as ±630kHz out of if center frequency of 85.38MHz and at the same time, receives differential IF signal modulated to QPSK. This real spectrum is converted to I and Q complex spectrums by orthogonal transformation with 85.38MHz local signal and distributed between 1kHz and 630kHz. As components exceeding 750kHz belong to range beyond CDMA band, they are subjected to low-pass filtering in order to reduce interference with unwanted signals, resulting in obtaining wanted signals of baseband. Analog I and Q baseband components are converted to digital signals by the two distinguishable 4 bit flash ADC. CDMA ADC is converted to a new digital value at each rising edge of CHIPx8(9.8304MHz) which is ADC clock. CHIPx8 ADC clock frequency is synthesized from TCXO(19.68MHz) which is system reference.

4.2.5.2 IFT3000 ; Transmit IF Signal Path

This outputs IF center frequency of 130.38MHz, which is converted from digital I and Q baseband complex spectrum data received from MSM3000, to RF transmitter. 8 bit I and Q transmit data in MSM3000 are inputted to CDMA DAC of IFT3000. I data are stored in 1 DAC at rising edge of transmit clock; Q data are stored in Q DAC at falling edge of transmit clock. Unnecessary frequency components are contained in CDMA DAC output spectrum, and these components are removed through anti-aliasing low-pass filter with 630 kHz bandwidth. I and Q baseband components converted to analog are outputted as real spectrum 130.38 MHz differential signal.