Rev C+ HomePortal

Layout Note:

All SDRAM traces 50 ohm controlled impedance, surface routed, 6 mil, 1/2 oz copper.

Place r232,r233,c360 as close to pins of U9 as possible.

Minimize distance of PCI_CLK between Chips(1 inch), Route in a Daisy chain w/minimized stubbs

For U9, Miniplane of 2.5v under chip, 1 via per ball on GND/Power pins

All Nets, including No connect pins shall be routed to a test pad.

D3 is Power LED, Located on top of the board.

D6 is Home Networking LED, Located on Bottom of the board.

D7 is Broadband Link LED, Located on Middle.

Assembly notes:

Gerber Number 2700-000192-003

SDRAM - 32 MB

Note: A13 on TM1300 is MSB on address, and A11,12 is Bank select; while A12, A13 is Bank select on SDRAM

20 Pin Header for JTAG, Place in fixed area

Flash Memory, 8MB Default, 16 MB Optional

NOTE

For dual file systems, stuff R167, R376

For single file systems, stuff R166, R196

Residential Gateway Platform	
Processor(TM 1300), SDRAM, and Flash Memory	
SCHEMATIC NUMBER 2700-000189-002	
Engineer: Jim Schley-May	Date: 3-30-2001, 9:33
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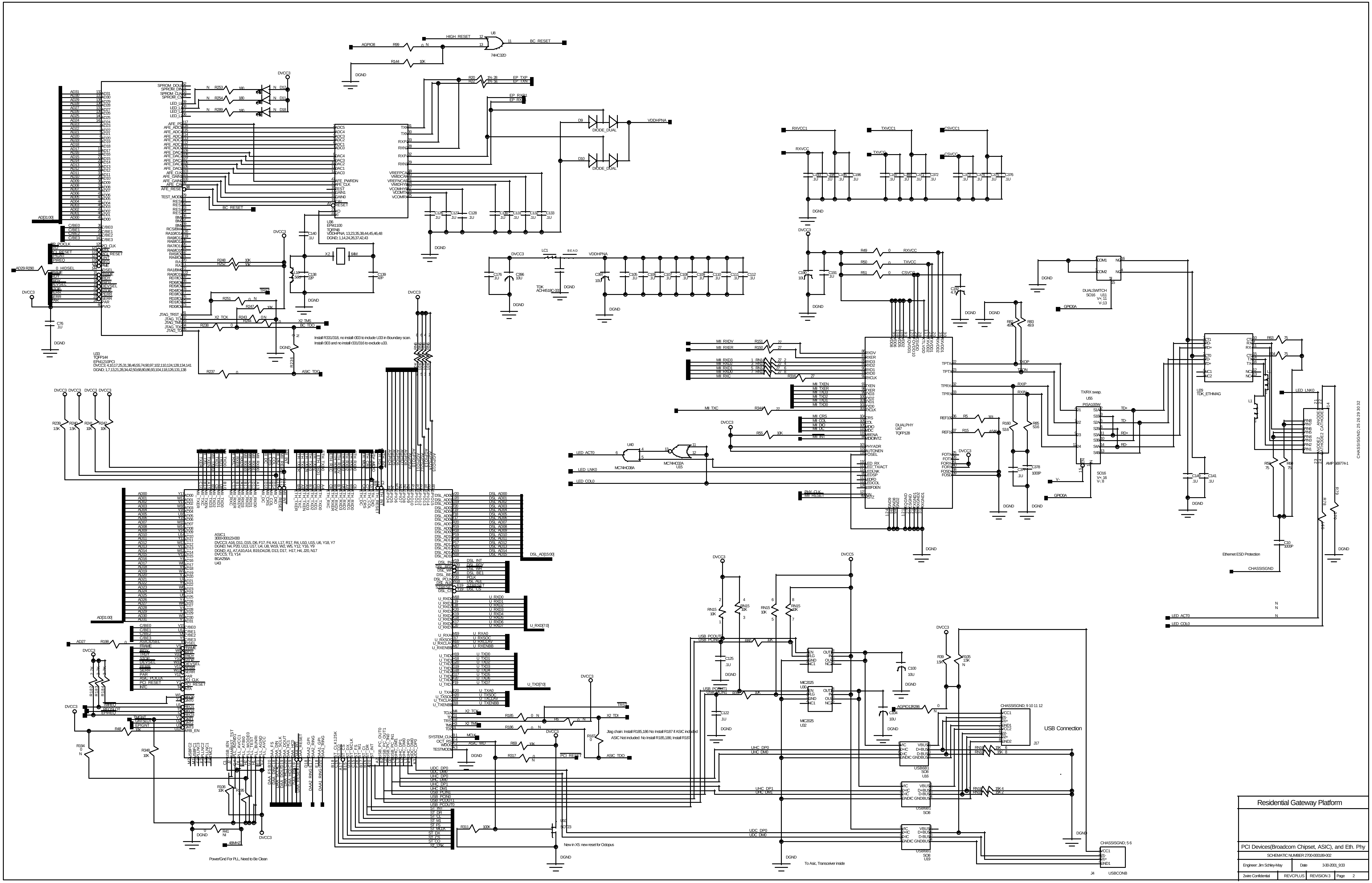
Residential Gateway Platform
PCI Devices(Broadcom Chipset, ASIC), and Eth. Phy
SCHEMATIC NUMBER 2700-000189-002
Engineer: Jim Schley-May
Date 3-30-2001_9:33
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Page 2
USB Connection
Ethernet ESD Protection
Install R331/318, no install r303 to include U33 in Boundary scan.
Install r303 and no install r331/316 to exclude u33.
Jtag chain: Install R185,186 No Install R187 if ASIC included
ASIC Not included: No Install R185,186; Install R187
New in X5: new reset for Octopus
To Asic, Transceiver inside
Power/Gnd For PLL, Need to Be Clean

Note - for DSLVCC3 filter, populate either L3 and C234 (47uF) OR U44, C294, and C234 (10uF)

DSL DMT CHIP

LC3

DSL AFE, Transmit

DSL AFE Receive and Hybrid

X5 new part: 6db atten. + active hybrid

L2,5,6,7 changed on x5 (dual footprint)

Selective Attenuation: 0dB, 6.4dB, 12.7 dB, 20dB

Residential Gateway Platform			
DSL Chipset and AFE			
SCHEMATIC NUMBER 2700-00018 9-002			
Engineer: Jim Schley-May		Date	3-30-2001, 9:33
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3.3v to 2.5v LDO

Surface Mount LEDs for testing purposes

Active Low buffers, +/-24 ma drive.

74LVC273
DGND;10
DVCC3;20

DUALPHY
U67
TQFP128

MC74HC03A

DUALCOMP
SO8
U50

SO16
V+; 16
V-; 8

Interrupt mapping will be done on the FPGA Daughter Card

Sidactor, Teccor
P3100EB

Slow-Blow Fuse Teccor F1250T

To Daughter Card Header, Private PBX lines

DUALRJ11
CHASSISGND; 13, 14
J8

To Broadcom Chipset

Transformer to jump HPNA from Line1 to Line2

AMP 569774-1

Relay network to select DSL lines

2PCIRELAY

DUALSWITCH
SO16
U11
V+; 11
V-; 13

HPNA_MAC
DELTA
LFB028

HPNA_TDK
TDK
TLA-7T401

Power Connector

CHASSISGND; 5,6,7,8,9,10
DGND; 11
POWER_CON
J9

R378 = 24ohm 2W, 51ohm 1W, or not populated

R380 = 62ohm 3W, 120ohm 2W, or not populated

Residential Gateway Platform

Frontend Wiring and Ethernet Phy

SCHEMATIC NUMBER 2700-000189-002

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Mimow Daughter Card Connectors

Residential Gateway Platform	
Silicon DAAs and Daughtercard Connectors	
SCHEMATIC NUMBER 2700-000189-002	
Engineer: Jim Schley-May	Date: 3-30-2001_9:33
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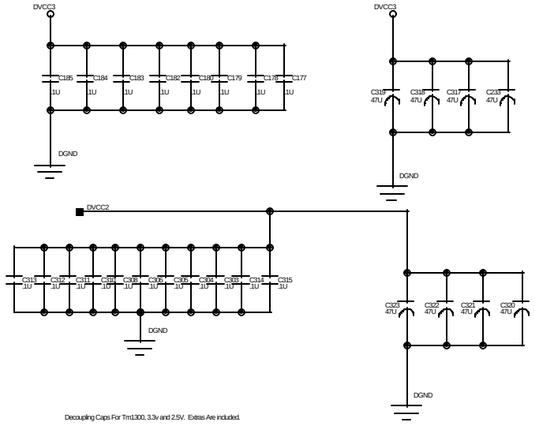
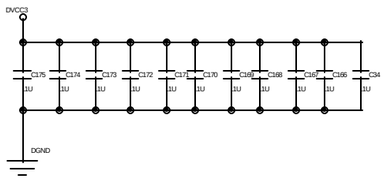
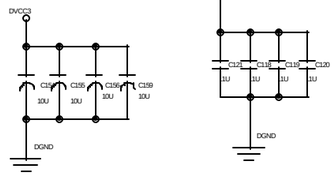


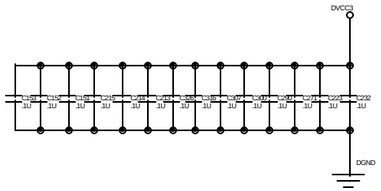
Decoupling Caps For Trm1300, 3.3v and 2.5V. Extras Are included.

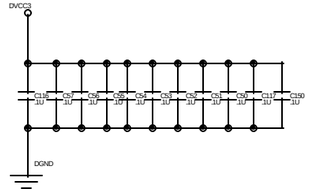




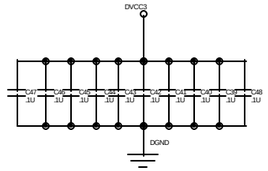
D Caps for Flash

Decoupling Caps For SDRAM

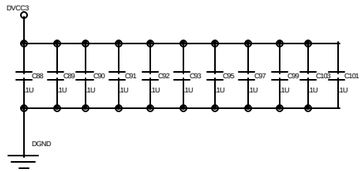


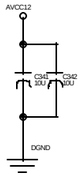


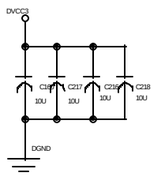
Decoupling Caps For ASIC

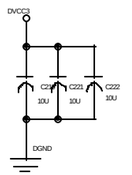


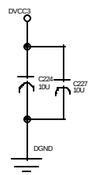
Decoupling Caps For Epigram

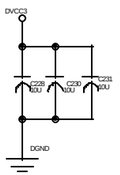


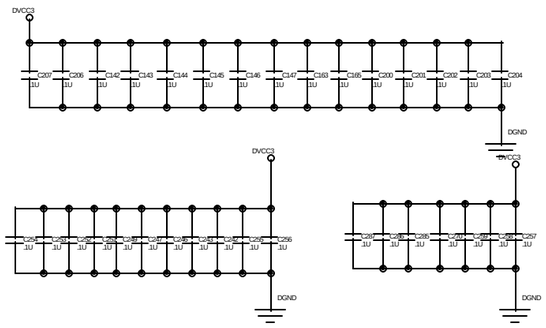












Residential Gateway Platform

Decoupling Caps, Test Connectors, and Test LEDs

SCHEMATIC NUMBER2700-000189-002

Engineer: Jim Schley-May	Date	3-30-2001_9:33	
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