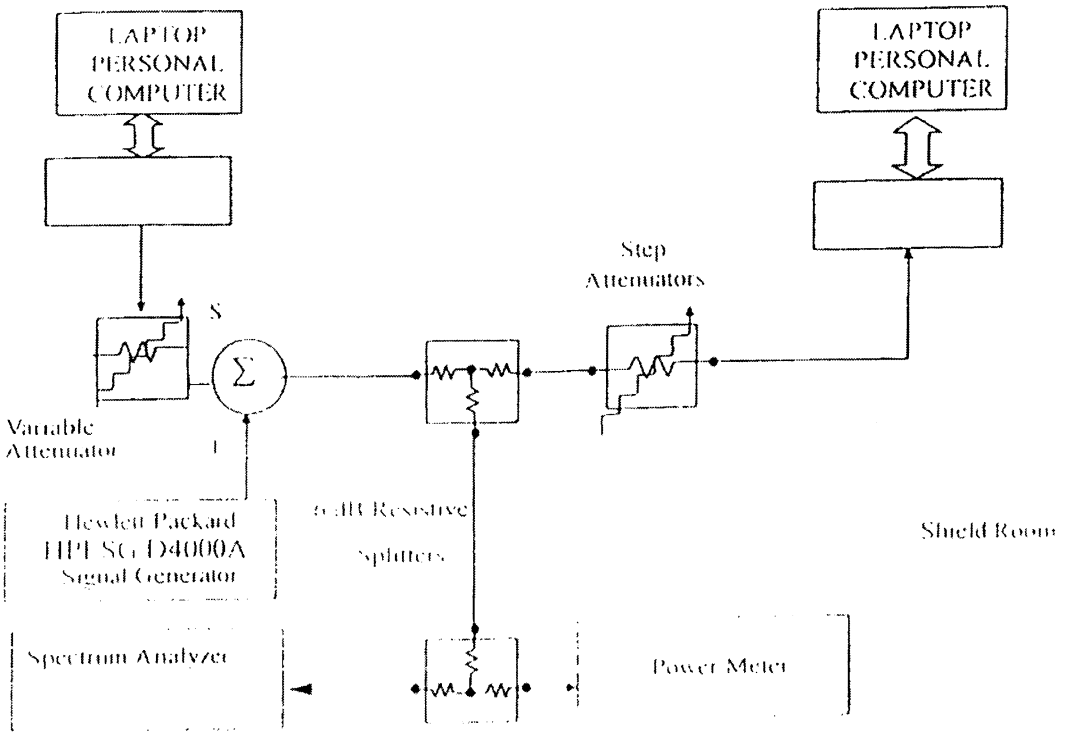
§15.247(e) Processing Gain (Cont.)

Reference

[1]. Intersil processing gain test document(Attached file).

Test Block Diagram



§15.247(e) Processing Gain (Cont.)

It is well know that the Eb/No of BPSK is 9.6dB for 1e-5BER, so therefore the coding gain of CCK over BPSK is 2.2dB. We add this to the processing gain of 9B to get 11.2dB overall processing gain for the CW jamming test.
Taking the calculation above, if the (J/S)>-8.4dB then the equipment passes the CW jamming test.

Test procedure:
Obtain the simplex link shown. Perform all independent instrumentation calibration prior to this procedure. Set operating levels using fixed and variable attenuator in system to meet the following objectives.

1. Signal Power at receiver is approximately -60dBm.
2. Signal Power at power meter between -20 and -30dBm.
3. Use spectrum analyzer to monitor test.
4. Ensure that CW jammer generator RF output is disabled and measure the power at the power meter port using HP437B power meter. This is relative power, Sr.
5. Disable TX and set CW jammer output frequency equal to the carrier frequency and enable generator output. Set reference CW jammer power level at power meter port 8.4dB below Sr(minimum J/S, or 10 dB processing gain reference level).
6. Disable CW jammer and re-establish Link. FER test should be essentially error free.
7. Enable the CW jammer at the reference power level and verify that FER at the reference power level and measure FER.
8. Repeat Step 7 for uniform steps in frequency increments of 50KHz across the receiver passband with the CW jammer. In this case, the receiver passband is 8.5MHz.

Test setup: as shown at next page

Processing Gain Test Result Summary:

Frequency Channel	Frequency (MHz)	Data Rate (Mbps)	Worst Point of the 8% FER (Limit is 20%)	Result
1	2413	11	18.8	Passed
6	2438	11	18.2	Passed
10	2458	11	19.1	Passed

§15.247(e) Processing Gain (Cont.)

$$P_c = 1 - P_{cl} = 1 - \frac{1}{\sqrt{2\pi}} \int_{\frac{S_{01}}{N_0}}^{\infty} \left[2\left(1 - Q\left\{ z + \sqrt{2\frac{E_b}{\eta}} \right\}\right) \right]^{2^{\frac{W}{2}}-1} \exp\left\{ -\frac{z^2}{2} \right\} dz$$

So the PER performance curve is given by[1] as below graph:

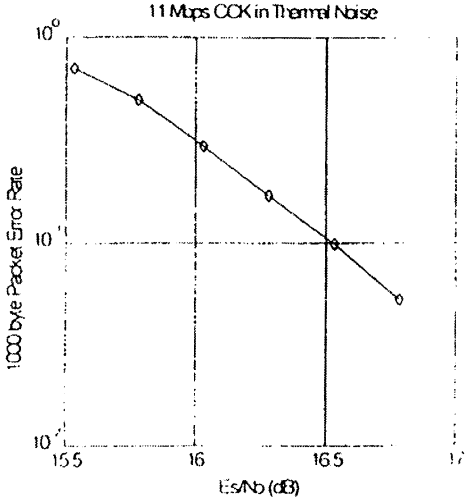


figure.1 1000 byte PER vs. Es/No

Therefore:

Gp (Es/No)o+ (J/S) +L.sys=16.4+2.0+(J/S)

Gp 18.4+(J/S) must >10dB

For the case of the HFA3861B, the bit rates are 1,2,5.5 and 11Mbps. The corresponding symbol rates are 1, 1, 1.375 and 1.375 MSPS. And 1 and 11Mbps are used within our system.

The chip rate is always 11Mcps, so the ratio of chip rate to symbol rate is 11:1 for the1Mbps and 8:1 for 11Mbps rate.

Since the symbol rate to bit rate is less than 10 for the higher rates, we supply the theoretical processing gain and coding are utilized. This is a reasonable in that they cannot be separated in the demodulation process. If a separable FEC coding scheme were used, we would not be comfortable making this assertion.

As can be seen from the curve of figure 1, the Es/No is 16.4dB at the PER of 8%.

§15.247(e) Processing Gain (Cont.)

Testing for compliance with FCC rules 15-247e

Scope

This report presents the test procedure, test configuration and test data associated with a FCC Part 15.247 (e) Jamming Margin test for the indirect measurement of processing gain.

Applicable Reference Documents.

1. "Operation within the bands 902-928 MHz, 2400-2483.5, and 5725-5850 MHz" ***Title 47 Part 15 section 247 (e) Code of Federal Regulations.*** **(47 CFR 15.247).**

2. "Report and Order: Amendment of Parts 2 and 15 of the Commission's Rules Regarding Spread Spectrum Transmitters. Appendix C: 'Guidance on Measurements for Direct Sequence Spread Spectrum Systems" ***FCC 97-114. ET Docket No. 96-8, RM-8435, RM-8608, RM-8609.***

3. "HFA3861A Direct Sequence Spread Spectrum Baseband Processor" ***Harris Corporation Semiconductor Sector Preliminary Data Sheet.*** Melbourne FL, July 1999

4. " M-ary Orthogonal Keying BER Curve".

Test Background and Procedure.

According to FCC regulations [1], a direct sequence spread spectrum system must have a processing gain, G_p of at least 10 dB. Compliance to this requirement can be shown by demonstrating a relative bit-error-ratio (BER) performance improvement (and corresponding signal to noise ratio per symbol improvement of at least 10 dB) between

§15.247(e) Processing Gain (Cont.)

intersil PRISM II radio Jamming Margin Test

the case where spread spectrum processes (coding, modulation) are engaged relative to the processes being bypassed. In some practical systems, the spread spectrum processing cannot simply be bypassed. In these cases, the processing gain can be indirectly measured by a jamming margin test [2]. In accordance with the new NPRM 99-231, if the vendor has a system with less than 10 chips per symbol, the CW jamming results must be supported by a theoretical explanation of the system processing gain.

Theoretical calculations

The processing gain is related to the jamming margin as follows [2]:

$$G_p = \left(\frac{S}{N}\right)_{output} + \left(\frac{J}{S}\right) + L_{system}$$

Where $BER_{REFERENCE}$ is the reference bit error ratio with its corresponding, theoretical output signal to noise ratio per symbol, $(S/N)_{output}$, (J/S) is the jamming margin (jamming signal power relative to desired signal power), and L_{system} are the system implementation losses.

The maximum allowed total system implementation loss is 2 dB.

The HFA3861A direct sequence spread spectrum baseband processor uses CCK modulation which is a form of M-ary Orthogonal Keying. The BER performance curve is given by [5]:

" The probability of error for generalized M-ary Orthogonal signaling using coherent demodulation is given by:

$$P_e = 1 - P_{c1} = 1 - \frac{1}{\sqrt{2\pi}} \int_{S_{01}} \left[2\left(1 - Q\left\{ z + \sqrt{2\frac{E_b}{\eta}} \right\}\right) \right]^{\frac{M}{2}-1} \exp\left\{ -\frac{z^2}{2} \right\} dz$$

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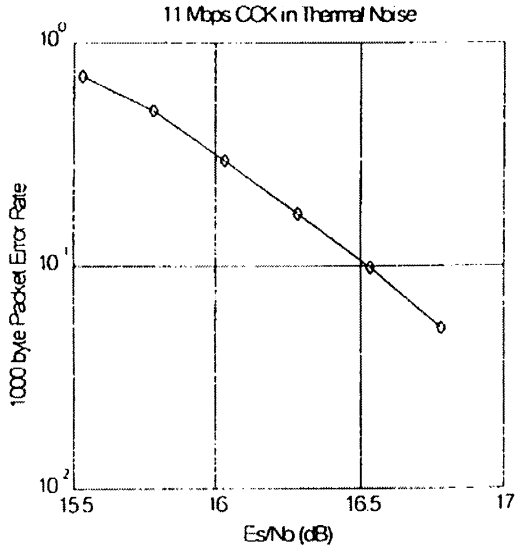
This integral cannot be solved in closed form, and numerical integration must be used. There are error rate extensions for differential decoding and descrambling that are also to be accounted for. This is done in a MATHCAD environment and is displayed in graphical format below.

1.1 1000 byte PER vs. Es/No



The reference PER is specified as 8%. The corresponding Es/No (signal to noise ratio per symbol) is 16.4 dB. The Es/No required to achieve the desired BER with maximum system implementation losses is 18.4 dB. The minimum processing gain is again, 10 dB, therefore:

$$G_p = \left(\frac{E_s}{N_o}\right)_{output} + \left(\frac{J}{S}\right) + L_{system} = 16.4dB + 2.0dB + \left(\frac{J}{S}\right) \geq 10dB$$

$$G_p = 18.4dB + \left(\frac{J}{S}\right) \geq 10dB$$

The minimum jammer to signal ratio is as follows:

§15.247(e) Processing Gain (Cont.)

intersil PRISM II radio Jamming Margin Test

$$\left(\frac{J}{S}\right) \geq -8.4\,dB$$

For the case of the HFA3861A, the bit rates are 1, 2, 5.5, and 11 Mbps. The corresponding symbol rates are 1, 1, 1.375, and 1.375 MSps. The chip rate is always 11 MCps, so the ratio of chip rate to symbol rate is 11:1 for the 1 and 2 Mbps rates and 8:1 for the 5.5 and 11 Mbps rates. Since the symbol rate to bit rate is less than 10 for the higher rates, we supply the theoretical processing gain calculation for these cases where spread spectrum processing gain with embedded coding gain is utilized. This is reasonable in that they cannot be separated in the demodulation process. If a separable FEC coding scheme were used, we would not be comfortable making this assertion.
As can be seen from the curve of figure 1, the Es/N0 is 16.4 dB at the PER of 8%. This PER can be related to a BER of 1e-5 on 1000 byte packets. With 8 bits per symbol, the Eb/N0 is then 7.4 dB or 9 dB less than the Es/N0. It is well known that the Eb/N0 of BPSK is 9.6 dB for 1e-5 BER, so therefore the coding gain of CCK over BPSK is 2.2 dB. We add this to the processing gain of 9 dB to get 11.2 dB overall processing gain for the CW jammer test.

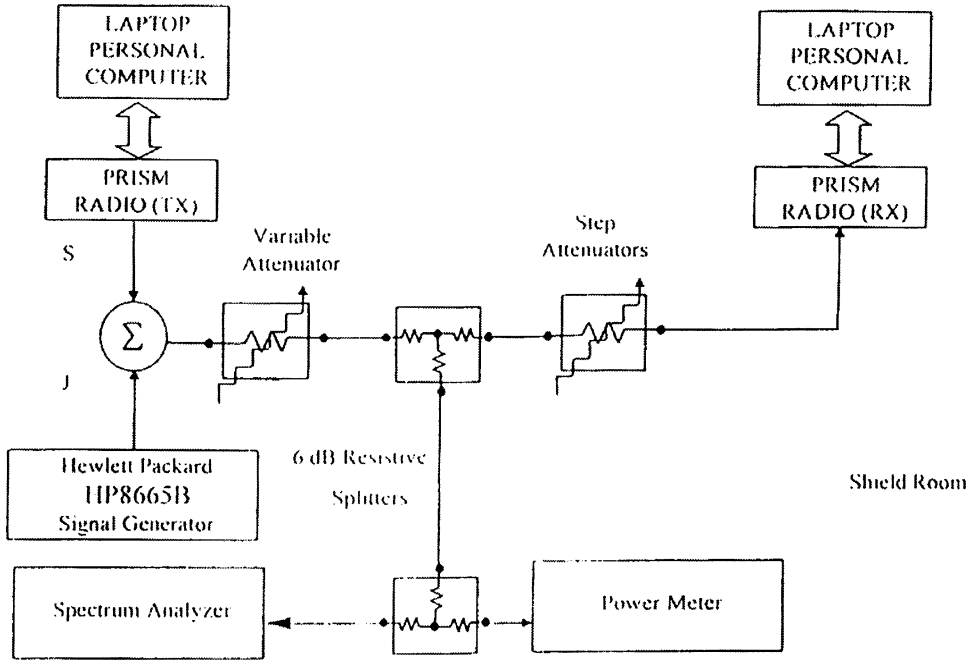
Taking the calculations above, if the $\left(\frac{J}{S}\right) \geq -8.4\,dB$ then the equipment passes the CW jamming test

Test Configuration: CW Jamming Margin (15.247) (e)

§15.247(e) Processing Gain (Cont.)

intersil PRISM II radio Jamming Margin Test

Basic Test Block Diagram



Test Procedure

Setup the simplex link shown. Perform all independent instrumentation calibrations prior to this procedure. Set operating power levels using fixed and variable attenuators in system to meet the following objectives:

- Signal Power at receiver approximately -60 dBm (above thermal sensitivity such that thermal noise does not cause bit errors).
- Signal Power at power meter (using high sensitivity probe) between -20 and -40 dBm for optimal linearity
- Use spectrum analyzer to monitor test.
- Ensure that CW Jammer generator RF output is disabled and measure the power at the power meter port using the power meter. This is the relative signal power, S_1

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intersil PRISM II radio Jamming Margin Test

- Disable Transmitter, and set CW Jammer generator RF output frequency equal to the carrier frequency and enable generator output. Set reference CW Jammer power level at power meter port 8.4 dB below S, (minimum J/S, or 10 dB processing gain reference level). Note the power level setting on the generator, this is the reference CW Jammer power setting, J_1.

- Disable CW Jammer, re-establish link. PER test should be operating essentially error-free.

- Adjust the CW Jammer level to that which causes 8% PER and verify that the S/J is less than 8.4 dB.

- Repeat step 7 for uniform steps in frequency increments of 50 kHz across the receiver passband with the CW Jammer. In this case the receiver passband is ±8.5 MHz.

The number of points where the S/J fails to achieve 8.4 dB (is higher than 8.4 dB) is determined and if this is above 20% of the total, the test is failed otherwise it is passed.

The numerical data associated with the following radio channels is tabulated and presented for:

Channel 1: 2413 MHz
Channel 6: 2438 MHz
Channel 10: 2458 MHz

PRISM II Radio HWB3163-02 Rev A card
Detailed Processing Gain Measurement Operating Instructions

1) Assemble equipment as shown in the block diagram
2) This test procedure assumes that the Computers are equipped with 3.3V PCMCIA slots and have the appropriate PCMCIA radio card Windows drivers installed. Also that the Prism 802.11 Wireless LAN Configuration Utility and CW10CON Console Command Line program is installed.
3) Use two Prism II radio cards. This procedure is written for HWB3163-02 Rev A, newer radio cards may require different software/firmware. The HWB3163-02 rev A uses the HFA3861A baseband processor. These radio cards are loaded with firmware.

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Firmware may be loaded in Genesis mode using the program "Download" revision 3.7 a DOS based utility.

4) The following programs and files are used in this test procedure.
C:\ laneval\laneval.exe (rev 2.03 or later) Windows LAN and PER utility.
C:\laneval\laneval.ini (autogenerated) Must edit this file to set the following:
PktDelay = 1 PktBurst = 6 (Settings for firmware 0709 rev 0.4+)
Pkt Size = 1000
PktFill = -1 (Random data or Optional data pattern may be specified with decimal byte value 0 to 255)
New firmware rev 0.4 will allow PktDelay less than 10.
C:\cw10con\cw10con.exe (rev 0.4)(8/4/99) Windows Console command line Utility
c:\cw10con\h3861ar1a.ini (8/4/99) Contains updated Baseband processor register values.

5) Insert HWB3163-02 Rev A Prism II radio into PCMCIA extender card 68 pin connector socket. Note: The PRISM II radio uses only 3.3V power. Cards with coversets are "keyed" for low voltage slots and will not fit into 5V slots. Cards without coversets must be manually centered and inserted into the 68 pin extender card socket.

6) Select desired frequency channel and data rate.
* Double Click the system icon at the lower left of the screen that looks like a "terminal with an antenna". This activates the "Prism 802.11 Wireless LAN Configuration Utility
* Select the desired channel (1,6 or 11 recommended) and "Fixed 11Mb/s" for data rate on both the TX and RX radios. The Configuration Utility modifies these settings dynamically so that NO Reboot is necessary. However, when the channel setting is modified, Configuration Utility reinitializes the radio card reverting all register settings back to the firmware defaults. It will be necessary to perform step 7) after each change of channel setting.
* An alternate method of changing channels without reinitializing the radio card register values is available through the cw10con program, described in step 7) under "Other useful commands".

7) Load correct Baseband processor (HFA3861) register values into both the TX and RX cards. Cards with firmware revision 0709 0.4+ have correct register settings and do not need modification except at indicated in step 7a)
* Execute program cw10con.exe (Enter -> ? for a list of available commands)
(Enter -> q for quit)
* Enter Command > bf h3861ar1.ini (loads BBP registers contained in file)
* Other useful commands in the cw10con program.
Enter Command > c 0838 a (dynamically changes radio frequency to channel 10 ["a" Hex] without reinitializing the radio registers. the channel field is a HEX number from 1 to e [1 to 14 decimal]).

§15.247(e) Processing Gain (Cont.)

intersil PRISM II radio Jamming Margin Test

Enter Command > c 0e38 5555 (Continuous transmit mode with data pattern 0101)
Enter Command > c 0f38 (Turn off transmit mode, refer to step 14)).
Enter Command > c 1338 (Run DC offset calibration on HFA3783)

7a) Cards with firmware 0709 rev 0.4+ or later require the CCA function turned off on the transmitter card during the Processing Gain test.
* Execute program cw10con.exe
* Enter Command > bw 09 00 (Change register 09(Dec) to value 00(Hex) original value is 20(Hex) user can verify change using the command br 09).

8) Set the approximate power to the input of the RX card to -60dBm by adjusting the Variable Attenuator and step attenuators.
9) Execute "Laneval.exe" on both TX and RX computers. Set for "Broadcast" mode and start transmission of the TX card. Set the RX card for "Broadcast" and start receiving with the RX card. Verify that the two cards are communicating by observing the "Total Packet Count" window of the RX computer. This window should be increasing in value as packets are received from the TX card. Also note the "Packet Error Rate" window should remain 0.0, indicating no errors in this large signal condition. Allow the radio cards, signal source and power meter to warm up for several hours.
10) Click the Stop TX and Stop RX buttons in Laneval.
11) Calibrate Power Sensor/Meter.
12) Click the CW10CON window previously opened to bring forward. Set the TX card to continuous transmit. Enter Command > c 0e38 5555 (Continuous transmit data pattern 0101)
13) Measure TX card output signal power and adjust Variable Attenuator for -30.0dBm at the power meter. This measurement should be taken quickly as the radio can change its output power about 0.5dB warming up in continuous mode. Remember that the RX card sees 30 dB less power than the power meter, so the RX card will see -60dBm.
14) Disable the TX card output. Enter Command > c 0f38 (Turn off TX output)
15) Set up Jammer Source. Adjust the frequency of the HP8665B (or equivalent) to center of the TX channel and adjust to output amplitude to -8.0dBm. Turn on the RF output of the Signal source.
16) Measure the Jammer power level at the power meter. Adjust Jammer signal amplitude at the source until you measure -38.4dBm (-68.4dBm at the RX card). This will give a Signal to Jammer ratio of 8.4dB, the limit to pass the 10dB processing gain test for a PER of 8%. Record this Jammer source output setting as all measurements will be recorded relative to this level.
17) Click the Laneval window at the TX computer and start transmitting in broadcast mode.
18) Click the Laneval window at the RX computer and start the RX card receiving. Measure the PER of the receiving unit.

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intersil PRISM II radio Jamming Margin Test

The tab and enter keys can replace the mouse click to start and stop the Laneval receive mode for PER measurements. The tab key will cycle through program options by highlighting the option button in the program window. Highlight the desired button with tab and then select the option with the Enter key.

The FCC specifies that the Processing Gain test will be measured with the CW Jammer in 50KHz steps across the bandwidth of the spread signal (+-8.5MHz for Prism II) or 340 test points per channel. It is recommended to measure channels 1,6 and 11. Processing Gain is measured by adjusting the CW Jammer source to find the S/J ratio for 8% PER at each jamming frequency. Record the Jammer source output setting and calculate the Processing Gain at each Jammer frequency in the band. Care should be taken to allow enough time for an accurate measurement, 1 minute is a minimum. A maximum of 68 points, or 20%, may fall below 10dB Processing Gain for the radio to still pass the Processing Gain requirement.

19) It is recommended to power down the Prism II PCMCIA card before removing from its slot. This can be done from the PCMCIA card system icon at the bottom of the Windows screen. Place the mouse pointer over the icon and a text bar will appear naming the driver "Harris Prism IEEE802.11 PC Card Adapter/EVB". Mouse click this text bar. A dialog window will appear verifying that the PC card has been powered down and that it is safe to remove it.

20) When reinserting the Prism II radio PC card, it is acceptable to "hot" insert the card when Windows is running. The driver application will automatically sense the new hardware and apply the correct 3.3V bus power. On power up the Prism II card will execute its own initialization program stored in on board ROM. This program provides default values for the baseband processor and other radio settings. These default settings need to be updated on each card insertion as described in steps 6) and 7) above with the CW10CON program.

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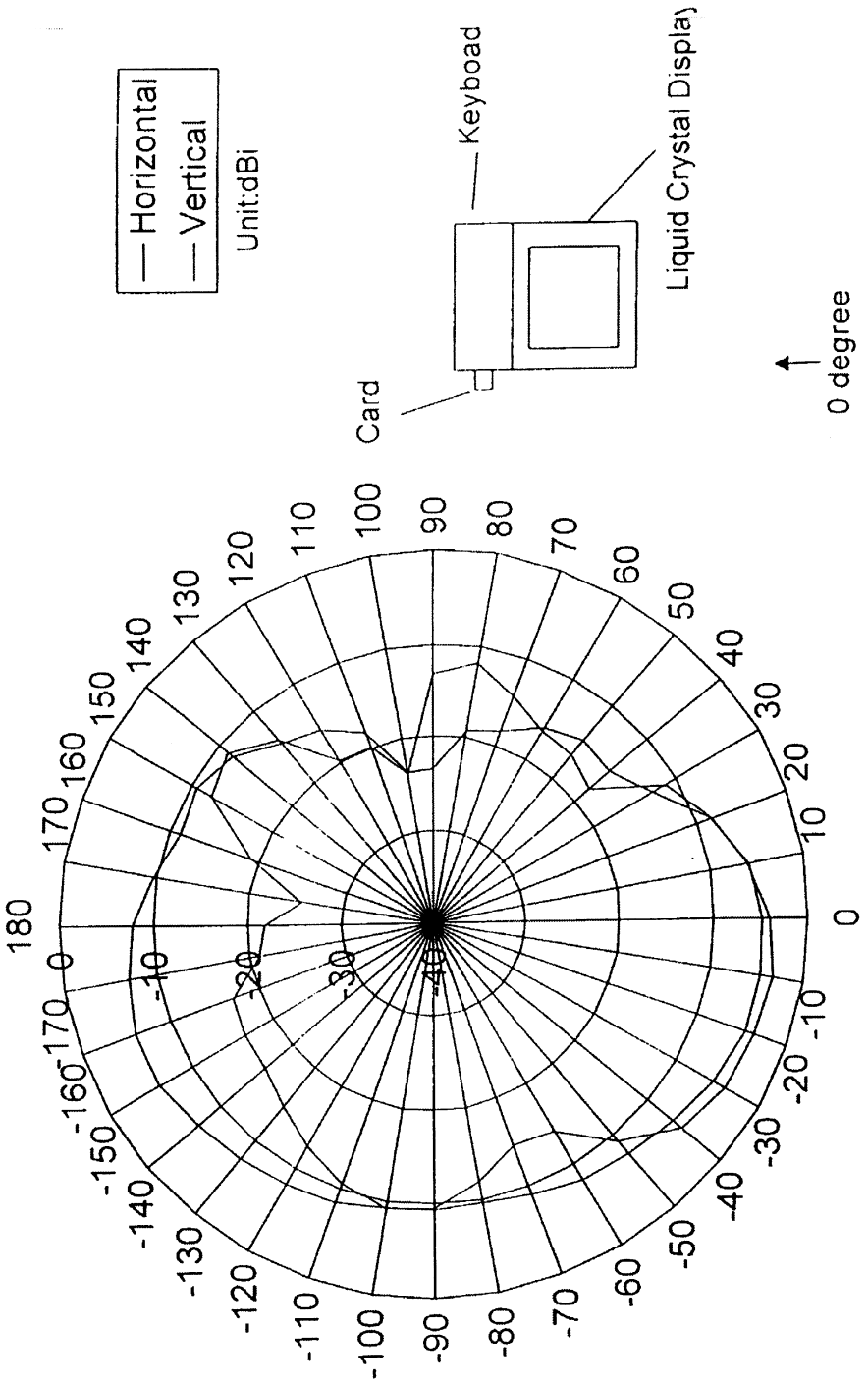
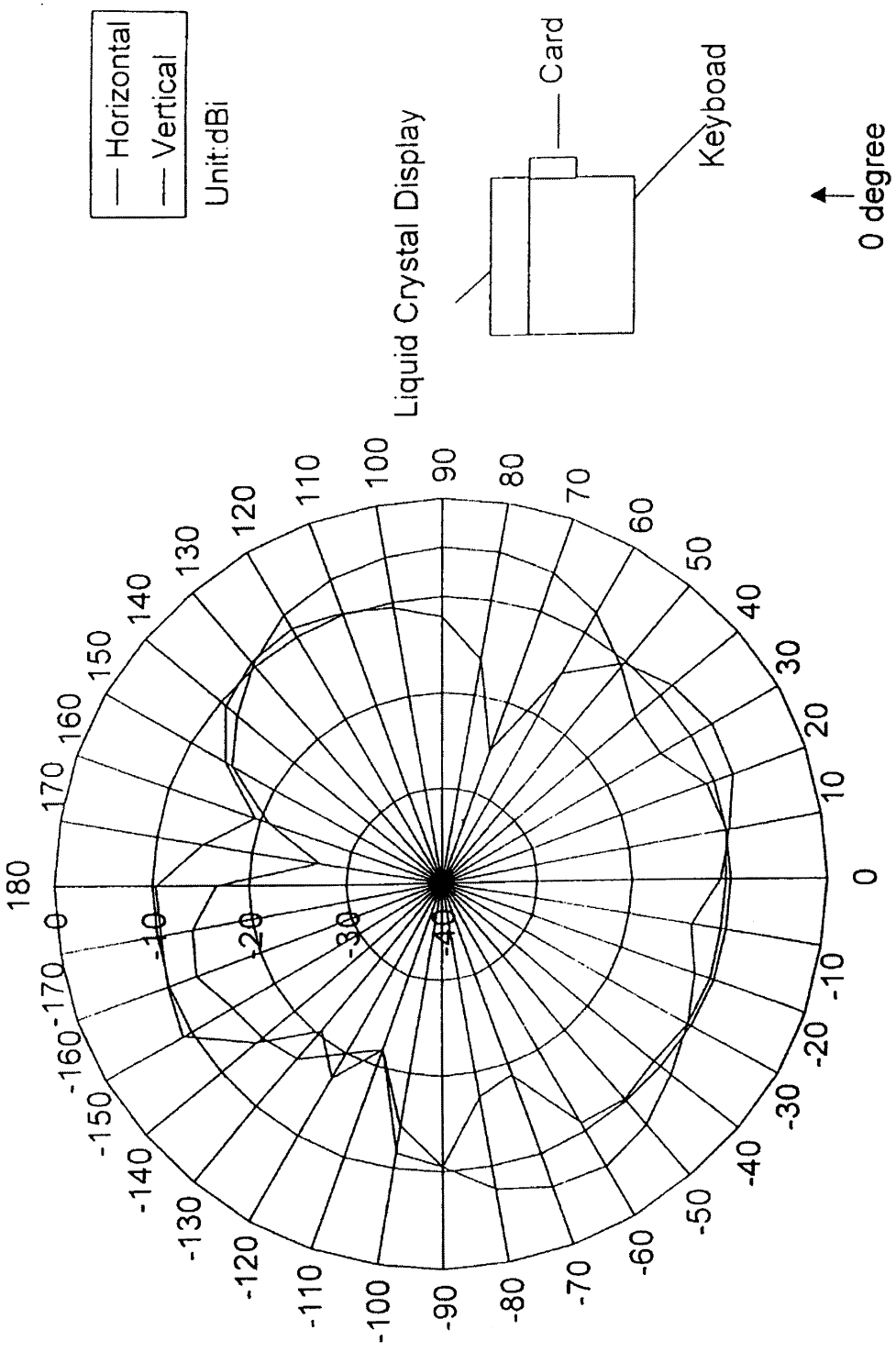


§15.247(e) Processing Gain (Cont.)



§15.247(e) Processing Gain (Cont.)