1. Introduction

This paper describes the ezWAVE AP circuits, specifications,layouts and partlist etc.

2. Circuit Description

2.1 The Architecture

The radio design is centered on the expected signal characteristics of the modulation method. A Differential Quadrature Phase Shift Keying (DQPSK) modulation encodes the data in terms of phase with minimal amplitude variation, improving noise immunity. This is joined with the IEEE 802.11 protocol standard Carrier Sense Multiple Access/Collision Avoidance (CSMA/CA) and with the FCC requirement for 10dB processing gain, to allow signals to be received with approximately 0dB Signal to Noise Ratio (SNR) for a 10 -5 Bit Error Rate (BER). The CSMA/CA protocol allows only one user, per channel, at a time (i.e., first come, first serve) making for a quieter medium. The processing gain, achieved by spreading the signal with a PN code, allows a faint signal to be pulled from the noise while suppressing non-correlating interferers. From the antenna, the received input is applied to the pre-select filter FL1. This filter is a two pole dielectric design, rejecting interferers outside the 2.4GHz ISM band and providing image rejection.
The signal enters the HFA3683 RF/IF Converter, first passing through the integrated LNA section and then enters the down converter section of the HFA3683. Low-side local oscillator injection is used to mix down to the single intermediate frequency, 374MHz. The IF receive filter FL3, is a Surface Acoustic Wave (SAW) device used for channel selection within the band. The SAW output is reactively matched to the IF input of the HFA3783 Quadrature IF Modulator/Demodulator. In receive mode, the HFA3783 provides two limiting amplifiers, a quadrature baseband demodulator, and two baseband low pass filters. The two limiting amplifiers or limiters provide most of the receiver gain, giving the radio it's sensitivity.
The baseband circuit samples the waveform with 7-bit ADCs and then despreads and demodulates the received data.

On the Transmit side, data can either be DBPSK or DQPSK modulated at 1MSPS (Mega Symbols Per Second), resulting in a baseband quadrature signal with I and Q components. These digital signals are output to the HFA3783 fifth order Butterworth low pass filters, which are used to provide shaping of the phase shift keyed (PSK) signal. The required transmit spectral mask, at the antenna, is -30dBc at the first side-lobe relative to the main lobe.
The signals are then quadrature modulated up to IF using the same 2xLO used for the quadrature

demodulation. The signal then goes to the high impedance input of the HFA3683 upconverting mixer for conversion to the 2.4GHz - 2.5GHz band. The mixer output goes to the pre-amplifier, in the HFA3683, amplifies the signal and easing the requirement for HFA3983 RFPA gain.
FL2, a two pole dielectric bandpass filter, is used to suppress both transmit LO leakage and the undesired sideband. The HFA3983 RFPA amplifies the transmit signal to approximately +18dBm. The transmit sidelobe performance is approximately -30dBc. Allowing for a 3dB loss in the band select filter FL1, this gives a final output power of +15dBm.

2.2 Transmit Chain Front End Cascade Analysis

The large gain in the Power Amplifier, HFA3983, keeps the signal level small for the whole chain before it. This helps conserve supply current and the cost associated with devices that need to handle large signals.
The output power at the RF filter is shown as 15dBm, with the output of the Power Amplifier at 18dBm. The design has been optimized for the best use of supply current and cost of the PA. If the output power was lower, the supply current and cost of the PA could be saved with smaller and cheaper devices. If the output power was higher, the signal will be too close to the P1dB and the signal will have excessive distortion, causing regrowth of the side lobes. The transmitted signal must suppress side lobes to -30dB to meet the 802.11 spectral mask specification.
Therefore, the output power needs to be controlled very carefully. The run to run variation in gain and insertion loss of the elements in the transmit chain requires either a manual power adjustment or an active power adjustment feedback circuit. In this design, a manual potentiometer is used to adjust output power and side lobe performance on each unit during manufacturing. For purposes of this analysis, the variable attenuator shows 0dB loss and the Modulator output as -12dBm. This was done for illustration purposes only, in actuality the Modulator output has a relatively large output (200mV P-P) that needs to be significantly attenuated to the level indicated.

2.3 Power Amplifier(HFA3983)

The HFA3983 is fabricated in the fastest SiGe BiCMOS process available, allowing superior RF performance, normally found only in GaAs ICs. Cost effective functions, normally requiring external components, are integrated into one IC. The HFA3983 integrates the following functions in one compact 28 pin EPTSSOP:
Two Stage, 30dB Gain RFPA,
Logarithmic power detect function (15dB Dynamic Range),
CMOS level compatible Power Up/Down function,
Single Supply, 2.7V to 3.6V Operation.
The HFA3983 contains a highly linear RFPA designed to deliver 18dBm and meet an ACPR specification of -30dBc in the 2.4 to 2.5GHz ISM band. The performance of this two stage RFPA can be optimized by adjusting the bias current in each stage with a dedicated resistor. No external

positive or negative power supplies are required to set the bias currents. The on chip bias network provides the optimum bias current temperature compensation when low TC external resistors are used. To get the best performance from the HFA3983, the output stage matching network can be tailored using external components.

2.4 2.4GHz RF/IF Converter and Synthesizer(HFA3683)

The HFA3683A is a monolithic SiGe half duplex RF/IF transceiver designed to operate in the 2.4GHz ISM band. The receive chain features a low noise, gain selectable amplifier (LNA) followed by a down-converter mixer. An up-converter mixer and a high performance preamplifier compose the transmit chain. The remaining circuitry comprises a high frequency Phase Locked Loop (PLL) synthesizer with a three wire programmable interface for local oscillator applications. A reduced filter count is realized by multiplexing the receive and transmit IF paths and by sharing a common differential matching network.

2.5 I/Q Modulator/Demodulator and Synthesizer(HFA3783)

The HFA3783 is a highly integrated and fully differential SiGe baseband converter for half duplex wireless applications. It features all the necessary blocks for quadrature modulation and demodulation of “I” and “Q” baseband signals.

It has an integrated AGC receive IF amplifier with frequency response to 600MHz. The AGC has 70dB of voltage gain and better than 70dB of gain control range. The transmit output also features gain control with 70dB of range.

The receive and transmit IF paths can share a common differential matching network to reduce the filter component count required for single IF half duplex transceivers. A pair of 2nd order antialiasing filters with an integrated DC offset cancellation architecture is included in the receive chain for baseband operation down to DC. In addition, an IF level detector is included in the AGC chain for threshold comparison. Up and down conversion are performed by doubly balanced mixers for “I” and “Q” IF processing. These converters are driven by a broadband quadrature LO generator with frequency of operation phase locked by an internal 3 wire interface synthesizer and PLL.

In the transmit path, DC coupled dual single end to differential baseband buffers have been added to the design to help interface the device with standard single end ground referenced source equipment. The differential buffer also applies the required common mode voltage (VREF) superimposed to the desired signal input to each one of the differential baseband inputs. In addition, a set of jumper pins (TX±, TX±) have also been added to permit direct monitoring of the differential stimulus/ DC differential offset or application of external baseband signals bypassing the evaluation board buffers. An output differential offset null capability is included and can be adjusted to zero for DC offset or to generate adjustable differential DC levels for carrier generation (vector modulation).

The 2XLO local oscillator generation is done by an on board 748MHz VCO. The PLL set for a loop

bandwidth of 1kHz at 2̃5mA. Its output can be monitored thru an on board loss pad for phase noise and spurious responses when switching from transmit to receive mode. The monitor port can also be used as an input, taking the pad loss in consideration for evaluation, when using external VCO's or generators, providing the on board VCO is disabled.
A couple of power supply regulators have been added to improve the transmit and receive switching characteristics of the HFA3783. DC current transients which occurs when the device is switched from transmit to receive cause VCO spurs to appear.

2.6 PLL

The HFA3783 includes a classical architecture Phase Lock Loop circuit with a three wire serial control interface to be used with an external VCO. It consists of a programmable "R" counter used to divide down the frequency of a very stable reference signal up to 50MHz to a phase comparator. A couple of counters ("A" and "B") with a front end prescaler ("P or P+1"), with dual modulus control, divides down the frequency of an external VCO signal to the same phase comparator. The comparator controls a charge pump circuit and an external loop filter closes the loop for VCO control. The VCO frequency dividing chain works with a dual modulus control as follows: At the beginning of a count cycle, and if the A counter is programmed with a value greater than zero, the prescaler is set to a division ratio of (P+1) where P can take programmable values of 16 or 32.
Notice that the prescaler output signal is always fed simultaneously to both A and B counters. Upon filling counter A, the prescaler division ratio becomes P and the B counter continues on its own with A standby. This processis known as "pulse swallowing". The expression B-A (counts) is the remainder of counts carried out by the B counter after A is full. Both A and B counters are reset at the end of the counting cycle when B fills up. As a result, the total count or division ratio used for the VCO signal is A*(P+1) + (B-A)*P which simplifies to [P*B+A]. (A and B counters are referred as the "N" counter).
The Charge Pump (current source/sink) has 4 programmable current settings. This variation allows the user to change the reference frequency for different objectives without changing the loop filter components. The user can program the charge pump sign based on the direction of increase or decrease of the VCO frequency. The most often used VCO's in the market have positive KVCO's where the VCO frequency increases with an increase in control voltage. In this case, the charge pump current shall "source" current (to the main capacitor of the loop filter) when the VCO frequency becomes less than the desired frequency of operation.

2.7 Direct Sequence Spread Spectrum Baseband Processor(HFA3861)

The HFA3861B has on-board A/D's and D/A for analog I and Q inputs and outputs, for which the HFA3783 IF QMODEM is recommended. Differential phase shift keying modulation schemes DBPSK and DQPSK, with data scrambling capability, are available along with Complementary Code Keying to provide a variety of data rates. Both Receive and Transmit AGC functions with 7-bit AGC

control obtain maximum performance in the analog portions of the transceiver. The HFA3861B is housed in a thin plastic quad flat package (TQFP) suitable for PCMCIA board applications.

The HFA3861B transmitter is designed as a Direct Sequence Spread Spectrum Phase Shift Keying (DSSS PSK) modulator. It can handle data rates of up to 11Mbps (refer to AC and DC specifications). The various modes of the modulator are Differential Binary Phase Shift Keying (DBPSK) for 1Mbps, Differential Quaternary Phase Shift Keying (DQPSK) for 2Mbps, and Complementary Code Keying (CCK) for 5.5Mbps and 11Mbps. These implement data rates as shown in Table 3. The major functional blocks of the transmitter include a network processor interface, DPSK modulator, high rate modulator, a data scrambler and a spreader, as shown in Figure 7. CCK is essentially a quadra-phase form of M-ARY Orthogonal Keying. A description of that modulation can be found in Chapter 5 of: “Telecommunications System Engineering”, by Lindsey and Simon, Prentis Hall publishing.
The preamble is always transmitted as the DBPSK waveform while the header can be configured to be either DBPSK, or DQPSK, and data packets can be configured for DBPSK, DQPSK, or CCK. The preamble is used by the receiver to achieve initial PN synchronization while the header includes the necessary data fields of the communications protocol to establish the physical layer link. The transmitter generates the synchronization preamble and header and knows when to make the DBPSK to DQPSK or CCK switchover, as required.

- **Header/Packet Description**

The HFA3861B is designed to handle packetized Direct Sequence Spread Spectrum (DSSS) data transmissions. The HFA3861B generates its own preamble and header information. It uses two packet preamble and header configurations. The first is backwards compatible with the existing IEEE 802.11-1997 1 and 2Mbps modes and the second is the optional shortened mode which maximizes throughput at the expense of compatibility with legacy equipment.
In the long preamble mode, the device uses a synchronization preamble of 128 symbols along with a header that includes four fields. The preamble is all 1's (before entering the scrambler) plus a start frame delimiter (SFD). The actual transmitted pattern of the preamble is randomized by the scrambler. The preamble is always transmitted as a DBPSK waveform (1Mbps). The duration of the long preamble and header is 19□s.
In the short preamble mode, the modem uses a synchronization field of 56 zero symbols along with an SFD transmitted at 1Mbps. The short header is transmitted at 2Mbps. The synchronization preamble is all 0’s to distinguish it from the long header mode and the short preamble SFD is the time reverse of the long preamble SFD. The duration of the short preamble and header is 9□s.

- **Scrambler and Data Encoder Description**

The modulator has a data scrambler that implements the scrambling algorithm specified in the IEEE 802.11 standard. This scrambler is used for the preamble, header, and data in all modes. The data

scrambler is a self synchronizing circuit. It consists of a 7-bit shift register with feedback from specified taps of the register. Both transmitter and receiver use the same scrambling algorithm. The scrambler can be disabled by setting CR32 bit 2 to 1

- **Spread Spectrum Modulator Description**

  The modulator is designed to generate DBPSK, DQPSK, and CCK spread spectrum signals. The modulator is capable of automatically switching its rate where the preamble is DBPSK modulated, and the data and/or header are modulated differently. The modulator can support date rates of 1, 2, 5.5 and 11Mbps. The programming details to set up the modulator are given at the introductory paragraph of this section. The HFA3861B utilizes Quadraphase (I/Q) modulation at baseband for all modulation modes. In the 1Mbps DBPSK mode, the I and Q Channels are connected together and driven with the output of the scrambler and differential encoder. The I and Q Channels are then both multiplied with the 11-bit Barker word at the spread rate. The I and Q signals go to the Quadrature upconverter (HFA3724) to be modulated onto a carrier. Thus, the spreading and data modulation are BPSK modulated onto the carrier.

  For the 2Mbps DQPSK mode, the serial data is formed into dibits or bit pairs in the differential encoder as detailed above. One of the bits from the differential encoder goes to the I Channel and the other to the Q Channel. The I and Q Channels are then both multiplied with the 11-bit Barker word at the spread rate. This forms QPSK modulation at the symbol rate with BPSK modulation at the spread rate.

- **Transmit Filter Description**

  To minimize the requirements on the analog transmit filtering, the transmit section shown in Figure 11 has an output digital filter. This filter is a Finite Impulse Response (FIR) style filter whose shape is set by tap coefficients. This filter shapes the spectrum to meet the radio spectral mask requirements while minimizing the peak to average amplitude on the output. To meet the particular spread spectrum processing gain regulatory requirements in Japan, an extra FIR filter shape has been included that has a wider main lobe. This increases the 90% power bandwidth from about 11MHz to 14MHz. It has the unavoidable side effect of increasing the amplitude modulation, so the available transmit power is compromised by 2dB when using this filter (CR 11 bit 5). The receive section Channel Matched Filter (CMF) is also tailored to match the characteristics of the transmit filter.

2.8 Wireless LAN Medium Access Controller(HFA3841)

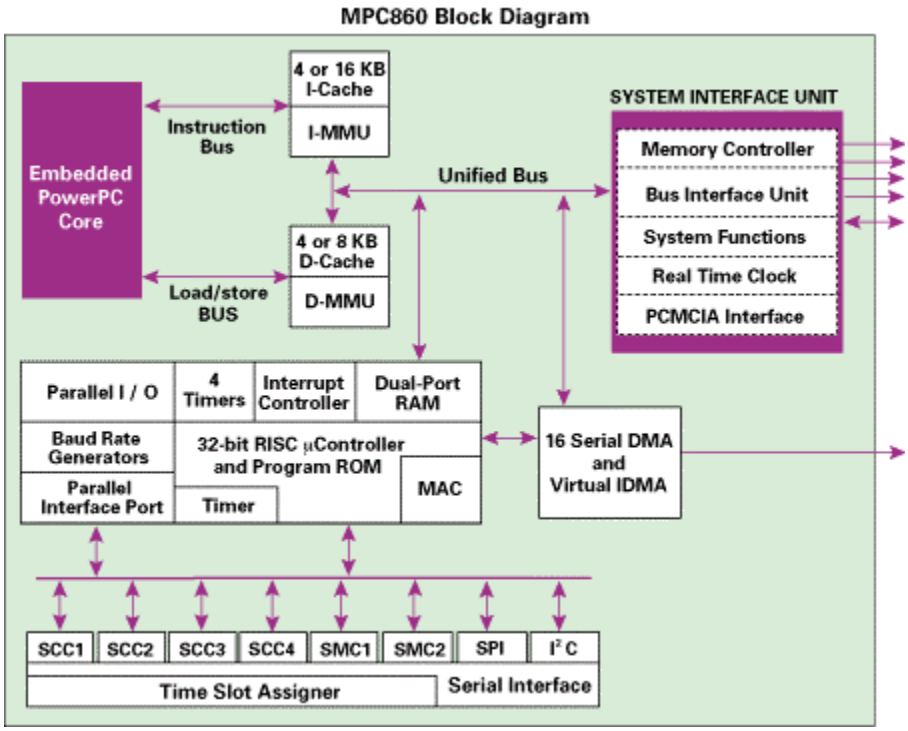
The HFA3841 is designed to provide maximum performance with minimum power consumption. External pin layout is organized to provide optimal PC board layout to all user interfaces. Firmware implements the full IEEE 802.11 Wireless LAN MAC protocol. It supports BSS and IBSS operation under DCF, and operation under the optional Point Coordination Function (PCF). Low level protocol functions such as RTS/CTS generation and acknowledgement, fragmentation and de-fragmentation,

and automatic beacon monitoring are handed without host intervention. Active scanning is performed autonomously once initiated by host command. Host interface command and status handshakes allow concurrent operations from multi-threaded I/O drivers.

2.9 Processor(MPC860/855)

The MPC860 PowerQUICC is a versatile one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications, excelling particularly in communications and networking products.

The PowerQUICC can be described as a next-generation MC68360 QUICC for network and data communication applications, providing higher performance in all areas of device operation including flexibility, extensions in capability, and integration.
The MPC860 PowerQUICC, like the MC68360 QUICC, integrates two processing blocks. One block is the Embedded PowerPC Core and the second block is a Communication Processor Module (CPM) that closely resembles the MC68360 CPM. The CPM supports four serial communications controllers (SCCs) on the device; however, there are actually eight serial channels -- four SCCs, two serial management controllers (SMCs), one serial peripheral interface (SPI) and one I^2C interface. This dual-processor architecture provides lower power consumption than traditional architectures because the CPM off-loads peripheral tasks from the Embedded PowerPC Core.



2.10 Flash ROM

Flash ROM's selectably used in AP as below.

- 32 pin 512Kbyte PLCC type AM29LV040B, M29W040B
- 40 pin 1Mbyte TSOP AM29LV080B, M29W040B, MT28F008
- 40 pin 2Mbyte TSOP AM29LV116D

2.11 Ethernet Interface

MPC860 SCC1 Port supports 10 Base-T Ethernet Interface at Access Point.

MPC860 Enternet Controller needs external Seirial Interface Adaptor(SIA) and Transceiver, WAP-1100E used LXT905LC device of LEVEL-ONE®.

The LXT905 Universal 10BASE-T Transceiver is designed for IEEE 802.3 Physical Layer (PHY) applications. It provides, in a single CMOS device, all the active circuitry for interfacing most standard 802.3 controllers to 10BASE-T media.