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UW2453/2453L
Data Sheet

(Preliminary)

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Revision History

| Revision	Date	Description of Change
0.0	March 18, 2005	Initial Version
0.1	July 20, 2005	Change GS5 and Bit[15] of Register 0101 step size from 0.5 to 3 dB

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1   Product Description

The UW2453 is a fully integrated single-chip transceiver (including PA) specifically designed for IEEE802.11b/g wireless local area networks (WLANs) applications. It supports data rate 6, 9, 12, 18, 24, 36, 48 and 54 Mbits/s in OFDM mode, 5.5 and 11 Mbits/s in CCK mode, 1 and 2 Mbits/s in DSSS mode. The UW2453 integrates a receiver, transmitter, VCO and PLL as well a power amplifier into a single IC. It uses direct conversion radio architecture to minimize external parts count and power consumption. Only one or two switches, one RF bandpass filter, one lowpass filter and several passive components are required to build a spec compliant 11b/g radio. The patented DC cancellation technique allows the receiver set its gain at super fast speed as required for the gain settling in the OFDM mode. The patent pending power amplifier design assures a very good TX linearity at a minimum current consumption. The UW2453 is fabricated by advanced SiGe BiCMOS process and is housed in a 48-pin QFN 7x7 mm^2 package. The UW2453L is a lower output power and lower current (TX) version of the UW2453. The UW2453L has the same package and pinout.

The low power consumption of the UW2453/UW2453L makes it an ideal candidate for WLAN applications in desktop/laptop PC, handheld devices and mobile handsets.

2   Features

o   IEEE 802.11 b/g specification compliant
o   6, 9, 12, 18, 24, 36, 48 and 54 Mbit/s in OFDM mode
o   1, 2, 5.5 and 11 Mbits/s in DSSS and CCK mode
o   2.4 to 2.5 GHz frequency operation
o   –87 dBm sensitivity at 11 Mbits/s CCK mode
o   –73 dBm sensitivity at 54M bits/s OFDM mode
o   High performance and low power consumption
o   Zero IF receive and direct conversion transmit architecture
o   Integrated low phase noise VCO and PLL loop filter
o   Integrated power amplifier
o   Shared RX and TX filter structure to minimize die size
o   High performance ΣΔ frequency synthesizer
o   High receiver and RSSI dynamic range
o   Support antenna diversity
o   Patented super fast DC cancellation
o   Ultra fast digital RX and TX gain settling time
o   Complementary 3-wire bus RX and TX gain control
o   +18 dBm transmit power (54 Mbits/s OFDM) for UW2453
o   +14 dBm transmit power (54 Mbits/s OFDM) for UW2453L
o   +21 dBm transmit power (11 Mbits/s CCK) for UW2453
o   +17 dBm transmit power (11 Mbits/s CCK) for UW2453L
o   MIMO transceiver support
o   5 uA sleep mode
o   Support 2.7 ~ 3.6 V supply
o   Small 48-pin leadless QFN 7x7 mm^2 package
o   SiGe BiCMOS technology
o   Low external component count

3   Block Diagram and Pin Configuration
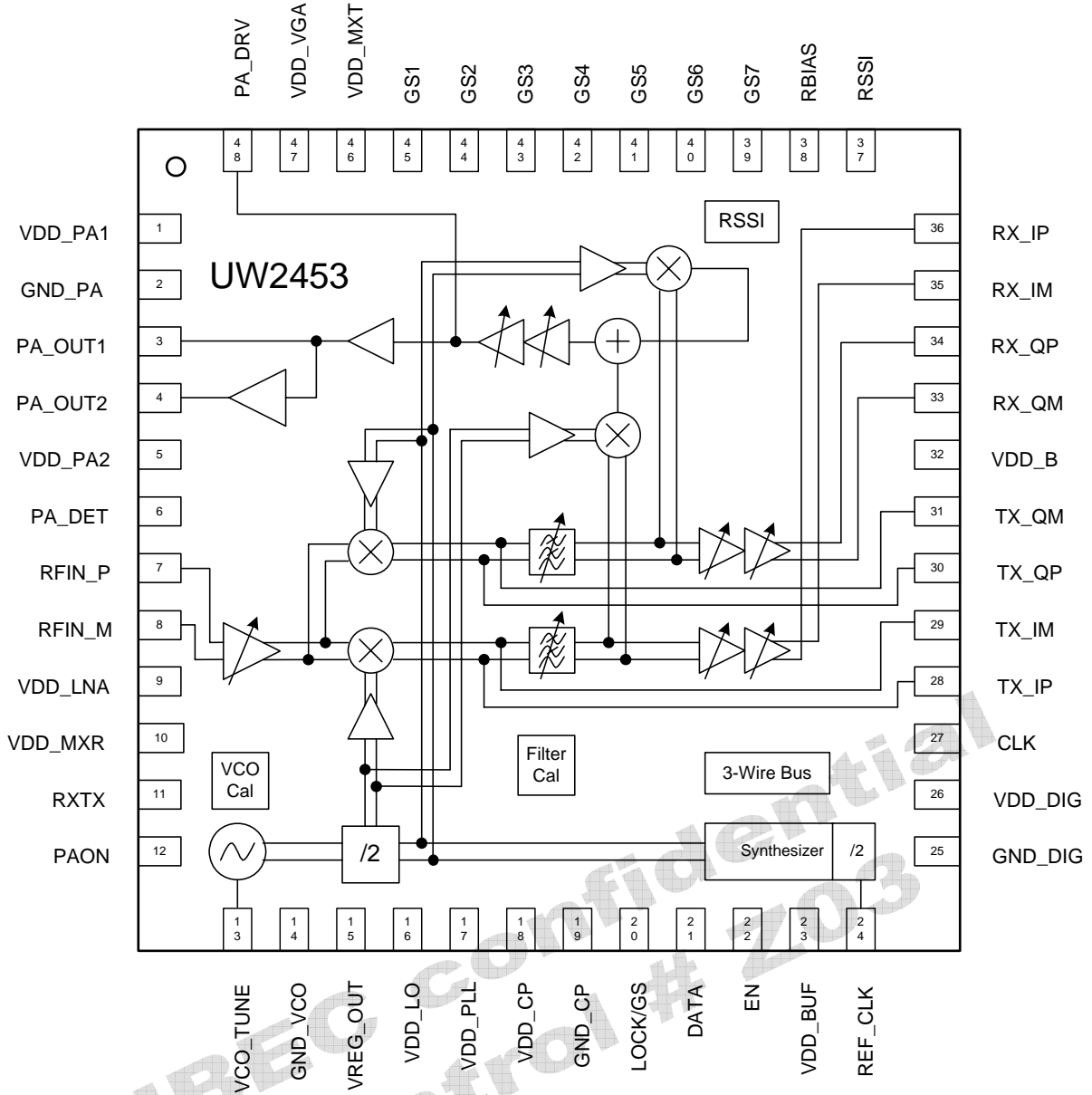
Figure 1.   UW2453/UW2453L Block Diagram and Pinning

Table 1.   Pin Descriptions

Pin type abbreviation: A = Analog, D = Digital, I = Input, O = Output

PIN	SYMBOL	TYPE	DESCRIPTION
1	VDD_PA1		PA power supply. Bypass with a cap as close to the pin as possible.
2	GND_PA		PA ground
3	PA_OUT1	AO	PA 1st stage open collector output.
4	PA_OUT2	AO	PA 2nd stage open collector output. It is TX RF output.
5	VDD_PA2		PA power supply. Bypass with a cap as close to the pin as possible.
6	PA_DET		PA power detector output.
7	RFIN_P	AI	LNA differential RF input (+)
8	RFIN_M	AI	LNA differential RF input (-)
9	VDD_LNA		LNA power supply. Bypass with a cap as close to the pin as possible.
10	VDD_MXR		RX mixer power supply. Bypass with a cap as close to the pin as possible.
11	RXTX	DI	RX and TX mode select
12	PAON	DI	PA turn on/off control
13	VCO_TUNE		PLL loop cap to ground
14	GND_VCO		VCO ground
15	VREG_OUT		Regulated supply for VCO. Bypass with caps to ground
16	VDD_LO		LO power supply. Bypass with a cap as close to the pin as possible.
17	VDD_PLL		PLL power supply. Bypass with a cap as close to the pin as possible.
18	VDD_CP		Charge-pump supply. Bypass with a cap as close to the pin as possible.
19	GND_CP		Ground for charge pump circuit
20	LOCK/GS	DIO	Synthesizer lock indicator or GS1~7 latch control
21	DATA	DI	Three-wire bus data signal
22	EN	DI	Three-wire bus enable
23	VDD_BUF		Clock buffer supply. Bypass with a cap as close to the pin as possible.
24	REF_CLK	AI	Reference clock input
25	GND_DIG		Ground for digital circuit
26	VDD_DIG		Digital circuit supply. Bypass with a cap as close to the pin as possible.
27	CLK	DI	Three-wire bus clock
28	TX_IP	AI	Transmitter I channel differential input (+)
29	TX_IM	AI	Transmitter I channel differential input (-)
30	TX_QP	AI	Transmitter Q channel differential input (+)
31	TX_QM	AI	Transmitter Q channel differential input (-)

32	VDD_B		Analog circuit supply. Bypass with a cap as close to the pin as possible.
33	RX_QM	AO	Receiver Q channel differential output (-)
34	RX_QP	AO	Receiver Q channel differential output (+)
35	RX_IM	AO	Receiver I channel differential output (-)
36	RX_IP	AO	Receiver I channel differential output (+)
37	RSSI	AO	RSSI output
38	RBIAS		Bias resistor pin. Connect an 12 kΩ (1%) resistor to the bias ground.
39	GS7	DI	2 dB VGA gain control pin
40	GS6	DI	4 dB VGA gain control pin
41	GS5	DI	8 dB VGA gain control pin
42	GS4	DI	16 dB VGA gain control pin
43	GS3	DI	32 dB VGA gain control pin
44	GS2	DI	LNA/filter gain control pin
45	GS1	DI	LNA/filter gain control pin
46	VDD_MXT		TX mixer power supply. Bypass with a cap as close to the pin as possible.
47	VDD_VGA		TX VGA power supply. Bypass with a cap as close to the pin as possible.
48	PA_DRV	AO	PA driver stage open collector output
	GND_SLUG		Chip ground. Connect to PCB ground plane using several via.

4 Operation Condition

Table 2. Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Storage temperature	-55	+150	°C
Supply voltage VDD pin to ground	-0.5	+4.2	V
Voltage applied to input pins	-0.5	VDD+0.5	V
Voltage applied to output pins	-0.5	VDD+0.5	V
Short circuit duration, to GND or VDD		5	sec

Table 3. Recommended Operating Conditions

PARAMETER	MIN	TYP	MAX	UNITS
Ambient Operating Temperature	-30		+85	°C
Supply Voltage	2.7	3.0	3.6	V
Logical high input voltage (for DI type pins)	VDD-0.4		VDD+0.3	V
Logical low input voltage (for DI type pins)	-0.3		0.4	V

5 Current Consumptions

Table 4. Current Consumptions

$T_A = 25\ ^oC$, VDD = 2.85 V

CHIP MODE	CONDITION	MIN	TYP	MAX	UNIT
SLEEP	Register 0000, Mode Bits = 0000		5		uA
IDLE	Register 0000, Mode Bits = 0001		28		mA
TX (18 dBm OFDM UW2453)	Register 0000, Mode Bits = 0010, RXTX=0		228		mA
TX (14 dBm OFDM UW2453L)	Register 0000, Mode Bits = 0010, RXTX=0		164		mA
RX	Register 0000, Mode Bits = 0010, RXTX=1		76		mA
CAL_FIL	Register 0000, Mode Bits = 0011		3		mA
CAL_VCO	Register 0000, Mode Bits = 0100		22		mA
RESET	Register 0000, Mode Bits = 0111		NA		mA

6   UW2453/UW2453L Functional Description

The UW2453/UW2453L receiver consists of a LNA, a pair of down-conversion mixers, I&Q channel filters, I&Q variable gain amplifiers (VGA), RSSI and programmable DC blocking cancellation blocks. The LO generation circuits (VCO, PLL and buffers) are shared with the receiver and transmitter. The LNA features a differential input for high performance. An external balum matching network is required. The LNA has 2 stepped gains. Along with one stepped gain inside the channel filter, three stepped gains are achieved in the receive chain from the LNA to the channel filters and they are controlled by two digital I/O pins, GS1 and GS2. The additional receive gain is realized by the RX VGA. The RX VGA has a gain resolution of 2 dB and the gain is set by Pins GS3~GS7. Pin GS7 sets a two dB change. Since the RX gain is set by the digital I/O pins, fast gain settling is realized. The RX gain can also be set by the regular or 3-wire bus in addition to the pins GS1~GS7.

The UW2453/UW2453L features a patented DC blocking circuit and the DC blocking circuit settles the receive DC offset for less than 10 mV at the RX outputs within 400 ns for any gain size change. To have a better control over the DC settling process, the settling time is programmable.

To set a proper RX gain without a prior knowledge of the received signal strength, the UW2453/UW2453L only needs a maximum of three times of gain adjustment with the help of the high dynamic range RSSI output. When the input signal is below –41 dBm, only two times of gain adjustment is required thanks to the high dynamic range of the RSSI circuit.

The UW2453/UW2453L also supports antenna diversity. However, antenna diversity requires a total settling time equivalent to a maximum of four times of gain adjustment. That means if in no diversity case, the worst total gain settling time is 2.4 us, it is 3.2 us with diversity.

Before the receiver properly demodulates the signal, filter and VCO calibration are needed. The filter and VCO calibration finds the correct filter corner frequency and VCO subband respectively, amid process, supply and temperature variation. The VCO and filter calibration are self-contained and no support from DSP side is required.

One unique feature is the receiver and transmitter share a pair of I&Q channel filter in order to minimize the die size and cost. However, the filter bandwidth in RX and TX mode can be independently programmed, thanks to the innovative design.

The switch between receive and transmit is controlled by Pin RXTX in the RXTX_EN chip mode. This pin also determines the filter bandwidth in conjunction with other register settings.

The transmitter features direct conversion architecture with +18 dBm output power with OFDM signal and +21 dBm output power with CCK signal with the integrated power amplifier for the UW2453 while the corresponding numbers are 14 and 17 dBm for the UW2453L. The output power adjustment range is 16 dB in one dB step. Pins GS1 to GS4 are used to set the TX front end gain (16 dB range). Like the receiver, the TX front end gain can also be programmed by the regular 3-wire bus.

The LO generation scheme of the UW2453/UW2453L employs a divided by 2 scheme to minimize pulling effect and to get a better phase imbalance. The VCO operates at the twice of the channel frequency. Additional feature is the ΣΔ frequency synthesizer having a fine frequency resolution. The wider loop bandwidth allowed by the ΣΔ frequency synthesizer is also helpful in tracking the VCO pulling and pushing effect. The VCO has a switched band design such that low phase noise, low VCO gain factor and high stability are realized. The advanced VCO calibration scheme makes it possible that the carrier frequency is always in the middle of one of the VCO bands. After reprogramming the channel frequency, a VCO calibration action is required. The PLL charge pump current is programmable so that the VCO gain variation for different bands can be compensated.

The UW2453/UW2453L has a power-up reset to set the registers to their default values. There is also a reset mode to allow the 3-wire bus to reset the IC at any time. After a reset, the UW2453/UW2453L automatically enters the sleep mode.

Pin 20 (LOCK/GS) is a special input/output pin. It can be programmed as the PLL lock detector output or as an enable pin for Pin GS1~GS7. If Pin 20 is configured as the GS1~GS7 enable pin, when Pin 20=1, any change on GS1~GS7 will cause RX or TX gain change. When Pin 20=0, any change on GS1~GS7 has no effect

on RX/TX gain and the receiver or transmitter uses the last GS1~GS7 values when Pin 20=1. That is a high to low transition will latch the GS1~GS7 value. This feature is useful so that multiple of the UW2453/UW2453L is used in a MIMO configuration without doubling or tripling the parallel control pins.

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7   Receiver AC Characteristics

Table 5.   Receiver AC Characteristics

Typical values are at $T_A = 25\ ^oC$, VDD = 2.85 V, LO frequency=2.447 GHz

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
RF input frequency		2.4		2.5	GHz
RF input range	Measured at balun matching input (DSSS/CCK)	-97		10	dBm
	Measured at balun matching input (OFDM)	-92		4	
LO frequency	VCO frequency divided by 2	2.4		2.5	GHz
LO leakage	Measured at balun matching network input			-65	dBm
Input return loss	External matched to 50Ω source by a balun matching network and for all gain range	-10	-12		dB
RX stepped voltage gain	GS1=1, GS2=1		48		dB
	GS1=1, GS2=0		32		
	GS1=0, GS2=1 or 0		9		
RX VGA maximum gain	GS3 GS4 GS5 GS6 GS7 = 11111		46		dB
RX VGA minimum gain	GS3 GS4 GS5 GS6 GS7 = 00000		-16		dB
RX VGA gain step	GS3		32		dB
	GS4		16		
	GS5		8		
	GS6		4		
	GS7		2		
Maximum RX voltage gain (Note 1)	GS1 GS2 GS3 GS4 GS5 GS6 GS7 = 1111111		94		dB
Minimum RX voltage gain (Note 1)	GS1 GS2 GS3 GS4 GS5 GS6 GS7 = 0000000		-7		dB
Gain settling time (Note 2)	Any gain size change		300		ns
DSB noise figure (Including matching)	GS1=1, GS2=1, VGA gain = 22 dB		3		dB
	GS1=1, GS2= 0, VGA gain = 22 dB		7		
	GS1=0, GS2=1, VGA gain = 22 dB		24		
	GS1=0, GS2=0, VGA gain = 22 dB		40		
Input IP3 (Including matching) (Note 3)	GS1=1, GS2=1, VGA gain = 16 dB		-12		dBm
	GS1=1, GS2= 0, VGA gain = 16 dB		-8		
	GS1=0, GS2=1, VGA gain = 16 dB		10		

	GS1=0, GS2=0, VGA gain = 16 dB		21		
Input IP2 (Including matching) (Note 4)	GS1=1, GS2=1, VGA gain = 16 dB	30			dBm
	GS1=1, GS2= 0, VGA gain = 16 dB	30			
	GS1=0, GS2=1, VGA gain = 16 dB	50			
	GS1=0, GS2=0, VGA gain = 16 dB	66			
I&Q Gain Mismatch	Without calibration	-0.3		0.3	dB
I&Q Phase Imbalance	Without calibration	-2		2	deg
Channel filter characteristics (after calibration)	Passband ripple (peak-to-peak 0.3~8.5 MHz)			0.5	dB
	Max group delay (peak-to-peak 0.3~8.5 MHz)		50		ns
	Attenuation @ freq >= 12 MHz	8			dB
	Attenuation @ freq >= 15 MHz	25			dB
	Attenuation @ freq >= 25 MHz	60			dB
CCK adjacent channel attenuation @25 MHz	Referenced to in-band CCK signal power	50			dB
OFDM adjacent channel attenuation @25 MHz	Referenced to in-band OFDM signal power	45			dB
3 dB DC blocking frequency	After DC settling		10		kHz
Linear RSSI voltage output	Input power –95 ~ -40 dBm. GS1GS2=11	0.7		2	V
	Input power –90 ~ -22 dBm. GS1GS2=10	0.4		2	V
	Input power –67 ~ 1 dBm. GS1GS2=01 or 00	0.4		2	V
RSSI slope	Average RSSI voltage change per 1 dB input level change		23.5		mV /dB
RSSI error	With OFDM short preamble	-3		3	dB
RSSI settling time	GS1GS2=11 change to GS1GS2=10 or 0x while GS3=GS4=GS5=GS6=GS7=1		300		ns
Resistive RSSI output load		10			kΩ
Capacitive RSSI output load				5	pF
TX to RX switching time	Output signal within 1 dB of final value with CW input			2	us
Resistive I&Q output load	Pin to ground/differential	5/10			kΩ
Capacitive I&Q output load	Pin to ground/differential			6/3	pF
Nominal I&Q output level	With gain adjustment. Differential peak to peak.		1000		mV$_{pp}$
Output 1 dB compression	Differential peak to peak	1.5			V$_{pp}$
I&Q output DC offset	After DC cancellation			10	mV
I&Q output common mode			1.2		V

Note 1: The voltage gain is measured by the voltage ratio between the differential output voltage at I or Q output and the input voltage at the balun matching network input.

Note 2: Guaranteed by design and characterization.

Note 3: At balun input two tones at 19 and 31 MHz offset from carrier frequency and each tone power –35 dBm are applied. IM3 is measured at 7 MHz. The inband gain at each setting is used to refer output IM3 back to input.

Note 4: At balun input two tones at 19 and 26 MHz offset from carrier frequency and each tone power –35 dBm are applied. IM2 is measured at 7 MHz. The inband gain at each setting is used to refer output IM2 back to input.

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8 Transmitter AC Characterictics

Table 6.   Transmitter AC Characteristics

Typical values are at $T_A = 25\ ^oC$, VDD = 2.85 V, LO frequency=2.447 GHz

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
RF carrier frequency		2.4		2.5	GHz
LO frequency	VCO frequency divided by 2	2.4		2.5	GHz
Maximum RF output, single ended	OFDM		18		dBm
	CCK		21		dBm
Minimum RF output	OFDM		2		dBm
	CCK		5		dBm
Input resistance	Differential	20			kΩ
Input capacitance	Differential			5	pF
OFDM input level			100	200	mVrms
CCK input level			150	400	mVrms
Input common mode voltage		1.2	1.5		V
TX maximum gain (UW2453)	GS1 GS2 GS3 GS4 GS5 = 11111		38		dBm/ dBV
TX maximum gain (UW2453L)	GS1 GS2 GS3 GS4 GS5 = 11111		34		dBm/ dBV
TX minimum gain (UW2453)	GS1 GS2 GS3 GS4 GS5 = 00000		20		dBm/ dBV
TX minimum gain (UW2453L)	GS1 GS2 GS3 GS4 GS5 = 00000		16		dBm/ dBV
TX VGA gain step	Controlled by GS1 or Bit[19] of Register 0101		8		dB
	Controlled by GS2 or Bit[18] of Register 0101		4		
	Controlled by GS3 or Bit[17] of Register 0101		2		
	Controlled by GS4 or Bit[16] of Register 0101		1		
TX filter gain step	Controlled by GS5 or Bit[15] of Register 0101		3		dB
Carrier suppression	At 100 mV RMS input		-25		dBc
TX spectrum mask for CCK at max power	11 <= offset frequency < 22 MHz	-36			dBr
	Offset frequency >= 22 MHz	-56			
TX spectrum mask for OFDM at max power	Offset frequency > = 10 MHz	-26			dBr
	Offset frequency >= 20 MHz	-36			
	Offset frequency >=30 MHz	-49			

TX EVM	At 54 Mbps and max power		-28	-26	dB
Sideband suppression	Without mismatch calibration		33		dBc
RX to TX switching time	With 1 dB of final signal power level			2	us
TX reconstruction filter	Passband ripple (peak-to-peak 0~8.5 MHz)		0.5		dB
	Max Group Delay (peak-to-peak 0~8.5 MHz)			50	ns
	Attenuation @30 MHz	50			dB
	Attenuation @40 MHz	60			dB
TX noise floor	At 40 MHz offset frequency. 1 MHz measurement bandwidth			-110	dBm/Hz
2nd harmonic power	Single tone input at max power			-15	dBm

Table 7.   VCO and PLL AC Characteristics

Typical values are at T_A = 25 ^{o}C, VDD = 2.85 V, LO frequency=2.447 GHz

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Reference frequency			20/40		MHz
Reference clock level		600			mVpp
Reference clock input impedance		10			kΩ
PFD comparison frequency			20		MHz
PLL frequency resolution	At 20 MHz comparison frequency		20		Hz
Charge pump current	Programmable in 100, 200, 300 and 500 uA	100		500	uA
Charge pump current mismatch				10	%
Charge pump compliant voltage		0.3		VDD-0.3	V
VCO frequency		4.8		5.0	GHz
LO frequency	VCO frequency divided by 2	2.4		2.5	GHz
VCO gain (Kvco)			50		MHz/V
VCO+PLL phase noise after divide by 2	At 100 kHz offset		-90		dBc/Hz
	At 30 MHz offset		-138		dBc/Hz
	Integrated from offset frequency 10 kHz to 8.5 MHz		-38		dBc

9 3-Wire Bus and Register Maps

The UW2543 features an 80 MHz 3-wire bus for various control purposes. There are eight write-only registers defined and each register has 20 data bits. Each register is identified by a four-digit address. The address is transmitted first before 20 bit data. The 3-wire bus consists of three digital lines: clock (Pin CLK), data (Pin DATA) and enable (Pin EN). When Pin EN is asserted low and the clock is active, A0 is the first bit clocked into the UW2453/UW2453L and D19 is the last bit. However, the 20 bit long data is latched by the rising edge of enable (EN). Note in this regular programming mode, the data length has to be 20 bits plus 4 address bits. Hence, the reserved or test bits need to be programmed according to their default values.

9.1 3-Wire Bus Data Format

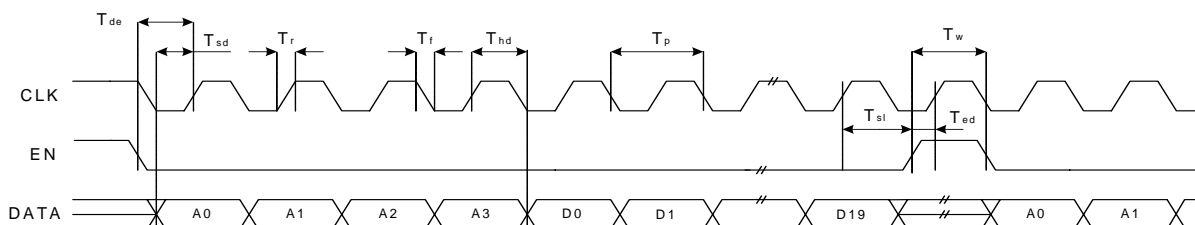| Address Bits				Data Bits														
A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	…	D13	D14	D15	D16	D17	D18	D19

9.2 3-Wire Bus Timing

Figure 2. 3-Wire Bus Timing Diagram for Regular Programming

Table 8.   3-Wire Bus Timing Parameters

PARAMETERS	MIN	TYP	MAX	UNIT
T_r: Clock rising time			2.5	ns
T_f: Clock falling time			2.5	ns
T_p: Clock period	12.5			ns
T_{ed}: 3-wire bus enable to disable setup time	2.5			ns
T_{de}: 3-wire bus disable to enable setup time	2.5			ns
T_{sl}: Data latch setup time	2.5			ns
T_w: Minimum 3-wire bus disable width	5			ns
T_{sd}: Data setup time	2.5			ns
T_{hd}: Data hold time	2.5			ns

9.3 Register Maps

REGISTER Address 0000 (A0A1A2A3): Chip Mode Control

BITS	NAME	DEFAULT	DESCRIPTION	
[19:16]	Mode	0000	Chip modes (see chip mode table)	
			0000: SLEEP	0001: IDLE
			0010: RXTX_EN	0011: CAL_FIL
			0100: Reserved	0101: CAL_VCO
			0110: Reserved	0111: RESET
[15]	TXGM	0	TX gain set mode 0: TX gain set by Pins GS1~GS5 1: TX gain set by Register Bits TXG	
[14]	RXGM	0	RX gain set mode 0: RX gain set by Pins GS1~GS7 1: RX gain set by Register Bits RXG_s and RXG_b	
[13]	RSSI$_{off}$	1	RSSI circuit powered up 0: RSSI circuit powered up; 1: RSSI circuit powered down	
[12:11]	DCBTa	00	2nd DC blocking extra precharge time (**Note 1**) 00: 0 ns; 01: 50 ns 10: 100 ns; 11: 150 ns	
[10:9]	DCBTb	00	1st and 2nd DC blocking settling time (**Note 1**) 00: 200 ns; 01: 250 ns 10: 300 ns; 11: 350 ns	
[8:7]	DCBTc	00	2nd DC blocking extra settling time (**Note 1**) 00: 0 ns; 01: 50 ns 10: 100 ns; 11: 150 ns	
[6]	DCHP2	0	2nd DC blocking highpass corner frequency	
[5]	DCHP	1	1st DC blocking highpasss corner frequency	
[4:3]	HPV	00	1st DC blocking corner frequency controlling voltage (V) 00: 0; 01: 0.3; 10: 0.6; 11: 0.9	
[2]	LOCK/GS	1	Pin is configured as 0: GS1~GS7 pin input enable control 1: Lock detector output	
[1]	RSSIrc	0	RSSI range control 0: Reduced range 1: Normal range	
[0]		0	Test/reserved bit	

Note 1: The total DC cancellation time equals DCBTa+DCBTb+DCBTc+50 ns.

Table 9. **Chip Mode Description Table**

CHIP MODE	DESCRIPTION
SLEEP	Sleep mode. Whole chip powered down except 3-wire bus. 3-wire bus is always active for all chip modes when the IC power supply is on.
IDLE	Idle mode. VCO, synthesizer and reference clock buffer are powered up. The rest circuits are powered down.
RXTX_EN	If Pin RXTX=1, UW2453/UW2453L is in the receive mode. LNA, RX mixers, RX filters, RX VGA, RX output buffers, VCO, synthesizer, divide by 2, RX LO buffers and reference clock buffer are powered up. RSSI is powered up or down independently by Bit "$RSSI_{off}$". The rest circuits are powered down.
	If Pin RXTX=0, UW2453/UW2453L is in the transmit mode. PA driver, TX mixers, TX VGA, TX filters, VCO, synthesizer, divide by 2, TX LO buffers and reference clock buffer are powered up. The rest circuits are powered down.
CAL_FIL	RX and TX filter calibration mode. Only the filter tuning circuit and reference clock buffer are powered up. After the filter calibration, UW2453/UW2453L enters the sleep mode automatically.
CAL_VCO	VCO calibration mode. Only VCO, synthesizer, divide by 2, reference clock buffer and VCO calibration circuit are powered up. After the VCO calibration, UW2453/UW2453L enters the idle mode automatically.
RESET	Reset mode. Reset all register bits to default. Enter SLEEP mode after reset.

REGISTER Address 0001: ΣΔ synthesizer

BITS	NAME	DEFAULT	DESCRIPTION
[19:14]	N_{off}	111010	Offset integer dividing ratio. N_{off} = N-64 **(Note 1)**
[13:12]	CPC	11	Charge pump current. 00: 100 uA; 01: 200 uA. 10: 300 uA; 11: 500 uA
[11]	DIV2	0	PLL comparison frequency is half of reference frequency 0: yes; 1: no
[10]	$LOCK_{en}$	0	PLL lock indicator enable 0: enabled; 1: disabled
[9]	T_{widen}	1	Widen backlash time 0: no; 1: yes
[8:0]		000000000	Test/reserved bits

Note 1: Denote channel center frequency F_c in MHz, let $2F_c/F_{ref} = N+\Delta N$ if DIV2=0 and $F_c/F_{ref} = N+\Delta N$ if DIV2=1. N is an integer and ΔN is a fraction number.

REGISTER Address 0010: ΣΔ synthesizer fractional divide ratio

BITS	NAME	DEFAULT	DESCRIPTION
[19:8]	K	010110011001	Integer input of ΣΔ modulator. (**Note 1**)
[7:0]			Test/reserved bits

Note 1: Denote channel center frequency F_c in MHz, let $2F_c/F_{ref} = N+\Delta N$ if DIV2=0 and $F_c/F_{ref} = N+\Delta N$ if DIV2=1. N is an integer divide ratio and ΔN is a fractional divide ratio. K equals to the integer part of $\Delta N*2^{12}$.

REGISTER Address 0011: VCO

BITS	NAME	DEFAULT	DESCRIPTION
[19]	MVCO	0	Manual VCO band selection enable 0: disabled; 1: enabled
[18:14]	VCO_band	10000	VCO band selection if MVCO=1 00000: highest band (frequency); 11111: lowest band
[13:11]	VCO_off	000	VCO band offset from the calibrated band 000: no offset 001: offset one band higher 010: offset two bands higher 011: offset three bands higher 100: no offset 101: offset one band lower 110: offset two bands lower 111: offset three bands lower
[10:9]	VCO_C	00	VCO current level (mA) 00: normal; 01: normal+3 10: reserved; 11: normal+6
[8:7]	RXLO_C	01	RX LO current level (uA) 00: 225; 01: 300; 10: 375; 11: 450
[6:5]	TXLO_C	000	TX LO current level (uA) 00: 200; 01: 250; 10: 300; 11: 350
[4:0]		00000	Test/reserved bits

REGISTER Address 0100: Receiver Gain

BITS	NAME	DEFAULT	DESCRIPTION
[19:18]	RXG_s	11	RX stepped gain set by 3-wire bus when RXGM=1 00 or 01: 9 dB; 10: 32 dB; 11: 48 dB.
[17:13]	RXG_b	11111	RX VGA gain set by 3-wire bus when RXGM=1 11111: 46 dB; 11110: 44 dB; … 00001: -14 dB; 00000: -16 dB
[12:0]		0000000000000	Test/reserved bits.

REGISTER Address 0101: Transmitter Gain

BITS	NAME	DEFAULT	DESCRIPTION
[19:16]	TXG	1111	TX VGA gain control 16 dB range in 1dB step set by 3-wire bus when TXGM=1 1111:15 dB; 1110: 14 dB; 1101: 13 dB; …; 0001: 1 dB; 0000: 0 dB
[15]	TRFG	1	TX/RF filter gain control set by 3-wire bus when TXGM=1 0: 0 dB; 1 3 dB
[14:12]	PTAT	010	TX power current parameter
[11:8]	PA1	1011	PA 1st stage current setting
[7:4]	PA2	1010	PA 2nd stage current setting
[3:0]		0000	Test/reserved bits

REGISTER Address 0110: Filter

BITS	NAME	DEFAULT	DESCRIPTION
[19]	RTXF$_{en}$	0	Manual RX/TX filter tuning enable 0: disabled; 1: enabled
[18:11]	RTXF$_{tune}$	01101011	Manual RX/TX filter tuning parameter 00000000: widest TX filter bandwidth … 11111111: narrowest TX filter bandwidth
[10:5]	RXF$_{off}$	000000	Offset filter tuning value from the filter calibration for RX filter 000000: no offset 000001: minimum positive (increase filter BW) offset … 011111: maximum positive offset 100000: no offset; 100001: minimum negative (decrease filter BW) offset … 111111: maximum negative offset
[4:0]	TXF$_{off}$	00000	Offset filter tuning value from the filter calibration for TX filter 00000: no offset 00001: minimum positive (increase filter BW) offset … 11111: maximum positive offset

REGISTER Address 0111: Test

BITS	NAME	DEFAULT	DESCRIPTION
[19]	TXG$_{ten}$	0	TX gain control enable in the test mode 0: disabled; 1: enabled
[18:15]	TST_PA	1111	PA driver current mode
[14:7]	TST_VGA	11111000	TX VGA current mode
[6]	TST_PA2	1	PA driver current reduced by half
[5]	TST_MIX	1	Mixer current mode
[4:0]		00000	Reserved

10　Application Notes

10.1　Suggested Power up Sequence

After the UW2453/UW2453L is powered up, certain procedure is required as follows

(1) Perform the filter calibration by programming register bits MODE=0011. The calibration time is 10 us. After the calibration, UW2453/UW2453L enters the sleep mode (MODE=0000).

(2) Perform VCO calibration with the channel planned to use by programming register bits MODE=0101. Reprogram the synthesizer if the default is not Channel 8. The VCO calibration takes 40 us. Always perform VCO calibration if there is a channel change afterwards. After the calibration, UW2453/UW2453L enters the idle mode. It takes the PLL less than 50 us to lock to the reference clock.

10.2　Suggested RX Stepped Gain Switching Point

The following switching points are valid for both AGC with or without the on chip RSSI assistance with two step switching.

(1) GS1 GS2 switches from 11 to 10: input equals to -49 dBm at LNA input;

(2) GS1 GS2 switches from 10 to 01 or 00: input equals to -34 dBm at LNA input;

With one step switching, i.e., when GS1 GS2 is switched from 11 to 01 or 00, the switching point is -34 dBm.

10.3　Suggested RX AGC Scheme Using RSSI Output

To perform the on chip RSSI measurement, GS3 through GS7 have to be set to 1. For each of four GS1 and GS2 combinations, there is a RSSI curve associated. The RSSI curves with GS1GS2=11 and GS1GS2=01 or 00 cover the widest dynamic range and therefore, these two curves are suggested for RX AGC with RSSI assistance. The procedure is as follows:

(1) Turn on RX and set GS1~GS7=1111111 or other proper value;

(2) Wait 300 ns or more;

(3) Measure and average RSSI for 300 ns, if the averaged RSSI voltage is greater than 2.1 V, go Step 4. Otherwise, go Step 9;

(4) Set GS1GS2=01 and keep GS3~GS7=11111;

(5) Wait 300 ns or more;

(6) Measure and average RSSI for 300 ns;

(7) Use RSSI curve for GS1GS2=11 to lookup the input power at LNA;

(8) Use the above gain switching point to find the GS1~GS7 setting according to the LNA input power and go Step11;

(9) Use RSSI curve for GS1GS2=01 to lookup the input power at LNA;

(10) Use the above gain switching point to find the GS1~GS7 setting according to the LNA input power and go Step11;

(11) Set the RX gain obtained from Step 8 or 10;

(12) Use I&Q ADC do a fine digital RSSI estimate and calculate the final gain adjustment in VGA;

(13) Setting the final VGA gain.

Note that the last fine gain adjustment only in VGA. This means that the GS1 and GS2 switching points may not comply the suggested switching points. It is obvious that AGC only needs a maximum of 3 times gain change to settle the correct RX gain.

## 10.4 Suggested Antenna Diversity Scheme Using RSSI Output

(1) Turn on RX and set GS1~GS7=1111111;

(2) Energy is detected;

(3) Measure and average RSSI output from the 1st antenna, if RSSI voltage is greater than 1.8 V, no antenna diversity is needed and go Step 9;

(4) Switch to the second antenna;

(5) Set GS1 or GS2 to 0 and set it back to 1 again after 25 ns (this activates the DC cancellation loop);

(6) Wait 300 ns or more;

(7) Measure and average RSSI output from the 2nd antenna;

(8) If RSSI (1st) is greater than RSSI (2nd) for at least 3 dB, switch back to the 1st antenna and go to Step 9. Otherwise, just go to Step 9;

(9) Do AGC gain setting as shown in 10.3.

Note that the antenna diversity based on carrier sensing or carrier sensing plus RSSI can follow a similar approach as described above.

11   Package Drawing
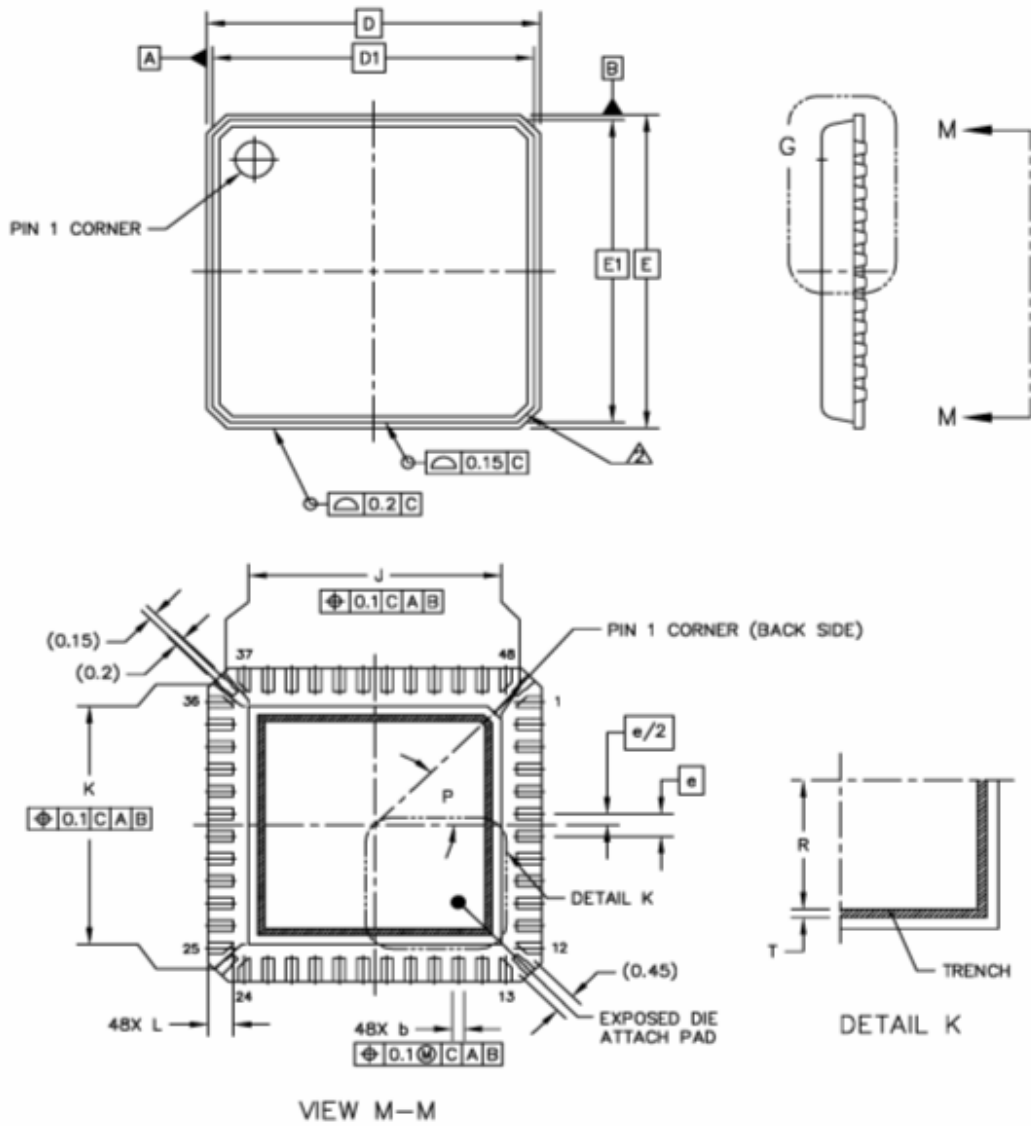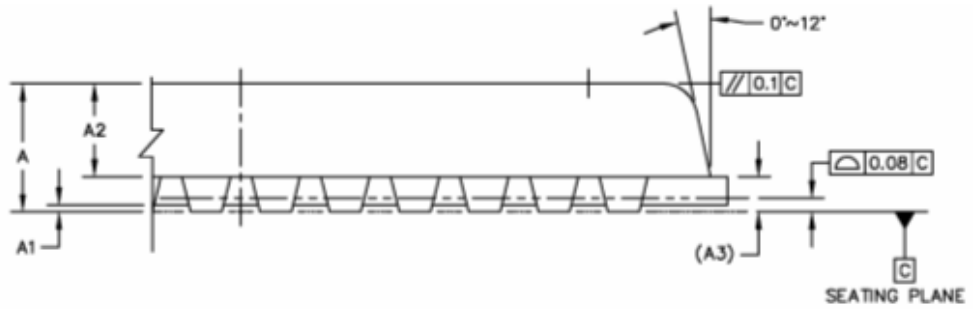
DETAIL G
VIEW ROTATED 90° CLOCKWISE

DIM	MIN	NOM	MAX	NOTES
A	0.8		0.9	1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
A1	0	0.02	0.05	
A2	0.611	0.65	0.689	⚠ EXACT SHAPE OF EACH CORNER IS OPTIONAL.
A3		0.203 REF.		
b	0.2	0.25	0.3	
D		7 BSC		
D1		6.75 BSC		
E		7 BSC		
E1		6.75 BSC		
e		0.5 BSC		
J	5.22	5.32	5.42	
K	5.22	5.32	5.42	
L	0.475	0.525	0.575	
P		45° REF		
R	2.21		2.41	
T	0.1		0.2	

UNIT	DIMENSION AND TOLERANCES	
MM	ASME Y14.5M	