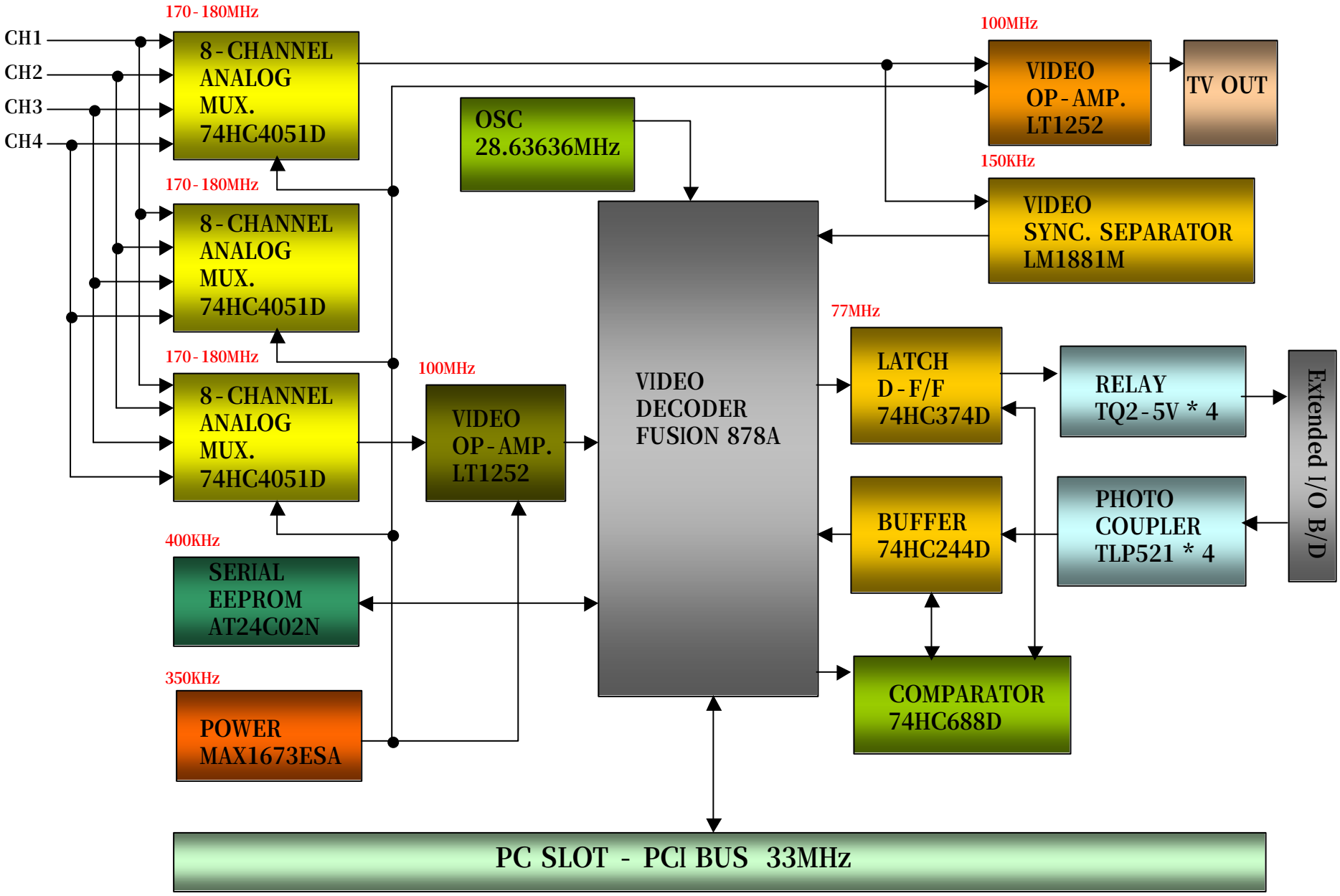
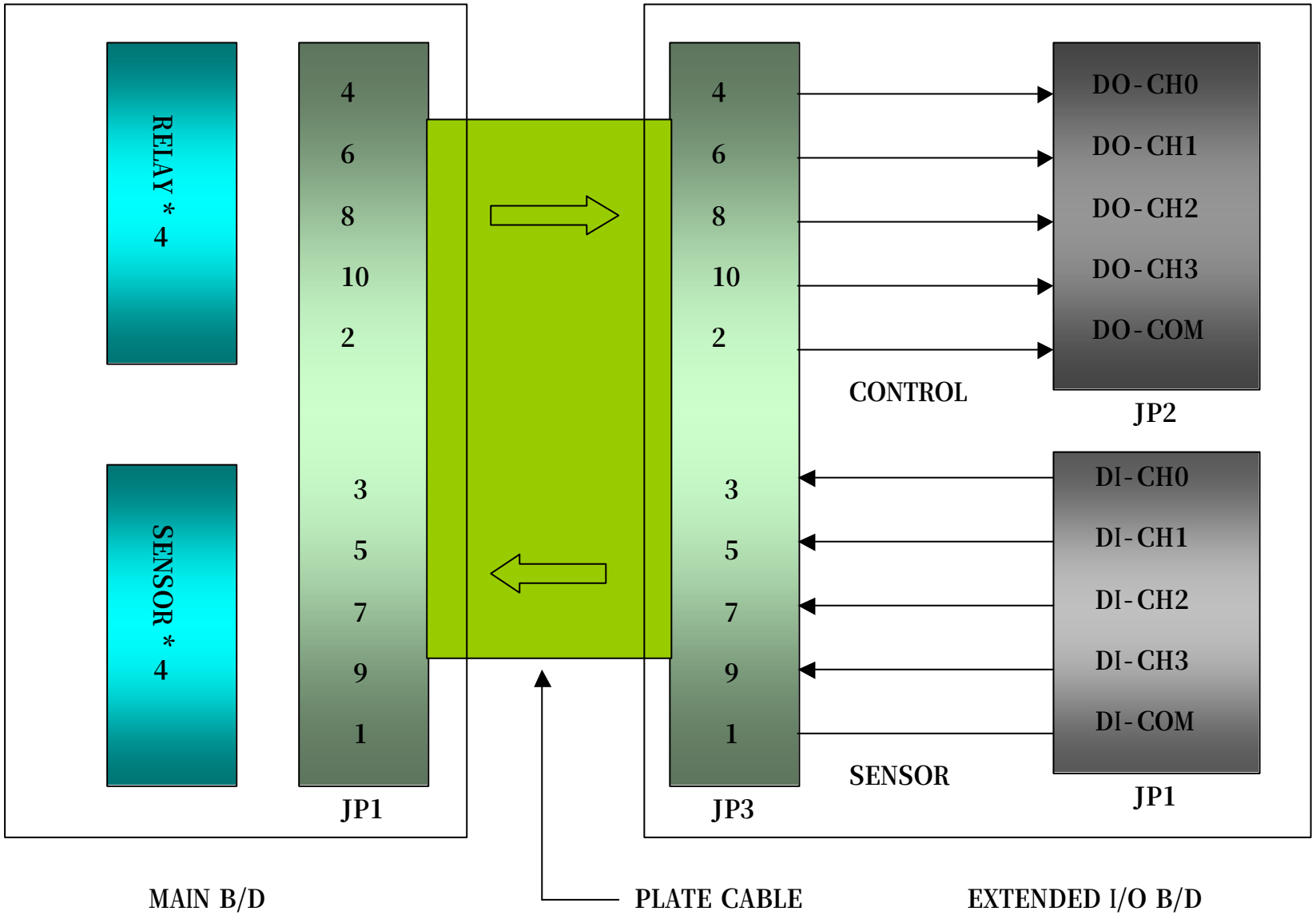
PDV-S100 MAIN B/D BLOCK DIAGRAM



PDV-S100 EXTENDED B/D BLOCK DIAGRAM



NOTICE> CONTROL = +12 VDC, 1A, SENSOR = TTL “L” ACTIVE

ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	typ.	UNIT	V_{CC} (V)	V_{EE} (V)	$V_{is(p-p)}$ (V)	CONDITIONS
	sine-wave distortion f = 1 kHz	0.04 0.02	% %	2.25 4.5	–2.25 –4.5	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig.14)
	sine-wave distortion f = 10 kHz	0.12 0.06	% %	2.25 4.5	–2.25 –4.5	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig.14)
	switch "OFF" signal feed-through	–50 –50	dB dB	2.25 4.5	–2.25 –4.5	note 1	R_L = 600 Ω; C_L = 50 pF (see Figs 12 and 15)
$V_{(p-p)}$	crosstalk voltage between control and any switch (peak-to-peak value)	110 220	mV mV	4.5 4.5	0 –4.5		R_L = 600 Ω; C_L = 50 pF; f = 1 MHz ($\overline{E}$ or S_n, square-wave between V_{CC} and GND, $t_r = t_f$ = 6 ns) (see Fig.16)
f_{max}	minimum frequency response (–3dB)	170 180	MHz MHz	2.25 4.5	–2.25 –4.5	note 2	R_L = 50 Ω; C_L = 10 pF (see Fig.13 and 14)
C_S	maximum switch capacitance independent (Y) common (Z)	 5 25	 pF pF				

AT24C02A Ordering Information

t_{WR} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT24C02A-10PC AT24C02AN-10SC AT24C02A-10TC	8P3 8S1 8T	Commercial (0°C to 70°C)
	3000	18	400	AT24C02A-10PI AT24C02AN-10SI AT24C02A-10TI	8P3 8S1 8T	Industrial (-40°C to 85°C)

MAXIM

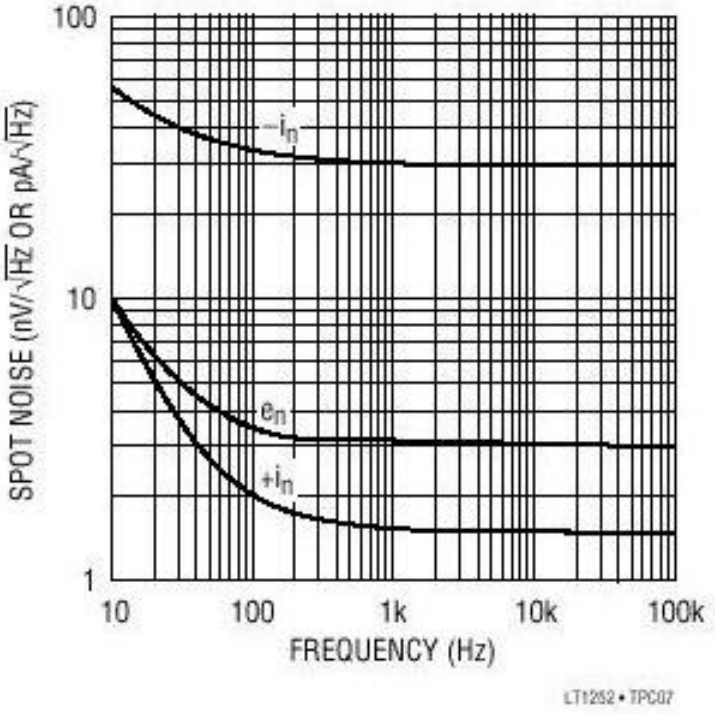
Regulated, 125mA-Output, Charge-Pump DC-DC Inverter

MAX1673

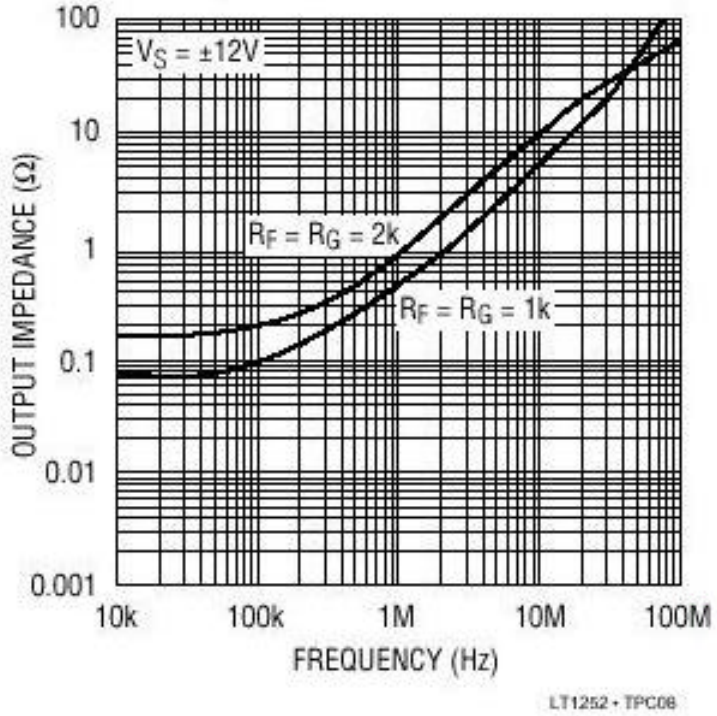
Features

- Regulated Negative Output Voltage (up to -1 x V_{IN})
- 125mA Output Current
- 35µA Quiescent Supply Current (Skip-mode regulation)
- 350kHz Fixed-Frequency, Low-Noise Output (Linear-mode regulation)
- 2V to 5.5V Input Range
- 1µA Logic-Controlled Shutdown

Spot Noise Voltage and Current vs Frequency

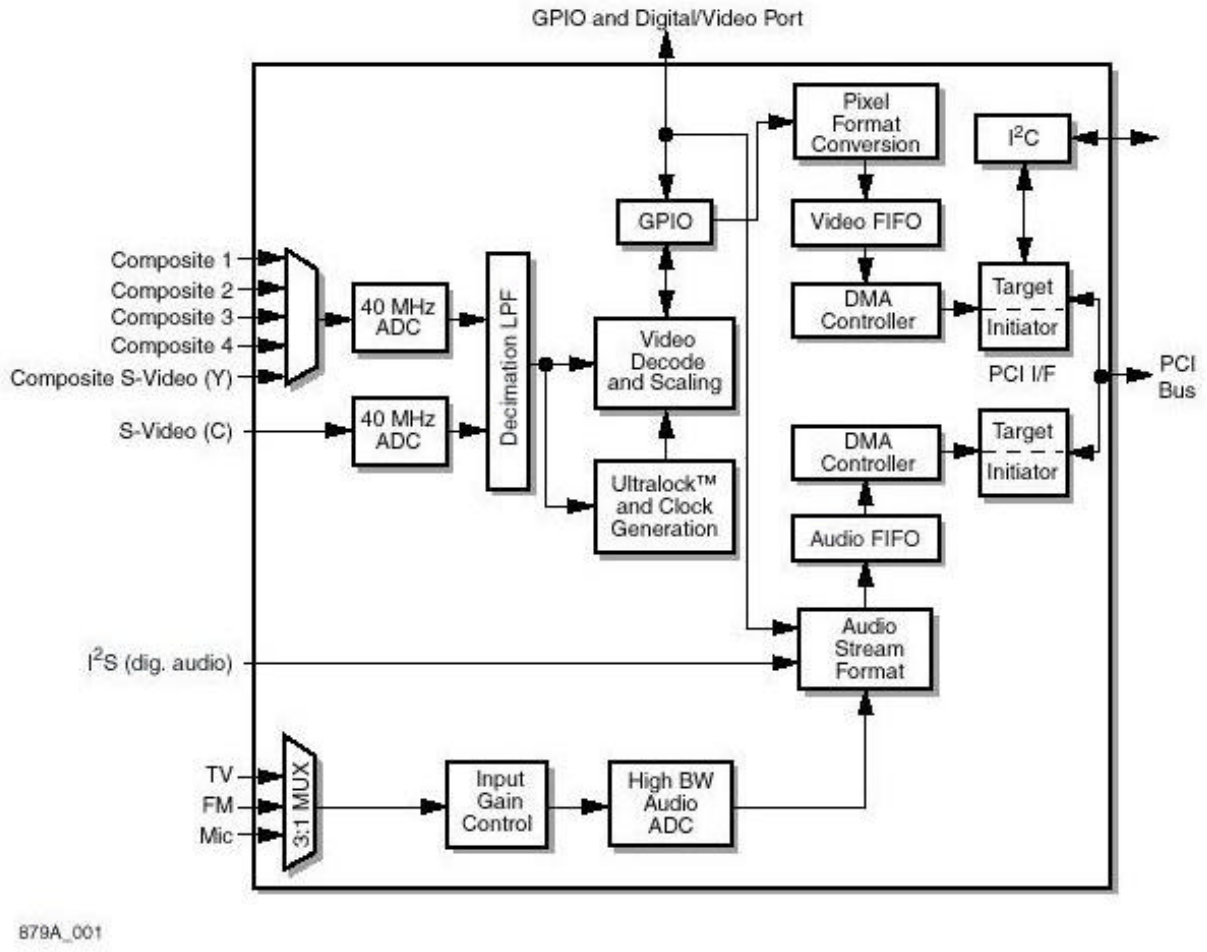


Output Impedance vs Frequency



FUSION878A(VIDEO DECODER) [EXTERNAL OSC : 28.63636MHz]

Functional Block Diagram



2.2 Composite Video Input Formats

Fusion 878A supports several composite video input formats. Table 2-1 shows the video formats and some of the countries in which each format is used.

Table 2-1. Video Input Formats Supported by the Fusion 878A

Format	Lines	Fields	F_{SC}	Country
NTSC-M	525	60	3.58 MHz	U.S., many others
NTSC-Japan(1)	525	60	3.58 MHz	Japan
PAL-B, G, H	625	50	4.43 MHz	Western/Central Europe, others
PAL-D	625	50	4.43 MHz	China
PAL-I	625	50	4.43 MHz	U.K., Ireland, South Africa
PAL-M	525	60	3.58 MHz	Brazil
PAL-N_C	625	50	3.58 MHz	Argentina
PAL-N	625	50	3.58 MHz	Paraguay, Uruguay
SECAM	625	50	4.406 MHz, 4.250 MHz	Eastern Europe, France, Middle East

NOTE(S):
(1) NTSC—Japan has 0 IRE setup.

LM1881M(VIDEO SYNC SEPARATOR)

National Semiconductor

April 2001

LM1881
Video Sync Separator

General Description

The LM1881 Video sync separator extracts timing information including composite and vertical sync, burst/back porch timing, and odd/even field information from standard negative going sync NTSC, PAL* and SECAM video signals with amplitude from 0.5V to 2V p-p. The integrated circuit is also capable of providing sync separation for non-standard, faster horizontal rate video signals. The vertical output is produced on the rising edge of the first serration in the vertical sync period. A default vertical output is produced after a time delay if the rising edge mentioned above does not occur within the externally set delay period, such as might be the case for a non-standard video signal.

Features

- AC coupled composite input signal
- >10 kΩ input resistance
- <10 mA power supply drain current
- Composite sync and vertical outputs
- Odd/even field output
- Burst gate/back porch output
- Horizontal scan rates to 150 kHz
- Edge triggered vertical output
- Default triggered vertical output for non-standard video signal (video games-home computers)

74HC374D(LATCH OCTAL D - F/F)

GENERAL DESCRIPTION

The 74HC/HCT374 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	15	13	ns
f_{max}	maximum clock frequency		77	48	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	17	17	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

74HC244D(OCTAL BUFFERS)

GENERAL DESCRIPTION

The 74HC/HCT244 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 15 pF; V_{CC} = 5 V	9	11	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	35	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	P_n, Q_n to $\overline{P = Q}$		17	17	ns
	E to $\overline{P = Q}$		8	12	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	30	30	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

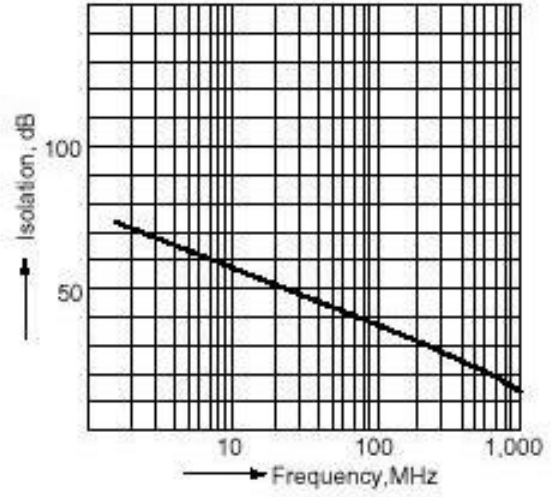
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

TQ

11.-(1) High-frequency characteristics
Isolation characteristics



11.-(2) High-frequency characteristics
Insertion loss characteristics