



## TCAS 3000 FCC Compliance Test Report

CAGE Code <b>1WYD3</b>	Initial Release Date <b>04-Jan-06</b>	Revision Date <b>N/A</b>	Document Number <b>8002224-001</b>	Revision <b>-</b>
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## Record of Revisions

<u>Rev</u>	<u>Date</u>	<u>Authorization</u>	<u>Description of Change</u>
-	4-Jan-06	ECR009169	Initial Release

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## 1 INTRODUCTION

The TCAS 3000 is a stand-alone TCAS II processor unit that will be installed in federated LRU (Line Replaceable Unit) aircraft configurations as a remote mount product. The TCAS 3000 complies with the interface requirements specified in ARINC Characteristic 735A-1 and meets the FAA certification requirements of TSO-C119b.

The TCAS 3000 will be available in a 4 MCU or 6 MCU versions. The 4 MCU TCAS 3000 is available in two versions: a 28 VDC only version and a 28 VDC/115 VAC 400 Hz version. The 6 MCU TCAS 3000 is available in a 28 VDC/115 VAC 400 Hz version.

The 6-MCU TCAS 3000 LRU is identified as:

Part No. 9003000-10YYY (DC/AC)  
(Y's denote the software version).

The 4-MCU TCAS 3000 LRU is identified as:

Part No. 9003000-55YYY (DC Only)  
Part No. 9003000-65YYY (DC/AC)  
(Y's denote the software version).

*Comment: The 9003000-10YYY and 9003000-65YYY units are able to accept either 115VAC 400Hz or 28VDC input power without any configuration changes (automatic switchover).*

The TCAS 3000 is fully interchangeable with the TCAS 2000 system. As such, the TCAS 3000 and TCAS 2000 share a common form factor, mounting tray, and connector (all fundamental interconnect wiring is identical for both the TCAS 2000 and TCAS 3000).

All TCAS 2000 functionality is implemented within the TCAS 3000. Additional functionality implemented within the TCAS 3000 does not prevent a TCAS 2000 from operating within a TCAS 3000 installation.



## 2 APPLICABLE TCAS 3000 UNIT PART NUMBERS

This document shall be applicable to the following TCAS 3000 part numbers:

ACSS Part Number	TCAS I/O	Input Power	Unit Size
9003000-10001	Digital & Analog	AC/DC	6MCU
9003000-55001	Digital & Analog	DC	4MCU
9003000-65001	Digital & Analog	AC/DC	4MCU

**Table 1: TCAS 3000 part numbers and key characteristics**

### 2.1 References

Applicable industry and regulatory documents are listed here. Unless otherwise specified, all references are to the document revision levels listed here.

<u>Ref #</u>	<u>Document No.</u>	<u>Description</u>
1	ABD0100	Airbus Industries Document: Equipment – Design / General Requirements for Suppliers
2	D200Z001	Boeing Document: General Technical Requirements for Electrical and Electronic Equipment
3	D6-44588	Boeing Document: Electrical Requirements for Utilization Equipment Installed on Commercial Transport Airplanes
4	DGT 81590	Dassault System General Technical Requirement (SGTR)
5	ICAO Annex 10	Amendment No. 77 (to include previous amendments) to the International Standards and Recommended Practices, Aeronautical Telecommunications, Volume III, (Communication Systems) and Volume IV (Surveillance Radar and Collision Avoidance Systems)
6	IEEE-1386/1386.1	IEEE Standard for a Common Mezzanine Card (CMC) Family  IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC)
7	RTCA DO-160D	Environmental Conditions and Test Procedures for Airborne Equipment, dated 7/29/97, with Change #1 (dated 12/14/00), Change #2 (dated 6/12/01), and Change #3 (dated 12/5/02).
8	RTCA DO-185A	Minimum Operational Performance Standards for Traffic Alert Collision Avoidance System II (TCAS II) Airborne Equipment
9	RTCA DO-254	Design Assurance Guidance for Airborne Electronic Hardware

<b>Ref #</b>	<b>Document No.</b>	<b>Description</b>
10	RTCA DO-260A	Minimum Operational Performance Standards for 1090MHz Automatic Dependent Surveillance – Broadcast (ADS-B) and Traffic Information Services – Broadcast (TIS-B)
11	ARINC 429	Mark 33 Digital Information Transfer System (DITS)
12	ARINC 600	Air Transport Avionics Equipment Interfaces
13	ARINC 413A	Aircraft Electrical Power Utilization and Transient Protection
14	ARINC 735A	Traffic Alert and Collision Avoidance System (TCAS)
15	Directive 8110.4B	Type Certification
16	AC No. 20-131A	Airworthiness and Operational Approval of Traffic Alert and Collision Avoidance Systems
17	ED-14D	Environmental Conditions and Test Procedures for Airborne Equipment dated July 1997, with Change #1 (dated December 2000) and Change #2 (dated June 2001).
18	8001193-001	TCAS 3000 Product Specification
19	8002050-001	TCAS 3000 System Requirements Specification
20	8002060-001	CCP System Requirements Specification
21	8002214-001	CCP Hardware Requirements Document
22	8002215-001	TCAS 3000 Hardware Requirements Document
23	8002216-001	TCAS 3000 Test Requirements Document
24	8002217-001	TCAS 3000 Acceptance Test Procedures
25	8002220-001	TCAS 3000 DO-160D Environmental Test Plan
26	8002221-001	TCAS 3000 DO-160D Environmental Test Procedures
27	8002222-001	TCAS 3000 DO-160D Environmental Test Report
36	8002223-001	TCAS 3000 FCC Compliance Test Plan and Procedures
37	8005063-001	Mini-VALFAC Validation Procedures
38	9003000-10001	TCAS 3000 6 MCU End Item Drawing
39	9003000-55001	TCAS 3000 4 MCU End Item Drawing
40	9003000-65001	TCAS 3000 4 MCU End Item Drawing
41	9003000-10	TCAS 3000 6 MCU Hardware Assembly Drawing
42	9003001-003	TCAS 3000 Outline and Installation Drawing
43	9003000-65	TCAS 3000 4 MCU Hardware Assembly Drawing

<u>Ref #</u>	<u>Document No.</u>	<u>Description</u>
44	9003000-55	TCAS 3000 4 MCU Hardware Assembly Drawing
45	9003010-002	TCAS 3000 Rear Interconnect Assembly Drawing
46	9003020-002	Common Processor Assembly Drawing
47	9003030-002	Common Power Supply Drawing
48	7517945-905	Receiver I/O Assembly Drawing
49	7517935-903	Transmitter Assembly Drawing
50	8005730-001	NTS Qual Test Reports and Data
51	8005748-001	NTS FCC Compliance Test Report
52	8003529-001	TCAS 3000 System Description and Installation Manual
53	9000299	Labels for T2CAS/APM and TCAS 3000

### 2.1.1 FCC Documents

CFR Title 47  
Chapter 1  
Part 2  
Subpart J

Code of Federal Regulations - Telecommunications  
Federal Communications Commission  
Frequency Allocations and Radio Treaty Matters; General Rules and Regulations  
Equipment Authorization Procedures  
Revised as of October 1, 2001

CFR Title 47  
Chapter 1  
Part 15  
Subpart A

Code of Federal Regulations - Telecommunications  
Federal Communications Commission  
Radio Frequency Devices  
General  
Revised as of October 1, 2001

CFR Title 47  
Chapter 1  
Part 87  
Subpart D

Code of Federal Regulations - Telecommunications  
Federal Communications Commission  
Aviation Services  
Technical Requirements  
Revised as of October 1, 2001

### 2.2 Acronyms and Abbreviations

AC            Advisory Circular  
CFR          Code of Federal Regulations  
CMC          Canadian Marconi Corporation  
CS            Conducted Susceptibility  
EB            Engineering Bulletin  
EMI          Electromagnetic Interference

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ESS	Environmental Stress Screen
ESD	Electrostatic Discharge
EUT	Equipment Under Test
FAA	Federal Aviation Administration
FCC	Federal Communications Commission
GPS	Global Positioning System
HIRF	High Intensity Radiated Fields
LISN	Line Impedance Stabilization Network
MOPS	Minimum Operational Performance Standards
NTS	National Technical Systems
RF	Radio Frequency
RFI	Radio Frequency Interference
RS	Radiated Susceptibility
RTCA	Radio Technical Commission for Aeronautics
TAWS	Terrain Avoidance Warning System
TCAS	Traffic Alert and Collision Avoidance System
T <sup>2</sup> CAS	Traffic and Terrain Collision Avoidance System
TSO	Technical Standard Order
UUT	Unit Under Test

### 3 GENERAL INFORMATION

#### 3.1 TYPE DESIGNATION

The equipment has been designated by ACSS as TCAS Computer Units, P/Ns 9003000-10001, 9003000-55001, and 9003000-65001.

#### 3.2 SERVICE AND RULE FOR INTENDED OPERATION

Air Traffic Control  
Part 87, Subpart A

#### 3.3 DESCRIPTION OF EQUIPMENT

##### 3.3.1 TCAS Functionality

###### 3.3.1.1 Type of Emission

18MOP1D

###### 3.3.1.2 Frequency Range

1030 + 0.01 MHz

###### 3.3.1.3 Power Rating

0.4 to 500 Watts Peak Effective Radiated Power (Pulsed)

###### 3.3.1.4 Final Power Amplifier

Solid State Balanced Amplifier (Class C) using two Motorola MRF10501 silicon bipolar transistors.

###### 3.3.1.5 Active Device Functions

<u>Function</u>		<u>Device Type</u>	<u>Manufacturer</u>
Oscillator	Temperature Compensated Crystal Oscillator (TCXO)	6206	Oscillatek
	Microwave Low Noise Transistor--Amplifier	AT-41511	HP
Transmitter	Monolithic Amplifier .1 Watt, Microwave Pulse Power	VNA – 25	Mini-Circuit

<u>Function</u>		<u>Device Type</u>	<u>Manufacturer</u>
Transmitter	Transistor--Amplifier, 1 watt Microwave Pulse Power	MRF1000MB	Motorola
	Transistor--Amplifier, 5 watt Microwave Pulse Power	MRF10005	Motorola
	Transistor--Amplifier, 30 watt Microwave Pulse Power	MRF10031	Motorola
	Transistor--Amplifier, 150 watt Microwave Pulse Power	MRF10120	Motorola
	Transistor--Amplifier, 500 watt	MRF10502 (2 ea)	Motorola
Pulse Modulator	N Channel FET Modulator	IRFR220	Motorola
	N Channel FET Envelope Modulator	IRFR9220	International Rectifier
DPSK Modulator	NPN Transistor (1) Modulator	BSR14	Generic
	NPN Transistor (2) Modulator	BSR16	Generic

### 3.3.2 Circuit Diagram

A block diagram and schematics will be provided with the FCC Form 731 when the application for certification is filed with the FCC.

### 3.3.3 Instruction Book

An ACSS document, System Description and Installation Manual, 8003529-001, provides instructions for the proper installation of the TCAS 3000 computer on a given aircraft.

### 3.3.4 Tune-up Procedure

No field tuning is required. Alignment is performed in the factory.

### 3.3.5 Oscillator Circuit

The 1030 MHz source consists of the following: 1.) a phase locked oscillator (PLO) is locked to a Temperature Compensated Crystal Oscillator (TCXO). The TCXO provides the required frequency stability for the 1030 MHz source. 2.) the output of the PLO is fed to a prescaler divider, which in turn provides the input to a multiplier circuit. 3.) the output of the multiplier is band pass filtered, and then amplified and distributed to both the receiver and transmitter circuits.

### 3.3.6 Frequency Stabilization

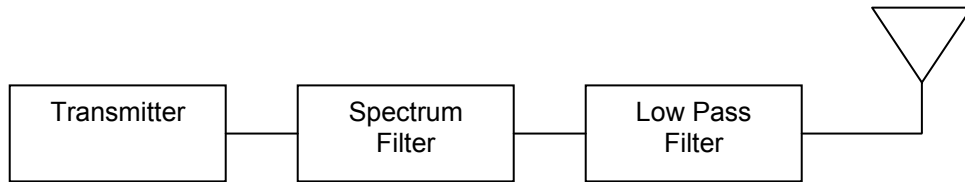
Temperature Compensated Crystal Oscillator (TCXO).

### 3.3.7 Modulation Limiting

Not Applicable

### 3.3.8 Radiated Interference Suppression

At the output of the transmitter is a two-pole high power cavity filter designed to attenuate spurious created by the DPSK modulation. This filter also offers good rejection of the even harmonics of the carrier. Following the high power cavity filter is a five pole reflective microstrip low pass filter designed for maximum rejection of the 2<sup>nd</sup> through 9<sup>th</sup> harmonics of the carrier



The spectral output of the 1030 MHz transmitter will be limited to the following schedule:

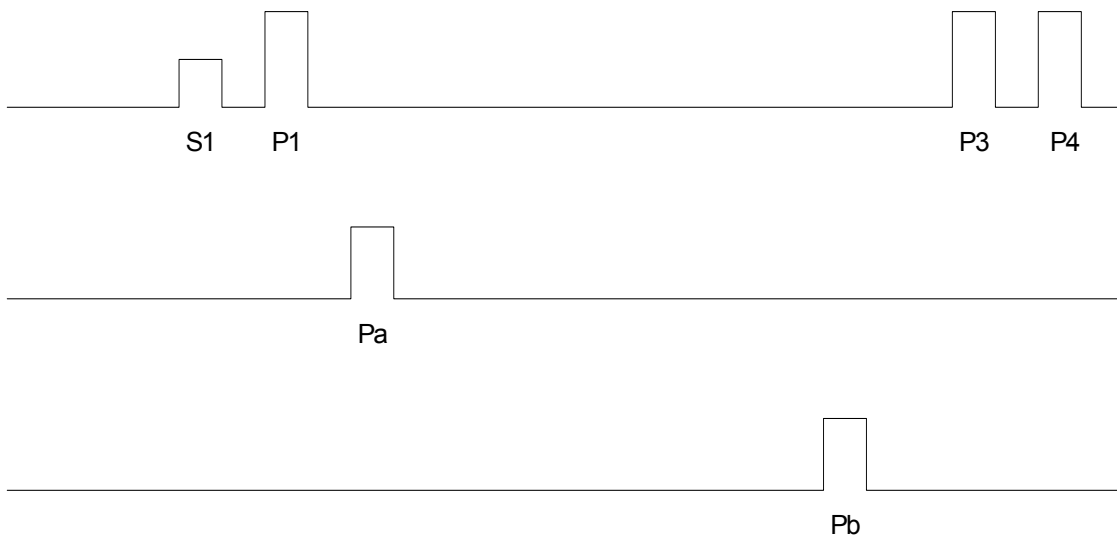
<u>Frequency difference (MHz from carrier)</u>	<u>Relative power (dB below maximum)</u>
≥ 4, < 6	6
≥ 6, < 8	11
≥ 8, < 10	15
≥ 10, < 20	19
≥ 20, < 30	31
≥ 30, < 40	38
≥ 40, < 50	43
≥ 50, < 60	47
≥ 60, < 90	50
≥ 90	60

## 4 MODULATION DETAILS

### 4.1 ATCRBS Interrogations

Interrogations are sent out on an intentionally jittered 1+0.2 second interval in increasing power levels according to the schedules shown in Table 4, Table 5, and Table 6. By transmitting the weakest signals first only the closest aircraft will reply. The interrogations progress in a roughly circular pattern weighted toward the front of the aircraft since that is the area from which the greatest closing speeds originate. In areas of high density the sequence is halted when the computer has reached a limit defined by a complex set of three inequalities. In this manner, interference to other TCAS equipped aircraft in the area is minimized since the strongest interrogations are the first to be dropped. The priority of elimination of steps for interference limiting is also shown in Table 4, Table 5, and Table 6. This priority is inversely related to the order of the step sequence.

Pulse Widths:  $0.8 + 0.05 \text{ usec}$   
 Rise Times (10% to 90%):  $\geq 0.05 \text{ usec.}, < 0.1 \text{ usec}$   
 Fall Times (90% to 10%):  $\geq 0.05 \text{ usec.}, < 0.2 \text{ usec}$



**Figure 1: ATCRBS Interrogations**

Pulses P1, P3, and P4 will appear in all interrogation steps of the whisper / shout sequence and will be at the same power level. Pulse S1 will appear in all steps except the initial step on each antenna direction and at a level two or three dB below the level of P1, etc. according to the schedules shown in Figures 1 through 3. The steps occur at intervals of two milliseconds until the entire program is complete. The program length depends upon the individual aircraft installation. Options are available from using either an omni-directional bottom antenna or a directional bottom antenna. The top antenna is always directional. Pulses Pa and Pb are transmitted on the antenna. They are used for suppression of sensitivity of the receiving aircraft to the indicated pulses:

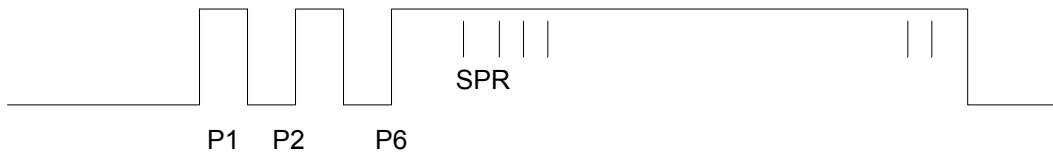


S1 = -2 microseconds  
 P1 = 0 microseconds  
 PA = 2 microseconds  
 PB = 19 microseconds  
 P3 = 21 microseconds  
 P4 = 23 microseconds

### 4.2 Mode S Interrogations

Details of the Mode S interrogations are shown in Figure 2 below. The preamble and the synchronizing phase reversal (SPR) will appear the same in all interrogations. The data block will be either 56 or 112 chips of 0.25 microseconds, depending upon the type of reply desired. The data chips will be reversed phase from their previous chips if their data bit are 1, they will remain the same phase as the previous chips is their data bits are 0. The allowable transition time of the phase reversals is a maximum of 80 nanoseconds. The Mode S interrogations are transmitted after the whisper/shout sequence of ATRBS interrogations. When no Mode S equipped aircraft are replying, the TCAS CU sends out Mode S broadcast interrogations based upon a 10 second pattern with 2 or 3 seconds between transmissions on the four lobes of the antenna. The time remaining after the Mode S transmissions are completed is used as a listening period for other unacquired aircraft.

- Preamble Pulse Widths: 0.8 + 0.05 usec
- Rise Times (10% to 90%): < 0.1 usec
- Fall Times (90% to 10%): < 0.2 usec



**Figure 2: Mode S Interrogations**

Timing of the Mode S interrogations is as follows, referenced to the leading edge of the P1 pulse:

P1	0.0 microseconds
P2	2.0 microseconds
P6	3.5 microseconds
SPR	4.75 microseconds
Bit 1	5.25 microseconds
End P6	19.75 microseconds (56 bits) 33.75 microseconds (112 bits)

**Table 2: Mode S Interrogation Timing**

Omni-Directional Antenna		
Nominal Power Levels (dB relative to full power)		
Level	P1,P3, P4 Pulses	S1 Pulse
00	-13	-16
01	-15	-18
02	-17	-20
03	-19	-22
04	-21	-24
05	-23	-26
06	-25	none

**Table 3: Mode S Interrogations, Omni-Directional Antenna**

Directional Antenna			
Nominal Power Levels (dB relative to full power)			
Level	P1,P3, P4	S1 Pulse	Pa, Pb Pulse
D0	0	-3	-2
D1	-1	-3	-3
D2	-2	-5	-4
D3	-3	-5	-5
D4	-4	-7	-6
D5	-5	-7	-7
D6	-6	-9	-8
D7	-7	-9	-9
D8	-8	-11	-10
D9	-9	-11	-11
D10	-10	-13	-12
D11	-11	-13	-13
D12	-12	-15	-14
D13	-13	-15	-15
D14	-14	-17	-16
D15	-15	-17	-17
D16	-16	-19	-18
D17	-17	-19	-19
D18	-18	-21	-20
D19	-19	-21	-21
D20	-20	-23	-22
D21	-21	-23	-23
D22	-22	-25	-24
D23	-23	-25	-25
D24	-24	-27	-26
D25	-25	-27	-27
D26	-26	--	-16 (P4 only)

**Table 4: Mode S Directional Antenna Interrogation Transmission Levels**

<b>Bottom Omni-Directional Antenna</b>			
<b>Interference Limiting Priority / Interrogation Level</b>			
98 / 06			
97 / 05			
96 / 04			
95 / 03			
94 / 02			
93 / 01			
92 / 00			
<b>Top Directional Antenna</b>			
<b>Interference Limiting Priority / Interrogation Level</b>			
<b>0'</b>	<b>180'</b>	<b>90'</b>	<b>270'</b>
91 / D26	-	-	-
90 / D25	-	-	-
89 / D24	-	-	-
88 / D23	-	87 / D26	86 / D26
85 / D22	-	84 / D25	83 / D25
82 / D21	-	81 / D24	80 / D24
79 / D20	-	78 / D23	77 / D23
76 / D19	-	75 / D23	74 / D22
73 / D18	72 / D26	71 / D21	70 / D21
69 / D17	68 / D25	67 / D20	66 / D20
65 / D16	64 / D24	63 / D20	62 / D19
61 / D15	60 / D23	59 / D18	58 / D18
57 / D14	56 / D22	55 / D17	54 / D17
49 / D12	48 / D20	47 / D15	46 / D15
45 / D11	44 / D19	43 / D14	42 / D14
41 / D10	40 / D18	39 / D13	38 / D13
37 / D9	36 / D17	35 / D12	34 / D12
33 / D8	32 / D16	31 / D11	30 / D11
29 / D7	28 / D15	27 / D10	26 / D10
25 / D6	24 / D14	23 / D9	22 / D9
21 / D5	20 / D13	19 / D8	18 / D8
17 / D4	16 / D12	15 / D7	14 / D7
13 / D3	12 / D11	11 / D6	10 / D6
9 / D2	8 / D10	7 / D5	6 / D5
5 / D1	4 / D10	3 / D4	2 / D4
1 / D0	-	-	-

(Interrogation sequence is right to left, top to bottom)

**Table 5: Top Directional / Bottom Omni-Directional Interrogation Sequence**

Interference Limiting Priority / Interrogation Level							
Top Directional Antenna				Bottom Directional Antenna			
0'	180'	90'	270'	0'	180'	90'	270'
113 / D26	-	-	-	112 / D26	-	-	-
111 / D25	-	-	-	-	110 / D25	-	-
109 / D24	-	-	-	108 / D24	-	-	-
107 / D23	-	-	-	106 / D23	-	-	-
-	-	105 / D26	104 / D26	-	-	103 / D26	102 / D26
101 / D22	-	-	-	100 / D22	-	-	-
-	-	99 / D25	98 / D25	-	-	97 / D25	96 / D25
95 / D21	-	-	-	94 / D21	93 / D26	-	-
-	-	92 / D24	91 / D24	-	-	90 / D24	89 / D24
88 / D20	-	-	-	87 / D20	86 / D25	-	-
-	-	85 / D23	84 / D23	-	-	83 / D23	82 / D23
81 / D19	-	-	-	80 / D19	79 / D24	-	-
-	-	78 / D22	77 / D22	-	-	76 / D22	75 / D22
74 / D18	-	-	-	73 / D18	-	-	-
-	72 / D26	71 / D21	70 / D21	Interrogations for each sector that has a TA or RA present			
69 / D17	68 / D25	67 / D20	66 / D20				
65 / D16	64 / D24	63 / D19	62 / D19				
61 / D15	60 / D23	59 / D18	58 / D18				
57 / D14	56 / D22	55 / D17	54 / D17				
53 / D13	52 / D21	51 / D16	50 / D16				
49 / D12	48 / D20	47 / D15	46 / D15				
41 / D10	40 / D18	39 / D13	38 / D13				
37 / D9	36 / D17	35 / D12	34 / D12				
33 / D8	32 / D16	31 / D11	30 / D11				
29 / D7	28 / D15	27 / D10	26 / D10				
25 / D6	24 / D14	23 / D9	22 / D9				
21 / D5	20 / D13	19 / D8	18 / D8				
17 / D4	16 / D12	15 / D7	14 / D7				
13 / D3	12 / D11	11 / D6	10 / D6				
9 / D2	8 / D5	7 / D5	6 / D5				
5 / D1	4 / D9	3 / D4	2 / D4				
1 / D0	-	-	-				
				1 / D17	1 / D23	1 / D21	1 / D21
				1 / D16	1 / D22	1 / D20	1 / D20
				1 / D15	1 / D21	1 / D19	1 / D19
				1 / D14	1 / D20	1 / D18	1 / D18
				1 / D13	1 / D19	1 / D17	1 / D17
					1 / D18	1 / D16	1 / D16
					1 / D17	1 / D15	1 / D15
					1 / D16	1 / D14	1 / D14
					1 / D15	1 / D13	1 / D13
					1 / D14		
					1 / D13		

(Interrogation sequence is right to left, top to bottom)

**Table 6: Top Directional / Bottom Directional Interrogation Sequence**

## 5 DRAWINGS AND PHOTOGRAPHS

### 5.1 Drawings

End Item and associated drawings will be furnished with the applications. Refer to Paragraph 2.1 for a list of these ACSS drawings that will be furnished with the application.

### 5.2 Photographs

Photographs of the TCAS 3000 unit illustrating the assembly drawings are listed below. All original photographs are available for inspection.

Figure Number	View
Figure 3	4 MCU Unit Front Name Plate
Figure 4	4 MCU Unit Front With Name Plate Showing
Figure 5	4 MCU Unit Rear With ARINC Connector
Figure 6	Right Side View of 4 MCU Unit, Covers Removed
Figure 5	Left Side View 4MCU Unit, Covers Removed
Figure 8	View of 4 MCU Unit With Top Bracket Removed
Figure 9	View of 4 MCU Unit Separated to show A4 Power Supply CCA
Figure 10	View of 4 MCU Unit Side, With A5 Receiver Removed
Figure 11	View of 4 MCU Unit With Front Panel Removed, Showing A2 Processor
Figure 12	View of 4 MCU Unit, With A2 Processor Removed Showing A3 Transmitter Assembly With Cover
Figure 13	View of 4 MCU Unit, Showing A1 Interconnect Assembly
Figure 14	6 MCU Unit Front Name Plate
Figure 15	Front of 6 MCU Unit, Showing Name Plate
Figure 16	Rear of 6 MCU Unit With ARINC Connector
Figure 17	Left Side View of 6 MCU Unit, Covers Removed
Figure 18	Right Side View of 6 MCU Unit, Covers Removed
Figure 19	Front View of 6 MCU Unit, Separated to show A4 Power Supply CCA
Figure 20	View of 6 MCU Unit With Front Panel Removed, Showing A2 Processor
Figure 21	View of 6 MCU Unit, With A2 Processor Removed Showing A3 Transmitter Assembly With Cover
Figure 22	View of 6 MCU Unit, Showing A1 Interconnect Assembly
Figure 23	Back Side View of A4 Power Supply Assembly
Figure 24	Front Side View of A4 Power Supply Assembly
Figure 25	Front Side View of A2 Processor Assembly
Figure 26	Back Side View of A2 Processor Assembly
Figure 27	View of A5 Receiver I/O Assembly, Cover Removed, Side A
Figure 28	View of A5 Receiver I/O Assembly, Cover Removed, Side B
Figure 29	View of A3 Transmitter Assembly, Cover Removed, Side A

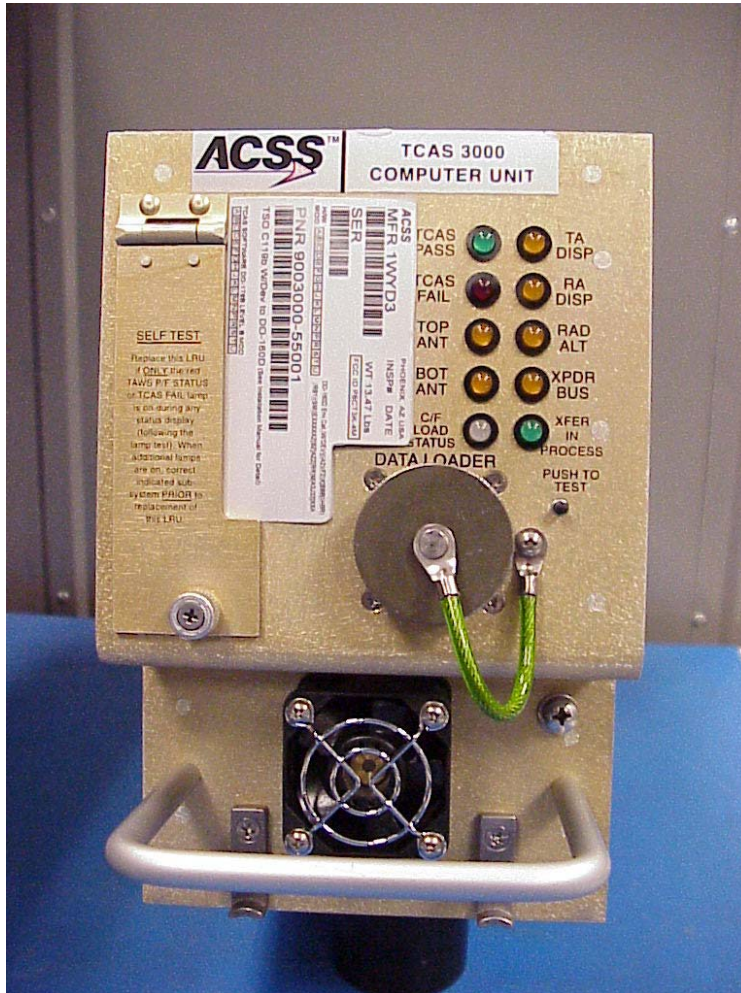


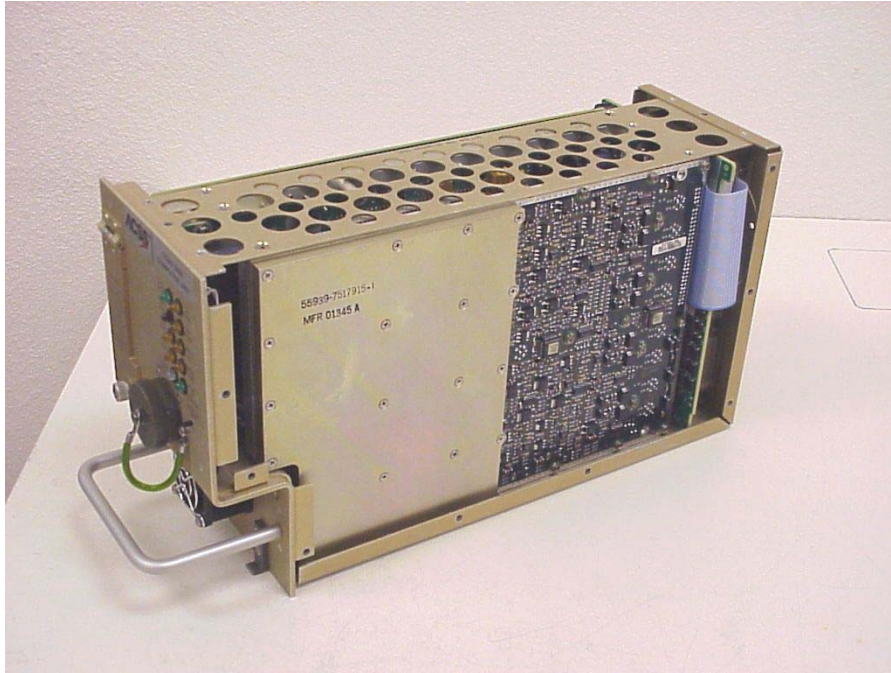
Figure 3: 4 MCU Unit Front Name Plate



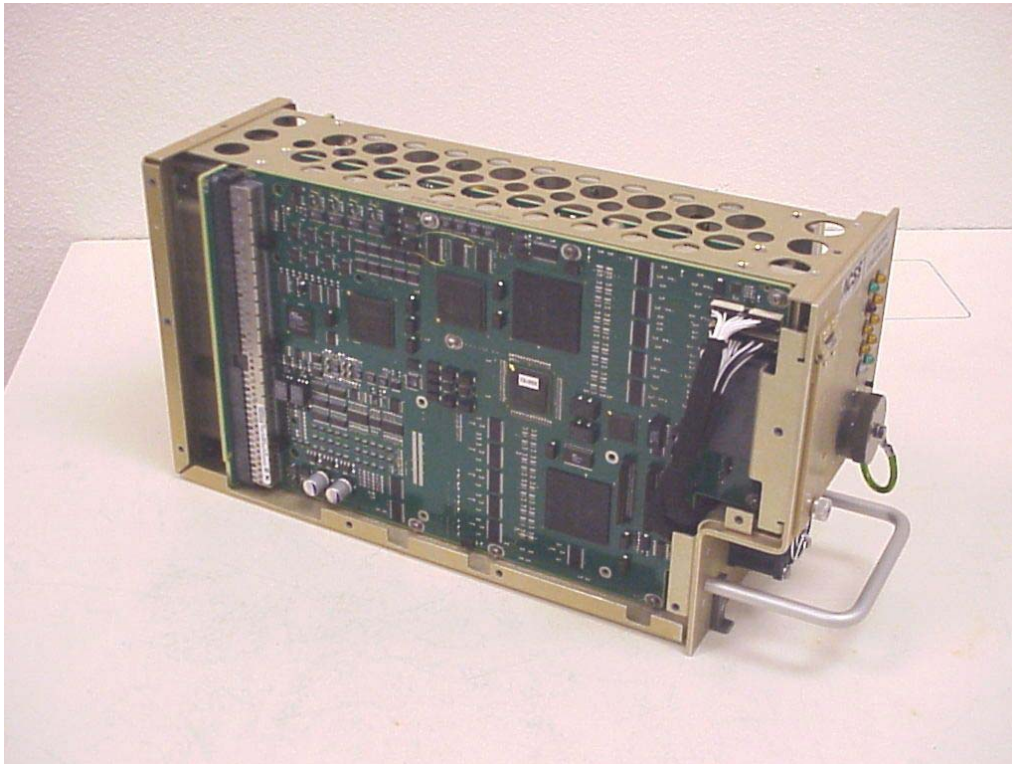
**Figure 4: Front View of 4 MCU Unit, Showing Name Plate**



**Figure 5: Rear View of 4 MCU Unit With ARINC Connector**

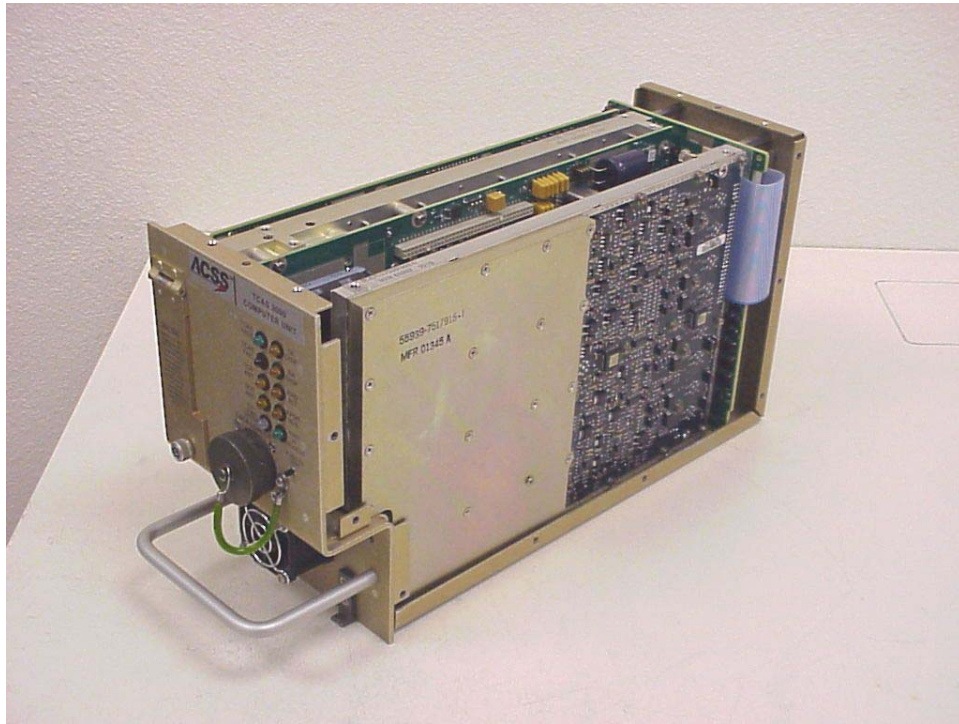


**Figure 6: Right Side View of 4 MCU Unit, Covers Removed**

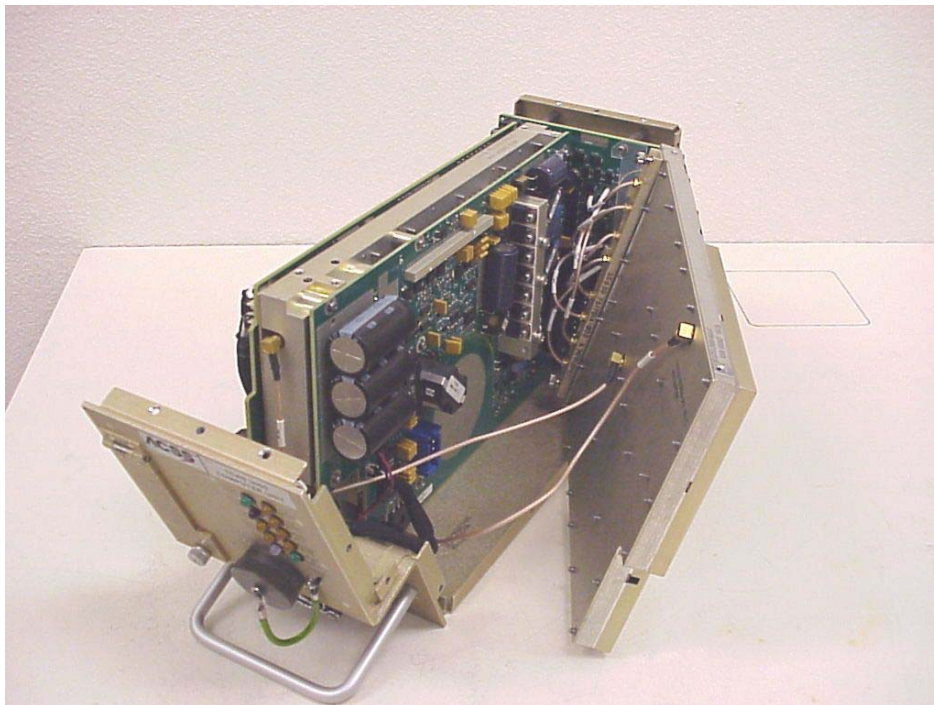


**Figure 7: Left Side View of 4MCU Unit, Covers Removed**

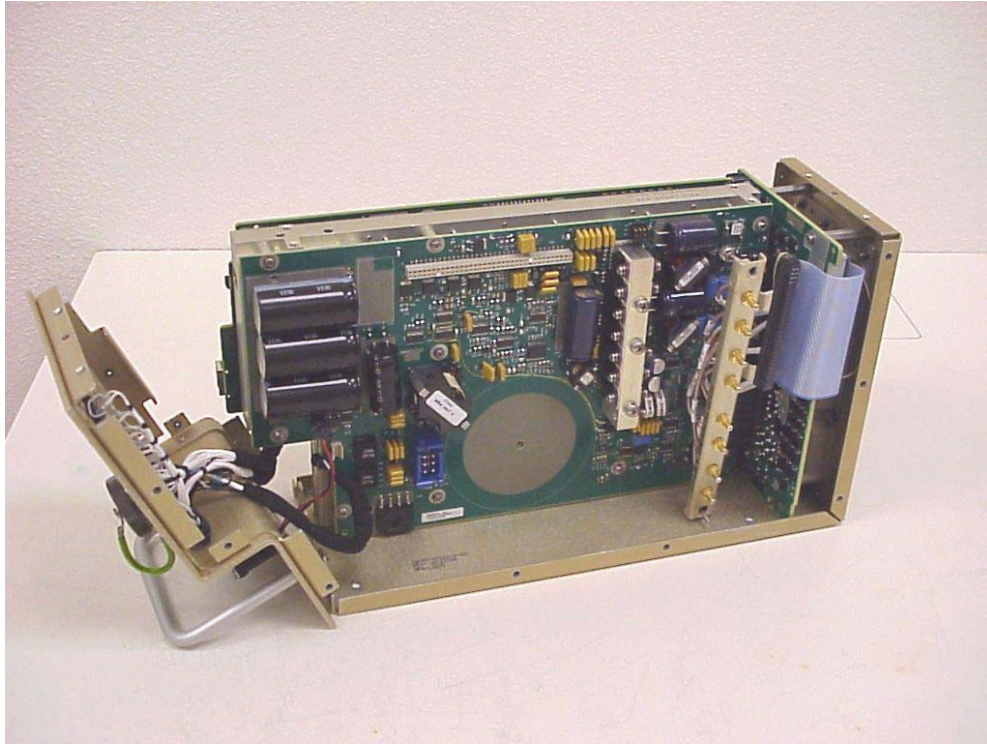




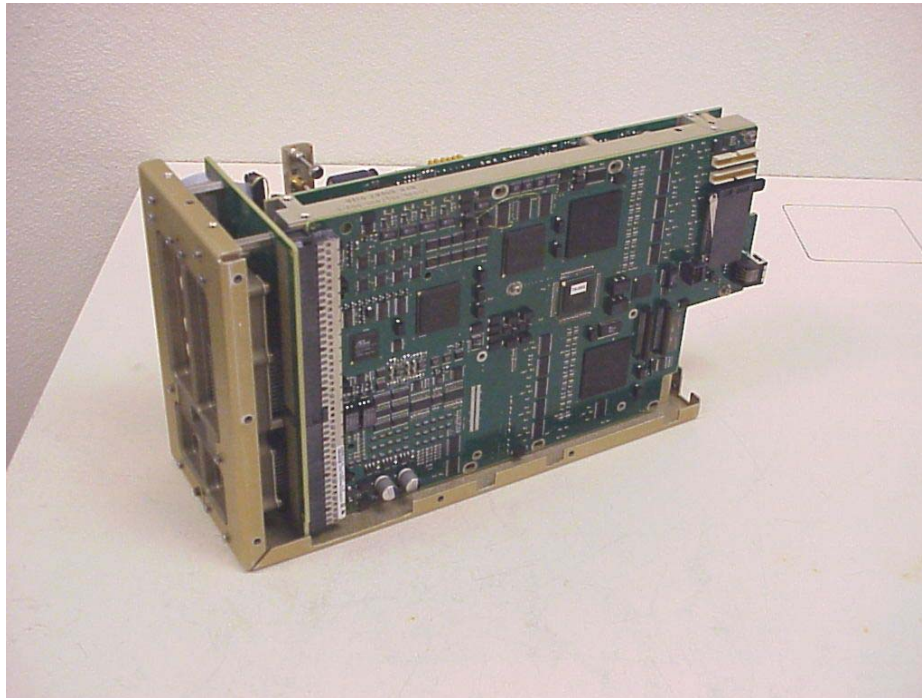
**Figure 8: Right Side View of 4 MCU Unit With Top Bracket Removed**



**Figure 9: View of 4 MCU Unit Separated to show A4 Power Supply CCA**

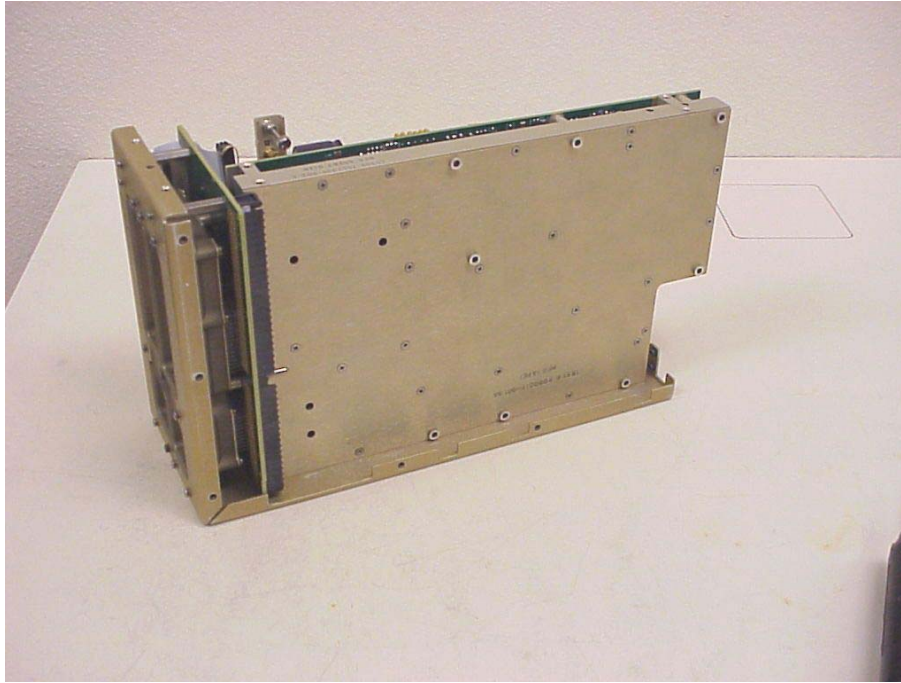


**Figure 10: View of 4 MCU Unit Side, With A5 Receiver Removed**



**Figure 11: View of 4 MCU Unit With Front Panel Removed, Showing A2 Processor**

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**Figure 12: View of 4 MCU Unit, With A2 Processor Removed Showing A3 Transmitter Assembly With Cover**



**Figure 13: View of 4 MCU Unit, Showing A1 Interconnect Assembly**



Figure 14: 6 MCU Unit Front Name Plate

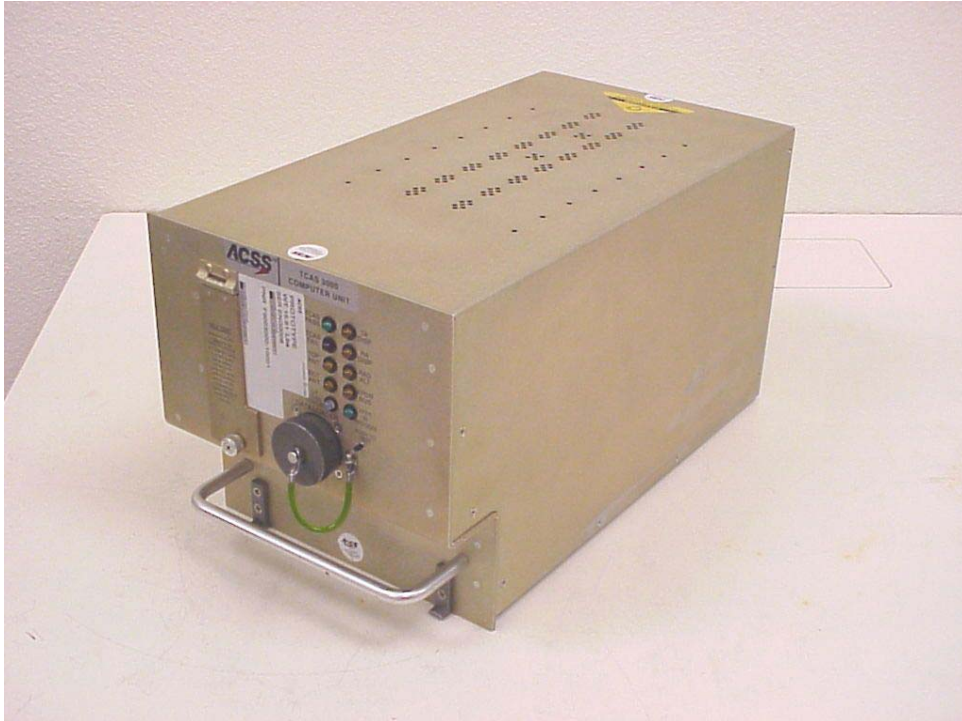
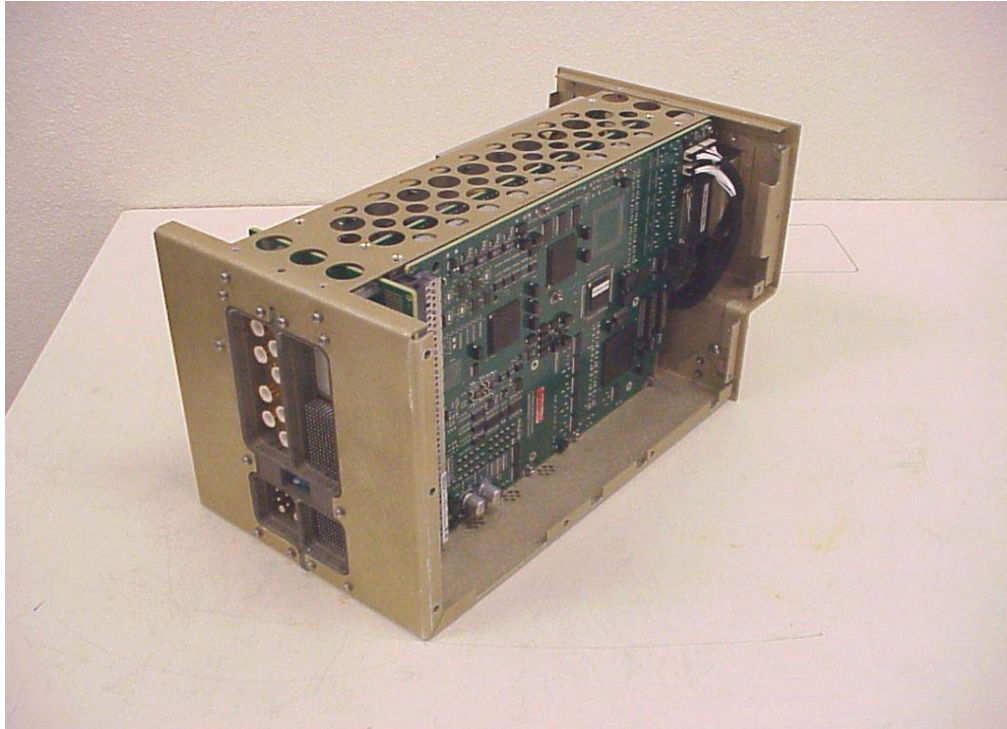


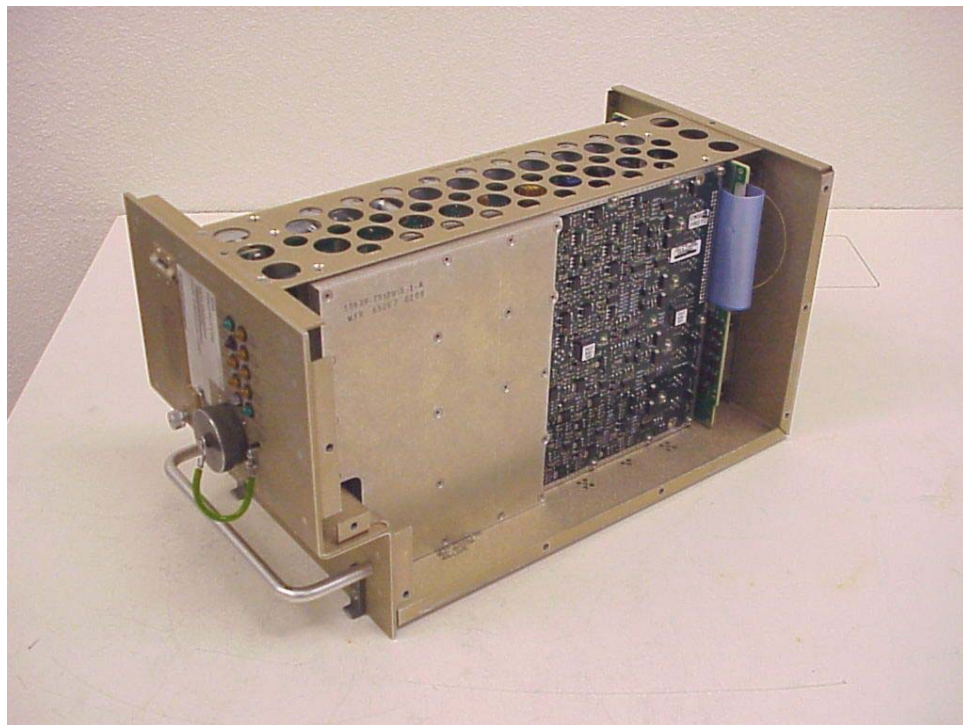
Figure 15: Front of 6 MCU Unit, Showing Name Plate



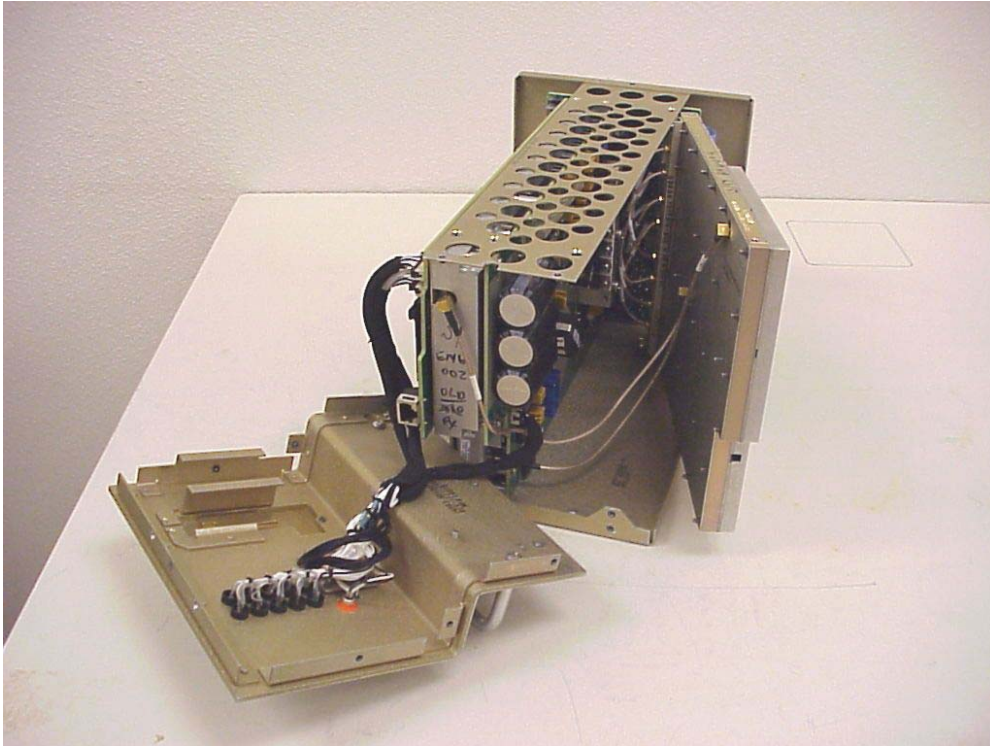
Figure 16: Rear of 6 MCU Unit With ARINC Connector



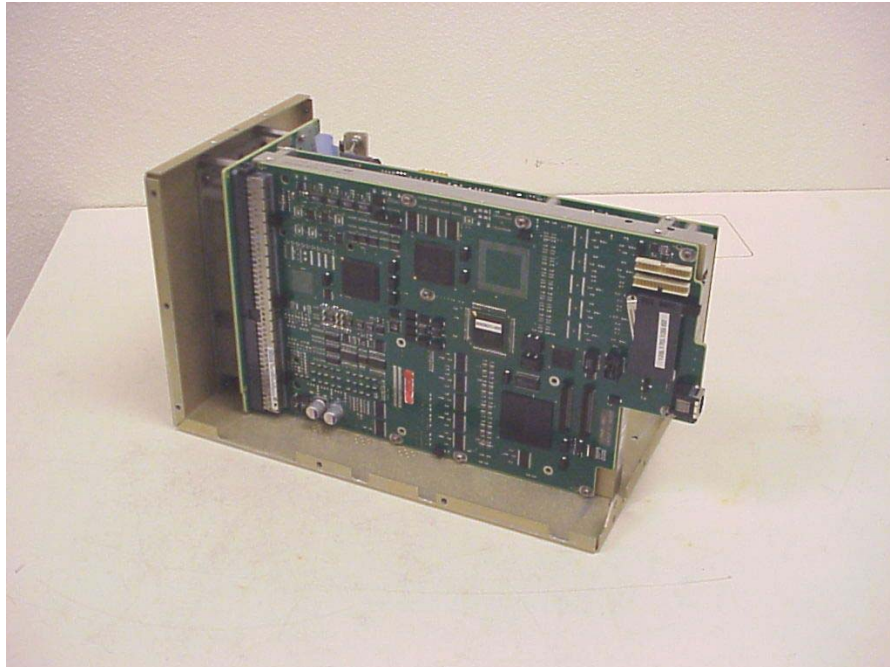
**Figure 17: Left Side View of 6 MCU Unit, Covers Removed**



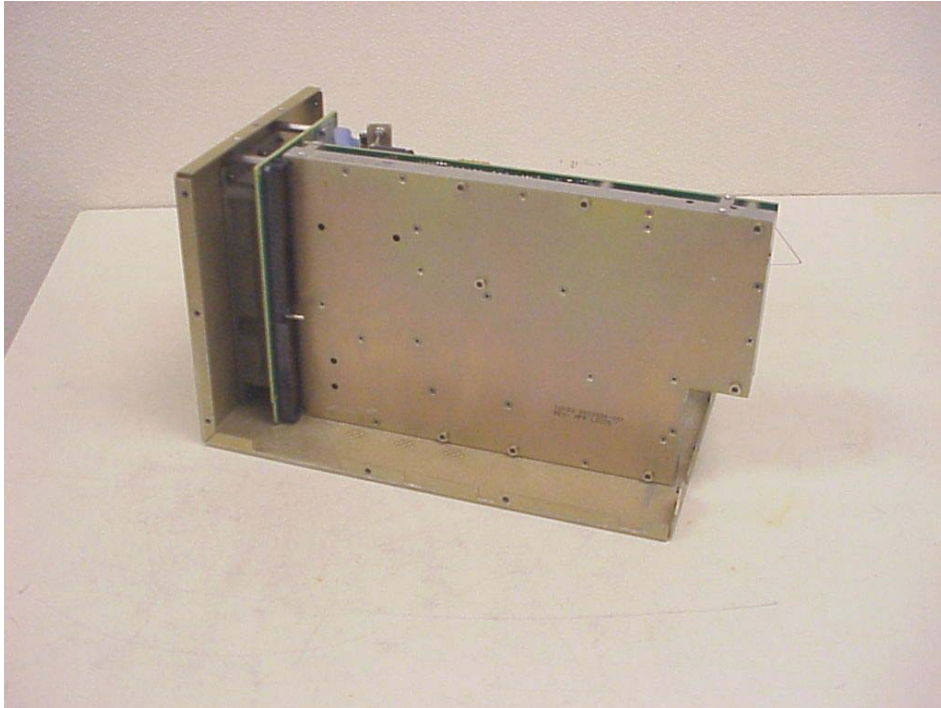
**Figure 18: Right Side View of 6 MCU Unit, Covers Removed**



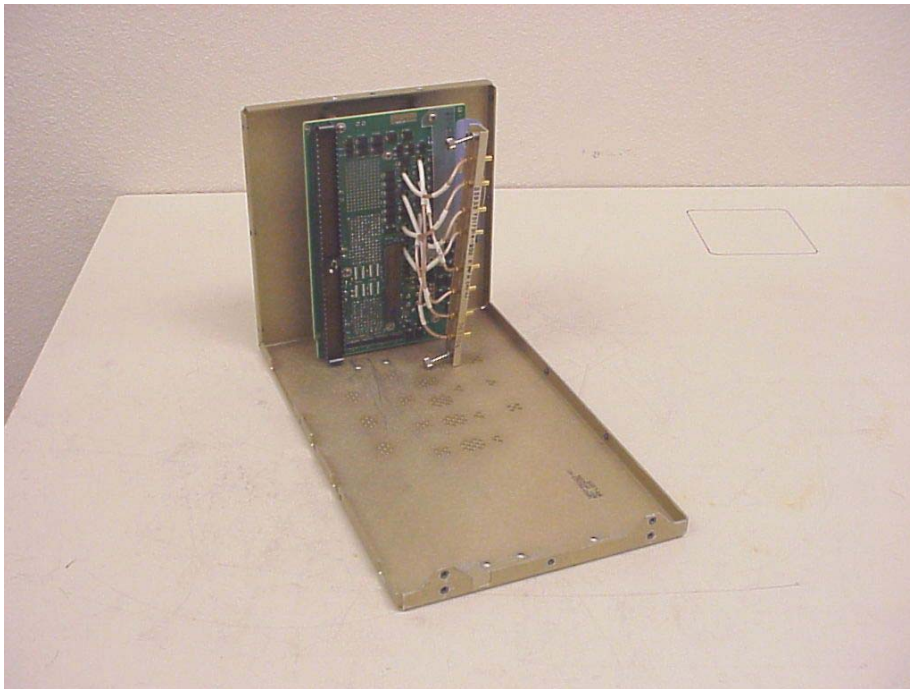
**Figure 19: Front View of 6 MCU Unit, Separated to show A4 Power Supply CCA**



**Figure 20: View of 6 MCU Unit With Front Panel Removed, Showing A2 Processor**

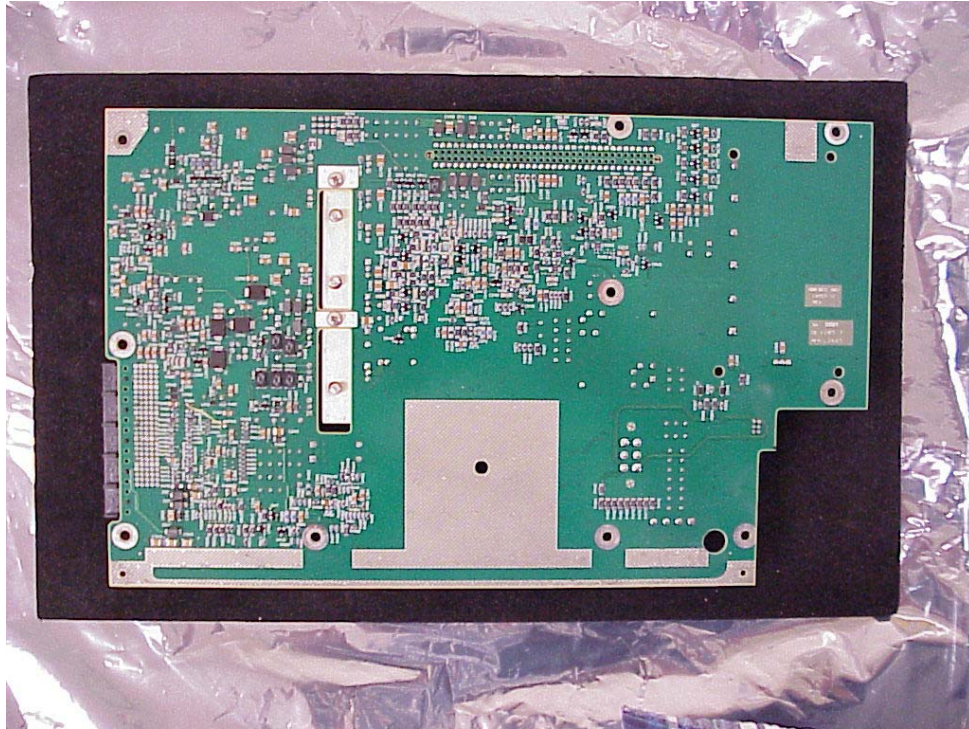


**Figure 21: View of 6 MCU Unit, With A2 Processor Removed Showing A3 Transmitter Assembly With Cover**

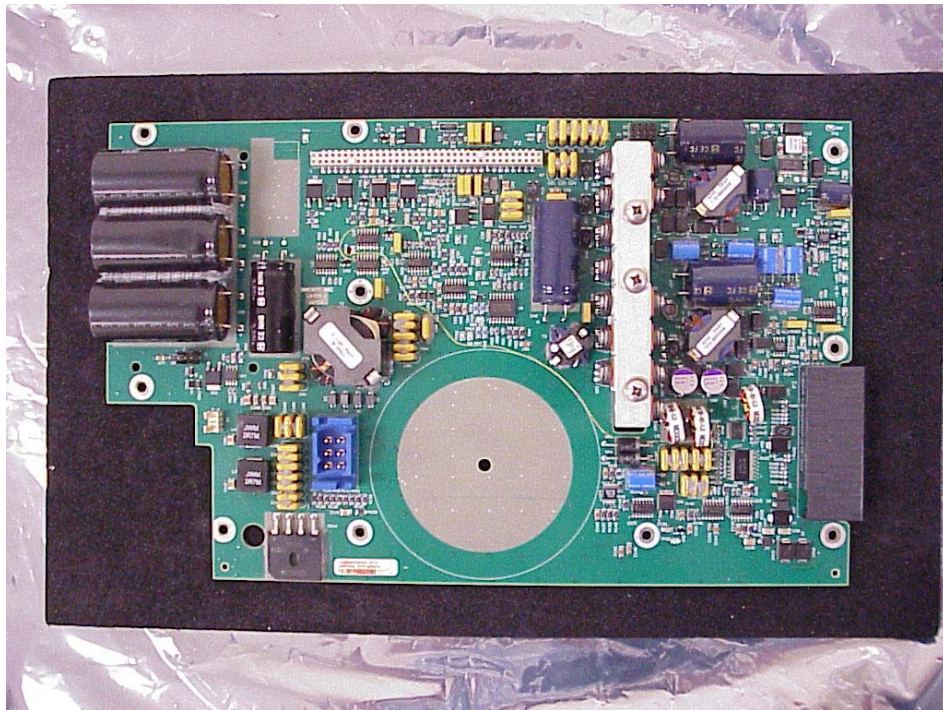


**Figure 22: View of 6 MCU Unit, Showing A1 Interconnect Assembly**

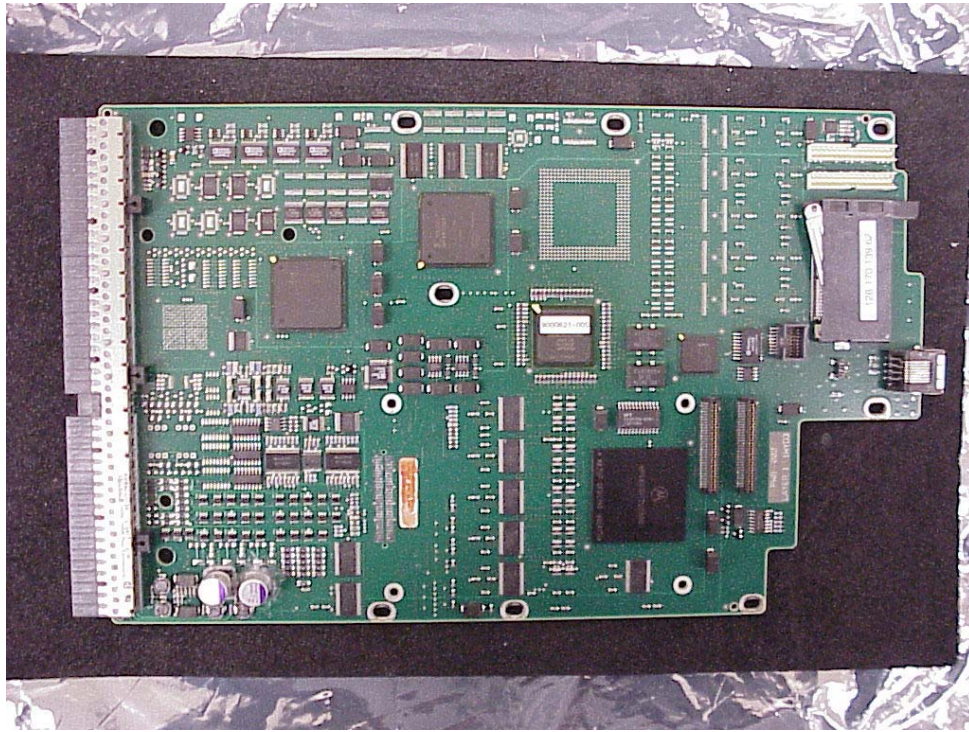




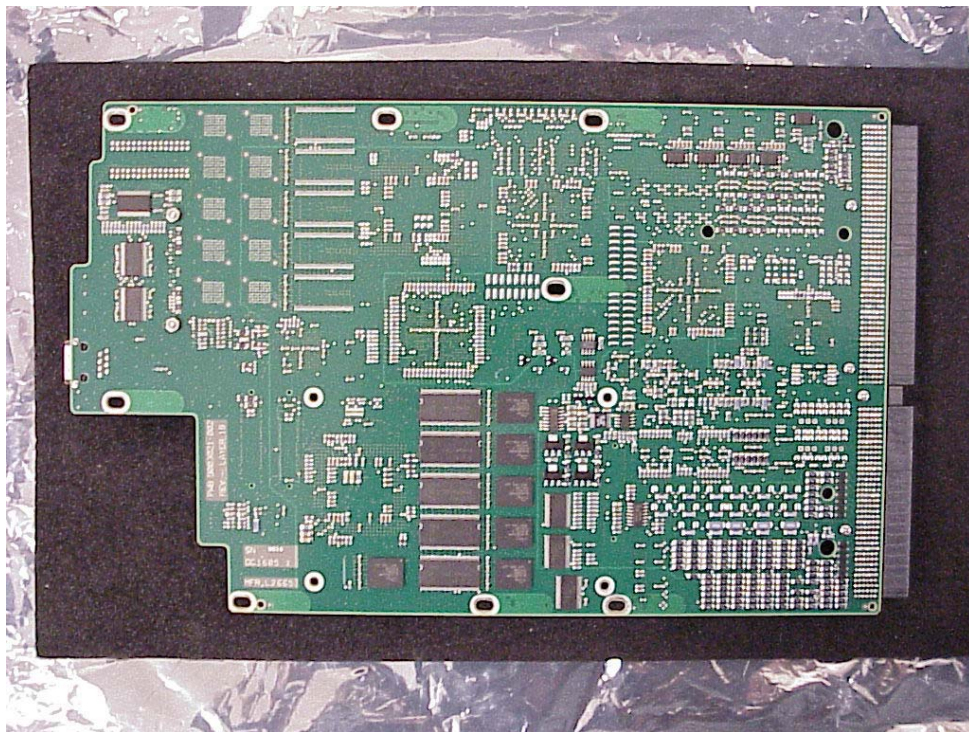
**Figure 23: Back Side View of A4 Power Supply Assembly**



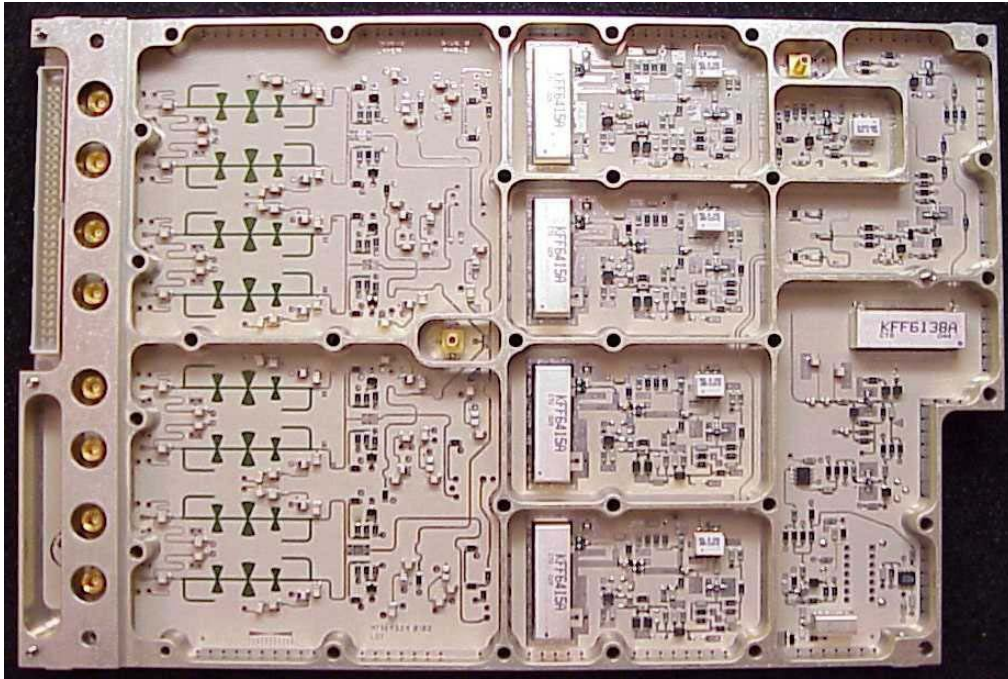
**Figure 24: Front Side View of A4 Power Supply Assembly**



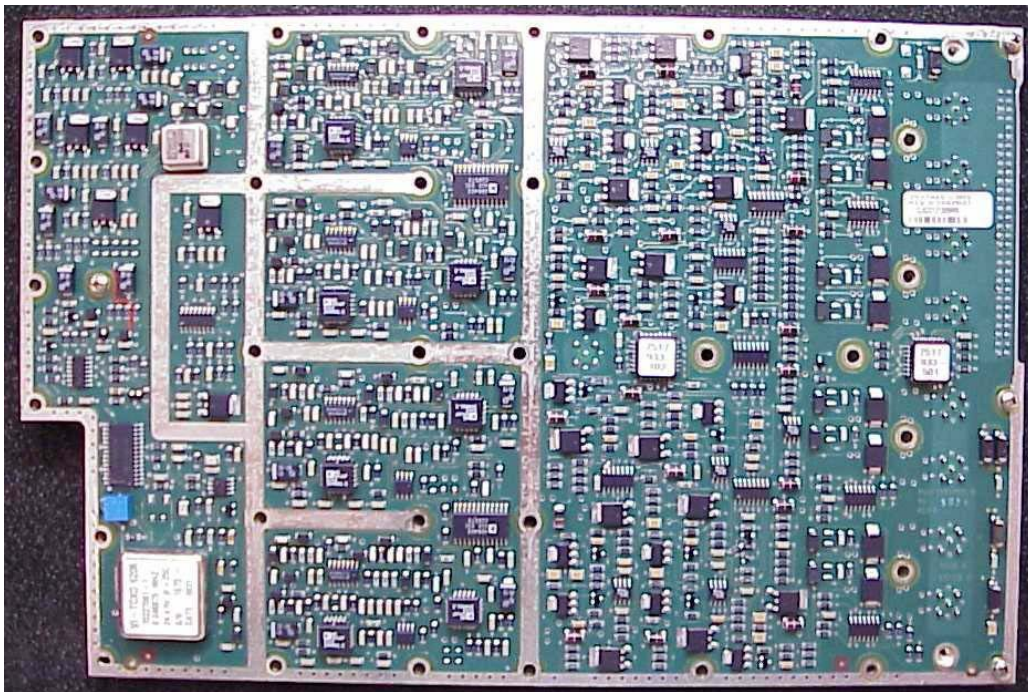
**Figure 25: Front Side View of A2 Processor Assembly**



**Figure 26: Back Side View of A2 Processor Assembly**



**Figure 27: View of A5 Receiver I/O Assembly, Cover Removed, Side A**



**Figure 28: View of A5 Receiver I/O Assembly, Cover Removed, Side B**