Aviation Communication and Surveillance Systems

TCAS 3000 Test Requirements Document

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1WYD3	**01-JUNE-05**	**15-DEC-05**	**8002216-001**	**C**

Record of Revisions

Rev	Date	Authorization	Description of Change
-	6/1/05	ECR008688	Initial Release
A	9/15/05	ECR008943	Addition of tests
B	10/12/05	ECR009051	Addition of tests
C	12/15/05	ECR009152	Addition of tests

Table of Contents

1 INTRODUCTION

This document is the Test Requirements Document for the TCAS 3000 Computer Unit.

1.1 Purpose

The purpose of this document is as follows:

- To provide instruction on the loading of Boot and FPGA software.
- To provide instruction on the loading of Hardware Test Software (HTS).
- To provide instruction on the calibration of a TCAS 3000.
- To define the specifications and test methods required for testing a TCAS 3000 LRU.

1.2 Scope

This Test Requirements Document establishes the requirements for performing an End Item Acceptance Test on a TCAS 3000 Line Replaceable Unit (LRU).

1.3 References

Document No.	Description	Revision
9003000-10XXX	End Item Drawing – TCAS 3000 6MCU (AC/DC)	- (or subsequent)
9003000-65XXX	End Item Drawing – TCAS 3000 4MCU (AC/DC)	- (or subsequent)
9003000-55XXX	End Item Drawing – TCAS 3000 4MCU (DC only)	- (or subsequent)
8002229-001	CCP Hardware Test Software TRD	- (or subsequent)
MT7024778	RFIU Cert. and Std	G (or subsequent)
8002050-001	TCAS 3000 System Requirements Specification	- (or subsequent)
8002215-001	TCAS 3000 Hardware Requirements Document	- (or subsequent)
8002206-001	CPA I/O FPGA Hardware Requirements Document	- (or subsequent)
8002210-001	CPA RF FPGA Hardware Requirements Document	- (or subsequent)
8002202-001	CPA CPLD Hardware Requirements Document	- (or subsequent)

1.4 Definitions

1.4.1 Acronyms and Abbreviations

Acronym	Definition
ACSS	Aviation Communication and Surveillance Systems
AIU	Aircraft Interface Unit
BITE	Built In Test Equipment
CCP	Common Computing Platform
CPA	Common Processor Assembly
CPLD	Complex Programmable Logic Devices
CRC	Cyclic Redundancy Check

ECC	Error Checking and Correction
EPROM	Erasable Programmable Read-Only Memory
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESS	Environment Stress Screening
FPGA	Field Programmable Gate Array
GPS	Global Positioning System
HBM	Heartbeat Monitor
HRD	Hardware Requirements Document
HTS	Hardware Test Software
I^2C	Inter-Integrated Circuit
IO	Input/Output
JTAG	Joint Test Action Group
LRU	Line Replaceable Unit
MMU	Memory Management Unit
Msec	Milliseconds
MTS	Manufacturing Test Station
P1	Processor 1
P2	Processor 2
PCI	Peripheral Components Interconnect
PDL	Portable Data Loader
QA	Quality Assurance
RFIU	RF Interface Unit
SDRAM	Synchronous Dynamic Random Access Memory
TCAS	Traffic Collision Avoidance System
TRD	Test Requirements Document
UART	Universal Asynchronous Receiver/Transmitter
UUT	Unit Under Test

1.4.2 Terms and Phrases

Term	**Definition**
4096 Code Information	Transponder transmissions may contain beacon 4096 code information, which can be used by the ground system to look up flight identification.
C2-SPI	Suppression Pulse Inhibit signal referenced to the C2 ATCRBS pulse.
Gillham Code	An eleven bit discrete word with altitude information encoded within.

2 GENERAL INFORMATION

2.1 General Requirements

The following conditions are recommended for performing tests on a TCAS 3000 LRU:

- Temperature = 25 ± 5 ºC
- Relative humidity = 95% maximum
- Pressure = between 20 and 32 in Hg
- Power to the UUT should be removed before attaching or removing any interconnecting systems.

2.2 General RF Test Requirements

- All antenna ports must be terminated in 50 ohms while power is applied to the UUT.
- Test equipment connected to the antenna ports must have a voltage standing wave ratio (VSWR) of less than 1.5:1.
- Test equipment connected to the antenna ports shall withstand peak power levels of at least 1000 W and average power levels of at least 2 W.
- RF power values are specified as measured at the rear connector of the UUT. If cabling or test equipment introduces losses into the measurement, these losses shall be allowed for in the values reported by the test equipment.
- **Figure 1** shows the basic characteristics which define a pulse. **Figure 2** through **Figure 4** provide information about pulse identification and the method of measuring pulse parameters for the RF measurements. The actual specification values for these parameters are listed in the RF test procedure paragraphs. **Figure 5** describes the format of the AOA Word.

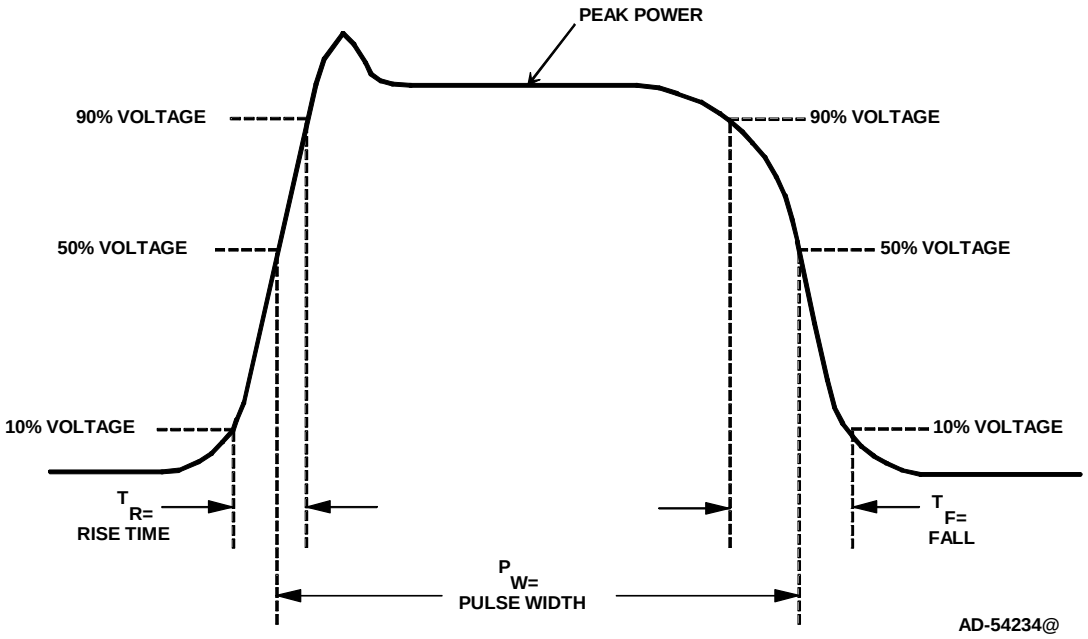


Figure 1. Basic Pulse Measurements

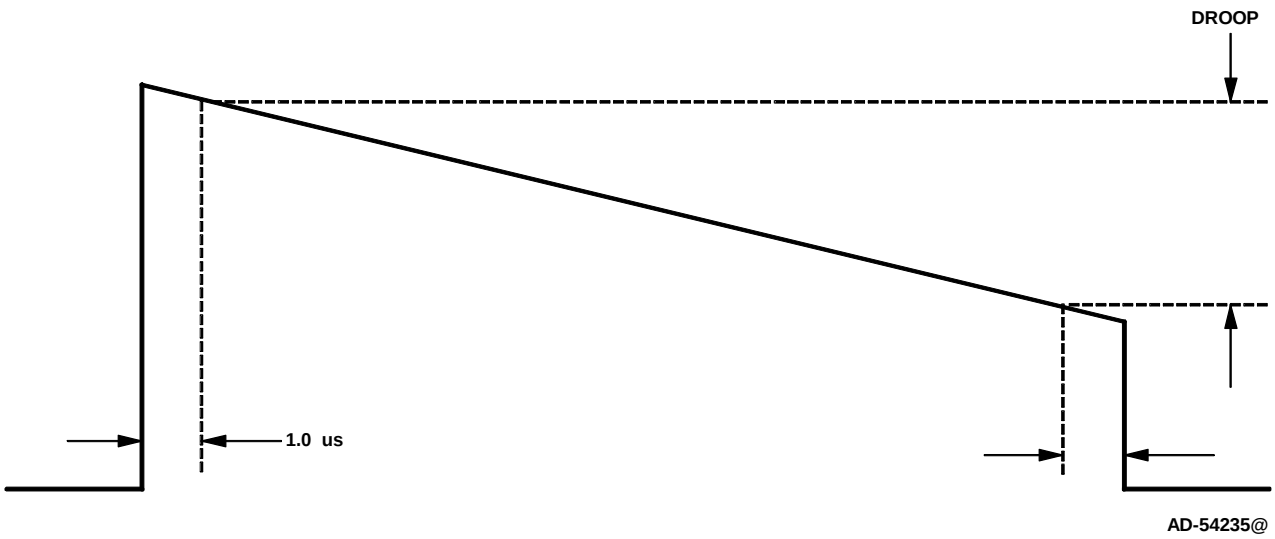


Figure 2. Pulse Droop Measurements

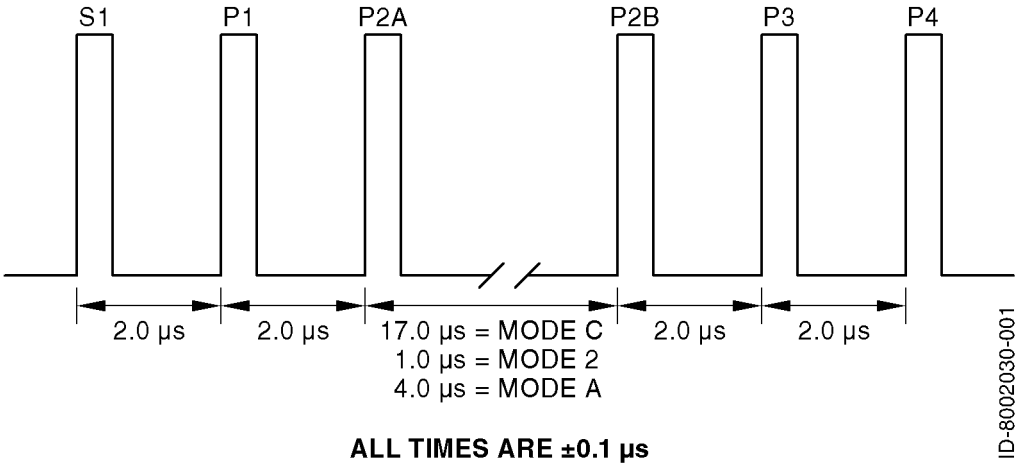


Figure 3. ATCRBS Pulse Format

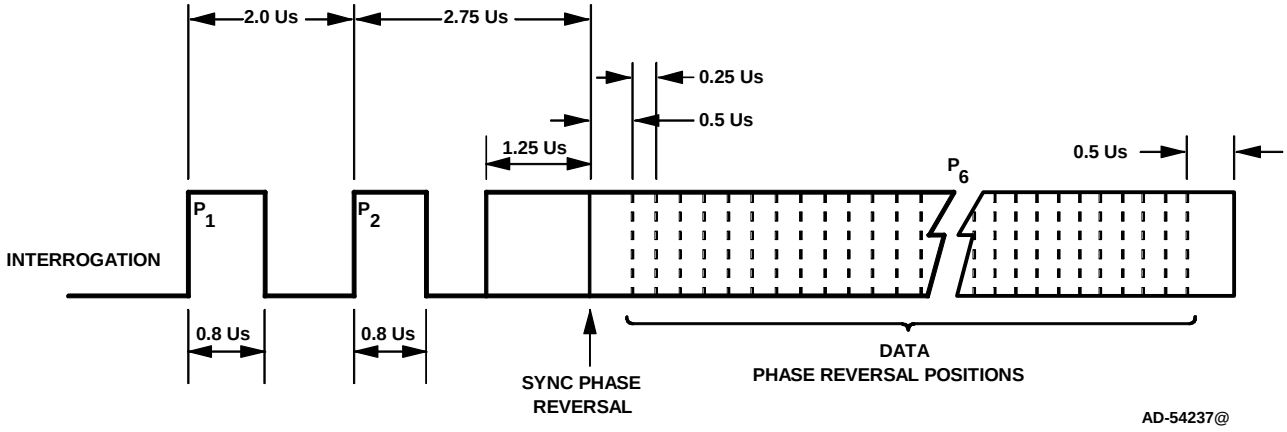


Figure 4. Mode S Pulse Format

```
Bit
 31 30 29  28              22  21            16 15 14 13  12              6  5               0
| Z | N | S |<----- CV ----->|<----- PD ------>| Z | N | S |<----- CV ----->|<----- PD ------>|
```

Figure 5. AOA Word 1&2 / 3&4 Format

NOTES:

Z = 1 : Power at 0 degree port > Power at 180 degree port
Z = 0 : Power at 0 degree port < Power at 180 degree port
N = 1 : Power at 90 degree port > Power at 270 degree port
N = 0 : Power at 90 degree port < Power at 270 degree port
S = 1 : Power at 0 or 180 degree port < Power at 90 or 270 degree port
S = 0 : Power at 0 or 180 degree port > Power at 90 or 270 degree port
PD = Power Difference in dB, 00 = 0.000 dB
3F = 18.207 dB

Multiply the PD (Power Difference in dB) by -1 if:

Z = 1 and N = 1 and S = 1
or Z = 0 and N = 1 and S = 0
or Z = 0 and N = 0 and S = 1
or Z = 1 and N = 0 and S = 0

CV = Composite Video (Overall Power Level) in dBm, 00 = -92.889 dBm
7F = -19.511 dBm

2.3 Power Requirements

The following are power requirements for operating test equipment:

- 115 Vac, 60 Hz, 20 A standard service power for test equipment operation.

3 TEST EQUIPMENT REQUIREMENTS

3.1 Test Equipment Hardware

The test equipment hardware that is required to perform the tests as described in this document is as follows:

- TCAS MTS, Part No. T336255 (Mod D or subsequent) - **Or equivalent functionality**

  T336255 contains the following assemblies which may be referenced in this document:

  - Aircraft interface unit (AIU) – Part No. T336253
  - RF interface unit (RIU) – Part No. T336254
  - PDL panel – Part No. T336259
  - Tray assembly – Part No. T336255-26

3.2 Test Equipment Software

If a TCAS MTS is to be used for performing the tests described in this document, the testing process may be automated using a version of the 'C' language such as National Instruments LabWindows CVI version 5.0.1 or subsequent.

Hardware Test Software (HTS) must be loaded into the UUT prior to executing the tests described in this document. Refer to Appendix A of this document for loading of HTS into the UUT.

3.3 Test Equipment / UUT Setup

Figure 6 shows the TCAS 3000 Architectural Block Diagram and **Figure 7** shows the TCAS 3000 System Block Diagram. **Figure 8** shows a typical interconnection between MTS test equipment and the UUT for performing the tests described in this document.

Step 1. Power up ACSS and commercial test equipment and allow it to warm up for at least 30 minutes. Verify that test equipment used is calibrated and functioning properly.

Step 2. If HTS has not been loaded into the UUT, perform the steps described in Appendix A of this document.

Step 3. If calibration has not been performed on the UUT, perform the steps in Appendix B & C

Step 4. From the test PC, launch HyperTerminal (or an application with similar capabilities i.e Labwindows etc) and setup the test PC's (RS232) COM2 port for the following:

Baud rate = 115200, Number of bits = 8, Parity = None, Stop Bits = 1, Flow Control = None.

Step 5. Connect PC COM2 pin 2 (Tx) to UUT PDL connector pin 40 (Rx). Connect PC COM2 pin 3 (Rx) to UUT PDL connector pin 41 (Tx) and connect PC COM2 pin 5 (Gnd) to UUT PDL connector pin 48 (Gnd).

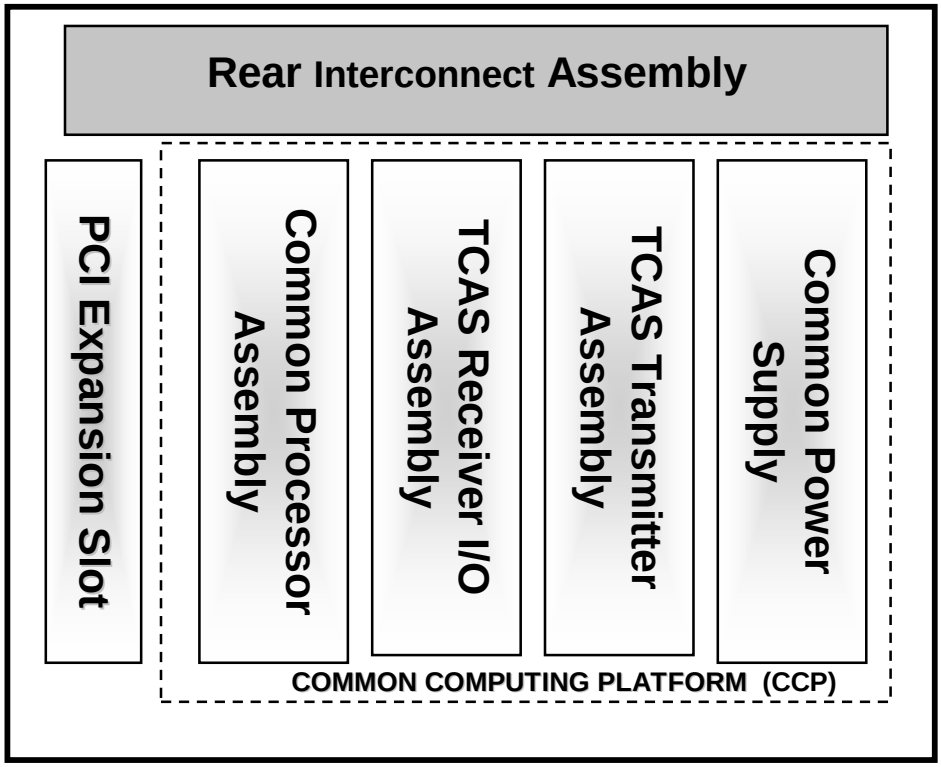


Figure 6. TCAS 3000 Architectural Block Diagram

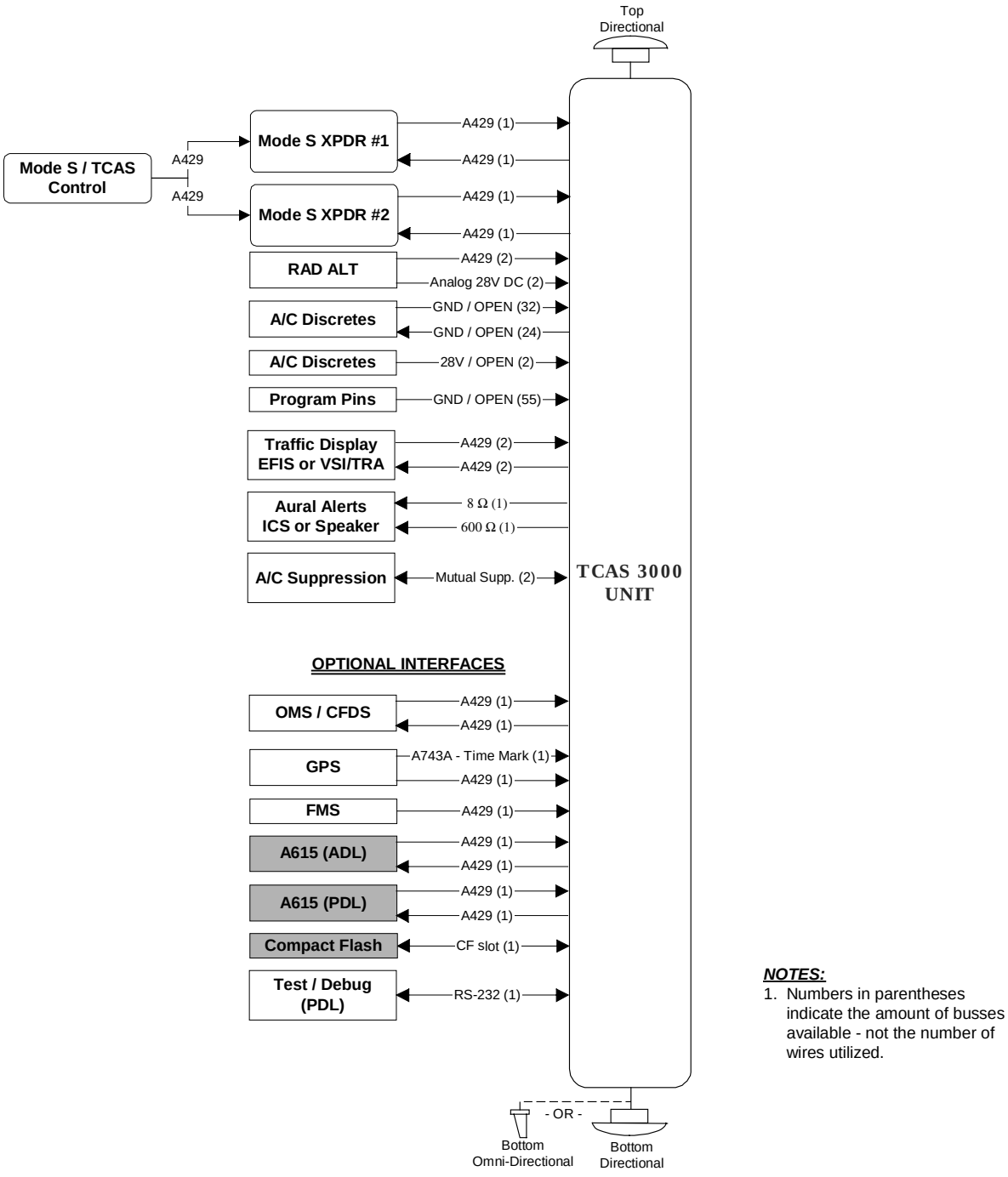


Figure 7. TCAS 3000 System Block Diagram

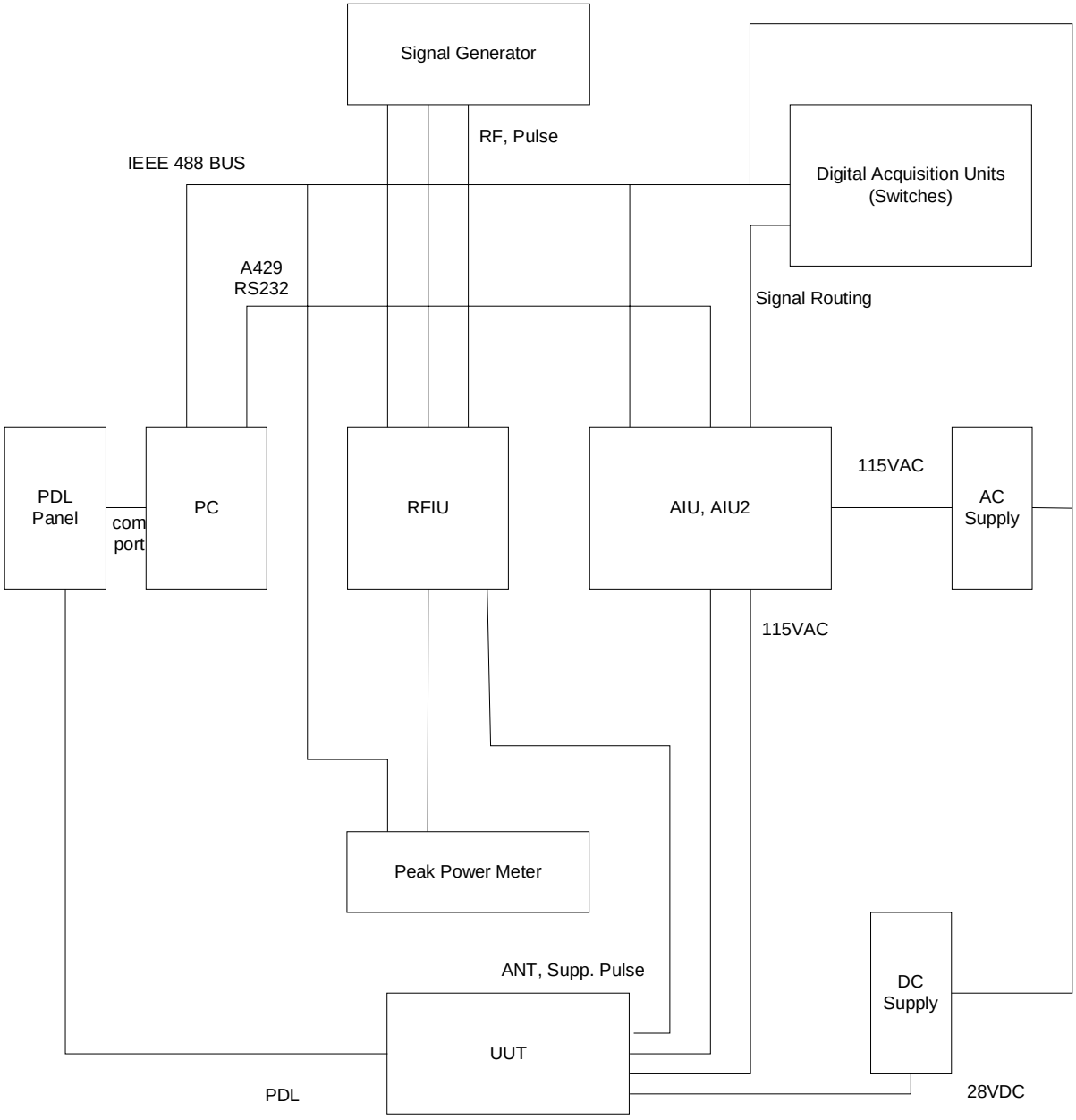


Figure 8. MTS / UUT Interconnect

4 TEST REQUIREMENTS

4.1 AC Input Power Tests

The following tests are only to be performed on a UUT that is able to accept AC input power. These tests will verify that the UUT consumes less than 70 W in the standby mode at min/max AC input voltage. PDL AC power is also verified at the PDL connector.

4.1.1 Input Power At Min AC Voltage Test

Step 1. If the UUT has DC input power applied, remove the DC input power before continuing.

Step 2. Connect the AC power supply output (H) to UUT pin LBP-1 and AC power supply output (C) to UUT pin LBP-7.

Step 3. Set the AC supply for 97 Vac (± 3.0 Vac).

Step 4. Read the current sourced from the power supply and verify the UUT input power does not exceed 70 W.

Step 5. After approx. 30 seconds from initial power up, the HyperTerminal window should display the HTS prompt. This indicates that the UUT has powered up successfully and is ready to accept test commands. If the HTS prompt is not shown, check all electrical connections and make sure that HyperTerminal has been configured correctly.

4.1.2 Internal Voltage Monitor (+80 Vdc) At Min AC Voltage Test

Step 1. Execute the following HTS commands to read the internal +80 Vdc via Mux #2: "*A2WDC P1 21 1*" , "*ANRDC P1 21 4 V N F*"

Step 2. Verify that the returned value is +80.0 Vdc (± 5.6 Vdc)

4.1.3 Input Power At Max AC Voltage Test

Step 1. Set the AC power supply to 134 Vac (± 2.0 Vac). Read the current sourced from the power supply and verify the UUT input power is less than 70 W.

4.1.4 PDL Power At Nom AC Voltage Test

Step 1. Set the AC power supply to 115 Vac (± 2.0 Vac).

Step 2. Setup the DMM for an ACV measurement. Connect the DMM positive (+) input to UUT PDL pin 20 and connect the DMM negative (-) input to UUT PDL pin 22.

Step 3. Verify that the DMM reads 115 Vac (± 8.0 Vac).

Step 4. Disconnect the DMM from the UUT PDL connector.

4.2 DC Input Power Tests

The following tests will verify that the UUT consumes less than 70 W in the standby mode at min/max DC input voltage. PDL DC power is also verified at the PDL connector.

4.2.1 Input Power At Min DC Voltage Test

Step 1. If the UUT has AC input power applied, remove the AC input power before continuing.

Step 2. Connect the DC power supply positive output (+) to UUT pin LBP-10. Connect the DC power supply negative output (-) to UUT pin LBP-3.

Step 3. Set the DC power supply to +20.5 Vdc (± 1.0 Vdc). Read the current sourced from the power supply and verify the UUT input power is less than 70 W.

Step 4. After approx. 30 seconds from initial power up, the HyperTerminal window should display the HTS prompt. This indicates that the UUT has powered up successfully and is ready to accept test commands. If the HTS prompt is not shown, check all electrical connections and make sure that HyperTerminal has been configured correctly.

4.2.2 Internal Voltage Monitor (+80 Vdc) At Min DC Voltage Test

Step 1. Execute the following HTS commands to read the internal +80 Vdc via Mux #2: "*A2WDC P1 21 1*" , "*ANRDC P1 21 4 V N F*"

Step 2. Verify that the returned value is +80.0 Vdc (± 5.6 Vdc)

4.2.3 Input Power At Max DC Voltage Test

Step 1. Set the DC power supply to +32.2 Vdc (± 1.0 Vdc). Read the current sourced from the power supply and verify the UUT input power is less than 70 W.

4.2.4 PDL Power At Nom DC Voltage Test

Step 1. Set the DC power supply to +27.5 Vdc (± 1.0 Vdc).

Step 2. Setup the DMM for a DCV measurement. Connect the DMM positive (+) input to UUT PDL pin 37 and connect the DMM negative (-) input to UUT PDL pin 38.

Step 3. Verify that the DMM reads +27.5 Vdc (± 1.0 VDC).

Step 4. Disconnect the DMM from the UUT PDL connector.

4.3 Data Log Retrieval

4.3.1 Maintenance Log Dump

The following steps will allow the UUT to dump the contents of it's maintenance log to the test PC's hard drive.

Step 1. Execute the HTS command "*MLD P1 2*", to begin the dump of the maintenance log to the PC's hard drive. Allow the dump to complete before continuing.

4.3.2 Event Log Dump

The following steps will allow the UUT to dump the contents of it's event log to the test PC's hard drive.

Step 1. Execute the HTS command "*ELD P1 2* to begin the dump of the event log to the PC's hard drive. Allow the dump to complete before continuing.

4.4 Voltage Monitor Tests

The following tests will verify that the internal voltage monitor circuitry is functioning correctly and that the internal fixed voltages are within specifications.

4.4.1 Internal Voltage Monitor (+1.2 Vdc) Test

The following steps will verify that the internal +1.2 Vdc is within specifications.

Step 1. Execute the following HTS commands to read the internal +1.2 Vdc via Mux #0: "*A2WDC P1 0 1*" , "*ANRDC P1 0 4 V N F*"

Step 2. Verify that the returned value is +1.2 Vdc (± 0.06 Vdc)

4.4.2 Internal Voltage Monitor (+2.0 Vdc) Test

The following steps will verify that the internal +2.0 Vdc is within specifications.

Step 1. Execute the following HTS commands to read the internal +2.0 Vdc via Mux #0: "*A2WDC P1 1 1*" , "*ANRDC P1 1 4 V N F*"

Step 2. Verify that the returned value is +2.0 Vdc (± 0.1 Vdc)

4.4.3 Internal Voltage Monitor (+2.5 Vdc) Test

The following steps will verify that the internal +2.5 Vdc is within specifications.

Step 1. Execute the following HTS commands to read the internal +2.5 Vdc via Mux #0: "*A2WDC P1 3 1*" , "*ANRDC P1 3 4 V N F*"

Step 2. Verify that the returned value is +2.5 Vdc (± 0.14 Vdc)

4.4.4 Internal Voltage Monitor (-2.5 Vdc) Test

The following steps will verify that the internal -2.5 Vdc is within specifications.

Step 1. Execute the following HTS commands to read the internal -2.5 Vdc via Mux #0: "*A2WDC P1 4 1*" , "*ANRDC P1 4 4 V N F*"

Step 2. Verify that the returned value is -2.5 Vdc (± 0.14 Vdc)

4.4.5 Internal Voltage Monitor (+3.3 Vdc) Test

The following steps will verify that the internal +3.3 Vdc Filtered is within specifications.

Step 1. Execute the following HTS commands to read the internal +3.3 Vdc via Mux #3: "*A2WDC P1 26 1*" , "*ANRDC P1 26 4 V N F*"

Step 2. Verify that the returned value is 3.3 Vdc (± 0.150 Vdc)

4.4.6 Internal Voltage Monitor (+5V Filter) Test

The following steps will verify that the internal +5.0 V Filter is within specifications.

Step 1. Execute the following HTS commands to read the internal +5V Filter via Mux #0: "*A2WDC P1 2 1*" , "*ANRDC P1 2 4 V N F*"

Step 2. Verify that the returned value is +5.0 Vdc (± 0.2 Vdc)

4.4.7 Internal Voltage Monitor (-5V Filter) Test

The following steps will verify that the internal -5 V Filter is within specifications.

Step 1. Execute the following HTS commands to read the internal -5V Filter via Mux #0: "*A2WDC P1 6 1*" , "*ANRDC P1 6 4 V N F*"

Step 2. Verify that the returned value is -5 Vdc (± 0.2 Vdc)

4.4.8 Internal Voltage Monitor (+12 Vdc for APM) Test

The following steps will verify that the internal +12 Vdc for APM is within specifications.

Step 1. Execute the following HTS commands to read the internal +12 Vdc via Mux #2: "*A2WDC P1 19 1*" , "*ANRDC P1 19 4 V N F*"

Step 2. Verify that the returned value is +12 Vdc (± 2.4 Vdc)

4.4.9 Internal Voltage Monitor (+15V Filtered) Test

The following steps will verify that the internal +15V Filtered is within specifications.

Step 1. Execute the following HTS commands to read the internal +15V Filtered via Mux #3: "*A2WDC P1 24 1*" , "*ANRDC P1 24 4 V N F*"

Step 2. Verify that the returned value is +15.0 Vdc (±1.7 Vdc)

4.4.10 Internal Voltage Monitor (-15V Filtered) Test

The following steps will verify that the internal -15V Filtered is within specifications.

Step 1. Execute the following HTS commands to read the internal -15V Filtered via Mux #3: "*A2WDC P1 25 1*" , "*ANRDC P1 25 4 V N F*"

Step 2. Verify that the returned value is -15.0 Vdc (± 1.7 Vdc)

4.4.11 Internal Voltage Monitor (+36 Vdc) Test

The following steps will verify that the internal +36 Vdc is within specifications.

Step 1. Execute the following HTS commands to read the internal +36 Vdc via Mux #2: "*A2WDC P1 18 1*" , "*ANRDC P1 18 4 V N F*"

Step 2. Verify that the returned value is +36 Vdc (± 2.9 Vdc)

4.4.12 Internal Voltage Monitor (-40 Vdc) Test

The following steps will verify that the internal (scaled) –40 Vdc is within specifications.

Step 1. Execute the following HTS commands to read the internal -40 Vdc via Mux #2: "*A2WDC P1 16 1*" , "*ANRDC P1 16 4 V N F*"

Step 2. Verify that -44.8 Vdc ≤ returned value ≤ –38.0 Vdc

4.4.13 Internal Voltage Monitor (+50 Vdc) Test

The following steps will verify that the internal +50 Vdc is within specifications.

Step 1. Execute the following HTS commands to read the internal +50 Vdc via Mux #2: "*A2WDC P1 17 1*" , "*ANRDC P1 17 4 V N F*

Step 2. Verify that the returned value is +50 Vdc (± 4.0 Vdc)

4.4.14 Internal Voltage Monitor (Temp Sensor) Test

The following steps will verify that the internal Temp Sensor is within specifications.

Step 1. Execute the following HTS commands to read the internal Temp Sensor via Mux #1: "*A2WDC P1 8 1*" , "*ANRDC P1 8 4 V N F*"

Step 2. Verify that the returned value is +2.98 Vdc (+0.65, -0.07 Vdc)

4.4.15 Internal Voltage Monitor (Mux #0 Gnd) Test

The following steps will verify that the internal Mux #0 Gnd is within specifications.

Step 1. Execute the following HTS commands to read the internal Gnd via Mux #0: "*A2WDC P1 7 1*" , "*ANRDC P1 7 4 V N F*"

Step 2. Verify that the returned value is 0.0 Vdc (± 0.1 Vdc)

4.4.16 Internal Voltage Monitor (Mux #1 Gnd) Test

The following steps will verify that the internal Mux #1 Gnd is within specifications.

Step 1. Execute the following HTS commands to read the internal Gnd via Mux #1: "*A2WDC P1 15 1*" , "*ANRDC P1 15 4 V N F*"

Step 2. Verify that the returned value is 0.0 Vdc (± 0.1 Vdc)

4.4.17 Internal Voltage Monitor (Mux #2 Gnd) Test

The following steps will verify that the internal Mux #2 Gnd is within specifications.

Step 1. Execute the following HTS commands to read the internal Gnd via Mux #2: "*A2WDC P1 23 1*" , "*ANRDC P1 23 4 V N F*"

Step 2. Verify that the returned value is 0.0 Vdc (± 0.1 Vdc)

4.4.18 Internal Voltage Monitor (Mux #3 Gnd1) Test

The following steps will verify that the internal Mux #3 Gnd1 is within specifications.

Step 1. Execute the following HTS commands to read the internal Gnd1 via Mux #3: "*A2WDC P1 27 1*" , "*ANRDC P1 27 4 V N F*"

Step 2. Verify that the returned value is 0.0 Vdc (± 0.1 Vdc)

4.4.19 Internal Voltage Monitor (Mux #3 Gnd2) Test

The following steps will verify that the internal Mux #3 Gnd2 is within specifications.

Step 1. Execute the following HTS commands to read the internal Gnd2 via Mux #3: "*A2WDC P1 28 1*" , "*ANRDC P1 28 4 V N F*"

Step 2. Verify that the returned value is 0.0 Vdc (± 0.1 Vdc)

4.4.20 Analog 2W DC (Radio Alt Input #1) Test

The following steps will verify that internal voltage monitor circuitry is functioning correctly and is able to read a voltage applied to the Radio Alt Input #1.

Note: If a TCAS MTS – Part No. T336255 is being used for this test, the UUT pin connections and associated circuitry are already available (connected) within the AIU.

Step 1. Apply +10 Vdc (± 1.0 Vdc) between UUT pin RMP-2H (+) and UUT RMP-2J (-).

Step 2. Execute the following HTS commands to read the external +10 Vdc via Mux #1: "*A2WDC P1 11 1*" , "*ANRDC P1 11 4 V N F*"

Step 3. Verify that the returned value is +10 Vdc (± 1.0 Vdc)

Step 4. Remove the +10 Vdc from the UUT.

4.4.21 Analog 2W DC (Radio Alt Input #2) Test

The following steps will verify that internal voltage monitor circuitry is functioning correctly and is able to read a voltage applied to the Radio Alt Input #2.

Note: If a TCAS MTS – Part No. T336255 is being used for this test, the UUT pin connections and associated circuitry are already available (connected) within the AIU.

Step 1. Apply +10 Vdc (± 1.0 Vdc) between UUT pin RBP-3A (+) and UUT RBP-3B (-).

Step 2. Execute the following HTS commands to read the external +10 Vdc via Mux #1: "*A2WDC P1 12 1*" , "*ANRDC P1 12 4 V N F*"

Step 3. Verify that the returned value is +10 Vdc (± 1.0 Vdc)

Step 4. Remove the +10 Vdc from the UUT.

4.5 Audio Output Tests

These tests will verify that the Audio Output circuitry is functioning correctly.

Note: If a TCAS MTS – Part No. T336255 is being used for these tests, the UUT pin connections and associated circuitry are already available (connected) within the AIU.

4.5.1 8 Ω Output Amplitude DAC : Pattern 1 Test

The following steps will verify that the 8 Ohm Output circuitry is functioning correctly and that the output amplitude is within specifications when the amplitude control DAC is set to maximum. The DAC is set to maximum when a pattern of all 1's is applied.

Step 1. Connect an 8 ohm (± 1%) 3 watt resistor between UUT pins RMP-2F and RMP-2G.

Step 2. Setup the DMM for an ACV measurement and connect the DMM across the 8 Ohm resistor.

Step 3. Generate a 1KHz tone at the UUT 8 ohm output for 2 seconds with the amplitude control DAC set to a maximum amplitude. This is accomplished by applying all ones to the amplitude control DAC via execution of the HTS command: "*SAY P1 1 255 0*"

Step 4. Read the DMM while the HTS command is executing and verify that the reading is as follows: 16.0 Vpp ≤ reading ≤ 18.0 Vpp.

4.5.2 8 Ω Output Amplitude DAC : Pattern 2 Test

The following steps will verify that the 8 Ohm Output circuitry is functioning correctly and that the output amplitude is within specifications when an alternating pattern of 1's and 0's is applied to the amplitude control DAC.

Step 1. Generate a 1KHz tone at the UUT 8 ohm output for 2 seconds at an amplitude set by an alternating ones and zeros pattern applied to the amplitude control DAC by executing the HTS command: "*SAY P1 1 170 0*"

Step 2. Read the DMM while the HTS command is executing and verify that the reading is as follows: 10.67 Vpp ≤ reading ≤ 12.67 Vpp.

4.5.3 8 Ω Output Amplitude DAC : Pattern 3 Test

The following steps will verify that the 8 Ohm Output circuitry is functioning correctly and that the output amplitude is within specifications when a complimentary (from previous test) alternating pattern of 1's and 0's is applied to the amplitude control DAC.

Step 1. Generate a 1KHz tone at the UUT 8 ohm output for 2 seconds at an amplitude set by an complementary alternating ones and zeros pattern applied to the audio DAC by executing the HTS command: "*SAY P1 1 85 0*"

Step 2. Read the DMM while the HTS command is executing and verify that the reading is as follows: 5.33 Vpp ≤ reading ≤ 7.33 Vpp

Step 3. Disconnect the DMM and 8 ohm resistor from the UUT.

4.5.4 600 Ω Output Amplitude DAC : Pattern 1 Test

The following steps will verify that the 600 Ohm Output circuitry is functioning correctly and that the output amplitude is within specifications when the amplitude control DAC is set to maximum. The DAC is set to maximum when a pattern of all 1's is applied.

Step 1. Connect a 600 ohm (± 5%) 3 watt resistor between UUT pins RMP-3F and RMP-3G.

Step 2. Setup the DMM for an ACV measurement and connect the DMM across the 600 ohm resistor.

Step 3. Generate a 1KHz tone at the 600 ohm output for 2 seconds with the amplitude control DAC set to a maximum amplitude. This is accomplished by applying all ones to the amplitude control DAC via execution of the HTS command: "*SAY P1 1 0 255*"

Step 4. Read the DMM while the HTS command is executing and verify that the reading is as follows: 19.6 Vpp ≤ reading ≤ 23.5 Vpp.

4.5.5 600 Ω Output Amplitude DAC : Pattern 2 Test

The following steps will verify that the 600 Ohm Output circuitry is functioning correctly and that the output amplitude is within specifications when an alternating pattern of 1's and 0's is applied to the amplitude control DAC.

Step 1. Generate a 1KHz tone at the 600 ohm output for 2 seconds at an amplitude set by an alternating ones and zeros pattern applied to the amplitude control DAC by executing the HTS command: "*SAY P1 1 0 170*".

Step 2. Read the DMM while the HTS command is executing and verify that the reading is as follows: 13.06 Vpp ≤ reading ≤ 15.6 Vpp

4.5.6 600 Ω Output Amplitude DAC : Pattern 3 Test

The following steps will verify that the 600 Ohm Output circuitry is functioning correctly and that the output amplitude is within specifications when a complimentary (from previous test) alternating pattern of 1's and 0's is applied to the amplitude control DAC.

Step 1. Generate a 1KHz tone at the 600 ohm output for 2 seconds at an amplitude set by a complementary alternating ones and zeros pattern applied to the amplitude control DAC by executing the HTS command: "*SAY P1 1 0 85*".

Step 2. Read the DMM while the HTS command is executing and verify that the reading is as follows: 6.53 Vpp ≤ reading ≤ 7.8 Vpp.

Step 3. Disconnect the DMM and 600 ohm resistor from the UUT.

4.5.7 8 Ohm Output Audio Test

This test will verify that the 8 Ohm Audio circuitry is able to produce clear, distortionless speech.

Step 1. Connect an 8 ohm speaker between UUT pins RMP-2F and RMP-2G.

Step 2. Execute the HTS command: "*SAY P1 2 100 0 F*". Verify that the speech is clear and recognizable.

Step 3. Disconnect the speaker from the UUT.

4.6 CPLD / Heartbeat Monitor / Power Off Timer Tests

These tests will verify that the CPLD, Heartbeat monitoring and Power Off Timer circuitry is functioning correctly .

4.6.1 CPLD Test

This test will test the general purpose bits within the CPLD register.

Step 1. Execute the HTS command: "*CPLD P1*" and verify that the response is "PASS"

4.6.2 Heartbeat Monitor Shunt Test

This test will verify that the jumper that disables the Heartbeat monitor is not installed.

Step 1. Execute the HTS command: "*HBT*" and verify that the response is "PASS"

4.6.3 Heartbeat Monitor Reset Test

This test will verify that the Heartbeat Monitor circuitry is functioning correctly by causing the UUT to reset when the Heartbeat is allowed to time-out.

Step 1. Execute the HTS command: "*HBF 1*".

Step 2. Verify that the UUT resets after approximately 30 seconds by observing that Boot messages are followed by the HTS prompt on the test PC's CRT.

4.6.4 Power Off Timer Test

This test will verify that the power off timer circuitry is function correctly by performing the charge/discharge/recharge operation.

Step 1. Execute the HTS command: *"POTT P1"* and verify that the response is "Ok"

4.7 Ethernet Tx/Rx Wrap Tests

These tests will verify that the Ethernet Interface is functioning correctly by transmitting and receiving several packets of alternating ones and zeros via a wrap around.

4.7.1 Ethernet Tx/Rx AA Test

Step 1. Connect a jumper between UUT PDL connector pins 6 and 23. This connects Ethernet Tx+ to Rx+.

Step 2. Connect a jumper between UUT PDL connector pins 7 and 39. This connects Ethernet Tx- to Rx-.

Step 3. Execute the following HTS commands: "*ETH P1 A*"

Step 4. Verify that the returned response is "PASS*"*

4.7.2 Ethernet Tx/Rx 55 Test

Step 1. Execute the following HTS commands: "*ETH P1 5*"

Step 2. Verify that the returned response is "PASS*"*

Step 3. Remove the jumpers from the UUT PDL connector

4.8 Compact Flash Tests

These test will verify that the compact flash interface circuitry is functioning correctly.

4.8.1 Compact Flash Detect Test

This test will verify that a compact flash card will be detected when inserted into the slot.

Step 1. Verify that a compact flash card is not currently inserted into the UUT.

Step 2. Execute the HTS command: "*RW P1 FF800000*" and verify that the returned response is "0xFXXX". Where X = don't care.

Step 3. Insert a formatted test compact flash card into the UUT's compact flash slot.

Step 4. Execute the HTS command: "RW P1 FF800000" and verify that the returned response is "0x7XXX". Where X = don't care.

4.8.2 Compact Flash Write/Read Test

This test will verify that the compact flash interface circuitry is functioning correctly and that data is able to be written to and read from a compact flash card.

Step 1. Verify that the test compact flash card is currently inserted into the UUT.

***Note*:** This card will be written to.

Step 2. Execute the following HTS command: "*TCF P1 A3E "*

Step 3. Verify that the returned result is "PASS"

4.9 Input Discretes Tests

These tests will verify that the input discretes circuitry is functioning correctly.

Note: If the MTS station is utilized for these tests, the input discrete pins (Words 1/2/3/7) are ganged together in groups (nets) which are then driven by the MTS drivers. Because the MTS station was designed for earlier versions of TCAS, the mapping of the input discrete pins to input discrete words for TCAS 3000 does not match the earlier versions of TCAS. Therefore, when an input discrete word is read, several adjacent bits may have the same value. As a consequence, input discrete words that are read back will not reflect the traditional alternating ones and zeros pattern. The tests as described below show the results as if adjacent pins (bits) are being driven by alternating ones and zeros (the ideal case).

4.9.1 Input Discrete Words: Pattern 1 Test

This test will verify that the interface from the UUT connector pins to the I/O FPGA Discrete In Words are functioning correctly. A pattern of alternating ones and zeros will be applied to the UUT pins which correspond to bits in Input Discrete Word # 1. All seven of the Input Discrete words will then be read back and verified that they have the correct bit patterns.

Step 1. Apply a ground to the following UUT pins:

Bit	UUT Pin		Bit	UUT Pin		Bit	UUT Pin		Bit	UUT Pin
31	RMP-12D		23	RMP-10K		15	N/C = 0		7	RMP-6J
29	RMP-12B		21	RMP-10H		13	N/C = 0		5	RMP-6G
27	RMP-11D		19	RMP-10D		11	RBP-6D		3	RMP-6E
25	RMP-11B		17	RMP-10B		9	RBP-6B		1	RMP-5F

Step 2. Read input discrete word #1 by executing the HTS command: "*RL P1 F0070000*" and verify that the returned response is "0x55551555".

Step 3. Read input discrete word #2 by executing the HTS command: "*RL P1 F0071000*" and verify that the returned response is "0xFFFFFFFF".

Step 4. Read input discrete word #3 by executing the HTS command: "*RL P1 F0072000*" and verify that the returned response is "0x20000007".

Step 5. Read input discrete word #4 by executing the HTS command: "*RL P1 F0073000*" and verify that the returned response is "0x00FFFFFF".

Step 6. Read input discrete word #5 by executing the HTS command: "*RL P1 F0074000*" and verify that the returned response is "0xFFFFFFFF".

Step 7. Read input discrete word #6 by executing the HTS command: "*RL P1 F0075000*" and verify that the returned response is "0xFFFFFFFF".

Step 8. Read input discrete word #7 by executing the HTS command: "*RL P1 F0076000*" and verify that the returned response is "0xFFFFFFFF".

Step 9. Remove the grounds from the UUT pins.

Note: If the MTS station is used for this test, the UUT pins are connected to nets that may result in shared bits. Therefore, verify that the read back patterns are as follows:

Word #1						Word #7
2AA51555	EAB5A96B	20000007	00FFFFFF	FFFFFFFF	FFFFFFFF	B9EAB1FA

4.9.2 Input Discrete Words: Pattern 2 Test

This test will verify that the interface from the UUT connector pins to the I/O FPGA Discrete In Words are functioning correctly. A pattern of complimentary alternating ones and zeros will be applied to the UUT pins which correspond to bits in Input Discrete Word # 1. All seven of the Input Discrete words will then be read back and verified that they have the correct bit patterns.

Step 1. Apply a ground to the following UUT pins:

Bit	UUT Pin		Bit	UUT Pin		Bit	UUT Pin		Bit	UUT Pin
30	RMP-12C		22	RMP-10J		14	N/C = 0		6	RMP-6H
28	RMP-12A		20	RMP-10G		12	Tst Sw = 1		4	RMP-6F
26	RMP-11C		18	RMP-10C		10	RBP-6C		2	RMP-5G
24	RMP-11A		16	RMP-10A		8	RBP-6A		0	RMP-5E

Step 2. Read input discrete word #1 by executing the HTS command: "*RL P1 F0070000*" and verify that the returned response is "0xAAAA1AAA".

Step 3. Read input discrete word #2 by executing the HTS command: "*RL P1 F0071000*" and verify that the returned response is "0xFFFFFFFF".

Step 4. Read input discrete word #3 by executing the HTS command: "*RL P1 F0072000*" and verify that the returned response is "0x20000007".

Step 5. Read input discrete word #4 by executing the HTS command: "*RL P1 F0073000*" and verify that the returned response is "0x00FFFFFF".

Step 6. Read input discrete word #5 by executing the HTS command: "*RL P1 F0074000*" and verify that the returned response is "0xFFFFFFFF".

Step 7. Read input discrete word #6 by executing the HTS command: "*RL P1 F0075000*" and verify that the returned response is "0xFFFFFFFF".

Step 8. Read input discrete word #7 by executing the HTS command: "*RL P1 F0076000*" and verify that the returned response is "0xFFFFFFFF".

Step 9. Remove the grounds from the UUT pins.

Note: If the MTS station is used for this test, the UUT pins are connected to nets that may result in shared bits. Therefore, verify that the read back patterns are as follows:

Word #1						Word #7
D55A1AAA	954A56F4	20000007	00FFFFFF	FFFFFFFF	FFFFFFFF	D7154EF5

4.9.3 Input Discrete Words: Pattern 3 Test

This test will verify that the interface from the UUT PDL connector pins to the I/O FPGA Discrete In Words are functioning correctly. Grounds will be applied to UUT PDL pins which correspond to bits in Input Discrete Word # 1. All of the Input Discrete words (1-7) will then be read back and verified that they have the correct bit patterns.

Step 1. Apply a ground to the following UUT pins: PDL-53 (Bit 11), PDL-51 (Bit 9)

Step 2. Read input discrete word #1 by executing the HTS command: "*RL P1 F0070000*" and verify that the returned response is "0xFFFF15FF".

Step 3. Read input discrete word #2 by executing the HTS command: "*RL P1 F0071000*" and verify that the returned response is "0xFFFFFFFF".

Step 4. Read input discrete word #3 by executing the HTS command: "*RL P1 F0072000*" and verify that the returned response is "0x20000007".

Step 5. Read input discrete word #4 by executing the HTS command: "*RL P1 F0073000*" and verify that the returned response is "0x00FFFFFF".

Step 6. Read input discrete word #5 by executing the HTS command: "*RL P1 F0074000*" and verify that the returned response is "0xFFFFFFFF".

Step 7. Read input discrete word #6 by executing the HTS command: "*RL P1 F0075000*" and verify that the returned response is "0xFFFFFFFF".

Step 8. Read input discrete word #7 by executing the HTS command: "*RL P1 F0076000*" and verify that the returned response is "0xFFFFFFFF".

Step 9. Remove the grounds from the UUT pins.

Note: If the MTS station is used for this test, the UUT pins are connected to nets that may result in shared bits. Therefore, verify that the read back patterns are as follows:

Word #1						Word #7
FFFF15FF	FFFFFFFF	20000007	00FFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF

4.9.4 Input Discrete Words: Pattern 4 Test

This test will verify that the interface from the UUT PDL connector and from the front panel test switch to the I/O FPGA Discrete In Words are functioning correctly. A ground will be applied to a UUT PDL pin which corresponds to a bit in Input Discrete Word # 1. The operator will also be prompted to press the test switch. All of the Input Discrete words (1-7) will then be read back and verified that they have the correct bit patterns.

Step 1. Apply a ground to UUT pin PDL-52 (Bit 10).

Step 2. While keeping the Test Switch on the front panel of the UUT depressed, read input discrete word #1 by executing the HTS command: "*RL P1 F0070000*" and verify that the returned response is "0xFFFF0BFF".

Step 3. Read input discrete word #2 by executing the HTS command: "*RL P1 F0071000*" and verify that the returned response is "0xFFFFFFFF".

Step 4. Read input discrete word #3 by executing the HTS command: "*RL P1 F0072000*" and verify that the returned response is "0x20000007".

Step 5. Read input discrete word #4 by executing the HTS command: "*RL P1 F0073000*" and verify that the returned response is "0x00FFFFFF".

Step 6. Read input discrete word #5 by executing the HTS command: "*RL P1 F0074000*" and verify that the returned response is "0xFFFFFFFF".

Step 7. Read input discrete word #6 by executing the HTS command: "*RL P1 F0075000*" and verify that the returned response is "0xFFFFFFFF".

Step 8. Read input discrete word #7 by executing the HTS command: "*RL P1 F0076000*" and verify that the returned response is "0xFFFFFFFF".

Step 9. Release the Test Switch and remove the ground from the UUT PDL pin.

Note: If the MTS station is used for this test, the UUT pins are connected to nets that may result in shared bits. Therefore, verify that the read back patterns are as follows:

Word #1						Word #7
FFFF0BFF	FFFFFFFF	20000007	00FFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF

4.9.5 Input Discrete Words: Pattern 5 Test

This test will verify that the interface from the UUT connector pins to the I/O FPGA Discrete In Words are functioning correctly. A pattern of alternating ones and zeros will be applied to the UUT pins which correspond to bits in Input Discrete Word #2. All seven of the Input Discrete words will then be read back and verified that they have the correct bit patterns.

Step 1. Apply a ground to the following UUT pins:

Bit	UUT Pin		Bit	UUT Pin		Bit	UUT Pin		Bit	UUT Pin
31	N/A = 0		23	RBP-8H		15	RBP-7J		7	RBP-7A
29	RBP-9G		21	RBP-8F		13	RBP-7G		5	RBP-6J
27	RBP-9E		19	RBP-8D		11	RBP-7E		3	RMP-12J
25	RBP-8K		17	RBP-8B		9	RBP-7C		1	RMP-12G

Step 2. Read input discrete word #1 by executing the HTS command: "*RL P1 F0070000*" and verify that the returned response is "0xFFFF1FFF".

Step 3. Read input discrete word #2 by executing the HTS command: "*RL P1 F0071000*" and verify that the returned response is "0x55555555".

Step 4. Read input discrete word #3 by executing the HTS command: "*RL P1 F0072000*" and verify that the returned response is "0x20000007".

Step 5. Read input discrete word #4 by executing the HTS command: "*RL P1 F0073000*" and verify that the returned response is "0x00FFFFFF".

Step 6. Read input discrete word #5 by executing the HTS command: "*RL P1 F0074000*" and verify that the returned response is "0xFFFFFFFF".

Step 7. Read input discrete word #6 by executing the HTS command: "*RL P1 F0075000*" and verify that the returned response is "0xFFFFFFFF".

Step 8. Read input discrete word #7 by executing the HTS command: "*RL P1 F0076000*" and verify that the returned response is "0xFFFFFFFF".

Step 9. Remove the grounds from the UUT pins.

Note: If the MTS station is used for this test, the UUT pins are connected to nets that may result in shared bits. Therefore, verify that the read back patterns are as follows:

Word #1 Word #7

DD5E1FAF 55DAD6D4 20000007 00FFFFFF FFFFFFFF FFFFFFFF D7354EF7

4.9.6 Input Discrete Words: Pattern 6 Test

This test will verify that the interface from the UUT connector pins to the I/O FPGA Discrete In Words are functioning correctly. A pattern of complimentary alternating ones and zeros will be applied to the UUT pins which correspond to bits in Input Discrete Word # 2. All seven of the Input Discrete words will then be read back and verified that they have the correct bit patterns.

Step 1. Apply +28 Vdc to UUT pin RMP-2K.

Step 2. Apply a ground to the following UUT pins:

Bit	UUT Pin		Bit	UUT Pin		Bit	UUT Pin		Bit	UUT Pin
30	RBP-10K		22	RBP-8G		14	RBP-7H		6	RBP-6K
28	RBP-9F		20	RBP-8E		12	RBP-7F		4	RMP-12K
26	RBP-9D		18	RBP-8C		10	RBP-7D		2	RMP-12H
24	RBP-8J		16	RBP-8A		8	RBP-7B		0	RMP-12E

Step 3. Read input discrete word #1 by executing the HTS command: "*RL P1 F0070000*" and verify that the returned response is "0xFFFF1FFF".

Step 4. Read input discrete word #2 by executing the HTS command: "*RL P1 F0071000*" and verify that the returned response is "0xAAAAAAAA".

Step 5. Read input discrete word #3 by executing the HTS command: "*RL P1 F0072000*" and verify that the returned response is "0x20000007".

Step 6. Read input discrete word #4 by executing the HTS command: "*RL P1 F0073000*" and verify that the returned response is "0x00FFFFFF".

Step 7. Read input discrete word #5 by executing the HTS command: "*RL P1 F0074000*" and verify that the returned response is "0xFFFFFFFF".

Step 8. Read input discrete word #6 by executing the HTS command: "*RL P1 F0075000*" and verify that the returned response is "0xFFFFFFFF".

Step 9. Read input discrete word #7 by executing the HTS command: "*RL P1 F0076000*" and verify that the returned response is "0xFFFFFFFF".

Step 10. Remove the +28 Vdc and grounds from the UUT pins.

Note: If the MTS station is used for this test, the UUT pins are connected to nets that may result in shared bits. Therefore, the read back patterns are specified as follows:

Word #1 Word #7

22A11357 AA25292B 20000007 00FFFFFF FFFFFFFF FFFFFFFF B9CAB1F8

4.9.7 Input Discrete Words: Pattern 7 Test

This test will verify that the interface from the UUT connector pins to the I/O FPGA Discrete In Words are functioning correctly. A pattern of alternating ones and zeros will be applied to the UUT pins which correspond to bits in Input Discrete Word #3. All seven of the Input Discrete words will then be read back and verified that they have the correct bit patterns.

Step 1. Apply +28 Vdc to UUT pins RBP-3C (Bit 2), and RMP-4K (Bit 0).

Step 2. Read input discrete word #1 by executing the HTS command: "*RL P1 F0070000*" and verify that the returned response is "0xFFFF1FFF".

Step 3. Read input discrete word #2 by executing the HTS command: "*RL P1 F0071000*" and verify that the returned response is "0xFFFFFFFF".

Step 4. Read input discrete word #3 by executing the HTS command: "*RL P1 F0072000*" and verify that the returned response is "0x20000005".

Step 5. Read input discrete word #4 by executing the HTS command: "*RL P1 F0073000*" and verify that the returned response is "0x00FFFFFF".

Step 6. Read input discrete word #5 by executing the HTS command: "*RL P1 F0074000*" and verify that the returned response is "0xFFFFFFFF".

Step 7. Read input discrete word #6 by executing the HTS command: "*RL P1 F0075000*" and verify that the returned response is "0xFFFFFFFF".

Step 8. Read input discrete word #7 by executing the HTS command: "*RL P1 F0076000*" and verify that the returned response is "0xFFFFFFFF".

Step 9. Remove the the +28 Vdc from the UUT pins.

Note: If the MTS station is used for this test, the UUT pins are connected to nets that may result in shared bits. Therefore, verify that the read back patterns are as follows:

Word #1						Word #7
FFFF1FFF	FFFFFFFF	20000005	00FFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF

4.9.8 Input Discrete Words: Pattern 8 Test

This test will verify that the interface from the UUT connector pins to the I/O FPGA Discrete In Words are functioning correctly. A pattern of complimentary alternating ones and zeros will be applied to the UUT pins which correspond to bits in Input Discrete Word #3. All seven of the Input Discrete words will then be read back and verified that they have the correct bit patterns.

Step 1. Apply +28 Vdc to UUT pin RMP-6C (Bit 1).

Step 2. Read input discrete word #1 by executing the HTS command: "*RL P1 F0070000*" and verify that the returned response is "0xFFFF1FFF".

Step 3. Read input discrete word #2 by executing the HTS command: "*RL P1 F0071000*" and verify that the returned response is "0xFFFFFFFF".

Step 4. Read input discrete word #3 by executing the HTS command: "*RL P1 F0072000*" and verify that the returned response is "0x20000002".

Step 5. Read input discrete word #4 by executing the HTS command: "*RL P1 F0073000*" and verify that the returned response is "0x00FFFFFF".

Step 6. Read input discrete word #5 by executing the HTS command: "*RL P1 F0074000*" and verify that the returned response is "0xFFFFFFFF".

Step 7. Read input discrete word #6 by executing the HTS command: "*RL P1 F0075000*" and verify that the returned response is "0xFFFFFFFF".

Step 8. Read input discrete word #7 by executing the HTS command: "*RL P1 F0076000*" and verify that the returned response is "0xFFFFFFFF".

Step 9. Remove the the +28 Vdc from the UUT pins.

Note: If the MTS station is used for this test, the UUT pins are connected to nets that may result in shared bits. Therefore, verify that the read back patterns are as follows:

Word #1						Word #7
FFFF1FFF	FFFFFFFF	20000002	00FFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF

4.9.9 Input Discrete Words: Pattern 9 Test

This test will verify that the interface from the UUT connector pins to the I/O FPGA Discrete In Words are functioning correctly. A pattern of alternating ones and zeros will be applied to the UUT pins which correspond to bits in Input Discrete Word #7. All seven of the Input Discrete words will then be read back and verified that they have the correct bit patterns. The Serial In (Internal)Test discrete will also be tested.

Step 1. Apply a ground to the following UUT pins:

Bit	UUT Pin		Bit	UUT Pin		Bit	UUT Pin		Bit	UUT Pin
31	Ser In Test Disc (Internal)		23	RMP-7E		15	RBP-5F		7	N/C
29	RMP-3D		21	RMP-14C		13	RBP-5D		5	N/C
27	RMP-6D		19	RBP-4B		11	RBP-5B		3	RBP-5K
25	RMP-13E		17	RBP-4D		9	RBP-4G		1	RBP-5H

Step 2. Execute the HTS command: "*WL P1 F00B5000 1*". This will set bit 31 (Serial Input Test Discrete) to a logic 0.

Step 3. Read input discrete word #1 by executing the HTS command: "*RL P1 F0070000*" and verify that the returned response is "0xFFFF1FFF".

Step 4. Read input discrete word #2 by executing the HTS command: "*RL P1 F0071000*" and verify that the returned response is "0xFFFFFFFF".

Step 5. Read input discrete word #3 by executing the HTS command: "*RL P1 F0072000*" and verify that the returned response is "0x20000007".

Step 6. Read input discrete word #4 by executing the HTS command: "*RL P1 F0073000*" and verify that the returned response is "0x00FFFFFF".

Step 7. Read input discrete word #5 by executing the HTS command: "*RL P1 F0074000*" and verify that the returned response is "0xFFFFFFFF".

Step 8. Read input discrete word #6 by executing the HTS command: "*RL P1 F0075000*" and verify that the returned response is "0xFFFFFFFF".

Step 9. Read input discrete word #7 by executing the HTS command: "*RL P1 F0076000*" and verify that the returned response is "0x55555F5".

Step 10. Remove the grounds from the UUT pins.

Step 11. Execute the HTS command: "*WL P1 F00B5000 0*". This will set bit 31 (Serial Input Test Discrete) to a logic 1.

Note: If the MTS station is used for this test, the UUT pins are connected to nets that may result in shared bits. Therefore, verify that the read back patterns are as follows:

Word #1						Word #7

2A941F97 E9B5ACE7 20000007 00FFFFFF FFFFFFFF FFFFFFFF 5AB2BDFA

4.9.10 Input Discrete Words: Pattern 10 Test

This test will verify that the interface from the UUT connector pins to the I/O FPGA Discrete In Words are functioning correctly. A pattern of complimentary alternating ones and zeros will be applied to the UUT pins which correspond to bits in Input Discrete Word #7. All seven of the Input Discrete words will then be read back and verified that they have the correct bit patterns. The Serial In (Internal)Test discrete will also be tested.

Step 1. Apply a ground to the following UUT pins:

Bit	UUT Pin		Bit	UUT Pin		Bit	UUT Pin		Bit	UUT Pin
30	RMP-1J		22	RMP-13G		14	RBP-5E		6	N/C
28	N/C		20	RBP-4A		12	RBP-5C		4	N/C
26	RMP-7J		18	RBP-4C		10	RBP-5A		2	RBP-5J
24	RMP-13F		16	RBP-4E		8	RBP-4F		0	RBP-5G

Step 2. Read input discrete word #1 by executing the HTS command: "*RL P1 F0070000*" and verify that the returned response is "0xFFFF1FFF".

Step 3. Read input discrete word #2 by executing the HTS command: "*RL P1 F0071000*" and verify that the returned response is "0xFFFFFFFF".

Step 4. Read input discrete word #3 by executing the HTS command: "*RL P1 F0072000*" and verify that the returned response is "0x20000007".

Step 5. Read input discrete word #4 by executing the HTS command: "*RL P1 F0073000*" and verify that the returned response is "0x00FFFFFF".

Step 6. Read input discrete word #5 by executing the HTS command: "*RL P1 F0074000*" and verify that the returned response is "0xFFFFFFFF".

Step 7. Read input discrete word #6 by executing the HTS command: "*RL P1 F0075000*" and verify that the returned response is "0xFFFFFFFF".

Step 8. Read input discrete word #7 by executing the HTS command: "*RL P1 F0076000*" and verify that the returned response is "0xBAAAAAFA".

Step 9. Remove the grounds from the UUT pins.

Note: If the MTS station is used for this test, the UUT pins are connected to nets that may result in shared bits. Therefore, verify that the read back patterns are as follows:

Word #1 Word #7

D56B136F 964A5378 20000007 00FFFFFF FFFFFFFF FFFFFFFF B54D42F5

4.9.11 Input Discretes : Data Loader Link A Test

This test in conjuction with the following test will verify that the "Data Loader Link A" and "Air/Ground" discrete input circuitry is functioning correctly. These discretes are read from CPLD Status Register #0.

Step 1. Apply a ground to the following UUT pin PDL-18

Step 2. Execute the HTS command: "*RW P1 FF800000*" and verify that the Bits of the returned result are as follows: Bit 13 = 1, Bit 12 = 0 (the rest are don't care).

Step 3. Remove the ground from the UUT PDL pin.

4.9.12 Input Discretes : Air/Ground Test

This test in conjuction with the prior test will verify that the "Data Loader Link A" and "Air/Ground" discrete input circuitry is functioning correctly. These discretes are read from CPLD Status Reg#0.

Step 1. Apply a ground to the following UUT pin RMP-5K

Step 2. Execute the HTS command: "*RW P1 FF800000*" and verify that the Bits of the returned result are as follows: Bit 13 = 0, Bit 12 = 1 (the rest are don't care).

Step 3. Remove the ground from the UUT pin.

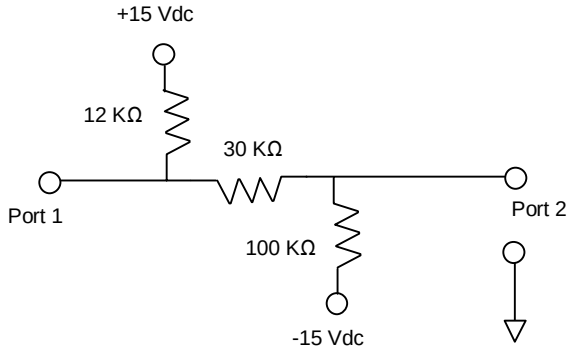
4.10 Output Discretes Tests

These tests will verify that the output discretes circuitry and corresponding discrete input wrap is functioning correctly. The front panel LEDs and Fan functionality are also verified as part of these tests.

Note: If a TCAS MTS – Part No. T336255 is being used for these tests, the UUT pin connections and associated circuitry are already available (connected) within the AIU.

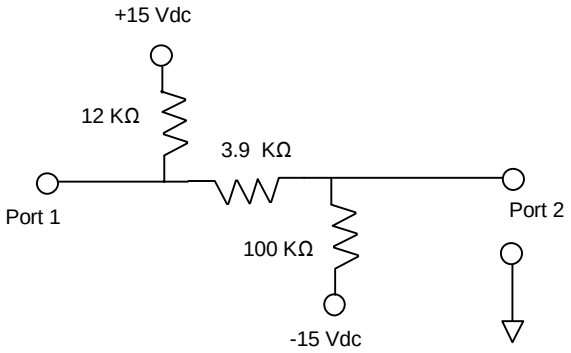
Step 1. Connect each of the following UUT pins to Port 1 of the figure shown below. Each of the UUT pins that are to be tested will be connected to it's own separate circuit.

Dout Bit	UUT Pin		Dout Bit	UUT Pin		Dout Bit	UUT Pin
0	RMP-1A		4	RMP-1E		20	RMP-3A
1	RMP-1B		5	RMP-1F		21	RMP-3B
2	RMP-1C		6	RMP-1K		22	RMP-3C
3	RMP-1D		7	RMP-2A		23	RMP-13K



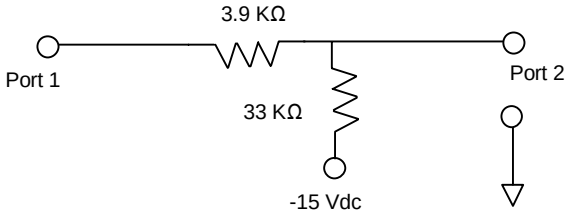
Step 2. Connect each of the following UUT pins to Port 1 of the figure shown below. Each of the UUT pins that are to be tested will be connected to it's own separate circuit.

Dout Bit	UUT Pin
8	RBP-1H
9	RBP-1J
10	RBP-1K
11	RBP-2H



Step 3. Connect each of the following UUT pins to Port 1 of the figure shown below. Each of the UUT pins that are to be tested will be connected to it's own separate circuit.

Dout Bit	UUT Pin		Dout Bit	UUT Pin
12	RBP-2J		16	RBP-3K
13	RBP-2K		17	RBP-4H
14	RBP-3H		18	RBP-4J
15	RBP-3J		19	RBP-4K



4.10.1 Output Discretes : Wrap Test

This test will walk a bit across the output discretes word Dout[0,23] while reading back all the bits via analog wrap Din Word #4 [23,0].

Step 1. Perform the following algorithm to initialize output discrete bits [0,23] to the off (logic 1) state. This will ensure that we start off with all output discrete in a known state (off).

FOR (Address = 0xF0080000) THROUGH (Address = 0xF0097000) STEP (0x1000)
{
    Execute the HTS command: "WL P1 Address 0"
}

Step 2. Perform the following algorithm to turn each output discrete on then off from lsb to msb. The bit will be turned on and then the full 24 bit word will be read back via the internal wrap (I/O FPGA input discrete word #4). Note: The read back bits are in reverse order i.e output bits [0,23] are read back via the wrap as [23,0].

***Note**:* When we turn a discrete ON, we read back a zero.

```
Bit = 0
FOR (Address = 0xF0080000) THROUGH (Address = 0xF0097000) STEP (0x1000)
{
    Execute the HTS command:   "WL P1 Address  1"
    Execute the HTS command:   "RL P1 F0073000"
    Reverse the  bit order of  'Returned Result'
    Let  X  =  ('Returned Result') BITWISE AND (0x00FFFFFF)
    Verify that X = (0x003FFFFF - 2 exp(Bit))
    Bit = Bit + 1
}
NEXT Address
Execute the HTS command:   "WL P1 Address  0"
```

***Note**:* The values that are to be verified while performing this loop are as follows:

XXFFFFFE , XXFFFFFD, XXFFFFFB, XXFFFFF7
XXFFFFEF , XXFFFFDF, XXFFFFBF, XXFFFF7F
XXFFFEFF , XXFFFDFF, XXFFFBFF, XXFFF7FF
XXFFEFFF , XXFFDFFF, XXFFBFFF, XXFF7FFF
XXFEFFFF , XXFDFFFF, XXFBFFFF, XXF7FFFF
XXEFFFFF , XXDFFFFF, XXBFFFFF, XX7FFFFF

Where X = don't care

4.10.2 Output Discretes : Pattern 1 Test

This test will verify that the output discretes circuitry is functioning correctly by reading the logic level of the loaded output. The output discretes will be driven with an alternating pattern of 1's and 0's.

***Note:** If a TCAS MTS – Part No. T336255 is being used for this test, the UUT pin connections and associated circuitry are already available (connected) within the AIU. The logic levels may then be read back via the AIU interface circuitry and an IEEE488 card.*

Step 1. If using a DMM to measure logic levels, setup the DMM to read DC volts with a range of 20 Vdc.

Step 2. Turn every other discrete on by performing the following algorithm:

```
FOR (Address = 0xF0081000) THROUGH (Address = 0xF0097000) STEP (0x2000)
{
    Execute the HTS command:   "WL P1 Address  1"
}
NEXT Address
```

Step 3. Read the voltage at Port 2 of each circuit that is connected to the UUT output discrete pins.

Step 4. Verify that the voltage at Port 2 is greater than 4.0 Vdc for each of the following UUT pins: RMP-1A, RMP-1C, RMP-1E, RMP-1K, RBP-1H, RBP-1K, RBP-2J, RBP-3H, RBP-3K, RBP-4J, RMP-3A, RMP-3C

Step 5. Verify that the voltage at Port 2 is less than 0.1 Vdc for each of the following UUT pins: RMP-1B, RMP-1D, RMP-1F, RMP-2A, RBP-1J, RBP-2H, RBP-2K, RBP-3J, RBP-4H, RBP-4K, RMP-3B, RMP-13K

Step 6. Turn the discretes off by performing the following algorithm:

FOR (Address = 0xF0081000) THROUGH (Address = 0xF0097000) STEP (0x2000)
{
Execute the HTS command: "*WL P1 Address 0*"
}
NEXT Address

Note: If the MTS is used for this test, verify that the read back data pattern is as follows:
XX555555 where X = don't care

4.10.3 Output Discretes : Pattern 2 Test

This test will verify that the output discretes circuitry is functioning correctly by measuring the logic level of the loaded output. The output discretes will be driven with a complimentary pattern of alternating 1's and 0's.

Note: If a TCAS MTS – Part No. T336255 is being used for this test, the UUT pin connections and associated circuitry are already available (connected) within the AIU. The logic levels may then be read back via the AIU interface circuitry and an IEEE488 card.

Step 1. If using a DMM to measure logic levels, setup the DMM to read DC volts with a range of 20 Vdc.

Step 2. Turn every other discrete on by performing the following algorithm:

FOR (Address = 0xF0080000) THROUGH (Address = 0xF0096000) STEP (0x2000)
{
Execute the HTS command: "*WL P1 Address 1*"
}
NEXT Address

Step 3. Measure the voltage at Port 2 of each circuit that is connected to the UUT output discrete pins.

Step 4. Verify that the voltage at Port 2 is less than 0.1 Vdc for each of the following UUT pins: RMP-1A, RMP-1C, RMP-1E, RMP-1K, RBP-1H, RBP-1K, RBP-2J, RBP-3H, RBP-3K, RBP-4J, RMP-3A, RMP-3C

Step 5. Verify that the voltage at Port 2 is greater than 4.0 Vdc for each of the following UUT pins: RMP-1B, RMP-1D, RMP-1F, RMP-2A, RBP-1J, RBP-2H, RBP-2K, RBP-3J, RBP-4H, RBP-4K, RMP-3B, RMP-13K

Step 6. Turn the discretes off by performing the following algorithm:

FOR (Address = 0xF0080000) THROUGH (Address = 0xF0096000) STEP (0x2000)
{
Execute the HTS command: "*WL P1 Address 0*"
}
NEXT Address

Note: If the MTS is used for this test, verify that the read back data pattern is as follows:
XXAAAAAA where X = don't care

4.10.4 Output Discretes : LED Sequence Test

This test will verify that the front panel LED's and associated output discretes circuitry are functioning correctly by sequencing (On/Off) through the LED's. The dual color LED will also be verified for correct color in the sequence.

Step 1. Perform the following steps and verify that all the LED's on the front panel turn ON then OFF in a counterclockwise sequence. At the "C/F LOAD STATUS" LED point of the sequence, verify that it goes through the following states before continuing to the next LED: (1) ON-Green, (2) OFF, (3) ON-RED, (4) OFF.

Step 2. TCAS PASS (ON) : Execute the HTS command: "*WL P1 F00A5000 1*"

Step 3. TCAS PASS (OFF) : Execute the HTS command: "*WL P1 F00A5000 0*"

Step 4. TCAS FAIL (ON) : Execute the HTS command: "*WL P1 F00A6000 1*"

Step 5. TCAS FAIL (OFF) : Execute the HTS command: "*WL P1 F00A6000 0*"

Step 6. TOP ANT (ON) : Execute the HTS command: "*WL P1 F00AB000 1*"

Step 7. TOP ANT (OFF) : Execute the HTS command: "*WL P1 F00AB000 0*"

Step 8. BOT ANT (ON) : Execute the HTS command: "*WL P1 F00AC000 1*"

Step 9. BOT ANT (OFF) : Execute the HTS command: "*WL P1 F00AC000 0*"

Step 10. C/F LOAD STATUS (ON-Green) : Execute the HTS command: "*WL P1 F00AD000 1*"

Step 11. C/F LOAD STATUS (OFF-Green) : Execute HTS command: "*WL P1 F00AD000 0*"

Step 12. C/F LOAD STATUS (ON-Red) : Execute the HTS command: "*WL P1 F00AE000 1*"

Step 13. C/F LOAD STATUS (OFF-Red) : Execute the HTS command: "*WL P1 F00AE000 0*"

Step 14. XFER IN PROCESS (ON) : Execute the HTS command: "*WL P1 F00AF000 1*"

Step 15. XFER IN PROCESS (OFF) : Execute the HTS command: "*WL P1 F00AF000 0*"

Step 16. XPDR BUS (ON) : Execute the HTS command: "*WL P1 F00AA000 1*"

Step 17. XPDR BUS (OFF) : Execute the HTS command: "*WL P1 F00AA000 0*"

Step 18. RAD ALT (ON) : Execute the HTS command: "*WL P1 F00A9000 1*"

Step 19. RAD ALT (OFF) : Execute the HTS command: "*WL P1 F00A9000 0*"

Step 20. RA DISP (ON) : Execute the HTS command: "*WL P1 F00A8000 1*"

Step 21. RA DISP (OFF) : Execute the HTS command: "*WL P1 F00A8000 0*"

Step 22. TA DISP (ON) : Execute the HTS command: "*WL P1 F00A7000 1*"

Step 23. TA DISP (OFF) : Execute the HTS command: "*WL P1 F00A7000 0*"

4.10.5 Output Discretes : Fan Test

This test will verify that the fan on the front panel of the 4MCU and associated output discretes circuitry is functioning correctly and that the fan is turning in the correct direction when commanded on.

Step 1. Execute the HTS command: "*WL P1 F00B7000 1*"

Step 2. Verify that the fan is turning and that it is blowing into the UUT.

4.11 ARINC 429 Tests

These tests will verify that the A429 TX/RX circuitry is functioning correctly.

4.11.1 ARINC 429 : Receiver Self Test

This test exercises the receiver and transmitter self-test function. The command transmits data on the IO FPGA ARINC test transmitter port and verifies that the ARINC receivers correctly receive the data. This test is an internal test only, no data is transmitted externally.

Step 1. Execute the HTS command: "*ART P1"*

Step 2. Verify that the returned result is "PASS"

4.11.2 ARINC 429 : Transmitter Self Test

This test excercises each of the ARINC transmitters by routing each of the transmitters to the test receiver and verifying that the data is received correctly. This test is an internal test only, no data is transmitted externally.

Step 1. Execute the HTS command: "*ATST P1*"

Step 2. Verify that the returned result is "PASS"

4.11.3 ARINC 429 : Tx14 / Rx2 Low Speed Test

This test exercises the 'CFDS A429 Output' transmitter and the 'Rsvd Perf Limit A429 Input' receiver. Data will be transmitted at low (12.5 Khz) speed and verified that it was received correctly.

Note: If a TCAS MTS – Part No. T336255 is being used for this test, the A429 transmitter / receiver connection shown in the following table is available.

Step 1. Connect the ARINC 429 Transmitter to the ARINC 429 Receiver as shown in the following table.

ARINC 429 Transmitter			**ARINC 429 Receiver**		
UUT Pin	**TCAS 3000 Signal Name**	**CCP Signal Name**	**UUT Pin**	**TCAS 3000 Signal Name**	**CCP Signal Name**
RBP-6E	CFDS A429 Output (A)	ARINC 429 Output #14 (A)	RMP-6A	Rsvd Perf Limit A429 Input (A)	ARINC 429 Input #2 (A)
RBP-6F	CFDS A429 Output (B)	ARINC 429 Output #14 (B)	RMP-6B	Rsvd Perf Limit A429 Input (B)	ARINC 429 Input #2 (B)

Step 2. Configure and enable the receiver for low speed and parity checking by executing the following HTS command: "*ARS P1 2 L G P* "

Step 3. Configure and enable the transmitter for low speed, parity generation and 4 bit time delay between words by executing the following HTS command: "*ATS P1 14 L E G R 0*"

Step 4. Transmit data by executing the following HTS commands:

"ATT P1 14 55555555"
"ATT P1 14 abcd1234"
"ATT P1 14 1234abcd"
"ATT P1 14 aaaaaaaa"

Step 5. Read the data received by Rx2 by executing the HTS command: "*ARR P1 2 4*"

Step 6. Verify that the result is equal to *"2aaaaaaa 1234abcd abcd1234 d5555555".*

4.11.4 ARINC 429 : Tx14 / Rx2 High Speed Test

This test exercises the 'CFDS A429 Output' transmitter and the 'Rsvd Perf Limit A429 Input' receiver. Data will be transmitted at high (100 Khz) speed and verified that it was received correctly.

Step 1. Configure and enable the receiver for high speed and parity checking by executing the following HTS command: "*ARS P1 2 H G P* "

Step 2. Configure and enable the transmitter for high speed, parity generation, and 4 bit time delay between words by executing the following HTS command: "*ATS P1 14 H E G R 0* "

Step 3. Transmit data by executing the following HTS commands:

"ATT P1 14 aaaaaaaa"
"ATT P1 14 1234abcd"
"ATT P1 14 abcd1234"
"ATT P1 14 55555555"

Step 4. Read the data received by Rx2 by executing the HTS command: "*ARR P1 2 4*"

Step 5. Verify that the result is equal to *"d5555555 abcd1234 1234abcd 2aaaaaaa".*

4.11.5 ARINC 429 : Tx1 / Rx3 Low Speed Test

This test exercises the 'TA/RA Display A429 Output #1' transmitter and the 'Rsvd Mag Heading/Attitude A429 Input' receiver. Data will be transmitted at low (12.5 Khz) speed and verified that it was received correctly.

Note: If a TCAS MTS – Part No. T336255 is being used for this test, the A429 transmitter / receiver connection shown in the following table is available.

Step 1. Connect the ARINC 429 Transmitter to the ARINC 429 Receiver as shown in the following table.

ARINC 429 Transmitter			**ARINC 429 Receiver**		
UUT Pin	**TCAS 3000 Signal Name**	**CCP Signal Name**	**UUT Pin**	**TCAS 3000 Signal Name**	**CCP Signal Name**
RMP-7C	TA/RA Display A429 Out #1 (A)	ARINC 429 Output #1 (A)	RMP-7A	Rsvd Mag Heading/Attitude A429 Input (A)	ARINC 429 Input #3 (A)
RMP-7D	TA/RA Display A429 Out #1 (B)	ARINC 429 Output #1 (B)	RMP-7B	Rsvd Mag Heading/Attitude A429 Input (B)	ARINC 429 Input #3 (B)

Step 2. Configure and enable the receiver for low speed and parity checking by executing the following HTS command: "*ARS P1 3 L G P* "

Step 3. Configure and enable the transmitter for low speed, parity generation, normal 4 bit time delay between words, by executing the following HTS command: "*ATS P1 1 L E G R 0*"

Step 4. Transmit data by executing the following HTS commands:

"ATT P1 1 55555555"
"ATT P1 1 abcd1234"
"ATT P1 1 1234abcd"
"ATT P1 1 aaaaaaaa"

Step 5. Read the data received by Rx3 by executing the HTS command: "*ARR P1 3 4*"

Step 6. Verify that the result is equal to *"2aaaaaaa 1234abcd abcd1234 d5555555".*

4.11.6 ARINC 429 : Tx1 / Rx3 High Speed Test

This test exercises the 'TA/RA Display A429 Output #1' transmitter and the 'Rsvd Mag Heading/Attitude A429 Input' receiver. Data will be transmitted at high (100 Khz) speed and verified that it was received correctly.

Step 1. Configure and enable the receiver for high speed and parity checking by executing the following HTS command: "*ARS P1 3 H G P* "

Step 2. Configure and enable the transmitter for high speed, parity generation, 4 bit time delay between words, by executing the following HTS command: "*ATS P1 1 H E G R 0* "

Step 3. Transmit data by executing the following HTS commands:

"ATT P1 1 aaaaaaaa"
"ATT P1 1 1234abcd"
"ATT P1 1 abcd1234"
"ATT P1 1 55555555"

Step 4. Read the data received by Rx3 by executing the HTS command: *"ARR P1 3 4"*

Step 5. Verify that the result is equal to *"d5555555 abcd1234 1234abcd 2aaaaaaa".*

4.11.7 ARINC 429 : Tx3 / Rx4 Low Speed Test

This test exercises the 'A615 Data Loader A429 Output' transmitter and the 'A615 Data Loader A429 Input' receiver. Data will be transmitted at low (12.5 Khz) speed and verified that it was received correctly.

Note: If a TCAS MTS – Part No. T336255 is being used for this test, the A429 transmitter / receiver connection shown in the following table is available.

Step 1. Connect the ARINC 429 Transmitter to the ARINC 429 Receiver as shown in the following table.

ARINC 429 Transmitter			**ARINC 429 Receiver**		
UUT Pin	**TCAS 3000 Signal Name**	**CCP Signal Name**	**UUT Pin**	**TCAS 3000 Signal Name**	**CCP Signal Name**

RMP-9A	A615 Data Ldr A429 Output (A)	ARINC 429 Output #3 (A)	RMP-8A	A615 Data Loader A429 Input (A)	ARINC 429 Input #4 (A)
RMP-9B	A615 Data Ldr A429 Output (B)	ARINC 429 Output #3 (B)	RMP-8B	A615 Data Loader A429 Input (B)	ARINC 429 Input #4 (B)

Step 2. Configure and enable the receiver for low speed and parity checking by executing the following HTS command: "*ARS P1 4 L G P* "

Step 3. Configure and enable the transmitter for low speed, parity generation, normal 4 bit time delay between words, by executing the following HTS command: "*ATS P1 3 L E G R 0*"

Step 4. Transmit data by executing the following HTS commands:

"ATT P1 3 55555555"
"ATT P1 3 abcd1234"
"ATT P1 3 1234abcd"
"ATT P1 3 aaaaaaaa"

Step 5. Read the data received by Rx4 by executing the HTS command: *"ARR P1 4 4"*

Step 6. Verify that the result is equal to *"2aaaaaaa 1234abcd abcd1234 d5555555".*

4.11.8 ARINC 429 : Tx3 / Rx4 High Speed Test

This test exercises the 'A615 Data Loader A429 Output' transmitter and the 'A615 Data Loader A429 Input' receiver. Data will be transmitted at high (100 Khz) speed and verified that it was received correctly.

Step 1. Configure and enable the receiver for high speed and parity checking by executing the following HTS command: "*ARS P1 4 H G P* "

Step 2. Configure and enable the transmitter for high speed, parity generation, 4 bit time delay between words, by executing the following HTS command: "*ATS P1 3 H E G R 0* "

Step 3. Transmit data by executing the following HTS commands:

"ATT P1 3 aaaaaaaa"
"ATT P1 3 1234abcd"
"ATT P1 3 abcd1234"
"ATT P1 3 55555555"

Step 4. Read the data received by Rx4 by executing the HTS command: *"ARR P1 4 4"*

Step 5. Verify that the result is equal to *"d5555555 abcd1234 1234abcd 2aaaaaaa".*

4.11.9 ARINC 429 : Tx1 / Rx5 Low Speed Test

This test exercises the 'TA/RA Display A429 Output #1' transmitter and the 'TA/RA Display Control A429 Input #1' receiver. Data will be transmitted at low (12.5 Khz) speed and verified that it was received correctly.

Note: If a TCAS MTS – Part No. T336255 is being used for this test, the A429 transmitter / receiver connection shown in the following table is available.

Step 1. Connect the ARINC 429 Transmitter to the ARINC 429 Receiver as shown in the following table.

ARINC 429 Transmitter			ARINC 429 Receiver		
UUT Pin	**TCAS 3000 Signal Name**	**CCP Signal Name**	**UUT Pin**	**TCAS 3000 Signal Name**	**CCP Signal Name**
PDL-33	TA/RA Display A429 Out #1 (A)	ARINC 429 Output #1 (A)	RMP-8C	TA/RA Display Ctrl A429 Input #1 (A)	ARINC 429 Input #5 (A)
PDL-34	TA/RA Display A429 Out #1 (B)	ARINC 429 Output #1 (B)	RMP-8D	TA/RA Display Ctrl A429 Input #1 (B)	ARINC 429 Input #5 (B)

Step 2. Configure and enable the receiver for low speed and parity checking by executing the following HTS command: "*ARS P1 5 L G P* "

Step 3. Configure and enable the transmitter for low speed, parity generation, normal 4 bit time delay between words, by executing the following HTS command: "*ATS P1 1 L E G R 0*"

Step 4. Transmit data by executing the following HTS commands:

"ATT P1 1 55555555"
"ATT P1 1 abcd1234"
"ATT P1 1 1234abcd"
"ATT P1 1 aaaaaaaa"

Step 5. Read the data received by Rx5 by executing the HTS command: *"ARR P1 5 4"*

Step 6. Verify that the result is equal to *"2aaaaaaa 1234abcd abcd1234 d5555555".*

4.11.10 ARINC 429 : Tx1 / Rx5 High Speed Test

This test exercises the 'TA/RA Display A429 Output #1' transmitter and the 'TA/RA Display Control A429 Input #1' receiver. Data will be transmitted at high (100 Khz) speed and verified that it was received correctly.

Step 1. Configure and enable the receiver for high speed and parity checking by executing the following HTS command: "*ARS P1 5 H G P* "

Step 2. Configure and enable the transmitter for high speed, parity generation, 4 bit time delay between words, by executing the following HTS command: "*ATS P1 1 H E G R 0* "

Step 3. Transmit data by executing the following HTS commands:

"ATT P1 1 aaaaaaaa"
"ATT P1 1 1234abcd"
"ATT P1 1 abcd1234"
"ATT P1 1 55555555"

Step 4. Read the data received by Rx5 by executing the HTS command: "*ARR P1 5 4*"

Step 5. Verify that the result is equal to *"d5555555 abcd1234 1234abcd 2aaaaaaa".*

4.11.11 ARINC 429 : Tx13 / Rx6 Low Speed Test

This test exercises the 'TX Coordination A429 Output #1' transmitter and the 'General Purpose A429 Input #1' receiver. Data will be transmitted at low (12.5 Khz) speed and verified that it was received correctly.

Note: If a TCAS MTS – Part No. T336255 is being used for this test, the A429 transmitter / receiver connection shown in the following table is available.

Step 1. Connect the ARINC 429 Transmitter to the ARINC 429 Receiver as shown in the following table.

ARINC 429 Transmitter			ARINC 429 Receiver		
UUT Pin	**TCAS 3000 Signal Name**	**CCP Signal Name**	**UUT Pin**	**TCAS 3000 Signal Name**	**CCP Signal Name**
RMP-15J	TX Coord A429 Output #1 (A)	ARINC 429 Output #13 (A)	RMP-8E	General Purpose A429 Input #1 (A)	ARINC 429 Input #6 (A)
RMP-15K	TX Coord A429 Output #1 (B)	ARINC 429 Output #13 (B)	RMP-8F	General Purpose A429 Input #1 (B)	ARINC 429 Input #6 (B)

Step 2. Configure and enable the receiver for low speed and parity checking by executing the following HTS command: "*ARS P1 6 L G P* "

Step 3. Configure and enable the transmitter for low speed, parity generation, normal 4 bit time delay between words, by executing the following HTS command: "*ATS P1 13 L E G R 0*"

Step 4. Transmit data by executing the following HTS commands:

"ATT P1 13 55555555"
"ATT P1 13 abcd1234"
"ATT P1 13 1234abcd"
"ATT P1 13 aaaaaaaa"

Step 5. Read the data received by Rx6 by executing the HTS command: *"ARR P1 6 4"*

Step 6. Verify that the result is equal to *"2aaaaaaa 1234abcd abcd1234 d5555555".*

4.11.12 ARINC 429 : Tx13 / Rx6 High Speed Test

This test exercises the 'TX Coordination A429 Output #1' transmitter and the 'General Purpose A429 Input #1' receiver. Data will be transmitted at high (100 Khz) speed and verified that it was received correctly.

Step 1. Configure and enable the receiver for high speed and parity checking by executing the following HTS command: "*ARS P1 6 H G P* "

Step 2. Configure and enable the transmitter for high speed, parity generation, 4 bit time delay between words, by executing the following HTS command: "*ATS P1 13 H E G R 0* "

Step 3. Transmit data by executing the following HTS commands:

"ATT P1 13 aaaaaaaa"
"ATT P1 13 1234abcd"
"ATT P1 13 abcd1234"
"ATT P1 13 55555555"

Step 4. Read the data received by Rx6 by executing the HTS command: *"ARR P1 6 4"*

Step 5. Verify that the result is equal to *"d5555555 abcd1234 1234abcd 2aaaaaaa".*

4.11.13 ARINC 429 : Tx11 / Rx7 Low Speed Test

This test exercises the 'TX Coordination A429 Output #2' transmitter and the 'TA/RA Display Control A429 Input #2' receiver. Data will be transmitted at low (12.5 Khz) speed and verified that it was received correctly.

Note: If a TCAS MTS – Part No. T336255 is being used for this test, the A429 transmitter / receiver connection shown in the following table is available.

Step 1. Connect the ARINC 429 Transmitter to the ARINC 429 Receiver as shown in the following table.

ARINC 429 Transmitter			ARINC 429 Receiver		
UUT Pin	**TCAS 3000 Signal Name**	**CCP Signal Name**	**UUT Pin**	**TCAS 3000 Signal Name**	**CCP Signal Name**
RMP-14A	TX Coord A429 Output #2 (A)	ARINC 429 Output #11 (A)	RMP-8G	TA/RA Disp Ctrl A429 In #2 (A)	ARINC 429 Input #7 (A)
RMP-14B	TX Coord A429 Output #2 (B)	ARINC 429 Output #11 (B)	RMP-8H	TA/RA Disp Ctrl A429 In #2 (B)	ARINC 429 Input #7 (B)

Step 2. Configure and enable the receiver for low speed and parity checking by executing the following HTS command: "*ARS P1 7 L G P* "

Step 3. Configure and enable the transmitter for low speed, parity generation, normal 4 bit time delay between words, by executing the following HTS command: *"ATS P1 11 L E G R 0"*

Step 4. Transmit data by executing the following HTS commands:

"ATT P1 11 55555555"
"ATT P1 11 abcd1234"
"ATT P1 11 1234abcd"
"ATT P1 11 aaaaaaaa"

Step 5. Read the data received by Rx7 by executing the HTS command: *"ARR P1 7 4"*

Step 6. Verify that the result is equal to *"2aaaaaaa 1234abcd abcd1234 d5555555".*

4.11.14 ARINC 429 : Tx11 / Rx7 High Speed Test

This test exercises the 'TX Coordination A429 Output #2' transmitter and the 'TA/RA Display Control A429 Input #2' receiver. Data will be transmitted at high (100 Khz) speed and verified that it was received correctly.

Step 1. Configure and enable the receiver for high speed and parity checking by executing the following HTS command: "*ARS P1 7 H G P* "

Step 2. Configure and enable the transmitter for high speed, parity generation, 4 bit time delay between words, by executing the following HTS command: "*ATS P1 11 H E G R 0* "

Step 3. Transmit data by executing the following HTS commands:

"ATT P1 11 aaaaaaaa"
"ATT P1 11 1234abcd"

"ATT P1 11 abcd1234"
"ATT P1 11 55555555"

Step 4. Read the data received by Rx7 by executing the HTS command: *"ARR P1 7 4"*

Step 5. Verify that the result is equal to *"d5555555 abcd1234 1234abcd 2aaaaaaa".*

4.11.15 ARINC 429 : Rx8 Low Speed Test

This test uses a PC based ARINC 429 card to exercise the 'General Purpose A429 Input #2' receiver. Data will be transmitted at low (12.5 Khz) speed and verified that it was received correctly.

Note: If a TCAS MTS – Part No. T336255 is being used for this test, the A429 transmitter / receiver connection shown in the following table is available via DAU #2 and the CONDOR card.

Step 1. Connect the ARINC 429 Transmitter to the ARINC 429 Receiver as shown in the following table.

ARINC 429 Transmitter	**ARINC 429 Receiver**		
PC based ARINC 429 card	**UUT Pin**	**TCAS 3000 Signal Name**	**CCP Signal Name**
A429 TX1+	RMP-8J	General Purpose A429 Input #2 (A)	ARINC 429 Input #8 (A)
A429 TX1-	RMP-8K	General Purpose A429 Input #2 (B)	ARINC 429 Input #8 (B)

Step 2. Configure and enable the receiver for low speed and parity checking by executing the following HTS command: "*ARS P1 8 L G P* "

Step 3. Configure and enable the PC based ARINC 429 card transmitter for low speed and parity generation.

Step 4. Transmit the following data words from the PC based ARINC 429 card:

"55555555", "abcd1234", "1234abcd", "aaaaaaaa"

Step 5. Read the data received by Rx8 by executing the HTS command: *"ARR P1 8 4"*

Step 6. Verify that the result is equal to *"2aaaaaaa 1234abcd abcd1234 d5555555".*

4.11.16 ARINC 429 : Rx8 High Speed Test

This test uses a PC based ARINC 429 card to exercise the 'General Purpose A429 Input #2' receiver. Data will be transmitted at high (100 Khz) speed and verified that it was received correctly.

Note: If a TCAS MTS – Part No. T336255 is being used for this test, the A429 transmitter / receiver is available via DAU #2 and the CONDOR card.

Step 1. Configure and enable the receiver for high speed and parity checking by executing the following HTS command: "*ARS P1 8 H G P* "

Step 2. Configure and enable the PC based ARINC 429 card transmitter for high speed and parity generation.

Step 3. Transmit the following data words from the PC based ARINC 429 card:

"aaaaaaaa", "1234abcd", "abcd1234", "55555555"

Step 4. Read the data received by Rx8 by executing the HTS command: *"ARR P1 8 4"*

Step 5. Verify that the result is equal to *"d5555555 abcd1234 1234abcd 2aaaaaaa".*

4.11.17 ARINC 429 : Tx9 / Rx11 Low Speed Test

This test exercises the 'RA Display A429 Output #1' transmitter and the 'Radio Altitude A429 Input #1' receiver. Data will be transmitted at low (12.5 Khz) speed and verified that it was received correctly.

Note: If a TCAS MTS – Part No. T336255 is being used for this test, the A429 transmitter / receiver connection shown in the following table is available.

Step 1. Connect the ARINC 429 Transmitter to the ARINC 429 Receiver as shown in the following table.

ARINC 429 Transmitter			**ARINC 429 Receiver**		
UUT Pin	**TCAS 3000 Signal Name**	**CCP Signal Name**	**UUT Pin**	**TCAS 3000 Signal Name**	**CCP Signal Name**
RMP-13A	RA Disp A429 Output #1 (A)	ARINC 429 Output #9 (A)	RMP-13H	Radio Altitude A429 Input #1 (A)	ARINC 429 Input #11 (A)
RMP-13B	RA Disp A429 Output #1 (B)	ARINC 429 Output #9 (B)	RMP-13J	Radio Altitude A429 Input #1 (B)	ARINC 429 Input #11 (B)

Step 2. Configure and enable the receiver for low speed and parity checking by executing the following HTS command: "*ARS P1 11 L G P* "

Step 3. Configure and enable the transmitter for low speed, parity generation, normal 4 bit time delay between words, by executing the following HTS command: "*ATS P1 9 L E G R 0*"

Step 4. Transmit data by executing the following HTS commands:

"ATT P1 9 55555555"
"ATT P1 9 abcd1234"
"ATT P1 9 1234abcd"
"ATT P1 9 aaaaaaaa"

Step 5. Read the data received by Rx11 by executing the HTS command: *"ARR P1 11 4"*

Step 6. Verify that the result is equal to *"2aaaaaaa 1234abcd abcd1234 d5555555"*.

4.11.18 ARINC 429 : Tx9 / Rx11 High Speed Test

This test exercises the 'RA Display A429 Output #1' transmitter and the 'Radio Altitude A429 Input #1' receiver. Data will be transmitted at high (100 Khz) speed and verified that it was received correctly.

Step 1. Configure and enable the receiver for high speed and parity checking by executing the following HTS command: "*ARS P1 11 H G P* "

Step 2. Configure and enable the transmitter for high speed, parity generation, 4 bit time delay between words, by executing the following HTS command: *"ATS P1 9 H E G R 0* "

Step 3. Transmit data by executing the following HTS commands:

"ATT P1 9 aaaaaaaa"
"ATT P1 9 1234abcd"
"ATT P1 9 abcd1234"
"ATT P1 9 55555555"

Step 4. Read the data received by Rx11 by executing the HTS command: *"ARR P1 11 4"*

Step 5. Verify that the result is equal to *"d5555555 abcd1234 1234abcd 2aaaaaaa".*

4.11.19 ARINC 429 : Tx2 / Rx12 Low Speed Test

This test exercises the 'TA/RA Display A429 Output #2' transmitter and the 'Selected Altitude A429 Input' receiver. Data will be transmitted at low (12.5 Khz) speed and verified that it was received correctly.

Note: If a TCAS MTS – Part No. T336255 is being used for this test, the A429 transmitter / receiver connection shown in the following table is available.

Step 1. Connect the ARINC 429 Transmitter to the ARINC 429 Receiver as shown in the following table.

ARINC 429 Transmitter			**ARINC 429 Receiver**		
UUT Pin	**TCAS 3000 Signal Name**	**CCP Signal Name**	**UUT Pin**	**TCAS 3000 Signal Name**	**CCP Signal Name**
RMP-7G	TA/RA Display A429 Out #2 (A)	ARINC 429 Output #2 (A)	RMP-14D	Selected Altitude A429 Input (A)	ARINC 429 Input #12 (A)
RMP-7H	TA/RA Display A429 Out #2 (B)	ARINC 429 Output #2 (B)	RMP-14E	Selected Altitude A429 Input (B)	ARINC 429 Input #12 (B)

Step 2. Configure and enable the receiver for low speed and parity checking by executing the following HTS command: "*ARS P1 12 L G P* "

Step 3. Configure and enable the transmitter for low speed, parity generation, normal 4 bit time delay between words, by executing the following HTS command: *"ATS P1 2 L E G R 0"*

Step 4. Transmit data by executing the following HTS commands:

"ATT P1 2 55555555"
"ATT P1 2 abcd1234"
"ATT P1 2 1234abcd"
"ATT P1 2 aaaaaaaa"

Step 5. Read the data received by Rx12 by executing the HTS command: *"ARR P1 12 4"*

Step 6. Verify that the result is equal to *"2aaaaaaa 1234abcd abcd1234 d5555555"*.

4.11.20 ARINC 429 : Tx2 / Rx12 High Speed Test

This test exercises the 'TA/RA Display A429 Output #2' transmitter and the 'Selected Altitude A429 Input' receiver. Data will be transmitted at high (100 Khz) speed and verified that it was received correctly.

Step 1. Configure and enable the receiver for high speed and parity checking by executing the following HTS command: "*ARS P1 12 H G P* "

Step 2. Configure and enable the transmitter for high speed, parity generation, 4 bit time delay between words, by executing the following HTS command: "*ATS P1 2 H E G R 0* "

Step 3. Transmit data by executing the following HTS commands:

"ATT P1 2 aaaaaaaa"
"ATT P1 2 1234abcd"
"ATT P1 2 abcd1234"
"ATT P1 2 55555555"

Step 4. Read the data received by Rx12 by executing the HTS command: *"ARR P1 12 4"*

Step 5. Verify that the result is equal to *"d5555555 abcd1234 1234abcd 2aaaaaaa".*

4.11.21 ARINC 429 : Tx13 / Rx13 Low Speed Test

This test exercises the 'TX Coordination A429 Output #1' transmitter and the 'XT Coordination A429 Input #1' receiver. Data will be transmitted at low (12.5 Khz) speed and verified that it was received correctly.

Note: If a TCAS MTS – Part No. T336255 is being used for this test, the A429 transmitter / receiver connection shown in the following table is available.

Step 1. Connect the ARINC 429 Transmitter to the ARINC 429 Receiver as shown in the following table.

ARINC 429 Transmitter			**ARINC 429 Receiver**		
UUT Pin	**TCAS 3000 Signal Name**	**CCP Signal Name**	**UUT Pin**	**TCAS 3000 Signal Name**	**CCP Signal Name**
RMP-15J	TX Coord A429 Output #1 (A)	ARINC 429 Output #13 (A)	RMP-14F	XT Coord A429 Input #1 (A)	ARINC 429 Input #13 (A)
RMP-15K	TX Coord A429 Output #1 (B)	ARINC 429 Output #13 (B)	RMP-14G	XT Coord A429 Input #1 (B)	ARINC 429 Input #13 (B)

Step 2. Configure and enable the receiver for low speed and parity checking by executing the following HTS command: "*ARS P1 13 L G P* "

Step 3. Configure and enable the transmitter for low speed, parity generation, normal 4 bit time delay between words, by executing the following HTS command: *"ATS P1 13 L E G R 0"*

Step 4. Transmit data by executing the following HTS commands:

"ATT P1 13 55555555"
"ATT P1 13 abcd1234"

"ATT P1 13 1234abcd"
"ATT P1 13 aaaaaaaa"

Step 5. Read the data received by Rx13 by executing the HTS command: *"ARR P1 13 4"*

Step 6. Verify that the result is equal to *"2aaaaaaa 1234abcd abcd1234 d5555555"*.

4.11.22 ARINC 429 : Tx13 / Rx13 High Speed Test

This test exercises the 'TX Coordination A429 Output #1' transmitter and the 'XT Coordination A429 Input #1' receiver. Data will be transmitted at high (100 Khz) speed and verified that it was received correctly.

Step 1. Configure and enable the receiver for high speed and parity checking by executing the following HTS command: "*ARS P1 13 H G P* "

Step 2. Configure and enable the transmitter for high speed, parity generation, 4 bit time delay between words, by executing the following HTS command: "*ATS P1 13 H E G R 0* "

Step 3. Transmit data by executing the following HTS commands:

"ATT P1 13 aaaaaaaa"
"ATT P1 13 1234abcd"
"ATT P1 13 abcd1234"
"ATT P1 13 55555555"

Step 4. Read the data received by Rx13 by executing the HTS command: *"ARR P1 13 4"*

Step 5. Verify that the result is equal to *"d5555555 abcd1234 1234abcd 2aaaaaaa"*.

4.11.23 ARINC 429 : Tx11 / Rx14 Low Speed Test

This test exercises the 'TX Coordination A429 Output #2' transmitter and the 'XT Coordination A429 Input #2' receiver. Data will be transmitted at low (12.5 Khz) speed and verified that it was received correctly.

Note: If a TCAS MTS – Part No. T336255 is being used for this test, the A429 transmitter / receiver connection shown in the following table is available.

Step 1. Connect the ARINC 429 Transmitter to the ARINC 429 Receiver as shown in the following table.

ARINC 429 Transmitter			**ARINC 429 Receiver**		
UUT Pin	**TCAS 3000 Signal Name**	**CCP Signal Name**	**UUT Pin**	**TCAS 3000 Signal Name**	**CCP Signal Name**
RMP-14A	TX Coord A429 Output #2 (A)	ARINC 429 Output #11 (A)	RMP-14H	XT Coord A429 Input #2 (A)	ARINC 429 Input #14 (A)
RMP-14B	TX Coord A429 Output #2 (B)	ARINC 429 Output #11 (B)	RMP-14J	XT Coord A429 Input #2 (B)	ARINC 429 Input #14 (B)

Step 2. Configure and enable the receiver for low speed and parity checking by executing the following HTS command: "*ARS P1 14 L G P* "

Step 3. Configure and enable the transmitter for low speed, parity generation, normal 4 bit time delay between words, by executing the following HTS command: *"ATS P1 11 L E G R 0"*

Step 4. Transmit data by executing the following HTS commands:

"ATT P1 11 55555555"
"ATT P1 11 abcd1234"
"ATT P1 11 1234abcd"
"ATT P1 11 aaaaaaaa"

Step 5. Read the data received by Rx14 by executing the HTS command: *"ARR P1 14 4"*

Step 6. Verify that the result is equal to *"2aaaaaaa 1234abcd abcd1234 d5555555"*.

4.11.24 ARINC 429 : Tx11 / Rx14 High Speed Test

This test exercises the 'TX Coordination A429 Output #2' transmitter and the 'XT Coordination A429 Input #2' receiver. Data will be transmitted at high (100 Khz) speed and verified that it was received correctly.

Step 1. Configure and enable the receiver for high speed and parity checking by executing the following HTS command: "*ARS P1 14 H G P* "

Step 2. Configure and enable the transmitter for high speed, parity generation, 4 bit time delay between words, by executing the following HTS command: *"ATS P1 11 H E G R 0"*

Step 3. Transmit data by executing the following HTS commands:

"ATT P1 11 aaaaaaaa"
"ATT P1 11 1234abcd"
"ATT P1 11 abcd1234"
"ATT P1 11 55555555"

Step 4. Read the data received by Rx14 by executing the HTS command: *"ARR P1 14 4"*

Step 5. Verify that the result is equal to *"d5555555 abcd1234 1234abcd 2aaaaaaa".*

4.11.25 ARINC 429 : Tx10 / Rx17 Low Speed Test

This test exercises the 'RA Display A429 Output #2' transmitter and the 'Radio Altitude A429 Input #2' receiver. Data will be transmitted at low (12.5 Khz) speed and verified that it was received correctly.

Note: If a TCAS MTS – Part No. T336255 is being used for this test, the A429 transmitter / receiver connection shown in the following table is available.

Step 1. Connect the ARINC 429 Transmitter to the ARINC 429 Receiver as shown in the following table.

ARINC 429 Transmitter			**ARINC 429 Receiver**		
UUT Pin	**TCAS 3000 Signal Name**	**CCP Signal Name**	**UUT Pin**	**TCAS 3000 Signal Name**	**CCP Signal Name**
RMP-13C	RA Display A429 Output #2 (A)	ARINC 429 Output #10 (A)	RBP-3D	Radio Altitude A429 Input #2 (A)	ARINC 429 Input #17 (A)

RMP-13D	RA Display A429 Output #2 (B)	ARINC 429 Output #10 (B)	RBP-3E	Radio Altitude A429 Input #2 (B)	ARINC 429 Input #17 (B)

Step 2. Configure and enable the receiver for low speed and parity checking by executing the following HTS command: "*ARS P1 17 L G P* "

Step 3. Configure and enable the transmitter for low speed, parity generation, normal 4 bit time delay between words, by executing the following HTS command: *"ATS P1 10 L E G R 0"*

Step 4. Transmit data by executing the following HTS commands:

"ATT P1 10 55555555"
"ATT P1 10 abcd1234"
"ATT P1 10 1234abcd"
"ATT P1 10 aaaaaaaa"

Step 5. Read the data received by Rx17 by executing the HTS command: *"ARR P1 17 4"*

Step 6. Verify that the result is equal to *"2aaaaaaa 1234abcd abcd1234 d5555555"*.

4.11.26 ARINC 429 : Tx10 / Rx17 High Speed Test

This test exercises the 'RA Display A429 Output #2' transmitter and the 'Radio Altitude A429 Input #2' receiver. Data will be transmitted at high (100 Khz) speed and verified that it was received correctly.

Step 1. Configure and enable the receiver for high speed and parity checking by executing the following HTS command: "*ARS P1 17 H G P* "

Step 2. Configure and enable the transmitter for high speed, parity generation, 4 bit time delay between words, by executing the following HTS command: *"ATS P1 10 H E G R 0"*

Step 3. Transmit data by executing the following HTS commands:

"ATT P1 10 aaaaaaaa"
"ATT P1 10 1234abcd"
"ATT P1 10 abcd1234"
"ATT P1 10 55555555"

Step 4. Read the data received by Rx17 by executing the HTS command: *"ARR P1 17 4"*

Step 5. Verify that the result is equal to *"d5555555 abcd1234 1234abcd 2aaaaaaa".*

4.11.27 ARINC 429 : Tx14 / Rx18 Low Speed Test

This test exercises the 'CFDS A429 Output' transmitter and the 'CFDS A429 Input' receiver. Data will be transmitted at low (12.5 Khz) speed and verified that it was received correctly.

Note: If a TCAS MTS – Part No. T336255 is being used for this test, the A429 transmitter / receiver connection shown in the following table is available.

Step 1. Connect the ARINC 429 Transmitter to the ARINC 429 Receiver as shown in the following table.

ARINC 429 Transmitter			ARINC 429 Receiver		
UUT Pin	**TCAS 3000 Signal Name**	**CCP Signal Name**	**UUT Pin**	**TCAS 3000 Signal Name**	**CCP Signal Name**
RBP-6E	CFDS A429 Output (A)	ARINC 429 Output #14 (A)	RBP-6G	CFDS A429 Input (A)	ARINC 429 Input #18 (A)
RBP-6F	CFDS A429 Output (B)	ARINC 429 Output #14 (B)	RBP-6H	CFDS A429 Input (B)	ARINC 429 Input #18 (B)

Step 2. Configure and enable the receiver for low speed and parity checking by executing the following HTS command: "*ARS P1 18 L G P* "

Step 3. Configure and enable the transmitter for low speed, parity generation, normal 4 bit time delay between words, by executing the following HTS command: *"ATS P1 14 L E G R 0"*

Step 4. Transmit data by executing the following HTS commands:

"ATT P1 14 55555555"
"ATT P1 14 abcd1234"
"ATT P1 14 1234abcd"
"ATT P1 14 aaaaaaaa"

Step 5. Read the data received by Rx18 by executing the HTS command: *"ARR P1 18 4"*

Step 6. Verify that the result is equal to *"2aaaaaaa 1234abcd abcd1234 d5555555"*.

4.11.28 ARINC 429 : Tx14 / Rx18 High Speed Test

This test exercises the 'CFDS A429 Output' transmitter and the 'CFDS A429 Input' receiver. Data will be transmitted at high (100 Khz) speed and verified that it was received correctly.

Step 1. Configure and enable the receiver for high speed and parity checking by executing the following HTS command: "*ARS P1 18 H G P* "

Step 2. Configure and enable the transmitter for high speed, parity generation, 4 bit time delay between words, by executing the following HTS command: *"ATS P1 14 H E G R 0"*

Step 3. Transmit data by executing the following HTS commands:

"ATT P1 14 aaaaaaaa"
"ATT P1 14 1234abcd"
"ATT P1 14 abcd1234"
"ATT P1 14 55555555"

Step 4. Read the data received by Rx18 by executing the HTS command: *"ARR P1 18 4"*

Step 5. Verify that the result is equal to *"d5555555 abcd1234 1234abcd 2aaaaaaa"*.

4.11.29 ARINC 429 : Rx19 Low Speed Test

This test uses a PC based ARINC 429 card to exercise the 'A615 Data Loader A429 Input' receiver. Data will be transmitted at low (12.5 Khz) speed and verified that it was received correctly.

Note: If a TCAS MTS – Part No. T336255 is being used for this test, the A429 transmitter / receiver connection shown in the following table is available.

Step 1. Connect the ARINC 429 Transmitter to the ARINC 429 Receiver as shown in the following table.

ARINC 429 Transmitter	ARINC 429 Receiver		
PC based ARINC 429 card	**UUT Pin**	**TCAS 3000 Signal Name**	**CCP Signal Name**
TX0_429A	PDL-1	A615 Data Loader A429 Input (A)	ARINC 429 Input #19 (A)
TX0_429A	PDL-2	A615 Data Loader A429 Input (B)	ARINC 429 Input #19 (A)

Step 2. Configure and enable the receiver for low speed and parity checking by executing the following HTS command: "*ARS P1 19 L G P* "

Step 3. Configure and enable the PC based ARINC 429 card transmitter for low speed and parity generation.

Step 4. Transmit the following data words from the PC based ARINC 429 card:

"55555555", "abcd1234", "1234abcd", "aaaaaaaa"

Step 5. Read the data received by Rx19 by executing the HTS command: *"ARR P1 19 4"*

Step 6. Verify that the result is equal to *"2aaaaaaa 1234abcd abcd1234 d5555555"*.

4.11.30 ARINC 429 : Rx19 High Speed Test

This test uses a PC based ARINC 429 card to exercise the 'A615 Data Loader A429 Input' receiver. Data will be transmitted at High (100 Khz) speed and verified that it was received correctly.

Note: If a TCAS MTS – Part No. T336255 is being used for this test, the A429 transmitter / receiver connection is available.

Step 1. Configure and enable the receiver for high speed and parity checking by executing the following HTS command: "*ARS P1 19 H G P* "

Step 2. Configure and enable the PC based ARINC 429 card transmitter for high speed and parity generation.

Step 3. Transmit the following data words from the PC based ARINC 429 card:

"aaaaaaaa", "1234abcd", "abcd1234", "55555555"

Step 4. Read the data received by Rx19 by executing the HTS command: *"ARR P1 19 4"*

Step 5. Verify that the result is equal to *"d5555555 abcd1234 1234abcd 2aaaaaaa".*

4.11.31 ARINC 429 : Tx3 Low Speed Test

This test uses a PC based ARINC 429 card to receive data from the 'A615 Data Loader A429 Output' transmitter. Data will be transmitted at low (12.5 Khz) speed and verified that it was received correctly.

Note: If a TCAS MTS – Part No. T336255 is being used for this test, the A429 transmitter / receiver connection shown in the following table is available.

Step 1. Connect the ARINC 429 Transmitter to the ARINC 429 Receiver as shown in the following table.

ARINC 429 Transmitter			ARINC 429 Receiver
UUT Pin	**TCAS 3000 Signal Name**	**CCP Signal Name**	**PC based ARINC 429 card**
PDL-8	A615 Data Loader A429 Output (A)	ARINC 429 Output #3 (A)	RX0_429A
PDL-9	A615 Data Loader A429 Output (B)	ARINC 429 Output #3 (B)	RX0_429B

Step 2. Configure and enable the PC based ARINC 429 receiver for low speed data.

Step 3. Configure and enable the transmitter for high speed, parity generation, 4 bit time delay between words, by executing the following HTS command: "*ATS P1 3 H E G R 0* "

Step 4. Transmit data by executing the following HTS commands:

"ATT P1 3 55555555"
"ATT P1 3 abcd1234"
"ATT P1 3 1234abcd"
"ATT P1 3 aaaaaaaa"

Step 5. Read the data received by the PC based ARINC 429 receiver and verify that it is equal to *"2aaaaaaa 1234abcd abcd1234 d5555555"*.

4.11.32 ARINC 429 : Tx3 High Speed Test

This test uses a PC based ARINC 429 card to receive data from the 'A615 Data Loader A429 Output' transmitter. Data will be transmitted at high (100 Khz) speed and verified that it was received correctly.

Note: If a TCAS MTS – Part No. T336255 is being used for this test, the A429 transmitter / receiver connection is available.

Step 1. Configure and enable the PC based ARINC 429 receiver for high speed data.

Step 2. Configure and enable the transmitter for high speed, parity generation, 4 bit time delay between words, by executing the following HTS command: "*ATS P1 3 H E G R 0* "

Step 3. Transmit data by executing the following HTS commands:

"ATT P1 3 aaaaaaaa"
"ATT P1 3 1234abcd"
"ATT P1 3 abcd1234"
"ATT P1 3 55555555"

Step 4. Read the data received by the PC based ARINC 429 receiver and verify that it is equal to *"d5555555 abcd1234 1234abcd 2aaaaaaa".*

4.12 RF FPGA Wrap And Suppression Pulse Tests

4.12.1 RF FPGA Digital Wrap 1 MODE S Pattern Test

This test will verify the digital functionality of the RF FPGA using a MODE S pattern test and priority 1 reply queue.

Step 1. Execute the following HTS command: "*RFWRAP P1 1 0*" and verify that the result is *"0000"*

4.12.2 RF FPGA Digital Wrap 1 MODE S Confidence Test

This test will verify the digital functionality of the RF FPGA using a MODE S confidence test and priority 1 reply queue.

Step 1. Execute the following HTS command: "RFWRAP P1 1 1" and verify that the result is "0000"

4.12.3 RF FPGA Digital Wrap 1 MODE S Fruit Test

This test will verify the digital functionality of the RF FPGA using a MODE S Fruit test and priority 1 reply queue.

Step 1. Execute the following HTS command: "*RFWRAP P1 1 2*" and verify that the result is *"0000"*

4.12.4 RF FPGA Digital Wrap 1 ATCRBS Pattern Test

This test will verify the digital functionality of the RF FPGA using a ATCRBS pattern test and priority 1 reply queue.

Step 1. Execute the following HTS command: "RFWRAP P1 1 3" and verify that the result is "0000"

4.12.5 RF FPGA Digital Wrap 2 MODE S Pattern Test

This test will verify the digital functionality of the RF FPGA using a MODE S pattern test and priority 2 reply queue.

Step 1. Execute the following HTS command: "*RFWRAP P1 2 0*" and verify that the result is *"0000"*

4.12.6 RF FPGA Digital Wrap 2 MODE S Confidence Test

This test will verify the digital functionality of the RF FPGA using a MODE S confidence test and priority 2 reply queue.

Step 1. Execute the following HTS command: "*RFWRAP P1 2 1*" and verify that the result is "0000"

4.12.7 RF FPGA Digital Wrap 2 MODE S Fruit Test

This test will verify the digital functionality of the RF FPGA using a MODE S Fruit test and priority 2 reply queue.

Step 1. Execute the following HTS command: "*RFWRAP P1 2 2*" and verify that the result is *"0000"*

4.12.8 RF FPGA Digital Wrap 2 ATCRBS Pattern Test

This test will verify the digital functionality of the RF FPGA using a ATCRBS pattern test and priority 2 reply queue.

Step 1. Execute the following HTS command: "*RFWRAP P1 2 3*" and verify that the result is "0000"

4.12.9 RF FPGA Self Test With Suppression Disabled Test

This test will perform a MODE-S RF wrap test using the Self Test Oscillator and Suppression disabled. The intent of this test is to verify that replies are received by the receiver.

Step 1. Execute the following HTS command: "*RFWRAP P1 1 4*" and verify that the received replies identifier, 'R', in the returned result string is as follows: R ≥ 8

4.12.10 RF FPGA Self Test With Suppression Enabled Test

This test will perform a MODE-S RF wrap test using the Self Test Oscillator and Suppression enabled. The intent of this test is to verify that replies are not received by the receiver.

Step 1. Execute the following HTS command: "*RFWRAP P1 1 4 S*" and verify that the received replies identifier, 'R', in the returned result string is as follows: R = 0

4.12.11 RF FPGA Suppression Pulse Width Test

This test will perform a MODE-S RF wrap test using the Self Test Oscillator and Suppression enabled. The intent of this test is to verify that the pulse width of the suppression pulse is within specifications.

Step 1. Setup the oscilloscope function of the Peak Power meter for measuring a 28V pulse of 130 µs duration.

Step 2. Using a x10 probe, connect the oscilloscope channel 3 to the AIU J6 (SUPPRESSION A)[P1C-12] connector.

Step 3. Execute the following HTS command: "*RFWRAP P1 1 4 S*" and verify that the suppression pulse width on P1C-12 is 128 ± 3 µs

4.12.12 RF FPGA Suppression Pulse Amplitude Test

This test will perform a MODE-S RF wrap test using the Self Test Oscillator and Suppression enabled. The intent of this test is to verify that the amplitude of the suppression pulse is within specifications.

Step 1. Setup the oscilloscope function of the Peak Power meter for measuring a 28V pulse of 130 µs duration.

Step 2. Using a x10 probe, connect the oscilloscope channel 3 to the AIU J7 (SUPPRESSION B)[P1C-13] connector.

Step 3. Execute the following HTS command: "*RFWRAP P1 1 4 S*" and verify that the suppression pulse amplitude on P1C-13 is 28 ± 4.5 Vdc

4.13 RF Receiver Tests

The following tests use replies injected into various antenna ports of the UUT to verify receiver characteristics and reply processing capability.

NOTE: *The actual output of the signal generator must be adjusted to account for the losses between the signal generator port and the unit antenna port.*

4.13.1 ATCRBS: Rejection 1090 MHz (Top Ant: 0/90 @ –81/–81 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 0 and Top 90 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –81.0 dBm will be applied at the UUT Top 0/90 antenna ports. The signal applied to the antenna ports will be 2 dB below the lowest acceptable MTL amplitude.

Step 4. Setup the MTS RFIU so that the RF level into the Top 90 antenna port is equal to the RF level into the Top 0 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 10 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≥ 9	-	-	-	-	-
OPR LIM	≥ 9	-	-	-	-	-

4.13.2 ATCRBS: MTL 1090 MHz (Top Ant: 0/90 @ –75/–78 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 0 and Top 90 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –75.0 dBm will be applied at the UUT Top 0 antenna port. The signal applied to the Top 0 antenna port will be equal to the largest acceptable MTL amplitude.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 90 antenna port to be 3 dB less than the signal on the Top 0 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 100 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≤ 10	-	-	1	1	-
OPR LIM	≤ 10	-	-	1	1	-

4.13.3 ATCRBS: MTL 1087 MHz (Top Ant: 0/90 @ –75/–78 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 0 and Top 90 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1087.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –75.0 dBm will be applied at the UUT Top 0 antenna port. The signal applied to the Top 0 antenna port will be equal to the largest acceptable MTL amplitude.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 90 antenna port to be 3 dB less than the signal on the Top 0 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 100 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≤ 10	-	-	1	1	-
OPR LIM	≤ 10	-	-	1	1	-

4.13.4 ATCRBS: MTL 1093 MHz (Top Ant: 0/90 @ –75/–78 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 0 and Top 90 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1093.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –75.0 dBm will be applied to the UUT Top 0 antenna port. The signal applied to the Top 0 antenna port will be equal to the largest acceptable MTL amplitude.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 90 antenna port to be 3 dB less than the signal on the Top 0 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 100 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≤ 10	-	-	1	1	-
OPR LIM	≤ 10	-	-	1	1	-

4.13.5 ATCRBS: 1090 MHz (Top Ant: 0/90 @ –72/–75 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 0 and Top 90 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –72.0 dBm will be applied to the UUT Top 0 antenna port. The signal applied to the Top 0 antenna port will be 3 dB higher than the largest acceptable MTL amplitude.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 90 antenna port to be 3 dB less than the signal on the Top 0 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 100 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≤ 1	-72.0 ± 2.5 dBm	3.0 ± 2.3 dBm	1	1	-
OPR LIM	≤ 1	-72.0 ± 3.0 dBm	3.0 ± 2.3 dBm	1	1	-

4.13.6 ATCRBS: 1090 MHz (Top Ant: 0/90 @ –60/–66 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 0 and Top 90 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –60.0 dBm will be applied to the UUT Top 0 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 90 antenna port to be 6 dB less than the signal on the Top 0 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 100 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≤ 1	-60.0 ± 2.0 dBm	6.0 ± 2.3 dBm	1	1	0
OPR LIM	≤ 1	-60.0 ± 2.5 dBm	6.0 ± 2.3 dBm	1	1	0

4.13.7 MODE-S: Pattern 1 (Top Ant: 0/90 @ –48/–57 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with a data pattern to simulate a Mode S data string. The data pattern will be a short message (56 bits) set to 80000000018567.

Step 2. Select the Top 0 and Top 90 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –48.0 dBm will be applied to the UUT Top 0 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 90 antenna port to be 9 dB less than the signal on the Top 0 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 379A0000*".

Step 9. Initiate the generation of 10 MODE-S replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	0	-48.0 ± 2.0 dBm	9.0 ± 2.3 dBm	1	1	0

OPR LIM	0	-48.0 ± 2.5 dBm	9.0 ± 2.3 dBm	1	1	0

4.13.8 MODE-S: Pattern 2 (Bot Ant: 0/90 @ –36/–48 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with a data pattern to simulate a Mode S data string. The data pattern will be a short message (56 bits) set to 55555555AA51C4.

Step 2. Select the Bottom 0 and Bottom 90 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –36.0 dBm will be applied to the UUT Bottom 0 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Bottom 90 antenna port to be 12 dB less than the signal on the Bottom 0 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 379A0000*".

Step 9. Initiate the generation of 10 MODE-S replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	0	-36.0 ± 2.0 dBm	12.0 ± 2.3 dBm	1	1	0
OPR LIM	0	-36.0 ± 2.5 dBm	12.0 ± 2.3 dBm	1	1	0

4.13.9 MODE-S: Pattern 3 (Bot Ant: 0/90 –24/–25 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with a data pattern to simulate a Mode S data string. The data pattern will be a short message (56 bits) set to AAAAAAAAAB5781.

Step 2. Select the Bottom 0 and Bottom 90 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –24.0 dBm will be applied to the UUT Bottom 0 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Bottom 90 antenna port to be 1 dB less than the signal on the Bottom 0 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 379B0000*".

Step 9. Initiate the generation of 10 MODE-S replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	0	-24.0 ± 2.0 dBm	1.0 ± 2.3 dBm	1	1	-
OPR LIM	0	-24.0 ± 2.5 dBm	1.0 ± 2.3 dBm	1	1	-

4.13.10 RCVR Self-Test 0/90 Rcvrs Test

This test verifies the RF wrap capability of the UUT. This is a self-test that is "wrapped" through the RF with the self test oscillator enabled. No externally injected replies are used. For this test, the 0 and 90 degree receivers are enabled. The self-test CV limits are read from memory for this test .

Step 1. Obtain the computed Self test Low Limit by executing the following macro instruction: **LL = GetSelfTestLimit (LowLimit)**. See Appendix D for description of this macro instruction.

Step 2. Obtain the computed Self test High Limit by executing the following macro instruction: **HL = GetSelfTestLimit (HighLimit)**. See Appendix D for description of this macro instruction.

Step 3. Set the UUT to generate RF Mode S wraparound replies without the suppression bus activated during the self-test reply by executing the following HTS command: "RFWRAP P1 1 4".

Step 4. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	0	LL ≤ CV ≤ HL	0 ± 3 dBm	1	1	-
OPR LIM	0	LL ≤ CV ≤ HL	0 ± 3 dBm	1	1	-

4.13.11 ATCRBS: 0 Rcvr 1065 MHz Out Of Band Reject (0/90 @ –17/–29 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 0 and Top 90 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1065.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –17.0 dBm will be applied to the UUT Top 0 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 90 antenna port to be 12 dB less than the signal on the Top 0 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 10 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	**≥** 5	-	-	-	-	-
OPR LIM	**≥** 1	-	-	-	-	-

4.13.12 ATCRBS: 0 Rcvr 1115 MHz Out Of Band Reject (0/90 @ –17/–29 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 0 and Top 90 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1115.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –17.0 dBm will be applied to the UUT Top 0 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 90 antenna port to be 12 dB less than the signal on the Top 0 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 10 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≥ 5	-	-	-	-	-
OPR LIM	≥ 1	-	-	-	-	-

4.13.13 MODE-S: Ext Range MTL 1090 Mhz (Bot Ant: 0/90 @ –81/–87 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with a data pattern to simulate a Mode S data string. The data pattern will be a short message (56 bits) set to 55555555AA51C4.

Step 2. Select the Bottom 0 and Bottom 90 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –81.0 dBm will be applied to the UUT Bottom 0 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Bottom 90 antenna port to be 6 dB less than the signal on the Bottom 0 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Initialize the RF FPGA Squitter Listening Noise/Slope Setup Register by executing the following HTS command: "*WL P1 88002004 17061200* ".

Step 9. Start squitter listening by executing the following HTS command: "*WL P1 88002000 14FB0000*".

Step 10. Initiate the generation of 50 MODE-S replies from the MTS.

Step 11. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 12. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 13. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≤ 5	-	-	-	-	-
OPR LIM	≤ 5	-	-	-	-	-

4.13.14 ATCRBS: Rejection 1090 MHz (Top Ant: 90/180 @ –81/–81 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 90 and Top 180 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –81.0 dBm will be applied at the UUT Top 90/180 antenna ports. The signal applied to the antenna ports will be 2 dB below the lowest acceptable MTL amplitude.

Step 4. Setup the MTS RFIU so that the RF level into the Top 180 antenna port is equal to the RF level into the Top 90 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 10 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	**≥** 9	-	-	-	-	-
OPR LIM	**≥** 9	-	-	-	-	-

4.13.15 ATCRBS: MTL 1090 MHz (Top Ant: 90/180 @ –75/–78 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 90 and Top 180 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –75.0 dBm will be applied at the UUT Top 90 antenna port. The signal applied to the Top 90 antenna port will be equal to the largest acceptable MTL amplitude.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 180 antenna port to be 3 dB less than the signal on the Top 90 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 100 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≤ 10	-	-	0	1	-
OPR LIM	≤ 10	-	-	0	1	-

4.13.16 ATCRBS: MTL 1087 MHz (Top Ant: 90/180 @ –75/–78 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 90 and Top 180 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1087.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –75.0 dBm will be applied at the UUT Top 90 antenna port. The signal applied to the Top 90 antenna port will be equal to the largest acceptable MTL amplitude.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 180 antenna port to be 3 dB less than the signal on the Top 90 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 100 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≤ 10	-	-	0	1	-
OPR LIM	≤ 10	-	-	0	1	-

4.13.17 ATCRBS: MTL 1093 MHz (Top Ant: 90/180 @ –75/–78 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 90 and Top 180 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1093.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –75.0 dBm will be applied to the UUT Top 90 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 180 antenna port to be 3 dB less than the signal on the Top 90 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 100 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≤ 10	-	-	0	1	-
OPR LIM	≤ 10	-	-	0	1	-

4.13.18 ATCRBS: 1090 MHz (Top Ant: 90/180 @ –72/–75 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 90 and Top 180 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –72.0 dBm will be applied to the UUT Top 90 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 180 antenna port to be 3 dB less than the signal on the Top 90 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 100 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≤ 1	-72.0 ± 2.5 dBm	3.0 ± 2.3 dBm	0	1	-
OPR LIM	≤ 1	-72.0 ± 3.0 dBm	3.0 ± 2.3 dBm	0	1	-

4.13.19 ATCRBS: 1090 MHz (Top Ant: 90/180 @ –60/–66 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 90 and Top 180 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –60.0 dBm will be applied to the UUT Top 90 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 180 antenna port to be 6 dB less than the signal on the Top 90 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 100 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≤ 1	-60.0 ± 2.0 dBm	6.0 ± 2.3 dBm	0	1	1
OPR LIM	≤ 1	-60.0 ± 2.5 dBm	6.0 ± 2.3 dBm	0	1	1

4.13.20 MODE-S: Pattern 1 (Top Ant: 90/180 @ –48/–57 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with a data pattern to simulate a Mode S data string. The data pattern will be a short message (56 bits) set to 80000000018567.

Step 2. Select the Top 90 and Top 180 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –48.0 dBm will be applied to the UUT Top 90 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 180 antenna port to be 9 dB less than the signal on the Top 90 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 379A0000*".

Step 9. Initiate the generation of 10 MODE-S replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	0	-48.0 ± 2.0 dBm	9.0 ± 2.3 dBm	0	1	1
OPR LIM	0	-48.0 ± 2.5 dBm	9.0 ± 2.3 dBm	0	1	1

4.13.21 MODE-S: Pattern 2 (Bot Ant: 90/180 @ –36/–48 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with a data pattern to simulate a Mode S data string. The data pattern will be a short message (56 bits) set to 55555555AA51C4.

Step 2. Select the Bottom 90 and Bottom 180 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –36.0 dBm will be applied to the UUT Bottom 90 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Bottom 180 antenna port to be 12 dB less than the signal on the Bottom 90 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 379A0000*".

Step 9. Initiate the generation of 10 MODE-S replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	0	-36.0 ± 2.0 dBm	12.0 ± 2.3 dBm	0	1	1
OPR LIM	0	-36.0 ± 2.5 dBm	12.0 ± 2.3 dBm	0	1	1

4.13.22 MODE-S: Pattern 3 (Bot Ant: 90/180 @ –24/–25 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with a data pattern to simulate a Mode S data string. The pattern will be a short message (56 bits) set to AAAAAAAAAB5781.

Step 2. Select the Bottom 90 and Bottom 180 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –24.0 dBm will be applied to the UUT Bottom 90 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Bottom 180 antenna port to be 1 dB less than the signal on the Bottom 90 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 379B0000*".

Step 9. Initiate the generation of 10 MODE-S replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	0	-24.0 ± 2.0 dBm	1.0 ± 2.3 dBm	0	1	-
OPR LIM	0	-24.0 ± 2.5 dBm	1.0 ± 2.3 dBm	0	1	-

4.13.23 RCVR Self-Test 90/180 Rcvrs Test

This test verifies the RF wrap capability of the UUT. This is a self-test that is "wrapped" through the RF with the self test oscillator enabled. For this test, the 90 and 180 degree receivers are enabled. The self-test CV limits are read from memory for this test

Step 1. Obtain the computed Self test Low Limit by executing the following macro instruction: **LL = GetSelfTestLimit (LowLimit)**. See Appendix D for description of this macro instruction.

Step 2. Obtain the computed Self test High Limit by executing the following macro instruction: **HL = GetSelfTestLimit (HighLimit)**. See Appendix D for description of this macro instruction.

Step 3. Set the UUT to generate RF Mode S wraparound replies without the suppression bus activated during the self-test reply by executing the following HTS command: "*RFWRAP P1 1 5*".

Step 4. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	0	LL ≤ CV ≤ HL	0 ± 3 dBm	0	1	-
OPR LIM	0	LL ≤ CV ≤ HL	0 ± 3 dBm	0	1	-

4.13.24 ATCRBS: 90 Rcvr 1065 MHz Out Of Band Reject (90/180 @ –17/–29 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 90 and Top 180 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1065.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –17.0 dBm will be applied to the UUT Top 90 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 180 antenna port to be 12 dB less than the signal on the Top 90 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 10 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S

MFG LIM	≥ 5	-	-	-	-	-
OPR LIM	≥ 1	-	-	-	-	-

4.13.25 ATCRBS: 90 Rcvr 1115 MHz Out Of Band Reject (90/180 @ –17/–29 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 90 and Top 180 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1115.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –17.0 dBm will be applied to the UUT Top 90 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 180 antenna port to be 12 dB less than the signal on the Top 90 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 10 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≥ 5	-	-	-	-	-
OPR LIM	≥ 1	-	-	-	-	-

4.13.26 MODE-S: Ext Range MTL 1090 Mhz (Bot Ant: 90/180 @ –81/–87 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with a data pattern to simulate a Mode S data string. The data pattern will be a short message (56 bits) set to 55555555AA51C4.

Step 2. Select the Bottom 90 and Bottom 180 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –81.0 dBm will be applied to the UUT Bottom 90 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Bottom 180 antenna port to be 6 dB less than the signal on the Bottom 90 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Initialize the RF FPGA Squitter Listening Noise/Slope Setup Register by executing the following HTS command: "*WL P1 88002004 17061200* ".

Step 9. Start squitter listening by executing the following HTS command: "*WL P1 88002000 14FB0000*".

Step 10. Initiate the generation of 50 MODE-S replies from the MTS.

Step 11. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 12. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 13. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≤ 5	-	-	-	-	-
OPR LIM	≤ 5	-	-	-	-	-

4.13.27 ATCRBS: Rejection 1090 MHz (Top Ant: 180/270 @ –81/–81 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 180 and Top 270 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –81.0 dBm will be applied at the UUT Top 180/270 antenna ports. The signal applied to the antenna ports will be 2 dB below the lowest acceptable MTL amplitude.

Step 4. Setup the MTS RFIU so that the RF level into the Top 270 antenna port is equal to the RF level into the Top 180 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 10 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≥ 9	-	-	-	-	-
OPR LIM	≥ 9	-	-	-	-	-

4.13.28 ATCRBS: MTL 1090 MHz (Top Ant: 180/270 @ –75/–78 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 180 and Top 270 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –75.0 dBm will be applied at the UUT Top 180 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 270 antenna port to be 3 dB less than the signal on the Top 180 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 100 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≤ 10	-	-	0	0	-
OPR LIM	≤ 10	-	-	0	0	-

4.13.29 ATCRBS: MTL 1087 MHz (Top Ant: 180/270 @ –75/–78 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 180 and Top 270 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1087.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –75.0 dBm will be applied at the UUT Top 180 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 270 antenna port to be 3 dB less than the signal on the Top 180 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 100 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≤ 10	-	-	0	0	-
OPR LIM	≤ 10	-	-	0	0	-

4.13.30 ATCRBS: MTL 1093 MHz (Top Ant: 180/270 @ –75/–78 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 180 and Top 270 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1093.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –75.0 dBm will be applied to the UUT Top 180 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 270 antenna port to be 3 dB less than the signal on the Top 180 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 100 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≤ 10	-	-	0	0	-
OPR LIM	≤ 10	-	-	0	0	-

4.13.31 ATCRBS: 1090 MHz (Top Ant: 180/270 @ –72/–75 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 180 and Top 270 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –72.0 dBm will be applied to the UUT Top 180 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 270 antenna port to be 3 dB less than the signal on the Top 180 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 100 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≤ 1	-72.0 ± 2.5 dBm	3.0 ± 2.3 dBm	0	0	-
OPR LIM	≤ 1	-72.0 ± 3.0 dBm	3.0 ± 2.3 dBm	0	0	-

4.13.32 ATCRBS: 1090 MHz (Top Ant: 180/270 @ –60/–66 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 180 and Top 270 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –60.0 dBm will be applied to the UUT Top 180 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 270 antenna port to be 6 dB less than the signal on the Top 180 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 100 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≤ 1	-60.0 ± 2.0 dBm	6.0 ± 2.3 dBm	0	0	0
OPR LIM	≤ 1	-60.0 ± 2.5 dBm	6.0 ± 2.3 dBm	0	0	0

4.13.33 MODE-S: Pattern 1 (Top Ant: 180/270 @ –48/–57 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with a data pattern to simulate a Mode S data string. The data pattern will be a short message (56 bits) set to 80000000018567.

Step 2. Select the Top 180 and Top 270 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –48.0 dBm will be applied to the UUT Top 180 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 270 antenna port to be 9 dB less than the signal on the Top 180 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 379A0000*".

Step 9. Initiate the generation of 10 MODE-S replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	0	-48.0 ± 2.0 dBm	9.0 ± 2.3 dBm	0	0	0
OPR LIM	0	-48.0 ± 2.5 dBm	9.0 ± 2.3 dBm	0	0	0

4.13.34 MODE-S: Pattern 2 (Bot Ant: 180/270 @ –36/–48 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with a data pattern to simulate a Mode S data string. The data pattern will be a short message (56 bits) set to 55555555AA51C4.

Step 2. Select the Bottom 180 and Bottom 270 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –36.0 dBm will be applied to the UUT Bottom 180 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Bottom 270 antenna port to be 12 dB less than the signal on the Bottom 180 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 379A0000*".

Step 9. Initiate the generation of 10 MODE-S replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	0	-36.0 ± 2.0 dBm	12.0 ± 2.3 dBm	0	0	0
OPR LIM	0	-36.0 ± 2.5 dBm	12.0 ± 2.3 dBm	0	0	0

4.13.35 MODE-S: Pattern 3 (Bot Ant: 180/270 @ –24/–25 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with a data pattern to simulate a Mode S data string. The pattern will be a short message (56 bits) set to AAAAAAAAAB5781.

Step 2. Select the Bottom 180 and Bottom 270 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –24.0 dBm will be applied to the UUT Bottom 180 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Bottom 270 antenna port to be 1 dB less than the signal on the Bottom 180 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 379B0000*".

Step 9. Initiate the generation of 10 MODE-S replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	0	-24.0 ± 2.0 dBm	1.0 ± 2.3 dBm	0	0	-
OPR LIM	0	-24.0 ± 2.5 dBm	1.0 ± 2.3 dBm	0	0	-

4.13.36 RCVR Self-Test 180/270 Rcvrs Test

This test verifies the RF wrap capability of the UUT. This is a self-test that is "wrapped" through the RF with the self test oscillator enabled. No externally injected replies are used. For this test, the 180 and 270 degree receivers are enabled. The self-test CV limits are read from memory for this test

Step 1. Obtain the computed Self test Low Limit by executing the following macro instruction: **LL = GetSelfTestLimit (LowLimit)**. See Appendix D for description of this macro instruction.

Step 2. Obtain the computed Self test High Limit by executing the following macro instruction: **HL = GetSelfTestLimit (HighLimit)**. See Appendix D for description of this macro instruction.

Step 3. Set the UUT to generate RF Mode S wraparound replies without the suppression bus activated during the self-test reply by executing the following HTS command: "*RFWRAP P1 1 6*".

Step 4. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	0	LL ≤ CV ≤ HL	0 ± 3 dBm	0	0	-
OPR LIM	0	LL ≤ CV ≤ HL	0 ± 3 dBm	0	0	-

4.13.37 ATCRBS: 180 Rcvr 1065 MHz Out Of Band Reject (180/270 @ –17/–29 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 180 and Top 270 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1065.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –17.0 dBm will be applied to the UUT Top 180 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 270 antenna port to be 12 dB less than the signal on the Top 180 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 10 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≥ 5	-	-	-	-	-
OPR LIM	≥ 1	-	-	-	-	-

4.13.38 ATCRBS: 180 Rcvr 1115 MHz Out Of Band Reject (180/270 @ –17/–29 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 180 and Top 270 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1115.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –17.0 dBm will be applied to the UUT Top 180 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 270 antenna port to be 12 dB less than the signal on the Top 180 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 10 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≥ 5	-	-	-	-	-
OPR LIM	≥ 1	-	-	-	-	-

4.13.39 MODE-S: Ext Range MTL 1090 Mhz (Bot Ant: 180/270 @ –81/–87 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with a data pattern to simulate a Mode S data string. The data pattern will be a short message (56 bits) set to 55555555AA51C4.

Step 2. Select the Bottom 180 and Bottom 270 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –81.0 dBm will be applied to the UUT Bottom 180 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Bottom 270 antenna port to be 6 dB less than the signal on the Bottom 180 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Initialize the RF FPGA Squitter Listening Noise/Slope Setup Register by executing the following HTS command: "*WL P1 88002004 17061200* ".

Step 9. Start squitter listening by executing the following HTS command: "*WL P1 88002000 14FB0000*".

Step 10. Initiate the generation of 50 MODE-S replies from the MTS.

Step 11. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 12. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 13. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≤ 5	-	-	-	-	-

OPR LIM	≤ 5	-	-	-	-	-

4.13.40 ATCRBS: Rejection 1090 MHz (Top Ant: 270/0 @ –81/–81 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 270 and Top 0 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –81.0 dBm will be applied at the UUT Top 270/0 antenna ports. The signal applied to the antenna ports will be 2 dB below the lowest acceptable MTL amplitude.

Step 4. Setup the MTS RFIU so that the RF level into the Top 0 antenna port is equal to the RF level into the Top 270 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 10 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≥ 9	-	-	-	-	-
OPR LIM	≥ 9	-	-	-	-	-

4.13.41 ATCRBS: MTL 1090 MHz (Top Ant: 270/0 @ –75/–78 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 270 and Top 0 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –75.0 dBm will be applied at the UUT Top 270 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 0 antenna port to be 3 dB less than the signal on the Top 270 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 100 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≤ 10	-	-	1	0	-
OPR LIM	≤ 10	-	-	1	0	-

4.13.42 ATCRBS: MTL 1087 MHz (Top Ant: 270/0 @ –75/–78 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 270 and Top 0 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1087.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –75.0 dBm will be applied at the UUT Top 270 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 0 antenna port to be 3 dB less than the signal on the Top 270 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 100 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≤ 10	-	-	1	0	-
OPR LIM	≤ 10	-	-	1	0	-

4.13.43 ATCRBS: MTL 1093 MHz (Top Ant: 270/0 @ –75/–78 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 270 and Top 0 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1093.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –75.0 dBm will be applied to the UUT Top 270 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 0 antenna port to be 3 dB less than the signal on the Top 270 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 100 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≤ 10	-	-	1	0	-
OPR LIM	≤ 10	-	-	1	0	-

4.13.44 ATCRBS: 1090 MHz (Top Ant: 270/0 @ –72/–75 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 270 and Top 0 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –72.0 dBm will be applied to the UUT Top 270 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 0 antenna port to be 3 dB less than the signal on the Top 270 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 100 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≤ 1	-72.0 ± 2.5 dBm	3.0 ± 2.3 dBm	1	0	-
OPR LIM	≤ 1	-72.0 ± 3.0 dBm	3.0 ± 2.3 dBm	1	0	-

4.13.45 ATCRBS: 1090 MHz (Top Ant: 270/0 @ –60/–66 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 270 and Top 0 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –60.0 dBm will be applied to the UUT Top 270 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 0 antenna port to be 6 dB less than the signal on the Top 270 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 100 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≤ 1	-60.0 ± 2.0 dBm	6.0 ± 2.3 dBm	1	0	1
OPR LIM	≤ 1	-60.0 ± 2.5 dBm	6.0 ± 2.3 dBm	1	0	1

4.13.46 MODE-S: Pattern 1 (Top Ant: 270/0 @ –48/–57 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with a data pattern to simulate a Mode S data string. The data pattern will be a short message (56 bits) set to 80000000018567.

Step 2. Select the Top 270 and Top 0 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –48.0 dBm will be applied to the UUT Top 270 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 0 antenna port to be 9 dB less than the signal on the Top 270 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 379A0000*".

Step 9. Initiate the generation of 10 MODE-S replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	0	-48.0 ± 2.0 dBm	9.0 ± 2.3 dBm	1	0	1
OPR LIM	0	-48.0 ± 2.5 dBm	9.0 ± 2.3 dBm	1	0	1

4.13.47 MODE-S: Pattern 2 (Bot Ant: 270/0 @ –36/–48 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with a data pattern to simulate a Mode S data string. The data pattern will be a short message (56 bits) set to 55555555AA51C4.

Step 2. Select the Bottom 270 and Bottom 0 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –36.0 dBm will be applied to the UUT Bottom 270 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Bottom 0 antenna port to be 12 dB less than the signal on the Bottom 270 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 379A0000*".

Step 9. Initiate the generation of 10 MODE-S replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	0	-36.0 ± 2.0 dBm	12.0 ± 2.3 dBm	1	0	1
OPR LIM	0	-36.0 ± 2.5 dBm	12.0 ± 2.3 dBm	1	0	1

4.13.48 MODE-S: Pattern 3 (Bot Ant: 270/0 @ –24/–25 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with a data pattern to simulate a Mode S data string. The pattern will be a short message (56 bits) set to AAAAAAAAAB5781.

Step 2. Select the Bottom 270 and Bottom 0 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –24.0 dBm will be applied to the UUT Bottom 270 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Bottom 0 antenna port to be 1 dB less than the signal on the Bottom 270 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 379B0000*".

Step 9. Initiate the generation of 10 MODE-S replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	0	-24.0 ± 2.0 dBm	1.0 ± 2.3 dBm	1	0	-
OPR LIM	0	-24.0 ± 2.5 dBm	1.0 ± 2.3 dBm	1	0	-

4.13.49 RCVR Self-Test 270/0 Rcvrs Test

This test verifies the RF wrap capability of the UUT. This is a self-test that is "wrapped" through the RF with the self test oscillator enabled. No externally injected replies are used. For this test, the 270 and 0 degree receivers are enabled. The self-test CV limits are read from memory for this test

Step 1. Obtain the computed Self test Low Limit by executing the following macro instruction: **LL = GetSelfTestLimit (LowLimit)**. See Appendix D for description of this macro instruction.

Step 2. Obtain the computed Self test High Limit by executing the following macro instruction: **HL = GetSelfTestLimit (HighLimit)**. See Appendix D for description of this macro instruction.

Step 3. Set the UUT to generate RF Mode S wraparound replies without the suppression bus activated during the self-test reply by executing the following HTS command: "*RFWRAP P1 1 7*".

Step 4. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	0	LL ≤ CV ≤ HL	0 ± 3 dBm	1	0	-
OPR LIM	0	LL ≤ CV ≤ HL	0 ± 3 dBm	1	0	-

4.13.50 ATCRBS: 270 Rcvr 1065 MHz Out Of Band Reject (270/0 @ –17/–29 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 270 and Top 0 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1065.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –17.0 dBm will be applied to the UUT Top 270 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 0 antenna port to be 12 dB less than the signal on the Top 270 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 10 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≥ 5	-	-	-	-	-
OPR LIM	≥ 1	-	-	-	-	-

4.13.51 ATCRBS: 270 Rcvr 1115 MHz Out Of Band Reject (270/0 @ –17/–29 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with the data patterns required to simulate an ATCRBS data string of F1, A1, A2, A3, B1, B2, B3, and F2 pulses with pulse widths of 500 ± 50 ns. All pulses will be present during each transmission.

Step 2. Select the Top 270 and Top 0 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1115.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –17.0 dBm will be applied to the UUT Top 270 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Top 0 antenna port to be 12 dB less than the signal on the Top 270 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Start squitter listening by executing the following HTS command: "*WL P1 88002000 37800000*".

Step 9. Initiate the generation of 10 ATCRBS replies from the MTS.

Step 10. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 11. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 12. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≥ 5	-	-	-	-	-
OPR LIM	≥ 1	-	-	-	-	-

4.13.52 MODE-S: Ext Range MTL 1090 Mhz (Bot Ant: 270/0 @ –81/–87 dBm) Test

Step 1. Setup the MTS RFIU to load it's FIFO with a data pattern to simulate a Mode S data string. The data pattern will be a short message (56 bits) set to 55555555AA51C4.

Step 2. Select the Bottom 270 and Bottom 0 ports on the MTS RFIU. Replies will be injected into the UUT from these ports simultaneously.

Step 3. Setup the MTS RF signal generator for a frequency of 1090.0 ± 0.1 Mhz and an RF level which should include compensation for any path losses such that –81.0 dBm will be applied to the UUT Bottom 270 antenna port.

Step 4. Set the MTS RFIU to select an attenuation which causes the signal on the Bottom 0 antenna port to be 6 dB less than the signal on the Bottom 270 antenna port.

Step 5. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 6. Initialize the Squitter Listening Queue to zeros by executing the following HTS command: "*FDB P1 003e0000 003e0c7c 00*".

Step 7. Initialize the RF FPGA Squitter Listening Queue Start Address Register by executing the following HTS command: "*WL P1 88002008 803E0000*".

Step 8. Initialize the RF FPGA Squitter Listening Noise/Slope Setup Register by executing the following HTS command: "*WL P1 88002004 17061200* ".

Step 9. Start squitter listening by executing the following HTS command: "*WL P1 88002000 14FB0000*".

Step 10. Initiate the generation of 50 MODE-S replies from the MTS.

Step 11. Stop squitter listening by executing the following HTS command: "*WL P1 88002000 00000000*".

Step 12. Read the UUT squitter reply queue by executing the following HTS command: "*RBL P1 3E0000 3E0C7C".*

Step 13. Verify the following:

	Missed Replies	Total Avg CV	Total Avg PD	Z	N	S
MFG LIM	≤ 5	-	-	-	-	-
OPR LIM	≤ 5	-	-	-	-	-

4.14 RF Xmtr: P2A Whisper/Shout Steps & Rise/Fall Time Tests

These tests cause the UUT to generate six-pulse MODE C ATCRBS interrogations out the Top 0 antenna port. Whisper Shout step size measurements shall be made by comparing the P2A pulse amplitudes of the appropriate interrogations. The six-pulse interrogation may be repeated at a maximum rate of once every 2 ms for averaging. Refer to Figures 1 and 3 for these tests.

Note: When making measurements, the losses from the antenna port to the peak power meter must be calibrated into the reading.

4.14.1 0 dB Whisper/Shout P2A Pulse Peak Power Test

This test verifies that the peak power of the P2A pulse when invoking the 0 dB Whisper/Shout attenuation level is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 500) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse.

Step 6. Verify that the resulting measurement is as follows:

MFG LIM	+53.33 dBm ≤ measurement ≤ +58.5 dBm
OPR LIM	+53.33 dBm ≤ measurement ≤ +58.5 dBm

4.14.2 0 dB Whisper/Shout P2A Pulse Rise Time Test

This test verifies that the rise time of the P2A pulse when invoking the 0 dB Whisper/Shout attenuation level is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making appropriate P2A rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P2A pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse.

Step 6. Verify that the resulting measurement is as follows:

MFG LIM	50 ns ≤ P2A rise time ≤ 100 ns
OPR LIM	50 ns ≤ P2A rise time ≤ 100 ns

4.14.3 0 dB Whisper/Shout P2A Pulse Fall Time Test

This test verifies that the fall time of the P2A pulse when invoking the 0 dB Whisper/Shout attenuation level is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making appropriate P2A fall time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the fall time of the P2A pulse. The measurement should be made between the 90% to 10% voltage points of the falling edge of the pulse.

Step 6. Verify that the resulting measurement is as follows:

MFG LIM	40 ns ≤ P2A fall time ≤ 175 ns
OPR LIM	40 ns ≤ P2A fall time ≤ 200 ns

4.14.4 1 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 0 dB and 1 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 0 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (01, 1, 01, 1, 01, 1, 01, 1, 01, 1, 01, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**0 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB
OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.5 1 dB Whisper/Shout P2A Pulse Rise Time Test

This test verifies that the rise time of the P2A pulse when invoking the 1 dB Whisper/Shout attenuation level is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making appropriate P2A rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (01, 1, 01, 1, 01, 1, 01, 1, 01, 1, 01, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P2A pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse.

Step 6. Verify that the resulting measurement is as follows:

MFG LIM	50 ns ≤ P2A rise time ≤ 100 ns
OPR LIM	50 ns ≤ P2A rise time ≤ 100 ns

4.14.6 1 dB Whisper/Shout P2A Pulse Fall Time Test

This test verifies that the fall time of the P2A pulse when invoking the 1 dB Whisper/Shout attenuation level is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making appropriate P2A fall time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (01, 1, 01, 1, 01, 1, 01, 1, 01, 1, 01, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the fall time of the P2A pulse. The measurement should be made between the 90% to 10% voltage points of the falling edge of the pulse.

Step 6. Verify that the resulting measurement is as follows:

MFG LIM	40 ns ≤ P2A fall time ≤ 175 ns
OPR LIM	40 ns ≤ P2A fall time ≤ 200 ns

4.14.7 2 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 1 dB and 2 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 1 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (02, 1, 02, 1, 02, 1, 02, 1, 02, 1, 02, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**1 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB
OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.8 2 dB Whisper/Shout P2A Pulse Rise Time Test

This test verifies that the rise time of the P2A pulse when invoking the 2 dB Whisper/Shout attenuation level is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making appropriate P2A rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (02, 1, 02, 1, 02, 1, 02, 1, 02, 1, 02, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P2A pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse.

Step 6. Verify that the resulting measurement is as follows:

MFG LIM	50 ns ≤ P2A rise time ≤ 100 ns
OPR LIM	50 ns ≤ P2A rise time ≤ 100 ns

4.14.9 3 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 2 dB and 3 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 2 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (02, 1, 02, 1, 02, 1, 02, 1, 02, 1, 02, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**2 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB

OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.10 3 dB Whisper/Shout P2A Pulse Rise Time Test

This test verifies that the rise time of the P2A pulse when invoking the 3 dB Whisper/Shout attenuation level is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making appropriate P2A rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (03, 1, 03, 1, 03, 1, 03, 1, 03, 1, 03, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P2A pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse.

Step 6. Verify that the resulting measurement is as follows:

MFG LIM	50 ns ≤ P2A rise time ≤ 100 ns
OPR LIM	50 ns ≤ P2A rise time ≤ 100 ns

4.14.11 4 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 3 dB and 4 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 3 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)

InitAtcTxWrds7Thru10 (04, 1, 04, 1, 04, 1, 04, 1, 04, 1, 04, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**3 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB
OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.12 4 dB Whisper/Shout P2A Pulse Rise Time Test

This test verifies that the rise time of the P2A pulse when invoking the 4 dB Whisper/Shout attenuation level is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making appropriate P2A rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (04, 1, 04, 1, 04, 1, 04, 1, 04, 1, 04, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P2A pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse.

Step 6. Verify that the resulting measurement is as follows:

MFG LIM	50 ns ≤ P2A rise time ≤ 100 ns
OPR LIM	50 ns ≤ P2A rise time ≤ 100 ns

4.14.13 5 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 4 dB and 5 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 4 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (05, 1, 05, 1, 05, 1, 05, 1, 05, 1, 05, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**4 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB
OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.14 5 dB Whisper/Shout P2A Pulse Rise Time Test

This test verifies that the rise time of the P2A pulse when invoking the 5 dB Whisper/Shout attenuation level is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making appropriate P2A rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (05, 1, 05, 1, 05, 1, 05, 1, 05, 1, 05, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P2A pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse.

Step 6. Verify that the resulting measurement is as follows:

MFG LIM	50 ns ≤ P2A rise time ≤ 100 ns
OPR LIM	50 ns ≤ P2A rise time ≤ 100 ns

4.14.15 6 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 5 dB and 6 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 5 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (06, 1, 06, 1, 06, 1, 06, 1, 06, 1, 06, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**5 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB
OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.16 6 dB Whisper/Shout P2A Pulse Rise Time Test

This test verifies that the rise time of the P2A pulse when invoking the 6 dB Whisper/Shout attenuation level is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making appropriate P2A rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (06, 1, 06, 1, 06, 1, 06, 1, 06, 1, 06, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P2A pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse.

Step 6. Verify that the resulting measurement is as follows:

MFG LIM	50 ns ≤ P2A rise time ≤ 100 ns
OPR LIM	50 ns ≤ P2A rise time ≤ 100 ns

4.14.17 7 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 6 dB and 7 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 6 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (07, 1, 07, 1, 07, 1, 07, 1, 07, 1, 07, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**6 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB
OPR LIM	0.500 dB ≤ result ≤ 1.500 dB

PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.18 7 dB Whisper/Shout P2A Pulse Rise Time Test

This test verifies that the rise time of the P2A pulse when invoking the 7 dB Whisper/Shout attenuation level is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making appropriate P2A rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (07, 1, 07, 1, 07, 1, 07, 1, 07, 1, 07, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1* ***n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P2A pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse.

Step 6. Verify that the resulting measurement is as follows:

MFG LIM	50 ns ≤ P2A rise time ≤ 100 ns
OPR LIM	50 ns ≤ P2A rise time ≤ 100 ns

4.14.19 8 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 7 dB and 8 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 7 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (08, 1, 08, 1, 08, 1, 08, 1, 08, 1, 08, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**7 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB
OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.20 8 dB Whisper/Shout P2A Pulse Rise Time Test

This test verifies that the rise time of the P2A pulse when invoking the 8 dB Whisper/Shout attenuation level is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making appropriate P2A rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (08, 1, 08, 1, 08, 1, 08, 1, 08, 1, 08, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P2A pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse.

Step 6. Verify that the resulting measurement is as follows:

MFG LIM	50 ns ≤ P2A rise time ≤ 100 ns
OPR LIM	50 ns ≤ P2A rise time ≤ 100 ns

4.14.21 9 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 8 dB and 9 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 8 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (09, 1, 09, 1, 09, 1, 09, 1, 09, 1, 09, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**8 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB
OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.22 9 dB Whisper/Shout P2A Pulse Rise Time Test

This test verifies that the rise time of the P2A pulse when invoking the 9 dB Whisper/Shout attenuation level is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making appropriate P2A rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (09, 1, 09, 1, 09, 1, 09, 1, 09, 1, 09, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P2A pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse.

Step 6. Verify that the resulting measurement is as follows:

MFG LIM	50 ns ≤ P2A rise time ≤ 100 ns
OPR LIM	50 ns ≤ P2A rise time ≤ 100 ns

4.14.23 10 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 9 dB and 10 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 9 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (0A, 1, 0A, 1, 0A, 1, 0A, 1, 0A, 1, 0A, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**9 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB
OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.24 10 dB Whisper/Shout P2A Pulse Rise Time Test

This test verifies that the rise time of the P2A pulse when invoking the 10 dB Whisper/Shout attenuation level is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making appropriate P2A rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (0A, 1, 0A, 1, 0A, 1, 0A, 1, 0A, 1, 0A, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1* ***n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P2A pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse.

Step 6. Verify that the resulting measurement is as follows:

MFG LIM	50 ns ≤ P2A rise time ≤ 100 ns
OPR LIM	50 ns ≤ P2A rise time ≤ 100 ns

4.14.25 11 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 10 dB and 11 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 10 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (0B, 1, 0B, 1, 0B, 1, 0B, 1, 0B, 1, 0B, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1* ***n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**10 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB
OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.26 11 dB Whisper/Shout P2A Pulse Rise Time Test

This test verifies that the rise time of the P2A pulse when invoking the 11 dB Whisper/Shout attenuation level is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making appropriate P2A rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (0B, 1, 0B, 1, 0B, 1, 0B, 1, 0B, 1, 0B, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P2A pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse.

Step 6. Verify that the resulting measurement is as follows:

MFG LIM	50 ns ≤ P2A rise time ≤ 100 ns
OPR LIM	50 ns ≤ P2A rise time ≤ 100 ns

4.14.27 12 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 11 dB and 12 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 11 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (0C, 1, 0C, 1, 0C, 1, 0C, 1, 0C, 1, 0C, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**11 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB
OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.28 12 dB Whisper/Shout P2A Pulse Rise Time Test

This test verifies that the rise time of the P2A pulse when invoking the 12 dB Whisper/Shout attenuation level is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making appropriate P2A rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (0C, 1, 0C, 1, 0C, 1, 0C, 1, 0C, 1, 0C, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P2A pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse.

Step 6. Verify that the resulting measurement is as follows:

MFG LIM	50 ns ≤ P2A rise time ≤ 100 ns
OPR LIM	50 ns ≤ P2A rise time ≤ 100 ns

4.14.29 13 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 12 dB and 13 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 12 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (0D, 1, 0D, 1, 0D, 1, 0D, 1, 0D, 1, 0D, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**12 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB
OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.30 13 dB Whisper/Shout P2A Pulse Rise Time Test

This test verifies that the rise time of the P2A pulse when invoking the 13 dB Whisper/Shout attenuation level is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making appropriate P2A rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (0D, 1, 0D, 1, 0D, 1, 0D, 1, 0D, 1, 0D, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P2A pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse.

Step 6. Verify that the resulting measurement is as follows:

MFG LIM	50 ns ≤ P2A rise time ≤ 100 ns
OPR LIM	50 ns ≤ P2A rise time ≤ 100 ns

4.14.31 14 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 13 dB and 14 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 13 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (0E, 1, 0E, 1, 0E, 1, 0E, 1, 0E, 1, 0E, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**13 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB
OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.32 14 dB Whisper/Shout P2A Pulse Rise Time Test

This test verifies that the rise time of the P2A pulse when invoking the 14 dB Whisper/Shout attenuation level is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making appropriate P2A rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (0E, 1, 0E, 1, 0E, 1, 0E, 1, 0E, 1, 0E, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P2A pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse.

Step 6. Verify that the resulting measurement is as follows:

MFG LIM	50 ns ≤ P2A rise time ≤ 100 ns
OPR LIM	50 ns ≤ P2A rise time ≤ 100 ns

4.14.33 15 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 14 dB and 15 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 14 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (0F, 1, 0F, 1, 0F, 1, 0F, 1, 0F, 1, 0F, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**14 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB
OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.34 15 dB Whisper/Shout P2A Pulse Rise Time Test

This test verifies that the rise time of the P2A pulse when invoking the 15 dB Whisper/Shout attenuation level is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making appropriate P2A rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (0F, 1, 0F, 1, 0F, 1, 0F, 1, 0F, 1, 0F, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P2A pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse.

Step 6. Verify that the resulting measurement is as follows:

MFG LIM	50 ns ≤ P2A rise time ≤ 100 ns
OPR LIM	50 ns ≤ P2A rise time ≤ 100 ns

4.14.35 16 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 15 dB and 16 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 15 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (10, 1, 10, 1, 10, 1, 10, 1, 10, 1, 10, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**15 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB

OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.36 16 dB Whisper/Shout P2A Pulse Rise Time Test

This test verifies that the rise time of the P2A pulse when invoking the 16 dB Whisper/Shout attenuation level is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making appropriate P2A rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (10, 1, 10, 1, 10, 1, 10, 1, 10, 1, 10, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P2A pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse.

Step 6. Verify that the resulting measurement is as follows:

MFG LIM	50 ns ≤ P2A rise time ≤ 100 ns
OPR LIM	50 ns ≤ P2A rise time ≤ 100 ns

4.14.37 17 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 16 dB and 17 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 16 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)

InitAtcTxWrds7Thru10 (11, 1, 11, 1, 11, 1, 11, 1, 11, 1, 11, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1* ***n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**16 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB
OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.38 17 dB Whisper/Shout P2A Pulse Rise Time Test

This test verifies that the rise time of the P2A pulse when invoking the 17 dB Whisper/Shout attenuation level is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making appropriate P2A rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (11, 1, 11, 1, 11, 1, 11, 1, 11, 1, 11, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1* ***n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P2A pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse.

Step 6. Verify that the resulting measurement is as follows:

MFG LIM	50 ns ≤ P2A rise time ≤ 100 ns
OPR LIM	50 ns ≤ P2A rise time ≤ 100 ns

4.14.39 18 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 17 dB and 18 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 17 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (12, 1, 12, 1, 12, 1, 12, 1, 12, 1, 12, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1* ***n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**17 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB
OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.40 18 dB Whisper/Shout P2A Pulse Rise Time Test

This test verifies that the rise time of the P2A pulse when invoking the 18 dB Whisper/Shout attenuation level is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making appropriate P2A rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (12, 1, 12, 1, 12, 1, 12, 1, 12, 1, 12, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1* ***n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P2A pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse.

Step 6. Verify that the resulting measurement is as follows:

MFG LIM	50 ns ≤ P2A rise time ≤ 100 ns
OPR LIM	50 ns ≤ P2A rise time ≤ 100 ns

4.14.41 19 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 18 dB and 19 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 18 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (13, 1, 13, 1, 13, 1, 13, 1, 13, 1, 13, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**18 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB
OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.42 19 dB Whisper/Shout P2A Pulse Rise Time Test

This test verifies that the rise time of the P2A pulse when invoking the 19 dB Whisper/Shout attenuation level is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making appropriate P2A rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (13, 1, 13, 1, 13, 1, 13, 1, 13, 1, 13, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P2A pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse.

Step 6. Verify that the resulting measurement is as follows:

MFG LIM	50 ns ≤ P2A rise time ≤ 100 ns
OPR LIM	50 ns ≤ P2A rise time ≤ 100 ns

4.14.43 20 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 19 dB and 20 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 19 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (14, 1, 14, 1, 14, 1, 14, 1, 14, 1, 14, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**19 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB
OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.44 20 dB Whisper/Shout P2A Pulse Rise Time Test

This test verifies that the rise time of the P2A pulse when invoking the 20 dB Whisper/Shout attenuation level is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making appropriate P2A rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (14, 1, 14, 1, 14, 1, 14, 1, 14, 1, 14, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P2A pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse.

Step 6. Verify that the resulting measurement is as follows:

MFG LIM	50 ns ≤ P2A rise time ≤ 100 ns
OPR LIM	50 ns ≤ P2A rise time ≤ 100 ns

4.14.45 20 dB (Absolute) Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the absolute step size between the 0 dB and 20 dB Whisper/Shout attenuation level is within specified limits.

Step 1. Subtract the P2A peak power measurement made in the "**20 dB Whisper/Shout P2A Pulse Peak Power Test**" from the P2A peak power measurement made in the "**0 dB Whisper/Shout P2A Pulse Peak Power Test**"

Step 2. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	18.5 dB ≤ result ≤ 21.5 dB
OPR LIM	18.0 dB ≤ result ≤ 22.0 dB

4.14.46 21 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 20 dB and 21 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 20 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (15, 1, 15, 1, 15, 1, 15, 1, 15, 1, 15, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1* ***n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**20 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB
OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.47 22 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 21 dB and 22 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 21 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (16, 1, 16, 1, 16, 1, 16, 1, 16, 1, 16, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1* ***n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**21 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB
OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.48 23 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 22 dB and 23 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 22 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (17, 1, 17, 1, 17, 1, 17, 1, 17, 1, 17, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**22 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB
OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.49 24 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 23 dB and 24 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 23 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (18, 1, 18, 1, 18, 1, 18, 1, 18, 1, 18, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**23 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB
OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.50 25 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 24 dB and 25 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 24 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (19, 1, 19, 1, 19, 1, 19, 1, 19, 1, 19, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**24 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB

OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.51 26 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 25 dB and 26 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 25 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (1A, 1, 1A, 1, 1A, 1, 1A, 1, 1A, 1, 1A, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**25 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB
OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.14.52 27 dB Whisper/Shout P2A Pulse Peak Power Test

This test will verify that the step size between the 26 dB and 27 dB Whisper/Shout attenuation levels is within specified limits. The peak power measurement made in this test will be subtracted from the measurement made for the 26 dB Whisper/Shout attenuation level and the result will be verified.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (1B, 1, 1B, 1, 1B, 1, 1B, 1, 1B, 1, 1B, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the peak power of the P2A pulse. Subtract this measurement from the peak power measurement recorded in the "**26 dB Whisper/Shout P2A Pulse Peak Power Test**".

Step 6. Verify that the result from the subtraction between the measurements is as follows:

MFG LIM	0.500 dB ≤ result ≤ 1.500 dB
OPR LIM	0.500 dB ≤ result ≤ 1.500 dB
PRETEST	0.625 dB ≤ result ≤ 1.375 dB

4.15 RF Xmtr: ATCRBS Deviation And Spacing Tests

These tests command the UUT to generate six-pulse ATCRBS interrogations out the Top 0 antenna port. All pulses are at full power. The six-pulse interrogation may be repeated at a maximum rate of once every 2 ms for averaging. Refer to Figures 1 and 3 for these tests.

4.15.1 ATCRBS MODE C: Amplitude Deviation Test

This test will verify that the amplitude deviation within the ATCRBS six-pulse sequence is within specified limits for MODE C.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the 6 pulses.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the amplitude of each pulse within the ATCRBS six- pulse sequence. Subtract the peak power amplitude of the lowest amplitude pulse from the peak power amplitude of the highest amplitude pulse. The difference shall be specified in the following step.

Step 6. Verify that the result from the subtraction between the measurements is as follows: (0.00 dB ≤ result ≤ 0.50 dB)

4.15.2 ATCRBS MODE C: S1 Pulse To P1 Pulse Timing Test

This test will verify that the spacing between the leading edge of the S1 pulse to the leading edge of the P1 pulse is within specified limits for MODE C.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate timing measurements of the S1 and P1 pulses.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the spacing between S1 and P1. The time between the 50% voltage points of the leading edges of the S1 and P1 pulses shall be as specified in the following step.

Step 6. Verify that the time between S1 and P1 is 2.0 ± 0.1 us.

4.15.3 ATCRBS MODE C: P1 Pulse To P2A Pulse Timing Test

This test will verify that the spacing between the leading edge of the P1 pulse to the leading edge of the P2A pulse is within specified limits for MODE C.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate timing measurements of the P1 and P2A pulses.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the spacing between the leading edge of the P1 pulse to the leading edge of the P2A pulse. The time between the 50% voltage points of the leading edges of the P1 and P2A pulses shall be as specified in the following step.

Step 6. Verify that the time between P1 and P2A is 2.0 ± 0.1 us.

4.15.4 ATCRBS MODE C: P2A Pulse To P2B Pulse Timing Test

This test will verify that the spacing between the leading edge of the P2A pulse to the leading edge of the P2B pulse is within specified limits for MODE C.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate timing measurements of the P2A and P2B pulses.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the spacing between the leading edge of the P2A pulse to the leading edge of the P2B pulse. The time between the 50% voltage points of the leading edges of the P2A and P2B pulses shall be as specified in the following step.

Step 6. Verify that the time between P2A and P2B is 17.0 ± 0.1 us.

4.15.5 ATCRBS MODE C: P2B Pulse To P3 Pulse Timing Test

This test will verify that the spacing between the leading edge of the P2B pulse to the leading edge of the P3 pulse is within specified limits for MODE C.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate timing measurements of the P2B and P3 pulses.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the spacing between the leading edge of the P2B pulse to the leading edge of the P3 pulse. The time between the 50% voltage points of the leading edges of the P2B and P3 pulses shall be as specified in the following step.

Step 6. Verify that the time between P2B and P3 is 2.0 ± 0.1 us.

4.15.6 ATCRBS MODE C: P3 Pulse To P4 Pulse Timing Test

This test will verify that the spacing between the leading edge of the P3 pulse to the leading edge of the P4 pulse is within specified limits for MODE C.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate timing measurements of the P3 and P4 pulses.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the spacing between the leading edge of the P3 pulse to the leading edge of the P4 pulse. The time between the 50% voltage points of the leading edges of the P3 and P4 pulses shall be as specified in the following step.

Step 6. Verify that the time between P3 and P4 is 2.0 ± 0.1 us.

4.15.7 ATCRBS MODE 2: Amplitude Deviation Test

This test will verify that the amplitude deviation within the ATCRBS six-pulse sequence is within specified limits for MODE 2.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the 6 pulses.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_2, Top)
InitAtcTxWrds7Thru10 (00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the amplitude of each pulse within the ATCRBS six- pulse sequence. Subtract the peak power amplitude of the lowest amplitude pulse from the peak power amplitude of the highest amplitude pulse. The difference shall be specified in the following step.

Step 6. Verify that the result from the subtraction between the measurements is as follows: (0.00 dB ≤ result ≤ 0.50 dB)

4.15.8 ATCRBS MODE 2: S1 Pulse To P1 Pulse Timing Test

This test will verify that the spacing between the leading edge of the S1 pulse to the leading edge of the P1 pulse is within specified limits for MODE 2.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate timing measurements of the S1 and P1 pulses.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_2, Top)
InitAtcTxWrds7Thru10 (00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the spacing between S1 and P1. The time between the 50% voltage points of the leading edges of the S1 and P1 pulses shall be as specified in the following step..

Step 6. Verify that the time between S1 and P1 is 2.0 ± 0.1 us.

4.15.9 ATCRBS MODE 2: P1 Pulse To P2A Pulse Timing Test

This test will verify that the spacing between the leading edge of the P1 pulse to the leading edge of the P2A pulse is within specified limits for MODE 2.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate timing measurements of the P1 and P2A pulses.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_2, Top)
InitAtcTxWrds7Thru10 (00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1* ***n***".

Step 5. Using the Peak Power Meter, measure the spacing between the leading edge of the P1 pulse to the leading edge of the P2A pulse. The time between the 50% voltage points of the leading edges of the P1 and P2A pulses shall be as specified in the following step.

Step 6. Verify that the time between P1 and P2A is 2.0 ± 0.1 us.

4.15.10 ATCRBS MODE 2: P2A Pulse To P2B Pulse Timing Test

This test will verify that the spacing between the leading edge of the P2A pulse to the leading edge of the P2B pulse is within specified limits for MODE 2.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate timing measurements of the P2A and P2B pulses.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_2, Top)
InitAtcTxWrds7Thru10 (00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1* ***n***".

Step 5. Using the Peak Power Meter, measure the spacing between the leading edge of the P2A pulse to the leading edge of the P2B pulse. The time between the 50% voltage points of the leading edges of the P2A and P2B pulses shall be as specified in the following step.

Step 6. Verify that the time between P2A and P2B is 1.0 ± 0.1 us.

4.15.11 ATCRBS MODE 2: P2B Pulse To P3 Pulse Timing Test

This test will verify that the spacing between the leading edge of the P2B pulse to the leading edge of the P3 pulse is within specified limits for MODE 2.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate timing measurements of the P2B and P3 pulses.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_2, Top)
InitAtcTxWrds7Thru10 (00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1* ***n***".

Step 5. Using the Peak Power Meter, measure the spacing between the leading edge of the P2B pulse to the leading edge of the P3 pulse. The time between the 50% voltage points of the leading edges of the P2B and P3 pulses shall be as specified in the following step.

Step 6. Verify that the time between P2B and P3 is 2.0 ± 0.1 us.

4.15.12 ATCRBS MODE 2: P3 Pulse To P4 Pulse Timing Test

This test will verify that the spacing between the leading edge of the P3 pulse to the leading edge of the P4 pulse is within specified limits for MODE 2.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate timing measurements of the P3 and P4 pulses.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_2, Top)
InitAtcTxWrds7Thru10 (00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1* ***n***".

Step 5. Using the Peak Power Meter, measure the spacing between the leading edge of the P3 pulse to the leading edge of the P4 pulse. The time between the 50% voltage points of the leading edges of the P3 and P4 pulses shall be as specified in the following step.

Step 6. Verify that the time between P3 and P4 is 2.0 ± 0.1 us.

4.15.13 ATCRBS MODE A: Amplitude Deviation Test

This test will verify that the amplitude deviation within the ATCRBS six-pulse sequence is within specified limits for MODE A.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the 6 pulses.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_A, Top)
InitAtcTxWrds7Thru10 (00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the amplitude of each pulse within the ATCRBS six- pulse sequence. Subtract the peak power amplitude of the lowest amplitude pulse from the peak power amplitude of the highest amplitude pulse. The difference shall be specified in the following step.

Step 6. Verify that the result from the subtraction between the measurements is as follows: (0.00 dB ≤ result ≤ 0.50 dB)

4.15.14 ATCRBS MODE A: S1 Pulse To P1 Pulse Timing Test

This test will verify that the spacing between the leading edge of the S1 pulse to the leading edge of the P1 pulse is within specified limits for MODE A.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate timing measurements of the S1 and P1 pulses.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_A, Top)
InitAtcTxWrds7Thru10 (00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1* ***n***".

Step 5. Using the Peak Power Meter, measure the spacing between S1 and P1. The time between the 50% voltage points of the leading edges of the S1 and P1 pulses shall be as specified in the following step..

Step 6. Verify that the time between S1 and P1 is 2.0 ± 0.1 us.

4.15.15 ATCRBS MODE A: P1 Pulse To P2A Pulse Timing Test

This test will verify that the spacing between the leading edge of the P1 pulse to the leading edge of the P2A pulse is within specified limits for MODE A.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate timing measurements of the P1 and P2A pulses.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_A, Top)
InitAtcTxWrds7Thru10 (00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1* ***n***".

Step 5. Using the Peak Power Meter, measure the spacing between the leading edge of the P1 pulse to the leading edge of the P2A pulse. The time between the 50% voltage points of the leading edges of the P1 and P2A pulses shall be as specified in the following step.

Step 6. Verify that the time between P1 and P2A is 2.0 ± 0.1 us.

4.15.16 ATCRBS MODE A: P2A Pulse To P2B Pulse Timing Test

This test will verify that the spacing between the leading edge of the P2A pulse to the leading edge of the P2B pulse is within specified limits for MODE A.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate timing measurements of the P2A and P2B pulses.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_A, Top)
InitAtcTxWrds7Thru10 (00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the spacing between the leading edge of the P2A pulse to the leading edge of the P2B pulse. The time between the 50% voltage points of the leading edges of the P2A and P2B pulses shall be as specified in the following step.

Step 6. Verify that the time between P2A and P2B is 4.0 ± 0.1 us.

4.15.17 ATCRBS MODE A: P2B Pulse To P3 Pulse Timing Test

This test will verify that the spacing between the leading edge of the P2B pulse to the leading edge of the P3 pulse is within specified limits for MODE A.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate timing measurements of the P2B and P3 pulses.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_A, Top)
InitAtcTxWrds7Thru10 (00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the spacing between the leading edge of the P2B pulse to the leading edge of the P3 pulse. The time between the 50% voltage points of the leading edges of the P2B and P3 pulses shall be as specified in the following step.

Step 6. Verify that the time between P2B and P3 is 2.0 ± 0.1 us.

4.15.18 ATCRBS MODE A: P3 Pulse To P4 Pulse Timing Test

This test will verify that the spacing between the leading edge of the P3 pulse to the leading edge of the P4 pulse is within specified limits for MODE A.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the same power level.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate timing measurements of the P3 and P4 pulses.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_A, Top)
InitAtcTxWrds7Thru10 (00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the spacing between the leading edge of the P3 pulse to the leading edge of the P4 pulse. The time between the 50% voltage points of the leading edges of the P3 and P4 pulses shall be as specified in the following step.

Step 6. Verify that the time between P3 and P4 is 2.0 ± 0.1 us.

4.16 RF Xmtr: ATCRBS Missing Pulses Peak Power Tests

4.16.1 ATCRBS: S1 Pulse (w/o P1/P3) Peak Power Test

This test will verify that the peak power of the S1 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the following levels:
S1 full power, P1 missing, P2A full power, P2B full power, P3 missing, P4 full power.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the S1 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (00, 1, -1, 1, 00, 1, 00, 1, -1, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, Measure the peak power of the S1 pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (S1 peak power **≥** +53.33 dBm)

4.16.2 ATCRBS: P1 Pulse (w/o P1/P3) Peak Power Test

This test will verify that the peak power of the P1 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the following levels: S1 full power, P1 missing, P2A full power, P2B full power, P3 missing, P4 full power.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P1 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (00, 1, -1, 1, 00, 1, 00, 1, -1, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1* ***n***".

Step 5. Using the Peak Power Meter, Measure the peak power of the P1 pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (P1 peak power **<** +35.0 dBm)

4.16.3 ATCRBS: P2A Pulse (w/o P1/P3) Peak Power Test

This test will verify that the peak power of the P2A pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the following levels: S1 full power, P1 missing, P2A full power, P2B full power, P3 missing, P4 full power.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (00, 1, -1, 1, 00, 1, 00, 1, -1, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1* ***n***".

Step 5. Using the Peak Power Meter, Measure the peak power of the P2A pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (P2A peak power **≥** +53.33 dBm)

4.16.4 ATCRBS: P2B Pulse (w/o P1/P3) Peak Power Test

This test will verify that the peak power of the P2B pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the following levels: S1 full power, P1 missing, P2A full power, P2B full power, P3 missing, P4 full power.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2B pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (00, 1, -1, 1, 00, 1, 00, 1, -1, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, Measure the peak power of the P2B pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (P2B peak power **≥** +53.33 dBm)

4.16.5 ATCRBS: P3 Pulse (w/o P1/P3) Peak Power Test

This test will verify that the peak power of the P3 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the following levels: S1 full power, P1 missing, P2A full power, P2B full power, P3 missing, P4 full power.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P3 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (00, 1, -1, 1, 00, 1, 00, 1, -1, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, Measure the peak power of the P3 pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (P3 peak power **<** +35.0 dBm)

4.16.6 ATCRBS: P4 Pulse (w/o P1/P3) Peak Power Test

This test will verify that the peak power of the P4 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the following levels: S1 full power, P1 missing, P2A full power, P2B full power, P3 missing, P4 full power.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P4 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (00, 1, -1, 1, 00, 1, 00, 1, -1, 1, 00, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, Measure the peak power of the P4 pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (P4 peak power **≥** +53.33 dBm)

4.17 RF Xmtr: Whisper/Shout (w/o S1/P2A/P2B/P4) Tests

These tests command the UUT to generate an ATCRBS interrogation out the Top 0 antenna port. The format of the interrogation is as follows: S1 missing, P1 full power, P2A missing, P2B missing, P3 full power, P4 missing. The interrogation may be repeated at a maximum rate of once every 2 ms for averaging. Refer to Figures 1 and 3 for these tests.

4.17.1 ATCRBS: S1 Pulse (w/o S1/P2A/P2B/P4) Peak Power Test

This test will verify that the peak power of the S1 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the following levels: S1 missing, P1 full power, P2A missing, P2B missing, P3 full power, P4 missing.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the S1 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (-1, 1, 00, 1, -1, 1, -1, 1, 00, 1, -1, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, Measure the peak power of the S1 pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (S1 peak power **<** +35.0 dBm)

4.17.2 ATCRBS: P1 Pulse (w/o S1/P2A/P2B/P4) Peak Power Test

This test will verify that the peak power of the P1 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the following levels:
S1 missing, P1 full power, P2A missing, P2B missing, P3 full power, P4 missing.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P1 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (-1, 1, 00, 1, -1, 1, -1, 1, 00, 1, -1, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, Measure the peak power of the P1 pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (P1 peak power **≥** +53.33 dBm)

4.17.3 ATCRBS: P2A Pulse (w/o S1/P2A/P2B/P4) Peak Power Test

This test will verify that the peak power of the P2A pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the following levels:
S1 missing, P1 full power, P2A missing, P2B missing, P3 full power, P4 missing.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (-1, 1, 00, 1, -1, 1, -1, 1, 00, 1, -1, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, Measure the peak power of the P2A pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (P2A peak power **<** +35.0 dBm)

4.17.4 ATCRBS: P2B Pulse (w/o S1/P2A/P2B/P4) Peak Power Test

This test will verify that the peak power of the P2B pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the following levels:
S1 missing, P1 full power, P2A missing, P2B missing, P3 full power, P4 missing.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P2B pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (-1, 1, 00, 1, -1, 1, -1, 1, 00, 1, -1, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, Measure the peak power of the P2B pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (P2B peak power **<** +35.0 dBm)

4.17.5 ATCRBS: P3 Pulse (w/o S1/P2A/P2B/P4) Peak Power Test

This test will verify that the peak power of the P3 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the following levels:
S1 missing, P1 full power, P2A missing, P2B missing, P3 full power, P4 missing.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P3 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)

InitAtcTxWrds7Thru10 (-1, 1, 00, 1, -1, 1, -1, 1, 00, 1, -1, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, Measure the peak power of the P3 pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (P3 peak power **≥** +53.33 dBm)

4.17.6 ATCRBS: P4 Pulse (w/o S1/P2A/P2B/P4) Peak Power Test

This test will verify that the peak power of the P4 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) using the Top antenna 0 degree port with each pulse set to the following levels:
S1 missing, P1 full power, P2A missing, P2B missing, P3 full power, P4 missing.

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurements of the P4 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (-1, 1, 00, 1, -1, 1, -1, 1, 00, 1, -1, 1, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, Measure the peak power of the P4 pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (P4 peak power **<** +35.0 dBm)

4.18 RF Xmtr: MODE-S (P1/P2/P6) Parametric Tests

These tests command the UUT to generate a Mode S interrogation (multiple times for averaging) out the Top 0 antenna port. Refer to Figures 1, 2 and 4 for these tests.

4.18.1 MODE-S: Xmtr Frequency (Umod P6/Long Reply) Test

This test will verify that the transmitter frequency is within the specified limits. The UUT will be commanded to generate a Mode S interrogation (multiple times for averaging) using the Top 0 Antenna and with the following transmission parameters:

Reply: Long P6 Pulse (unmodulated)
Whisper/Shout step: 00

Step 1. Configure the MTS RFIU to receive from the TOP Antenna, Quad 0 port.

Step 2. Setup the MTS RF Signal Generator for a frequency of 1029.9 MHZ (CW) , and amplitude of +22.0 DBM. This signal will be mixed with the UUT transmitter frequency within the RFIU to obtain the results.

Step 3. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 4. Setup the UUT to generate a single Mode S interrogation with an unmodulated P6 pulse by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitModeSTxWrds (Long, 00000000, 00000000, 00000000, 00000000)

Step 5. Transmit **n** MODE S interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 6. Read the transmitter frequency back from the MTS RFIU. The frequency shall be as specified in the following step.

Step 7. Verify that the transmitter frequency is as follows:

MFG LIM	1030 MHz ± 5 KHz
OPR LIM	1030 MHz ± 10 KHz

4.18.2 MODE-S: P1 Pulse (Umod P6/Long Reply) Peak Power Test

This test will verify that the peak power of the P1 pulse is within specified limits. The UUT will be commanded to generate a Mode S interrogation (multiple times for averaging) using the Top 0 Antenna and with the following transmission parameters:

Reply: Long P6 Pulse (unmodulated)
Whisper/Shout step: 00

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurement of the P1 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single Mode S interrogation with an unmodulated P6 pulse by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitModeSTxWrds (Long, 00000000, 00000000, 00000000, 00000000)

Step 4. Transmit **n** MODE S interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the peak power of the P1 pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (P1 peak power **≥** +53.33 dBm)

4.18.3 MODE-S: P1 Pulse (Umod P6/Long Reply) Pulse Width Test

This test will verify that the pulse width of the P1 pulse is within specified limits. The UUT will be commanded to generate a Mode S interrogation (multiple times for averaging) using the Top 0 Antenna and with the following transmission parameters:

Reply: Long P6 Pulse (unmodulated)
Whisper/Shout step: 00

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate pulse width measurement of the P1 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single Mode S interrogation with an unmodulated P6 pulse by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitModeSTxWrds (Long, 00000000, 00000000, 00000000, 00000000)

Step 4. Transmit **n** MODE S interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the pulse width of the P1 pulse (time between the 50% to 50% voltage points on the pulse). The pulse width between the 50% to 50% voltage points of the P1 pulse shall be as specified in the following step.

Step 6. Verify that (P1 pulse width = 800 ± 50 ns)

4.18.4 MODE-S: P1 Pulse to P2 Pulse (Umod P6/Long Reply) Timing Test

This test will verify that the spacing between the leading edge of the P1 pulse to the leading edge of the P2 pulse is within specified limits. The UUT will be commanded to generate a Mode S interrogation (multiple times for averaging) using the Top 0 Antenna and with the following transmission parameters:

Reply: Long P6 Pulse (unmodulated)
Whisper/Shout step: 00

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate timing measurement between the P1 and P2 pulses.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single Mode S interrogation with an unmodulated P6 pulse by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitModeSTxWrds (Long, 00000000, 00000000, 00000000, 00000000)

Step 4. Transmit **n** MODE S interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the spacing between the leading edge of the P1 pulse to the leading edge of the P2 pulse (time between the 50% voltage points of the leading edge of each pulse). The time between the 50% voltage points of the leading edges of the P1 and P2 pulses shall be as specified in the following step.

Step 6. Verify that (P1 to P2 Timing = 2.0 ± 0.1 us)

4.18.5 MODE-S: P2 Pulse (Umod P6/Long Reply) Peak Power Test

This test will verify that the peak power of the P2 pulse is within specified limits. The UUT will be commanded to generate a Mode S interrogation (multiple times for averaging) using the Top 0 Antenna and with the following transmission parameters:

Reply: Long P6 Pulse (unmodulated)
Whisper/Shout step: 00

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurement of the P2 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single Mode S interrogation with an unmodulated P6 pulse by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitModeSTxWrds (Long, 00000000, 00000000, 00000000, 00000000)

Step 4. Transmit **n** MODE S interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1* ***n***".

Step 5. Using the Peak Power Meter, measure the peak power of the P2 pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (P2 peak power **≥** +53.33 dBm)

4.18.6 MODE-S: P2 Pulse (Umod P6/Long Reply) Pulse Width Test

This test will verify that the pulse width of the P2 pulse is within specified limits. The UUT will be commanded to generate a Mode S interrogation (multiple times for averaging) using the Top 0 Antenna and with the following transmission parameters:

Reply: Long P6 Pulse (unmodulated)
Whisper/Shout step: 00

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate pulse width measurement of the P2 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single Mode S interrogation with an unmodulated P6 pulse by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitModeSTxWrds (Long, 00000000, 00000000, 00000000, 00000000)

Step 4. Transmit **n** MODE S interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1* ***n***".

Step 5. Using the Peak Power Meter, measure the pulse width of the P2 pulse (time between the 50% to 50% voltage points on the pulse). The pulse width between the 50% to 50% voltage points of the P2 pulse shall be as specified in the following step.

Step 6. Verify that (P2 pulse width = 800 ± 50 ns)

4.18.7 MODE-S: P6 Pulse (Umod P6/Long Reply) Peak Power Test

This test will verify that the peak power of the P6 pulse is within specified limits. The UUT will be commanded to generate a Mode S interrogation (multiple times for averaging) using the Top 0 Antenna and with the following transmission parameters:

Reply: Long P6 Pulse (unmodulated)
Whisper/Shout step: 00

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurement of the P6 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single Mode S interrogation with an unmodulated P6 pulse by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitModeSTxWrds (Long, 00000000, 00000000, 00000000, 00000000)

Step 4. Transmit **n** MODE S interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1* ***n***".

Step 5. Using the Peak Power Meter, measure the peak power of the P6 pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (P6 peak power ≥ +53.33 dBm)

4.18.8 MODE-S: P6 Pulse (Umod P6/Long Reply) Droop Test

This test will verify that the droop of the P6 pulse is within specified limits. The UUT will be commanded to generate a Mode S interrogation (multiple times for averaging) using the Top 0 Antenna and with the following transmission parameters:

Reply: Long P6 Pulse (unmodulated)
Whisper/Shout step: 00

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate droop measurement of the P6 pulse. The droop is the difference in amplitude sampled at a rate faster than 2μs/ sample from 1 μsec in from the leading edge of the P6 pulse to 1 μsec before the end of the P6 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single Mode S interrogation with an unmodulated P6 pulse by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitModeSTxWrds (Long, 00000000, 00000000, 00000000, 00000000)

Step 4. Transmit **n** MODE S interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1* ***n***".

Step 5. Using the Peak Power Meter, measure the droop of the P6 pulse. No measurement along the pulse shall be outside the specified limit in the following step.

Step 6. Verify that the droop measurement is as follows:

MFG LIM	P6 droop ≤ 1.0 dB
OPR LIM	P6 droop ≤ 1.5 dB

4.18.9 MODE-S: P6 Pulse (Umod P6/Long Reply) Pulse Width Test

This test will verify that the pulse width of the P6 pulse is within specified limits. The UUT will be commanded to generate a Mode S interrogation (multiple times for averaging) using the Top 0 Antenna and with the following transmission parameters:

Reply: Long P6 Pulse (unmodulated)
Whisper/Shout step: 00

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate pulse width measurement of the P6 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single Mode S interrogation with an unmodulated P6 pulse by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitModeSTxWrds (Long, 00000000, 00000000, 00000000, 00000000)

Step 4. Transmit **n** MODE S interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the pulse width of the P6 pulse (time between the 50% to 50% voltage points on the pulse). The pulse width between the 50% to 50% voltage points of the P6 pulse shall be as specified in the following step.

Step 6. Verify that (P6 pulse width = 30.250 ± 0.125 us)

4.18.10 MODE-S: P6 Pulse to SPR Position (Umod P6/Long Reply) Delay Test

This test will verify that the delay between the leading edge of the P6 pulse and the SPR position is within specified limits. The UUT will be commanded to generate a Mode S interrogation (multiple times for averaging) using the Top 0 Antenna and with the following transmission parameters:

Reply: Long P6 Pulse (unmodulated)
Whisper/Shout step: 00

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate P6 pulse to SPR position timing measurement.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single Mode S interrogation with an unmodulated P6 pulse by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitModeSTxWrds (Long, 00000000, 00000000, 00000000, 00000000)

Step 4. Transmit **n** MODE S interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the delay between the leading edge of the P6 pulse and the position of the SPR. The delay shall be as specified in the following step.

Step 6. Verify that P6 to SPR Delay is as follows:

MFG LIM	1.250 ± 0.035 us
OPR LIM	1.250 ± 0.040 us

4.18.11 MODE-S: DPSK (Mod P6/Long Reply) Decoding Test

This test will verify that the UUT is able to transmit a modulated MODE-S interrogation from the Top 0 Antenna port. The UUT will be commanded to generate a Mode S interrogation with a modulated P6 pulse. The DPSK data will be set to all ones (maximum phase reversals) during transmission. The transmitted message will be received demodulated by the test fixture. The demodulated data shall be equivalent to the transmitted data. This test will be performed 10 times in succession and must pass at least 9 times. The transmission parameters are as follows:

Reply: Long P6 Pulse (modulated)
Whisper/Shout step: 00

Step 1. Setup the MTS RFIU to receive Mode S interrogations with P6 modulated.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single Mode S interrogation with the DPSK data set to all ones (maximum phase reversals) by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitModeSTxWrds (Long, FFFFFFFF, FFFFFFFF, 39FFFFFF, 0000B434)

Step 4. Transmit 1 MODE S interrogations by executing the following HTS command: "*RFXMIT P1 1*".

Step 5. Read the data received by the MTS RFIU.

Step 6. Verify that that the received data is as follows:

"FFFFFFFFFFFFFFFFFFFFFFFFFFFF" (28 F's)

Step 7. Repeat steps 4 through 6 so that we have received a a total of 10 Mode S interrogations. Verify that in at least 9 out of 10 times, the data that was received by the MTS RFIU was "FFFFFFFFFFFFFFFFFFFFFFFFFFFF" (28 F's)

4.18.12 MODE-S: P6 Pulse (Umod P6/Short Reply) Pulse Width Test

This test will verify that the pulse width of the P6 pulse (Short) is within specified limits. The UUT will be commanded to generate a Mode S interrogation (multiple times for averaging) using the Top 0 Antenna and with the following transmission parameters:

Reply: Short P6 Pulse (unmodulated)
Whisper/Shout step: 00

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate pulse width measurement of the P6 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single Mode S interrogation with an unmodulated P6 pulse by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitModeSTxWrds (Long, 00000000, 00000000, 00000000, 00000000)

Step 4. Transmit **n** MODE S interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the pulse width of the P6 pulse (time between the 50% to 50% voltage points on the pulse). The pulse width between the 50% to 50% voltage points of the P6 pulse shall be as specified in the following step.

Step 6. Verify that (P6 pulse width = 16.250 ± 0.125 us)

4.19 RF I/O Directional Switching On Top Antenna Ports Tests

These tests will command the UUT to generate an ATCRBS interrogation out all four Top antenna ports and verifies the directional switching capability of the I/O. During these tests, at least one pulse will be present at each port (S1/P4 @ Top 0, P1 @ Top 90, P2A/P2B @ Top 180, P3 @ Top 270). Refer to Figures 1 and 3 for these tests.

4.19.1 RF I/O: S1 Pulse (S1/P4 On Top 0 Ant) Peak Power Test

This test will verify that the peak power of the S1 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Top 0 Ant Port	S1 / P4	0 dB
Top 90 Ant Port	P1	27 dB
Top 180 Ant Port	P2A / P2B	27 dB
Top 270 Ant Port	P3	27 dB

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurement of the S1 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (00, 01, 1B, 02, 1B, 04, 1B, 04, 1B, 08, 00, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the peak power of the S1 pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (S1 peak power **≥** +53.33 dBm)

4.19.2 RF I/O: S1 Pulse (S1/P4 On Top 0 Ant) Pulse Width Test

This test will verify that the pulse width of the S1 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Top 0 Ant Port	S1 / P4	0 dB
Top 90 Ant Port	P1	27 dB
Top 180 Ant Port	P2A / P2B	27 dB
Top 270 Ant Port	P3	27 dB

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate pulse width measurement of the S1 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (00, 01, 1B, 02, 1B, 04, 1B, 04, 1B, 08, 00, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the pulse width of the S1 pulse (time between the 50% to 50% voltage points on the pulse). The pulse width between the 50% to 50% voltage points of the S1 pulse shall be as specified in the following step.

Step 6. Verify that (S1 pulse width **=** 800 ± 50 ns)

4.19.3 RF I/O: S1 Pulse (S1/P4 On Top 0 Ant) Rise Time Test

This test will verify that the rise time of the S1 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Top 0 Ant Port	S1 / P4	0 dB
Top 90 Ant Port	P1	27 dB
Top 180 Ant Port	P2A / P2B	27 dB
Top 270 Ant Port	P3	27 dB

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making appropriate S1 rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (00, 01, 1B, 02, 1B, 04, 1B, 04, 1B, 08, 00, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the S1 pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse. The rise time shall be as specified in the following step

Step 6. Verify that the resulting measurement is as follows:

(50 ns ≤ S1 rise time ≤ 100 ns)

4.19.4 RF I/O: P4 Pulse (S1/P4 On Top 0 Ant) Peak Power Test

This test will verify that the peak power of the P4 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Top 0 Ant Port	S1 / P4	0 dB
Top 90 Ant Port	P1	27 dB
Top 180 Ant Port	P2A / P2B	27 dB
Top 270 Ant Port	P3	27 dB

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate peak power measurement of the P4 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (00, 01, 1B, 02, 1B, 04, 1B, 04, 1B, 08, 00, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the peak power of the P4 pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (P4 peak power **≥** +53.33 dBm)

4.19.5 RF I/O: P4 Pulse (S1/P4 On Top 0 Ant) Pulse Width Test

This test will verify that the pulse width of the P4 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Top 0 Ant Port	S1 / P4	0 dB
Top 90 Ant Port	P1	27 dB
Top 180 Ant Port	P2A / P2B	27 dB
Top 270 Ant Port	P3	27 dB

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making the appropriate pulse width measurement of the P4 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (00, 01, 1B, 02, 1B, 04, 1B, 04, 1B, 08, 00, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the pulse width of the P4 pulse (time between the 50% to 50% voltage points on the pulse). The pulse width between the 50% to 50% voltage points of the P4 pulse shall be as specified in the following step.

Step 6. Verify that (P4 pulse width = 800 ± 50 ns)

4.19.6 RF I/O: P4 Pulse (S1/P4 On Top 0 Ant) Rise Time Test

This test will verify that the rise time of the P4 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Top 0 Ant Port	S1 / P4	0 dB
Top 90 Ant Port	P1	27 dB
Top 180 Ant Port	P2A / P2B	27 dB
Top 270 Ant Port	P3	27 dB

Step 1. Connect the Peak Power meter to TOP 0 antenna port and setup for making appropriate P4 rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (00, 01, 1B, 02, 1B, 04, 1B, 04, 1B, 08, 00, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P4 pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse. The rise time shall be as specified in the following step

Step 6. Verify that the resulting measurement is as follows:

(50 ns ≤ P4 rise time ≤ 100 ns)

4.19.7 RF I/O: P1 Pulse (P1 On Top 90 Ant) Peak Power Test

This test will verify that the peak power of the P1 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Top 0 Ant Port	S1 / P4	27 dB
Top 90 Ant Port	P1	0 dB
Top 180 Ant Port	P2A / P2B	27 dB
Top 270 Ant	P3	27 dB

Port		

Step 1. Connect the Peak Power meter to TOP 90 antenna port and setup for making the appropriate peak power measurement of the P1 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (1B, 01, 00, 02, 1B, 04, 1B, 04, 1B, 08, 1B, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the peak power of the P1 pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (P1 peak power **≥** +53.33 dBm)

4.19.8 RF I/O: P1 Pulse (P1 On Top 90 Ant) Pulse Width Test

This test will verify that the pulse width of the P1 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Top 0 Ant Port	S1 / P4	27 dB
Top 90 Ant Port	P1	0 dB
Top 180 Ant Port	P2A / P2B	27 dB
Top 270 Ant Port	P3	27 dB

Step 1. Connect the Peak Power meter to TOP 90 antenna port and setup for making the appropriate pulse width measurement of the P1 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (1B, 01, 00, 02, 1B, 04, 1B, 04, 1B, 08, 1B, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the pulse width of the P1 pulse (time between the 50% to 50% voltage points on the pulse). The pulse width between the 50% to 50% voltage points of the P1 pulse shall be as specified in the following step.

Step 6. Verify that (P1 pulse width **=** 800 ± 50 ns)

4.19.9 RF I/O: P1 Pulse (P1 On Top 90 Ant) Rise Time Test

This test will verify that the rise time of the P1 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Top 0 Ant Port	S1 / P4	27 dB
Top 90 Ant Port	P1	0 dB
Top 180 Ant Port	P2A / P2B	27 dB
Top 270 Ant Port	P3	27 dB

Step 1. Connect the Peak Power meter to TOP 90 antenna port and setup for making appropriate P1 rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (1B, 01, 00, 02, 1B, 04, 1B, 04, 1B, 08, 1B, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P1 pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse. The rise time shall be as specified in the following step

Step 6. Verify that the resulting measurement is as follows:

(50 ns **≤** P1 Rise Time **≤** 100 ns)

4.19.10 RF I/O: P2A Pulse (P2A/P2B On Top 180 Ant) Peak Power Test

This test will verify that the peak power of the P2A pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Top 0 Ant Port	S1 / P4	27 dB

Top 90 Ant Port	P1	27 dB
Top 180 Ant Port	P2A / P2B	0 dB
Top 270 Ant Port	P3	27 dB

Step 1. Connect the Peak Power meter to TOP 180 antenna port and setup for making the appropriate peak power measurement of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (1B, 01, 1B, 02, 00, 04, 00, 04, 1B, 08, 1B, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the peak power of the P2A pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (P2A peak power **≥** +53.33 dBm)

4.19.11 RF I/O: P2A Pulse (P2A/P2B On Top 180 Ant) Pulse Width Test

This test will verify that the pulse width of the P2A pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Top 0 Ant Port	S1 / P4	27 dB
Top 90 Ant Port	P1	27 dB
Top 180 Ant Port	P2A / P2B	0 dB
Top 270 Ant Port	P3	27 dB

Step 1. Connect the Peak Power meter to TOP 180 antenna port and setup for making the appropriate pulse width measurement of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (1B, 01, 1B, 02, 00, 04, 00, 04, 1B, 08, 1B, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the pulse width of the P2A pulse (time between the 50% to 50% voltage points on the pulse). The pulse width between the 50% to 50% voltage points of the P2A pulse shall be as specified in the following step.

Step 6. Verify that (P2A pulse width **=** 800 ± 50 ns)

4.19.12 RF I/O: P2A Pulse (P2A/P2B On Top 180 Ant) Rise Time Test

This test will verify that the rise time of the P2A pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Top 0 Ant Port	S1 / P4	27 dB
Top 90 Ant Port	P1	27 dB
Top 180 Ant Port	P2A / P2B	0 dB
Top 270 Ant Port	P3	27 dB

Step 1. Connect the Peak Power meter to TOP 180 antenna port and setup for making appropriate P2A rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (1B, 01, 1B, 02, 00, 04, 00, 04, 1B, 08, 1B, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P2A pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse. The rise time shall be as specified in the following step

Step 6. Verify that the resulting measurement is as follows:

(50 ns **≤** P2A Rise Time **≤** 100 ns)

4.19.13 RF I/O: P2B Pulse (P2A/P2B On Top 180 Ant) Peak Power Test

This test will verify that the peak power of the P2B pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Top 0 Ant Port	S1 / P4	27 dB
Top 90 Ant Port	P1	27 dB
Top 180 Ant Port	P2A / P2B	0 dB
Top 270 Ant Port	P3	27 dB

Step 1. Connect the Peak Power meter to TOP 180 antenna port and setup for making the appropriate peak power measurement of the P2B pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (1B, 01, 1B, 02, 00, 04, 00, 04, 1B, 08, 1B, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the peak power of the P2B pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (P2B peak power **≥** +53.33 dBm)

4.19.14 RF I/O: P2B Pulse (P2A/P2B On Top 180 Ant) Pulse Width Test

This test will verify that the pulse width of the P2B pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Top 0 Ant Port	S1 / P4	27 dB
Top 90 Ant Port	P1	27 dB
Top 180 Ant Port	P2A / P2B	0 dB
Top 270 Ant Port	P3	27 dB

Step 1. Connect the Peak Power meter to TOP 180 antenna port and setup for making the appropriate pulse width measurement of the P2B pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (1B, 01, 1B, 02, 00, 04, 00, 04, 1B, 08, 1B, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the pulse width of the P2B pulse (time between the 50% to 50% voltage points on the pulse). The pulse width between the 50% to 50% voltage points of the P2B pulse shall be as specified in the following step.

Step 6. Verify that (P2B pulse width **=** 800 ± 50 ns)

4.19.15 RF I/O: P2B Pulse (P2A & P2B On Top 180 Ant) Rise Time Test

This test will verify that the rise time of the P2B pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Top 0 Ant Port	S1 / P4	27 dB
Top 90 Ant Port	P1	27 dB
Top 180 Ant Port	P2A / P2B	0 dB
Top 270 Ant Port	P3	27 dB

Step 1. Connect the Peak Power meter to TOP 180 antenna port and setup for making appropriate P2B rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (1B, 01, 1B, 02, 00, 04, 00, 04, 1B, 08, 1B, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P2B pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse. The rise time shall be as specified in the following step

Step 6. Verify that the resulting measurement is as follows:

(50 ns **≤** P2B Rise Time **≤** 100 ns)

4.19.16 RF I/O: P3 Pulse (P3 On Top 270 Ant) Peak Power Test

This test will verify that the peak power of the P3 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Top 0 Ant Port	S1 / P4	27 dB
Top 90 Ant Port	P1	27 dB
Top 180 Ant Port	P2A / P2B	27 dB
Top 270 Ant Port	P3	0 dB

Step 1. Connect the Peak Power meter to the TOP 270 antenna port and setup for making the appropriate peak power measurement of the P3 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (1B, 01, 1B, 02, 1B, 04, 1B, 04, 00, 08, 1B, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the peak power of the P3 pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (P3 peak power **≥** +53.33 dBm)

4.19.17 RF I/O: P3 Pulse (P3 On Top 270 Ant) Pulse Width Test

This test will verify that the pulse width of the P3 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Top 0 Ant Port	S1 / P4	27 dB
Top 90 Ant Port	P1	27 dB
Top 180 Ant Port	P2A / P2B	27 dB
Top 270 Ant Port	P3	0 dB

Step 1. Connect the Peak Power meter to TOP 270 antenna port and setup for making the appropriate pulse width measurement of the P3 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (1B, 01, 1B, 02, 1B, 04, 1B, 04, 00, 08, 1B, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the pulse width of the P3 pulse (time between the 50% to 50% voltage points on the pulse). The pulse width between the 50% to 50% voltage points of the P3 pulse shall be as specified in the following step.

Step 6. Verify that (P3 pulse width **=** 800 ± 50 ns)

4.19.18 RF I/O: P3 Pulse (P3 On Top 270 Ant) Rise Time Test

This test will verify that the rise time of the P3 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Bottom 0 Ant Port	S1 / P4	27 dB
Bottom 90 Ant Port	P1	27 dB
Bottom 180 Ant Port	P2A / P2B	27 dB
Bottom 270 Ant Port	P3	0 dB

Step 1. Connect the Peak Power meter to TOP 90 antenna port and setup for making appropriate P3 rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Top)
InitAtcTxWrds7Thru10 (1B, 01, 1B, 02, 1B, 04, 1B, 04, 00, 08, 1B, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P3 pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse. The rise time shall be as specified in the following step

Step 6. Verify that the resulting measurement is as follows:

(50 ns **≤** P3 Rise Time **≤** 100 ns)

4.20 RF I/O Directional Switching On Bottom Antenna Ports Tests

These tests will command the UUT to generate an ATCRBS interrogation out all four Bottom antenna ports and verifies the directional switching capability of the I/O. During these tests, at least one pulse will be present at each port (S1/P4 @ Bottom 0, P1 @ Bottom 90, P2A/P2B @ Bottom 180, P3 @ Bottom 270). Refer to Figures 1 and 3 for these tests.

4.20.1 RF I/O: S1 Pulse (S1/P4 On Bottom 0 Ant) Peak Power Test

This test will verify that the peak power of the S1 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Bottom 0 Ant Port	S1 / P4	0 dB
Bottom 90 Ant Port	P1	27 dB
Bottom 180 Ant Port	P2A / P2B	27 dB
Bottom 270 Ant Port	P3	27 dB

Step 1. Connect the Peak Power meter to Bottom 0 antenna port and setup for making the appropriate peak power measurement of the S1 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Bot)
InitAtcTxWrds7Thru10 (00, 01, 1B, 02, 1B, 04, 1B, 04, 1B, 08, 00, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the peak power of the S1 pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (S1 peak power **≥** +53.33 dBm)

4.20.2 RF I/O: S1 Pulse (S1/P4 On Bottom 0 Ant) Pulse Width Test

This test will verify that the pulse width of the S1 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Bottom 0 Ant Port	S1 / P4	0 dB
Bottom 90 Ant Port	P1	27 dB
Bottom 180 Ant Port	P2A / P2B	27 dB

Bottom 270 Ant Port	P3	27 dB

Step 1. Connect the Peak Power meter to Bottom 0 antenna port and setup for making the appropriate peak power measurement of the S1 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Bot)
InitAtcTxWrds7Thru10 (00, 01, 1B, 02, 1B, 04, 1B, 04, 1B, 08, 00, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the pulse width of the S1 pulse (time between the 50% to 50% voltage points on the pulse). The pulse width between the 50% to 50% voltage points of the S1 pulse shall be as specified in the following step.

Step 6. Verify that (S1 pulse width **=** 800 ± 50 ns)

4.20.3 RF I/O: S1 Pulse (S1/P4 On Bottom 0 Ant) Rise Time Test

This test will verify that the rise time of the S1 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Bottom 0 Ant Port	S1 / P4	0 dB
Bottom 90 Ant Port	P1	27 dB
Bottom 180 Ant Port	P2A / P2B	27 dB
Bottom 270 Ant Port	P3	27 dB

Step 1. Connect the Peak Power meter to Bottom 0 antenna port and setup for making appropriate S1 rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Bot)
InitAtcTxWrds7Thru10 (00, 01, 1B, 02, 1B, 04, 1B, 04, 1B, 08, 00, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the S1 pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse. The rise time shall be as specified in the following step

Step 6. Verify that the resulting measurement is as follows:

(50 ns ≤ S1 rise time ≤ 100 ns)

4.20.4 RF I/O: P4 Pulse (S1/P4 On Bottom 0 Ant) Peak Power Test

This test will verify that the peak power of the P4 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Bottom 0 Ant Port	S1 / P4	0 dB
Bottom 90 Ant Port	P1	27 dB
Bottom 180 Ant Port	P2A / P2B	27 dB
Bottom 270 Ant Port	P3	27 dB

Step 1. Connect the Peak Power meter to Bottom 0 antenna port and setup for making the appropriate peak power measurement of the P4 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Bot)
InitAtcTxWrds7Thru10 (00, 01, 1B, 02, 1B, 04, 1B, 04, 1B, 08, 00, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the peak power of the P4 pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (P4 peak power ≥ +53.33 dBm)

4.20.5 RF I/O: P4 Pulse (S1/P4 On Bottom 0 Ant) Pulse Width Test

This test will verify that the pulse width of the P4 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuatio

		n
Bottom 0 Ant Port	S1 / P4	0 dB
Bottom 90 Ant Port	P1	27 dB
Bottom 180 Ant Port	P2A / P2B	27 dB
Bottom 270 Ant Port	P3	27 dB

Step 1. Connect the Peak Power meter to the Bottom 0 antenna port and setup for making the appropriate pulse width measurement of the P4 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Bot)
InitAtcTxWrds7Thru10 (00, 01, 1B, 02, 1B, 04, 1B, 04, 1B, 08, 00, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the pulse width of the P4 pulse (time between the 50% to 50% voltage points on the pulse). The pulse width between the 50% to 50% voltage points of the P4 pulse shall be as specified in the following step.

Step 6. Verify that (P4 pulse width **=** 800 ± 50 ns)

4.20.6 RF I/O: P4 Pulse (S1/P4 On Bottom 0 Ant) Rise Time Test

This test will verify that the rise time of the P4 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	**Pulse**	**Attenuation**
Bottom 0 Ant Port	S1 / P4	0 dB
Bottom 90 Ant Port	P1	27 dB
Bottom 180 Ant Port	P2A / P2B	27 dB
Bottom 270 Ant Port	P3	27 dB

Step 1. Connect the Peak Power meter to the Bottom 0 antenna port and setup for making appropriate P4 rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Bot)
InitAtcTxWrds7Thru10 (00, 01, 1B, 02, 1B, 04, 1B, 04, 1B, 08, 00, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P4 pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse. The rise time shall be as specified in the following step

Step 6. Verify that the resulting measurement is as follows: (50 ns ≤ P4 rise time ≤ 100 ns)

4.20.7 RF I/O: P1 Pulse (P1 On Bottom 270 Ant) Peak Power Test

This test will verify that the peak power of the P1 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Bottom 0 Ant Port	S1 / P4	27 dB
Bottom 90 Ant Port	P3	27 dB
Bottom 180 Ant Port	P2A / P2B	27 dB
Bottom 270 Ant Port	P1	0 dB

Step 1. Connect the Peak Power meter to the Bottom 270 antenna port and setup for making the appropriate peak power measurement of the P1 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Bot)
InitAtcTxWrds7Thru10 (1B, 01, 00, 08, 1B, 04, 1B, 04, 1B, 02, 1B, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the peak power of the P1 pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (P1 peak power **≥** +53.33 dBm)

4.20.8 RF I/O: P1 Pulse (P1 On Bottom 270 Ant) Pulse Width Test

This test will verify that the pulse width of the P1 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Bottom 0 Ant Port	S1 / P4	27 dB
Bottom 90 Ant Port	P3	27 dB
Bottom 180 Ant Port	P2A / P2B	27 dB
Bottom 270 Ant Port	P1	0 dB

Step 1. Connect the Peak Power meter to the Bottom 270 antenna port and setup for making the appropriate pulse width measurement of the P1 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Bot)
InitAtcTxWrds7Thru10 (1B, 01, 00, 08, 1B, 04, 1B, 04, 1B, 02, 1B, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the pulse width of the P1 pulse (time between the 50% to 50% voltage points on the pulse). The pulse width between the 50% to 50% voltage points of the P1 pulse shall be as specified in the following step.

Step 6. Verify that (P1 pulse width **=** 800 ± 50 ns)

4.20.9 RF I/O: P1 Pulse (P1 On Bottom 270 Ant) Rise Time Test

This test will verify that the rise time of the P1 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Bottom 0 Ant Port	S1 / P4	27 dB
Bottom 90 Ant Port	P3	27 dB
Bottom 180 Ant Port	P2A / P2B	27 dB
Bottom 270 Ant Port	P1	0 dB

Step 1. Connect the Peak Power meter to the Bottom 270 antenna port and setup for making appropriate P1 rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Bot)
InitAtcTxWrds7Thru10 (1B, 01, 00, 08, 1B, 04, 1B, 04, 1B, 02, 1B, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P1 pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse. The rise time shall be as specified in the following step

Step 6. Verify that the resulting measurement is as follows:

(50 ns ≤ P1 Rise Time ≤ 100 ns)

4.20.10 RF I/O: P2A Pulse (P2A/P2B On Bottom 180 Ant) Peak Power Test

This test will verify that the peak power of the P2A pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Bottom 0 Ant Port	S1 / P4	27 dB
Bottom 90 Ant Port	P3	27 dB
Bottom 180 Ant Port	P2A / P2B	0 dB
Bottom 270 Ant Port	P1	27 dB

Step 1. Connect the Peak Power meter to the Bottom 180 antenna port and setup for making the appropriate peak power measurement of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Bot)
InitAtcTxWrds7Thru10 (1B, 01, 1B, 08, 00, 04, 00, 04, 1B, 02, 1B, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the peak power of the P2A pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (P2A peak power ≥ +53.33 dBm)

4.20.11 RF I/O: P2A Pulse (P2A/P2B On Bottom 180 Ant) Pulse Width Test

This test will verify that the pulse width of the P2A pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Bottom 0 Ant Port	S1 / P4	27 dB
Bottom 90 Ant Port	P3	27 dB
Bottom 180 Ant Port	P2A / P2B	0 dB
Bottom 270 Ant Port	P1	27 dB

Step 1. Connect the Peak Power meter to the Bottom 180 antenna port and setup for making the appropriate pulse width measurement of the P2A pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Bot)
InitAtcTxWrds7Thru10 (1B, 01, 1B, 08, 00, 04, 00, 04, 1B, 02, 1B, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the pulse width of the P2A pulse (time between the 50% to 50% voltage points on the pulse). The pulse width between the 50% to 50% voltage points of the P2A pulse shall be as specified in the following step.

Step 6. Verify that (P2A pulse width **=** 800 ± 50 ns)

4.20.12 RF I/O: P2A Pulse (P2A/P2B On Bottom 180 Ant) Rise Time Test

This test will verify that the rise time of the P2A pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Bottom 0 Ant Port	S1 / P4	27 dB
Bottom 90 Ant Port	P3	27 dB
Bottom 180 Ant Port	P2A / P2B	0 dB
Bottom 270 Ant Port	P1	27 dB

Step 1. Connect the Peak Power meter to the Bottom 180 antenna port and setup for making appropriate P2A rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Bot)
InitAtcTxWrds7Thru10 (1B, 01, 1B, 08, 00, 04, 00, 04, 1B, 02, 1B, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P2A pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse. The rise time shall be as specified in the following step

Step 6. Verify that the resulting measurement is as follows:

(50 ns ≤ P2A Rise Time ≤ 100 ns)

4.20.13 RF I/O: P2B Pulse (P2A/P2B On Bottom 180 Ant) Peak Power Test

This test will verify that the peak power of the P2B pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Bottom 0 Ant Port	S1 / P4	27 dB
Bottom 90 Ant Port	P3	27 dB
Bottom 180 Ant Port	P2A / P2B	0 dB
Bottom 270 Ant Port	P1	27 dB

Step 1. Connect the Peak Power meter to the Bottom 180 antenna port and setup for making the appropriate peak power measurement of the P2B pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Bot)
InitAtcTxWrds7Thru10 (1B, 01, 1B, 08, 00, 04, 00, 04, 1B, 02, 1B, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the peak power of the P2B pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (P2B peak power ≥ +53.33 dBm)

4.20.14 RF I/O: P2B Pulse (P2A/P2B On Bottom 180 Ant) Pulse Width Test

This test will verify that the pulse width of the P2B pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Bottom 0 Ant Port	S1 / P4	27 dB
Bottom 90 Ant Port	P3	27 dB
Bottom 180 Ant Port	P2A / P2B	0 dB
Bottom 270 Ant Port	P1	27 dB

Step 1. Connect the Peak Power meter to the Bottom 180 antenna port and setup for making the appropriate pulse width measurement of the P2B pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Bot)
InitAtcTxWrds7Thru10 (1B, 01, 1B, 08, 00, 04, 00, 04, 1B, 02, 1B, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the pulse width of the P2B pulse (time between the 50% to 50% voltage points on the pulse). The pulse width between the 50% to 50% voltage points of the P2B pulse shall be as specified in the following step.

Step 6. Verify that (P2B pulse width **=** 800 ± 50 ns)

4.20.15 RF I/O: P2B Pulse (P2A/P2B On Bottom 180 Ant) Rise Time Test

This test will verify that the rise time of the P2B pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Bottom 0 Ant Port	S1 / P4	27 dB
Bottom 90 Ant Port	P3	27 dB
Bottom 180 Ant Port	P2A / P2B	0 dB
Bottom 270 Ant Port	P1	27 dB

Step 1. Connect the Peak Power meter to BOTTOM 180 antenna port and setup for making appropriate P2B rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Bot)
InitAtcTxWrds7Thru10 (1B, 01, 1B, 08, 00, 04, 00, 04, 1B, 02, 1B, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P2B pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse. The rise time shall be as specified in the following step

Step 6. Verify that the resulting measurement is as follows:

(50 ns ≤ P2B Rise Time ≤ 100 ns)

4.20.16 RF I/O: P3 Pulse (P3 On Bottom 90 Ant) Peak Power Test

This test will verify that the peak power of the P3 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Bottom 0 Ant Port	S1 / P4	27 dB
Bottom 90 Ant Port	P3	0 dB
Bottom 180 Ant Port	P2A / P2B	27 dB
Bottom 270 Ant Port	P1	27 dB

Step 1. Connect the Peak Power meter to the Bottom 90 antenna port and setup for making the appropriate peak power measurement of the P3 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Bot)
InitAtcTxWrds7Thru10 (1B, 01, 1B, 08, 1B, 04, 1B, 04, 00, 02, 1B, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the peak power of the P3 pulse. The peak power shall be as specified in the following step.

Step 6. Verify that (P3 peak power ≥ +53.33 dBm)

4.20.17 RF I/O: P3 Pulse (P3 On Bottom 90 Ant) Pulse Width Test

This test will verify that the pulse width of the P3 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Bottom 0 Ant Port	S1 / P4	27 dB
Bottom 90 Ant Port	P3	0 dB
Bottom 180 Ant Port	P2A / P2B	27 dB
Bottom 270 Ant Port	P1	27 dB

Step 1. Connect the Peak Power meter to the Bottom 90 antenna port and setup for making the appropriate pulse width measurement of the P3 pulse.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Bot)
InitAtcTxWrds7Thru10 (1B, 01, 1B, 08, 1B, 04, 1B, 04, 00, 02, 1B, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure the pulse width of the P3 pulse (time between the 50% to 50% voltage points on the pulse). The pulse width between the 50% to 50% voltage points of the P3 pulse shall be as specified in the following step.

Step 6. Verify that (P3 pulse width **=** 800 ± 50 ns)

4.20.18 RF I/O: P3 Pulse (P3 On Bottom 90 Ant) Rise Time Test

This test will verify that the rise time of the P3 pulse is within specified limits.

The UUT will be commanded to generate a single whisper/shout interrogation (multiple times for averaging) with each pulse set individually and with the following transmission parameters:

Port	Pulse	Attenuation
Bottom 0 Ant Port	S1 / P4	27 dB
Bottom 90 Ant Port	P3	0 dB
Bottom 180 Ant Port	P2A / P2B	27 dB
Bottom 270 Ant Port	P1	27 dB

Step 1. Connect the Peak Power meter to the Bottom 90 antenna port and setup for making appropriate P3 rise time measurements.

Step 2. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 3. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instructions. See Appendix D for the description of these macro instructions.

InitAtcTxWrds1Thru6 (Mode_C, Bot)
InitAtcTxWrds7Thru10 (1B, 01, 1B, 08, 1B, 04, 1B, 04, 00, 02, 1B, 01, 0)

Step 4. Transmit **n** ATCRBS interrogations (where **n** is an integer between 100 and 1000) for a desired average of readings by executing the following HTS command: "*RFXMIT P1 **n***".

Step 5. Using the Peak Power Meter, measure and record the rise time of the P3 pulse. The measurement should be made between the 10% to 90% voltage points of the leading edge of the pulse. The rise time shall be as specified in the following step

Step 6. Verify that the resulting measurement is as follows:

(50 ns ≤ P3 Rise Time ≤ 100 ns)

4.21 Antenna Fault Sensing Tests

These tests verifiy the antenna fault sensing capability of the RX/IO CCA. Various values of dc resistance are connected between the center conductor of the antenna ports and ground, and then the RF Antenna BITE/Status register is read to verify proper status.

4.21.1 Ant Fault Sense: DC BITE (Top Ports Nom) Test

This test will verify that the fault sensing functionality is within specifications by loading the Top antenna ports with nominal resistances.

Step 1. Connect the following resistances to the Top/Bottom Antenna ports:

Antenna Ports	Resistance
Top 0	Nom: 1000 ± 50 Ohms
Top 90	Nom: 2000 ± 50 Ohms
Top 180	Nom: 4020 ± 50 Ohms
Top 270	Nom: 8060 ± 50 Ohms
Bottom 0	50 ± 5 Ohms
Bottom 90	50 ± 5 Ohms
Bottom 180	50 ± 5 Ohms
Bottom 270	50 ± 5 Ohms

Step 2. Initiate the Antenna DC BITE operation by executing the following HTS command: "*WL P1 88004000 80000000*".

Step 3. Read the the Antenna BITE/Status register by executing the following HTS command: "*RL P1 88004000*".

Step 4. Verify that the returned result is equal to "*002A8000*"

4.21.2 Ant Fault Sense: DC BITE (Top 0: High) Test

This test will verify that the fault sensing functionality is within specifications by loading the Top 0 antenna port with out of tolerance resistance.

Step 1. Connect the following resistances to the Top/Bottom Antenna ports:

Antenna Ports	Resistance
Top 0	High: > 1050 Ohms
Top 90	Nom: 2000 ± 50 Ohms
Top 180	Nom: 4020 ± 50 Ohms
Top 270	Nom: 8060 ± 50 Ohms
Bottom 0	50 ± 5 Ohms
Bottom 90	50 ± 5 Ohms
Bottom 180	50 ± 5 Ohms
Bottom 270	50 ± 5 Ohms

Step 2. Initiate the Antenna DC BITE operation by executing the following HTS command: "*WL P1 88004000 80000000*".

Step 3. Read the the Antenna BITE/Status register by executing the following HTS command: "*RL P1 88004000*".

Step 4. Verify that the returned result is equal to "*102A8000*"

4.21.3 Ant Fault Sense: DC BITE (Top 90: Low) Test

This test will verify that the fault sensing functionality is within specifications by loading the Top 90 antenna port with out of tolerance resistance.

Step 1. Connect the following resistances to the Top/Bottom Antenna ports:

Antenna Ports	Resistance
Top 0	Nom: 1000 ± 50 Ohms
Top 90	Low: < 1950 Ohms
Top 180	Nom: 4020 ± 50 Ohms
Top 270	Nom: 8060 ± 50 Ohms
Bottom 0	50 ± 5 Ohms
Bottom 90	50 ± 5 Ohms
Bottom 180	50 ± 5 Ohms
Bottom 270	50 ± 5 Ohms

Step 2. Initiate the Antenna DC BITE operation by executing the following HTS command: "*WL P1 88004000 80000000*".

Step 3. Read the the Antenna BITE/Status register by executing the following HTS command: "*RL P1 88004000*".

Step 4. Verify that the returned result is equal to "*082A8000*"

4.21.4 Ant Fault Sense: DC BITE (Top 180: High) Test

This test will verify that the fault sensing functionality is within specifications by loading the Top 180 antenna port with out of tolerance resistance.

Step 1. Connect the following resistances to the Top/Bottom Antenna ports:

Antenna Ports	Resistance
Top 0	Nom: 1000 ± 50 Ohms
Top 90	Nom: 2000 ± 50 Ohms
Top 180	High: > 4070 Ohms
Top 270	Nom: 8060 ± 50 Ohms
Bottom 0	50 ± 5 Ohms
Bottom 90	50 ± 5 Ohms
Bottom 180	50 ± 5 Ohms
Bottom 270	50 ± 5 Ohms

Step 2. Initiate the Antenna DC BITE operation by executing the following HTS command: "*WL P1 88004000 80000000*".

Step 3. Read the the Antenna BITE/Status register by executing the following HTS command: "*RL P1 88004000*".

Step 4. Verify that the returned result is equal to "*012A8000*".

4.21.5 Ant Fault Sense: DC BITE (Top 270: Low) Test

This test will verify that the fault sensing functionality is within specifications by loading the Top 270 antenna port with out of tolerance resistance.

Step 1. Connect the following resistances to the Top/Bottom Antenna ports:

Antenna Ports	Resistance
Top 0	Nom: 1000 ± 50 Ohms
Top 90	Nom: 2000 ± 50 Ohms
Top 180	Nom: 4020 ± 50 Ohms
Top 270	Low: < 8010 Ohms
Bottom 0	50 ± 5 Ohms
Bottom 90	50 ± 5 Ohms
Bottom 180	50 ± 5 Ohms
Bottom 270	50 ± 5 Ohms

Step 2. Initiate the Antenna DC BITE operation by executing the following HTS command: "*WL P1 88004000 80000000*".

Step 3. Read the the Antenna BITE/Status register by executing the following HTS command: "*RL P1 88004000*".

Step 4. Verify that the returned result is equal to "*00AA8000*".

4.21.6 Ant Fault Sense: DC BITE (Top 0: Low) Test

This test will verify that the fault sensing functionality is within specifications by loading the Top 0 antenna port with out of tolerance resistance.

Step 1. Connect the following resistances to the Top/Bottom Antenna ports:

Antenna Ports	Resistance
Top 0	Low: < 950 Ohms
Top 90	Nom: 2000 ± 50 Ohms
Top 180	Nom: 4020 ± 50 Ohms

Top 270	Nom: 8060 ± 50 Ohms
Bottom 0	50 ± 5 Ohms
Bottom 90	50 ± 5 Ohms
Bottom 180	50 ± 5 Ohms
Bottom 270	50 ± 5 Ohms

Step 2. Initiate the Antenna DC BITE operation by executing the following HTS command: "*WL P1 88004000 80000000*".

Step 3. Read the the Antenna BITE/Status register by executing the following HTS command: "*RL P1 88004000*".

Step 4. Verify that the returned result is equal to "*202A8000*"

4.21.7 Ant Fault Sense: DC BITE (Top 90: High) Test

This test will verify that the fault sensing functionality is within specifications by loading the Top 90 antenna port with out of tolerance resistance.

Step 1. Connect the following resistances to the Top/Bottom Antenna ports:

Antenna Ports	Resistance
Top 0	Nom: 1000 ± 50 Ohms
Top 90	High: > 2050 Ohms
Top 180	Nom: 4020 ± 50 Ohms
Top 270	Nom: 8060 ± 50 Ohms
Bottom 0	50 ± 5 Ohms
Bottom 90	50 ± 5 Ohms
Bottom 180	50 ± 5 Ohms
Bottom 270	50 ± 5 Ohms

Step 2. Initiate the Antenna DC BITE operation by executing the following HTS command: "*WL P1 88004000 80000000*".

Step 3. Read the the Antenna BITE/Status register by executing the following HTS command: "*RL P1 88004000*".

Step 4. Verify that the returned result is equal to "*042A8000*"

4.21.8 Ant Fault Sense: DC BITE (Top 180: Low) Test

This test will verify that the fault sensing functionality is within specifications by loading the Top 180 antenna port with out of tolerance resistance.

Step 1. Connect the following resistances to the Top/Bottom Antenna ports:

Antenna Ports	Resistance
Top 0	Nom: 1000 ± 50 Ohms
Top 90	Nom: 2000 ± 50 Ohms
Top 180	Low: < 3970 Ohms
Top 270	Nom: 8060 ± 50 Ohms
Bottom 0	50 ± 5 Ohms
Bottom 90	50 ± 5 Ohms
Bottom 180	50 ± 5 Ohms

Bottom 270	50 ± 5 Ohms

Step 2. Initiate the Antenna DC BITE operation by executing the following HTS command: "*WL P1 88004000 80000000*".

Step 3. Read the the Antenna BITE/Status register by executing the following HTS command: "*RL P1 88004000*".

Step 4. Verify that the returned result is equal to "*022A8000*".

4.21.9 Ant Fault Sense: DC BITE (Top 270: High) Test

This test will verify that the fault sensing functionality is within specifications by loading the Top 270 antenna port with out of tolerance resistance.

Step 1. Connect the following resistances to the Top/Bottom Antenna ports:

Antenna Ports	Resistance
Top 0	Nom: 1000 ± 50 Ohms
Top 90	Nom: 2000 ± 50 Ohms
Top 180	Nom: 4020 ± 50 Ohms
Top 270	High: > 8110 Ohms
Bottom 0	50 ± 5 Ohms
Bottom 90	50 ± 5 Ohms
Bottom 180	50 ± 5 Ohms
Bottom 270	50 ± 5 Ohms

Step 2. Initiate the Antenna DC BITE operation by executing the following HTS command: "*WL P1 88004000 80000000*".

Step 3. Read the the Antenna BITE/Status register by executing the following HTS command: "*RL P1 88004000*".

Step 4. Verify that the returned result is equal to "*006A8000*".

4.21.10 Ant Fault Sense: DC BITE (Bottom Ports Nom) Test

This test will verify that the fault sensing functionality is within specifications by loading the Bottom antenna ports with nominal resistances.

Step 1. Connect the following resistances to the Top/Bottom Antenna ports:

Antenna Ports	Resistance
Top 0	50 ± 5 Ohms
Top 90	50 ± 5 Ohms
Top 180	50 ± 5 Ohms
Top 270	50 ± 5 Ohms
Bottom 0	Nom: 1000 ± 50 Ohms
Bottom 90	Nom: 2000 ± 50 Ohms
Bottom 180	Nom: 4020 ± 50 Ohms
Bottom 270	Nom: 8060 ± 50 Ohms

Step 2. Initiate the Antenna DC BITE operation by executing the following HTS command: "*WL P1 88004000 80000000*".

Step 3. Read the the Antenna BITE/Status register by executing the following HTS command: "*RL P1 88004000*".

Step 4. Verify that the returned result is equal to "*2A800000*"

4.21.11 Ant Fault Sense: DC BITE (Bottom 0: High) Test

This test will verify that the fault sensing functionality is within specifications by loading the Bottom 0 antenna port with out of tolerance resistance.

Step 1. Connect the following resistances to the Top/Bottom Antenna ports:

Antenna Ports	Resistance
Top 0	50 ± 5 Ohms
Top 90	50 ± 5 Ohms
Top 180	50 ± 5 Ohms
Top 270	50 ± 5 Ohms
Bottom 0	High: > 1050 Ohms
Bottom 90	Nom: 2000 ± 50 Ohms
Bottom 180	Nom: 4020 ± 50 Ohms
Bottom 270	Nom: 8060 ± 50 Ohms

Step 2. Initiate the Antenna DC BITE operation by executing the following HTS command: "*WL P1 88004000 80000000*".

Step 3. Read the the Antenna BITE/Status register by executing the following HTS command: "*RL P1 88004000*".

Step 4. Verify that the returned result is equal to "*2A900000*"

4.21.12 Ant Fault Sense: DC BITE (Bottom 90: Low) Test

This test will verify that the fault sensing functionality is within specifications by loading the Bottom 90 antenna port with out of tolerance resistance.

Step 1. Connect the following resistances to the Top/Bottom Antenna ports:

Antenna Ports	Resistance
Top 0	50 ± 5 Ohms
Top 90	50 ± 5 Ohms
Top 180	50 ± 5 Ohms
Top 270	50 ± 5 Ohms
Bottom 0	Nom: 1000 ± 50 Ohms
Bottom 90	Low: < 1950 Ohms
Bottom 180	Nom: 4020 ± 50 Ohms
Bottom 270	Nom: 8060 ± 50 Ohms

Step 2. Initiate the Antenna DC BITE operation by executing the following HTS command: "*WL P1 88004000 80000000*".

Step 3. Read the the Antenna BITE/Status register by executing the following HTS command: "*RL P1 88004000*".

Step 4. Verify that the returned result is equal to "*2A880000*".

4.21.13 Ant Fault Sense: DC BITE (Bottom 180: High) Test

This test will verify that the fault sensing functionality is within specifications by loading the Bottom 180 antenna port with out of tolerance resistance.

Step 1. Connect the following resistances to the Top/Bottom Antenna ports:

Antenna Ports	Resistance
Top 0	50 ± 5 Ohms
Top 90	50 ± 5 Ohms
Top 180	50 ± 5 Ohms
Top 270	50 ± 5 Ohms
Bottom 0	Nom: 1000 ± 50 Ohms
Bottom 90	Nom: 2000 ± 50 Ohms
Bottom 180	High: > 4070 Ohms
Bottom 270	Nom: 8060 ± 50 Ohms

Step 2. Initiate the Antenna DC BITE operation by executing the following HTS command: "*WL P1 88004000 80000000*".

Step 3. Read the the Antenna BITE/Status register by executing the following HTS command: "*RL P1 88004000*".

Step 4. Verify that the returned result is equal to "*2A810000*".

4.21.14 Ant Fault Sense: DC BITE (Bottom 270: Low) Test

This test will verify that the fault sensing functionality is within specifications by loading the Bottom 270 antenna port with out of tolerance resistance.

Step 1. Connect the following resistances to the Top/Bottom Antenna ports:

Antenna Ports	Resistance
Top 0	50 ± 5 Ohms
Top 90	50 ± 5 Ohms
Top 180	50 ± 5 Ohms
Top 270	50 ± 5 Ohms
Bottom 0	Nom: 1000 ± 50 Ohms
Bottom 90	Nom: 2000 ± 50 Ohms
Bottom 180	Nom: 4020 ± 50 Ohms
Bottom 270	Low: < 8010 Ohms

Step 2. Initiate the Antenna DC BITE operation by executing the following HTS command: "*WL P1 88004000 80000000*".

Step 3. Read the the Antenna BITE/Status register by executing the following HTS command: "*RL P1 88004000*".

Step 4. Verify that the returned result is equal to "*2A808000*".

4.21.15 Ant Fault Sense: DC BITE (Bottom 0: Low) Test

This test will verify that the fault sensing functionality is within specifications by loading Bottom 0 antenna port with out of tolerance resistance.

Step 1. Connect the following resistances to the Top/Bottom Antenna ports:

Antenna Ports	Resistance
Top 0	50 ± 5 Ohms
Top 90	50 ± 5 Ohms
Top 180	50 ± 5 Ohms
Top 270	50 ± 5 Ohms
Bottom 0	Low: < 950 Ohms
Bottom 90	Nom: 2000 ± 50 Ohms
Bottom 180	Nom: 4020 ± 50 Ohms
Bottom 270	Nom: 8060 ± 50 Ohms

Step 2. Initiate the Antenna DC BITE operation by executing the following HTS command: "*WL P1 88004000 80000000*".

Step 3. Read the the Antenna BITE/Status register by executing the following HTS command: "*RL P1 88004000*".

Step 4. Verify that the returned result is equal to "*2AA00000*"

4.21.16 Ant Fault Sense: DC BITE (Bottom 90: High) Test

This test will verify that the fault sensing functionality is within specifications by loading the Bottom 90 antenna port with out of tolerance resistance.

Step 1. Connect the following resistances to the Top/Bottom Antenna ports:

Antenna Ports	Resistance
Top 0	50 ± 5 Ohms
Top 90	50 ± 5 Ohms
Top 180	50 ± 5 Ohms
Top 270	50 ± 5 Ohms
Bottom 0	Nom: 1000 ± 50 Ohms
Bottom 90	High: > 2050 Ohms
Bottom 180	Nom: 4020 ± 50 Ohms
Bottom 270	Nom: 8060 ± 50 Ohms

Step 2. Initiate the Antenna DC BITE operation by executing the following HTS command: "*WL P1 88004000 80000000*".

Step 3. Read the the Antenna BITE/Status register by executing the following HTS command: "*RL P1 88004000*".

Step 4. Verify that the returned result is equal to "*2A840000*"

4.21.17 Ant Fault Sense: DC BITE (Bottom 180: Low) Test

This test will verify that the fault sensing functionality is within specifications by loading the Bottom 180 antenna port with out of tolerance resistance.

Step 1. Connect the following resistances to the Top/Bottom Antenna ports:

Antenna Ports	Resistance
Top 0	50 ± 5 Ohms
Top 90	50 ± 5 Ohms
Top 180	50 ± 5 Ohms
Top 270	50 ± 5 Ohms
Bottom 0	Nom: 1000 ± 50 Ohms
Bottom 90	Nom: 2000 ± 50 Ohms
Bottom 180	Low: < 3970 Ohms
Bottom 270	Nom: 8060 ± 50 Ohms

Step 2. Initiate the Antenna DC BITE operation by executing the following HTS command: "*WL P1 88004000 80000000*".

Step 3. Read the the Antenna BITE/Status register by executing the following HTS command: "*RL P1 88004000*".

Step 4. Verify that the returned result is equal to "*2A820000*".

4.21.18 Ant Fault Sense: DC BITE (Bottom 270: High) Test

This test will verify that the fault sensing functionality is within specifications by loading the Bottom 270 antenna port with out of tolerance resistance.

Step 1. Connect the following resistances to the Top/Bottom Antenna ports:

Antenna Ports	Resistance
Top 0	50 ± 5 Ohms
Top 90	50 ± 5 Ohms
Top 180	50 ± 5 Ohms
Top 270	50 ± 5 Ohms
Bottom 0	Nom: 1000 ± 50 Ohms
Bottom 90	Nom: 2000 ± 50 Ohms
Bottom 180	Nom: 4020 ± 50 Ohms
Bottom 270	High: > 8110 Ohms

Step 2. Initiate the Antenna DC BITE operation by executing the following HTS command: "*WL P1 88004000 80000000*".

Step 3. Read the the Antenna BITE/Status register by executing the following HTS command: "*RL P1 88004000*".

Step 4. Verify that the returned result is equal to "*2A804000*".

4.22 Power Valid Sense Tests

These tests verifiy the Power Valid sense capability of the RX/IO CCA. Odd numbered tests shall start at full power and monitor the power valid bit status as power is reduced 1 dB at a time by invoking whisper-shout steps. Data output shall be the last whisper/shout step invoked which reported valid power. To pass the test, the step number must be greater than or equal to (more attenuation than) 8 dB. Even numbered tests shall start at the 27 dB whisper-shout step and monitor the power valid bit status as power is increased 1 dB at a time. Data output shall be the last whisper/shout step invoked which reported invalid power. To pass the test, the step number must be less than or equal to (less attenuation than) 17 dB..

4.22.1 PV Sense: Top 0 Ant (Min To Max Whisp/Shout Step) Test

This test will generate ATCRBS interrogations out the top 0 antenna port with only the S1 pulse being present. The last whisper-shout step reporting valid power will then be verified.

Step 1. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 2. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitAtcTxWrds1Thru6 (Mode_C, Top)

Step 3. Perform the following algorithm (where Atten = Whisper/Shout Step):

FOR (Atten = 0x0 TO Atten < 0x1C)
{

1. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

   InitAtcTxWrds7Thru10 (Atten, 1, -1, 0, -1, 0, -1, 0, -1, 0, -1, 0, 0)

2. Transmit a single ATCRBS interrogation by executing the following HTS command: "*RFXMIT P1 1*".

3. Read the Transmission Status Word # 1 by executing the following HTS command: "*RL P1 340000*" and swap bytes for Little Endian format

4. If Bit 15 of the result is equal to 0, Exit from this loop. The previous **Atten** value is the last Whisp/Shout Step where power was valid (Bit 15 =1).

5. **Atten** = **Atten** + 1;

}

Step 4. Verify that the last attenuation setting where power was valid is greater than or equal to 8 dB or per the above algorithm (Atten -1 **≥** 8 dB).

4.22.2 PV Sense: Top 0 Ant (Max To Min Whisp/Shout Step) Test

This test will generate ATCRBS interrogations out the top 0 antenna port with only the S1 pulse being present. The last whisper-shout step reporting valid power will then be verified.

Step 1. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 2. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitAtcTxWrds1Thru6 (Mode_C, Top)

Step 3. Perform the following algorithm (where Atten = Whisper/Shout Step):

FOR (Atten = 0x1B TO Atten >= 0x0)
{

1. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

   InitAtcTxWrds7Thru10 (Atten, 1, -1, 0, -1, 0, -1, 0, -1, 0, -1, 0, 0)

2. Transmit a single ATCRBS interrogation by executing the following HTS command: "*RFXMIT P1 1*".

3. Read the Transmission Status Word # 1 by executing the following HTS command: "*RL P1 340000*" and swap bytes for Little Endian format

4. If Bit 15 of the result is equal to 1, Exit from this loop. The **Atten** value is the first Whisp/Shout Step where power becomes valid (Bit 15 =1).

5. **Atten** = **Atten** - 1;

}

Step 4. Verify that the first attenuation setting where power becomes valid was Less than or equal to 17 dB or per the above algorithm (**Atten ≤** 17 dB).

4.22.3 PV Sense: Top 90 Ant (Min To Max Whisp/Shout Step) Test

This test will generate ATCRBS interrogations out the top 90 antenna port with only the S1 pulse being present. The last whisper/shout step reporting valid power will then be verified.

Step 1. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 2. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitAtcTxWrds1Thru6 (Mode_C, Top)

Step 3. Perform the following algorithm (where Atten = Whisper/Shout Step):

FOR (Atten = 0x0 TO Atten < 0x1C)
{

1. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitAtcTxWrds7Thru10 (Atten, 2, -1, 0, -1, 0, -1, 0, -1, 0, -1, 0, 0)

2. Transmit a single ATCRBS interrogation by executing the following HTS command: "*RFXMIT P1 1*".

3. Read the Transmission Status Word # 1 by executing the following HTS command: "*RL P1 340000*" and swap bytes for Little Endian format

4. If Bit 15 of the result is equal to 0, Exit from this loop. The previous **Atten** value is the last Whisp/Shout Step where power was valid (Bit 15 =1).

5. **Atten** = **Atten** + 1;

}

Step 4. Verify that the last attenuation setting where power was valid is greater than or equal to 8 dB or per the above algorithm (Atten -1 **≥** 8 dB).

4.22.4 PV Sense: Top 90 Ant (Max To Min Whisp/Shout Step) Test

This test will generate ATCRBS interrogations out the top 90 antenna port with only the S1 pulse being present. The first whisper/shout step reporting valid power will then be verified.

Step 1. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 2. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitAtcTxWrds1Thru6 (Mode_C, Top)

Step 3. Perform the following algorithm (where Atten = Whisper/Shout Step):

FOR (Atten = 0x1B TO Atten >= 0x0)
{

1. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitAtcTxWrds7Thru10 (Atten, 2, -1, 0, -1, 0, -1, 0, -1, 0, -1, 0, 0)

2. Transmit a single ATCRBS interrogation by executing the following HTS command: "*RFXMIT P1 1*".

3. Read the Transmission Status Word # 1 by executing the following HTS command: "*RL P1 340000*" and swap bytes for Little Endian format

4. If Bit 15 of the result is equal to 1, Exit from this loop. The **Atten** value is the first Whisp/Shout Step where power becomes valid (Bit 15 =1).

5. **Atten** = **Atten** - 1;

}

Step 4. Verify that the first attenuation setting where power becomes valid was Less than or equal to 17 dB or per the above algorithm (Atten **≤** 17 dB).

4.22.5 PV Sense: Top 180 Ant (Min To Max Whisp/Shout Step) Test

This test will generate ATCRBS interrogations out the top 180 antenna port with only the S1 pulse being present. The last whisper/shout step reporting valid power will then be verified.

Step 1. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 2. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitAtcTxWrds1Thru6 (Mode_C, Top)

Step 3. Perform the following algorithm (where Atten = Whisper/Shout Step):

FOR (Atten = 0x0 TO Atten < 0x1C)
{

1. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

   InitAtcTxWrds7Thru10 (Atten, 4, -1, 0, -1, 0, -1, 0, -1, 0, -1, 0, 0)

2. Transmit a single ATCRBS interrogation by executing the following HTS command: "*RFXMIT P1 1*".

3. Read the Transmission Status Word # 1 by executing the following HTS command: "*RL P1 340000*" and swap bytes for Little Endian format

4. If Bit 15 of the result is equal to 0, Exit from this loop. The previous **Atten** value is the last Whisp/Shout Step where power was valid (Bit 15 =1).

5. **Atten** = **Atten** + 1;

}

Step 4. Verify that the last attenuation setting where power was valid is greater than or equal to 8 dB or per the above algorithm (Atten -1 **≥** 8 dB).

4.22.6 PV Sense: Top 180 Ant (Max To Min Whisp/Shout Step) Test

This test will generate ATCRBS interrogations out the top 180 antenna port with only the S1 pulse being present. The first whisper/shout step reporting valid power will then be verified.

Step 1. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 2. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitAtcTxWrds1Thru6 (Mode_C, Top)

Step 3. Perform the following algorithm (where Atten = Whisper/Shout Step):

FOR (Atten = 0x1B TO Atten >= 0x0)

{

1. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

   InitAtcTxWrds7Thru10 (Atten, 4, -1, 0, -1, 0, -1, 0, -1, 0, -1, 0, 0)

2. Transmit a single ATCRBS interrogation by executing the following HTS command: "*RFXMIT P1 1*".

3. Read the Transmission Status Word # 1 by executing the following HTS command: "*RL P1 340000*" and swap bytes for Little Endian format

4. If Bit 15 of the result is equal to 1, Exit from this loop. The **Atten** value is the first Whisp/Shout Step where power becomes valid (Bit 15 =1).

5. **Atten** = **Atten** - 1;

}

Step 4. Verify that the first attenuation setting where power becomes valid was Less than or equal to 17 dB or per the above algorithm (Atten **≤** 17 dB).

4.22.7 PV Sense: Top 270 Ant (Min To Max Whisp/Shout Step) Test

This test will generate ATCRBS interrogations out the top 270 antenna port with only the S1 pulse being present. The last whisper/shout step reporting valid power will then be verified.

Step 1. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 2. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitAtcTxWrds1Thru6 (Mode_C, Top)

Step 3. Perform the following algorithm (where Atten = Whisper/Shout Step):

FOR (Atten = 0x0 TO Atten < 0x1C)

{

1. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

   InitAtcTxWrds7Thru10 (Atten, 8, -1, 0, -1, 0, -1, 0, -1, 0, -1, 0, 0)

2. Transmit a single ATCRBS interrogation by executing the following HTS command: "*RFXMIT P1 1*".

3. Read the Transmission Status Word # 1 by executing the following HTS command: "*RL P1 340000*" and swap bytes for Little Endian format

4. If Bit 15 of the result is equal to 0, Exit from this loop. The previous **Atten** value is the last Whisp/Shout Step where power was valid (Bit 15 =1).

5. **Atten** = **Atten** + 1;

}

Step 4. Verify that the last attenuation setting where power was valid is greater than or equal to 8 dB or per the above algorithm (Atten -1 **≥** 8 dB).

4.22.8 PV Sense: Top 270 Ant (Max To Min Whisp/Shout Step) Test

This test will generate ATCRBS interrogations out the top 270 antenna port with only the S1 pulse being present. The first whisper/shout step reporting valid power will then be verified.

Step 1. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 2. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitAtcTxWrds1Thru6 (Mode_C, Top)

Step 3. Perform the following algorithm (where Atten = Whisper/Shout Step):

FOR (Atten = 0x1B TO Atten >= 0x0)
{

1. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

   InitAtcTxWrds7Thru10 (Atten, 8, -1, 0, -1, 0, -1, 0, -1, 0, -1, 0, 0)

2. Transmit a single ATCRBS interrogation by executing the following HTS command: "*RFXMIT P1 1*".

3. Read the Transmission Status Word # 1 by executing the following HTS command: "*RL P1 340000*" and swap bytes for Little Endian format

4. If Bit 15 of the result is equal to 1, Exit from this loop. The **Atten** value is the first Whisp/Shout Step where power becomes valid (Bit 15 =1).

5. **Atten** = **Atten** - 1;

}

Step 4. Verify that the first attenuation setting where power becomes valid was Less than or equal to 17 dB or per the above algorithm (Atten **≤** 17 dB).

4.22.9 PV Sense: Bottom 0 Ant (Min To Max Whisp/Shout Step) Test

This test will generate ATCRBS interrogations out the bottom 0 antenna port with only the S1 pulse being present. The last whisper-shout step reporting valid power will then be verified.

Step 1. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 2. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitAtcTxWrds1Thru6 (Mode_C, Bot)

Step 3. Perform the following algorithm (where Atten = Whisper/Shout Step):

FOR (Atten = 0x0 TO Atten < 0x1C)
{

1. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

   InitAtcTxWrds7Thru10 (Atten, 1, -1, 0, -1, 0, -1, 0, -1, 0, -1, 0, 0)

2. Transmit a single ATCRBS interrogation by executing the following HTS command: "*RFXMIT P1 1*".

3. Read the Transmission Status Word # 1 by executing the following HTS command: "*RL P1 340000*" and swap bytes for Little Endian format

4. If Bit 15 of the result is equal to 0, Exit from this loop. The previous **Atten** value is the last Whisp/Shout Step where power was valid (Bit 15 =1).

5. **Atten** = **Atten** + 1;

}

Step 4. Verify that the last attenuation setting where power was valid is greater than or equal to 8 dB or per the above algorithm (Atten -1 **≥** 8 dB).

4.22.10 PV Sense: Bottom 0 Ant (Max To Min Whisp/Shout Step) Test

This test will generate ATCRBS interrogations out the bottom 0 antenna port with only the S1 pulse being present. The last whisper-shout step reporting valid power will then be verified.

Step 1. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 2. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitAtcTxWrds1Thru6 (Mode_C, Bot)

Step 3. Perform the following algorithm (where Atten = Whisper/Shout Step):

FOR (Atten = 0x1B TO Atten >= 0x0)
{

1. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

   InitAtcTxWrds7Thru10 (Atten, 1, -1, 0, -1, 0, -1, 0, -1, 0, -1, 0, 0)

2. Transmit a single ATCRBS interrogation by executing the following HTS command: "*RFXMIT P1 1*".

3. Read the Transmission Status Word # 1 by executing the following HTS command: "*RL P1 340000*" and swap bytes for Little Endian format

4. If Bit 15 of the result is equal to 1, Exit from this loop. The **Atten** value is the first Whisp/Shout Step where power becomes valid (Bit 15 =1).

5. **Atten** = **Atten** - 1;

}

Step 4. Verify that the first attenuation setting where power becomes valid was Less than or equal to 17 dB or per the above algorithm (**Atten ≤** 17 dB).

4.22.11 PV Sense: Bottom 90 Ant (Min To Max Whisp/Shout Step) Test

This test will generate ATCRBS interrogations out the bottom 90 antenna port with only the S1 pulse being present. The last whisper/shout step reporting valid power will then be verified.

Step 1. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 2. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitAtcTxWrds1Thru6 (Mode_C, Bot)

Step 3. Perform the following algorithm (where Atten = Whisper/Shout Step):

FOR (Atten = 0x0 TO Atten < 0x1C)
{

1. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

   InitAtcTxWrds7Thru10 (Atten, 2, -1, 0, -1, 0, -1, 0, -1, 0, -1, 0, 0)

2. Transmit a single ATCRBS interrogation by executing the following HTS command: "*RFXMIT P1 1*".

3. Read the Transmission Status Word # 1 by executing the following HTS command: "*RL P1 340000*" and swap bytes for Little Endian format

4. If Bit 15 of the result is equal to 0, Exit from this loop. The previous **Atten** value is the last Whisp/Shout Step where power was valid (Bit 15 =1).

5. **Atten** = **Atten** + 1;

}

Step 4. Verify that the last attenuation setting where power was valid is greater than or equal to 8 dB or per the above algorithm (Atten -1 **≥** 8 dB).

4.22.12 PV Sense: Bottom 90 Ant (Max To Min Whisp/Shout Step) Test

This test will generate ATCRBS interrogations out the bottom 90 antenna port with only the S1 pulse being present. The first whisper/shout step reporting valid power will then be verified.

Step 1. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 2. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitAtcTxWrds1Thru6 (Mode_C, Bot)

Step 3. Perform the following algorithm (where Atten = Whisper/Shout Step):

FOR (Atten = 0x1B TO Atten >= 0x0)
{

1. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

   InitAtcTxWrds7Thru10 (Atten, 2, -1, 0, -1, 0, -1, 0, -1, 0, -1, 0, 0)

2. Transmit a single ATCRBS interrogation by executing the following HTS command: "*RFXMIT P1 1*".

3. Read the Transmission Status Word # 1 by executing the following HTS command: "*RL P1 340000*" and swap bytes for Little Endian format

4. If Bit 15 of the result is equal to 1, Exit from this loop. The **Atten** value is the first Whisp/Shout Step where power becomes valid (Bit 15 =1).

5. **Atten** = **Atten** - 1;

}

Step 4. Verify that the first attenuation setting where power becomes valid was Less than or equal to 17 dB or per the above algorithm (Atten **≤** 17 dB).

4.22.13 PV Sense: Bottom 180 Ant (Min To Max Whisp/Shout Step) Test

This test will generate ATCRBS interrogations out the bottom 180 antenna port with only the S1 pulse being present. The last whisper/shout step reporting valid power will then be verified.

Step 1. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 2. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitAtcTxWrds1Thru6 (Mode_C, Bot)

Step 3. Perform the following algorithm (where Atten = Whisper/Shout Step):

FOR (Atten = 0x0 TO Atten < 0x1C)
{

1. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitAtcTxWrds7Thru10 (Atten, 4, -1, 0, -1, 0, -1, 0, -1, 0, -1, 0, 0)

2. Transmit a single ATCRBS interrogation by executing the following HTS command: "*RFXMIT P1 1*".

3. Read the Transmission Status Word # 1 by executing the following HTS command: "*RL P1 340000*" and swap bytes for Little Endian format

4. If Bit 15 of the result is equal to 0, Exit from this loop. The previous **Atten** value is the last Whisp/Shout Step where power was valid (Bit 15 =1).

5. **Atten** = **Atten** + 1;

}

Step 4. Verify that the last attenuation setting where power was valid is greater than or equal to 8 dB or per the above algorithm (Atten -1 **≥** 8 dB).

4.22.14 PV Sense: Bottom 180 Ant (Max To Min Whisp/Shout Step) Test

This test will generate ATCRBS interrogations out the bottom 180 antenna port with only the S1 pulse being present. The first whisper/shout step reporting valid power will then be verified.

Step 1. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 2. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitAtcTxWrds1Thru6 (Mode_C, Bot)

Step 3. Perform the following algorithm (where Atten = Whisper/Shout Step):

FOR (Atten = 0x1B TO Atten >= 0x0)
{

1. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitAtcTxWrds7Thru10 (Atten, 4, -1, 0, -1, 0, -1, 0, -1, 0, -1, 0, 0)

2. Transmit a single ATCRBS interrogation by executing the following HTS command: "*RFXMIT P1 1*".

3. Read the Transmission Status Word # 1 by executing the following HTS command: "*RL P1 340000*" and swap bytes for Little Endian format

4. If Bit 15 of the result is equal to 1, Exit from this loop. The **Atten** value is the first Whisp/Shout Step where power becomes valid (Bit 15 =1).

5. **Atten** = **Atten** - 1;

}

Step 4. Verify that the first attenuation setting where power becomes valid was Less than or equal to 17 dB or per the above algorithm (Atten **≤** 17 dB).

4.22.15 PV Sense: Bottom 270 Ant (Min To Max Whisp/Shout Step) Test

This test will generate ATCRBS interrogations out the bottom 270 antenna port with only the S1 pulse being present. The last whisper/shout step reporting valid power will then be verified.

Step 1. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 2. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitAtcTxWrds1Thru6 (Mode_C, Bot)

Step 3. Perform the following algorithm (where Atten = Whisper/Shout Step):

FOR (Atten = 0x0 TO Atten < 0x1C)
{

1. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

   InitAtcTxWrds7Thru10 (Atten, 8, -1, 0, -1, 0, -1, 0, -1, 0, -1, 0, 0)

2. Transmit a single ATCRBS interrogation by executing the following HTS command: "*RFXMIT P1 1*".

3. Read the Transmission Status Word # 1 by executing the following HTS command: "*RL P1 340000*" and swap bytes for Little Endian format

4. If Bit 15 of the result is equal to 0, Exit from this loop. The previous **Atten** value is the last Whisp/Shout Step where power was valid (Bit 15 =1).

5. **Atten** = **Atten** + 1;

}

Step 4. Verify that the last attenuation setting where power was valid is greater than or equal to 8 dB or per the above algorithm (Atten -1 **≥** 8 dB).

4.22.16 PV Sense: Bottom 270 Ant (Max To Min Whisp/Shout Step) Test

This test will generate ATCRBS interrogations out the bottom 270 antenna port with only the S1 pulse being present. The first whisper/shout step reporting valid power will then be verified.

Step 1. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for the description of this macro instruction.

Step 2. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitAtcTxWrds1Thru6 (Mode_C, Bot)

Step 3. Perform the following algorithm (where Atten = Whisper/Shout Step):

FOR (Atten = 0x1B TO Atten >= 0x0)
{

1. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

   InitAtcTxWrds7Thru10 (Atten, 8, -1, 0, -1, 0, -1, 0, -1, 0, -1, 0, 0)

2. Transmit a single ATCRBS interrogation by executing the following HTS command: "*RFXMIT P1 1*".

3. Read the Transmission Status Word # 1 by executing the following HTS command: "*RL P1 340000*" and swap bytes for Little Endian format

4. If Bit 15 of the result is equal to 1, Exit from this loop. The **Atten** value is the first Whisp/Shout Step where power becomes valid (Bit 15 =1).

5. **Atten** = **Atten** - 1;

}

Step 4. Verify that the first attenuation setting where power becomes valid was Less than or equal to 17 dB or per the above algorithm (Atten **≤** 17 dB).

4.23 PIN Diode Monitor Tests

These tests verify that the Whisper/Shout PIN diode open/short monitor is functioning. The PIN diode monitor is tested at each whisper/shout step from step 0 through step 27. These tests are performed on the top 0 degree antenna port.

4.23.1 PIN Diode Monitor (Whisp/Shout Steps 0 dB To 27 dB) Test

Step 1. Initialize the UUT RF FPGA registers by executing the following macro instruction: **InitRegisters ( )**. See Appendix D for description of this macro instruction.

Step 2. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitAtcTxWrds1Thru6 (Mode_C, Top)

Step 3. Perform the following algorithm (where Atten = Whisper/Shout Step):

FOR (Atten = 0x0 TO Atten < 0x1C)
{

1. Initialize Word #4 of the Xmit queue for PIN Diode SelfTest Enable and positive/negative slope value by executing the following HTS command: *"WL P1 30000C 15020000*"

2. Setup the UUT to generate a single whisper/shout interrogation by executing the following macro instruction. See Appendix D for the description of this macro instruction.

InitAtcTxWrds7Thru10 (Atten, 1, Atten, 1, Atten, 1, Atten, 1, Atten, 1, Atten, 1, 0)

3. Transmit a single ATCRBS interrogation by executing the following HTS command: "*RFXMIT P1 1*".

4. Read the Transmission Status Word # 1 by executing the following HTS command: "*RL P1 340000*" and swap bytes for Little Endian format

5. Verify that Bit 10 = 0 and Bit 11 = 0 for each iteration of this loop.

6. **Atten** = **Atten** + 1;

}

Step 4. Verify that for all 28 iterations (Whisp/Shout Step 0 -27), Bits 10 & 11 of Transmission Status Word # 1 were equal to 0.

4.24 Data Log Tests

4.24.1 Maintenance Log Tests

This test will verify that the Maintenance Log Flash can be written to and read from.

Note: If this test is performed, all calibration data will be ERASED. Automating this test will require saving the calibration data in a different location and then restoring the data at the conclusion of this test.

Step 1. Execute the HTS command "*MLTST P1*" to begin read/write testing of the maintenance log. This test may take up to 30 seconds.

Step 2. Verify that the returned result is "PASS"

Step 3. Erase the test data that was left in the Maintenance log flash by executing the HTS command "*MLCLR P1*"

Step 4. Verify that the returned result is "PASS"

4.24.2 Event Log Tests

This test will verify that the Event Log Flash can be written to and read from.

Step 1. Execute the HTS command "*ELTST P1*" to begin read/write testing of the event log. This test may take up to 30 seconds.

Step 2. Verify that the returned result is "PASS"

Step 3. Erase the test data that was left in the Event Log Flash by executing the HTS command "*ELCLR P1*"

Step 4. Verify that the returned result is "PASS"

4.25 UUT Test Software/Firmware Configuration Tests

4.25.1 CPLD Part Number Test

Step 1. Read back the CPLD dash number by executing the HTS command "*RBL P1 7FC00010 7FC0001C*". Concatenate the dash number to the CPLD part number prefix.

Step 2. Verify that it matches the part number and dash of the CPLD that was installed in the UUT.

4.25.2 Hardware Configuration Software Part Number Test

Step 1. Read back the Hardware Configuration Software part number by executing the HTS command "*RBL P1 7FF80FC0 7FF80FD0*". The returned data will be in hex so it must be converted to ASCII characters.

Step 2. Verify that it matches the part number of the Hardware Configuration Software that was loaded into the UUT.

4.25.3 Hardware Configuration Software Image CRC Test

Step 1. Read the embedded Hardware Configuration Software CRC by executing the HTS command "*RL P1 7FF80FFC".* Log this result.

Step 2. Compute the Hardware Configuration Software CRC by executing the HTS command "*CRC P1 7FF80060 7FF80FFB".*

Step 3. Verify that the computed result returned in Step 2 matches the embedded result returned in Step 1.

4.25.4 HTS Software Part Number Test

Step 1. Read back the HTS software part number by executing the HTS command "*RBL P1 7F000010 7F00001C*". The returned data will be in hex so it must be converted to ASCII characters.

Step 2. Verify that it matches the part number of the HTS software that was loaded into the UUT.

4.25.5 HTS Image CRC Test

Step 1. Read the embedded HTS Image CRC by executing the HTS command "*RL P1 7F0000F8".* Log this result.

Step 2. Compute the HTS Image CRC by executing the HTS command "*CRC P1 7F000100 7F1FFFFF".*

Step 3. Verify that the computed result returned in Step 2 matches the embedded result returned in Step 1.

4.25.6 Boot Software Part Number Test

Step 1. Read back the Boot software part number by executing the HTS command "*RBL P1 7FF00010 7FF0001C*". The returned data will be in hex so it must be converted to ASCII characters.

Step 2. Verify that it matches the part number of the Boot software that was loaded into the UUT.

4.25.7 Boot Image CRC Test

Step 1. Read the embedded Boot Image CRC by executing the HTS command "*RL P1 7FF000F8".* Log this result.

Step 2. Compute the Boot Image CRC by executing the HTS command "*CRC P1 7FF00100 7FF7FFFF".*

Step 3. Verify that the computed result returned in Step 2 matches the embedded result returned in Step 1.

4.25.8 Data Loader Software Part Number Test

Step 1. Read back the Data Loader software part number by executing the HTS command "*RBL P1 7F700010 7F70001C*". The returned data will be in hex so it must be converted to ASCII characters.

Step 2. Verify that it matches the part number of the Data Loader software that was loaded into the UUT.

4.25.9 Data Loader Software Image CRC Test

Step 1. Read the embedded Data Loader software image CRC by executing the HTS command "*RL P1 7F7000F8".* Log this result.

Step 2. Read the embedded Data Loader software image length by executing the HTS command "*RL P1 7F7000F4"* and assign this value to a 32 bit integer defined as **ImageLen.**

Step 3. Compute the end address of the image by performing the following assignment: **EndAddr** = 0x7F700100 + **ImageLen** -1.

Step 4. Convert **EndAddr** to the 8 character equivalent of it's long integer representation.

Step 5. Compute the Data Loader Image CRC by executing the HTS command "*CRC P1* 7F700100 ***EndAddr****".*

Step 6. Verify that the computed result returned in Step 5 matches the embedded result returned in Step 1.

4.25.10 I/O FPGA Part Number Test

Step 1. Read back the I/O FPGA part number by executing the HTS command "*RBL P1 7FD00010 7FD0001C*". The returned data will be in hex so it must be converted to ASCII characters.

Step 2. Verify that it matches the part number of the I/O FPGA that was installed and programmed in the UUT.

4.25.11 I/O FPGA Image CRC Test

Step 1. Read the embedded I/O FPGA Image CRC by executing the HTS command "*RL P1 RL P1 7FD000F8".* Log this result.

Step 2. Compute the I/O FPGA Image CRC by executing the HTS command "*CRC P1 7FD00100 7FD626F7".*

Step 3. Verify that the computed result returned in Step 2 matches the embedded result returned in Step 1.

4.25.12 I/O FPGA Read-Back CRC Test

This test will command the CPLD to perform an internal CRC of the programmed I/O FPGA and then the HTS will verify that the CPLD result matches the embedded I/O FPGA read-back CRC value.

Step 1. Executing the HTS command "*FPGACRC P1 0 0*".

Step 2. Verify that the returned result is "Ok"

4.25.13 RF FPGA Part Number Test

Step 1. Read back the RF FPGA part number by executing the HTS command "*RBL P1 7FC00010 7FC0001C*". The returned data will be in hex so it must be converted to ASCII characters.

Step 2. Verify that it matches the part number of the RF FPGA that was installed and programmed in the UUT.

4.25.14 RF FPGA Image CRC Test

Step 1. Read the embedded RF FPGA Image CRC by executing the HTS command "*RL P1 RL P1 7FC000F8".* Log this result.

Step 2. Compute the RF FPGA Image CRC by executing the HTS command "*CRC P1 7FC00100 7FC626F7".*

Step 3. Verify that the computed result returned in Step 2 matches the embedded result returned in Step 1.

4.25.15 RF FPGA Read-Back CRC Test

This test will command the CPLD to perform an internal CRC of the programmed RF FPGA and then the HTS will verify that the CPLD result matches the embedded RF FPGA read-back CRC value.

Step 1. Executing the HTS command "*FPGACRC P1 1 0*".

Step 2. Verify that the returned result is "Ok"

4.25.16 UUT Part Number Test

The UUT Part Number that will be programmed into the UUT must be comprised of 32 bytes or a total of 64 Hex digits Program the UUT part number into the Maintenance Log using the following algorithm:

Step 1. Convert each ASCII character of the 13 character UUT Part Number into a two digit Hex equivalent. The part number must be left justified so pad the remainder of the 32 byte total with Hex zeros. As an example, for a UUT part number of "9003000-55001", the converted string including the zero's padding should appear as follows:

"393030333030302D353530303130303030303030303030303030303030303030"

Step 2. Perform the following loop algorithm to load the converted part number string into the UUT.

For (Addr = FF401000 TO Addr = FF40101C)
{
Execute HTS command "*WCAL P1 Addr Data*"

Where 'Data' is 8 characters from the converted part number string starting from the left most character and incrementing by 8 characters for each new address.

Addr = Addr + 4
}

Step 3. Read back the part number by executing the HTS command "*RBL P1 FF401000 FF40101C*" and verify that it matches the data that was programmed in.

4.25.17 UUT Serial Number Test

The UUT serial number that will be programmed into the UUT must be comprised of 32 bytes or a total of 64 Hex digits Program the UUT serial number into the Maintenance Log using the following algorithm:

Step 1. Convert each ASCII character of the 8 character UUT serial number into a two digit Hex equivalent. The serial number must be left justified so pad the remainder of the 32 byte total with Hex zeros. As an example, for a UUT serial number of "12345678", the converted string including the zero's padding should appear as follows:

"31323334353637383030303030303030303030303030303030303030303030303030"

Step 2. Perform the following loop algorithm to load the converted part number string into the UUT.

For (Addr = FF401020 TO Addr = FF40103C)
{
Execute HTS command "*WCAL P1 Addr Data*"

Where 'Data' is 8 characters from the converted serial number string starting from left most character and incrementing by 8 characters for each new address.

Addr = Addr + 4
}

Step 3. Read back the serial number by executing the HTS command "*RBL P1 FF401020 FF40103C*" and verify that it matches the data that was programmed in.

4.25.18 UUT Hardware Mod Letter Test

The UUT hardware mod letter that will be programmed into the UUT must be comprised of 32 bytes or a total of 64 Hex digits Program the UUT hardware mod letter into the Maintenance Log using the following algorithm:

Step 1. Convert each ASCII character of the UUT hardware mod letter into a two digit Hex equivalent. The hardware mod letter must be left justified so pad the remainder of

the 32 byte total with Hex zeros. As an example, for a UUT hardware mod letter of "A", the converted string including the zero's padding should appear as follows:

"413030303030303030303030303030303030303030303030303030303030303030"

Step 2. Perform the following loop algorithm to load the converted hardware mod letter into the UUT.

```
For (Addr = FF401040  TO   Addr  =  FF40105C)
 {
       Execute HTS command   "WCAL P1 Addr  Data"

       Where 'Data' is 8 characters  from the converted hardware mod letter string
       starting from the left most character and incrementing by 8 characters for each
       new address.

       Addr = Addr + 4
}
```

Step 3. Read back the hardware mod letter by executing the HTS command "*RBL P1 FF401040 FF40105C*" and verify that it matches the data that was programmed in.

4.25.19 UUT Calibration Data Dump Test

Step 1. Dump the UUT calibration data from the maintenance log by executing the HTS command "*RBL P1 FF400000 FF4003FC*".

Step 2. Verify that the cal data is not all F's .

4.25.20 Loading And Verification Of Operational Flight Software

Step 1. Remove input power from the UUT.

Step 2. Assert the Air/Ground discrete by applying a ground to UUT pin RMP-5K.

Step 3. Insert the compact flash card that contains the operational flight software that is required for the UUT and Re-apply power to the UUT.

Step 4. The 'XFER IN PROCESS' LED should begin to flash green approx. 5 - 15 seconds after power is applied.

Step 5. The 'XFER IN PROCESS' LED should stop flashing (after 1-3 min) and be illuminated a steady green as files are being loaded into the UUT.

Step 6. When all files have been loaded (3-10 min), the 'XFER IN PROCESS' LED will turn off and the 'C/F LOAD STATUS' LED will be a steady green (no flashing).

Step 7. Use the WebEDDIT software tool or the MTS test program with integrated WebEDDIT to verify that all files were loaded correctly.

APPENDIX A

TCAS 3000 SOFTWARE/FIRMWARE LOADING PROCEDURE

1 INTRODUCTION

The TCAS 3000 FLASH memory must be loaded with several images prior to an application being able to execute. This procedure uses the T3000 Multi-Core Single Scan Chain VisionClick with emulator to load the required images.

1.1 Emulator Initialization

Step 1. Insert the processor card to be programmed into the CPA Test Fixture.

Step 2. Jumper the HBM_disable at J9-1 to 2 in order for the emulator to erase flash.

Step 3. Connect emulator cable (cable labeled with powerpc dual-in-line connector) to P1 using a JTAG Test Adapter.

Step 4. Power-up the emulator (switch is on the rear). There should be a green light (power) on the front of the emulator box when the emulator is ready.

Step 5. Apply power to the CPA Test Fixture and press red RESET button on test fixture.

Step 6. Invoke VisionClick (7.11) from the start menu or desktop shortcut to start up an emulator connection to the first processor (P1).

Step 7. Close the "Welcome To visionCLICK" window.

Step 8. Click on the "Open Download/Project Dialog" menu bar button (yellow folder at far left). This will bring up the "PROJECTS/LOAD" Dialog window.

Step 9. In the "PROJECTS/Dialog" window, click on the "T3000_P1_Blue_Emulator.prj" project.

Step 10. In the "PROJECTS/Dialog" window, click on the "Activate" menu button on the bottom. This should cause the "Active Project" text for the project that you selected to turn red.

Step 11. In the "PROJECTS/Dialog" window, click on the "OK" button until the PROJECTS/LOAD" Dialog window disappears. This may take several clicks if you do it before visionClick has completed the activation of the project.

Step 12. Enter "rst" at the "BKM" prompt of the "Terminal" window, then click on the "Reset Target and Emulator" menu bar button (blue crooked arrow to the right of the button that looks like a stop sign). At this point you should have a "BKM" prompt in the "Terminal" window and there should be a checkmark by the PCI register group within the "Registers" window.

1.2 Flash Programming

Step 1. See Appendix A of the Acceptance Test Procedure For TCAS 3000 (8002217-001) to obtain the Master Media P/N(s) of the image(s) to be loaded onto the TCAS3000 processor card. Since the emulator will be used to program Flash, the Master Media P/N(s) should specify that the image(s) reside on a CD.

Step 2. Enter "rst" at the "BKM" prompt of the "Terminal" window of any instance of visionClick that you have connected to P1.

Step 3. Click on the "Open Flash Programming Window" menu bar button (black and blue flash chip at the middle of the menu bar). This will bring up the "TF FLASH PROGRAMMING" window.

Step 4. Depending upon which software/firmware requires to be loaded, enter the Start Address, End Address, and Bias in the "TF FLASH PROGRAMMING" window as follows:

Image	Start Address	End Address	Bias
Boot	0x7FF00000	0x7FF7FFFF	0x00000000
Data Loader IMAGE 1	0x7F700000	0x7F97FFFF	0x7F700000
Data Loader IMAGE 2	0x7F980000	0x7FBFFFFF	0x7F980000
I/O FPGA IMAGE 1	0x7FD00000	0x7FDFFFFF	0x7FD00000
I/O FPGA IMAGE 2	0x7FE00000	0x7FEFFFFF	0x7FE00000
RF FPGA	0x7FC00000	0x7FCFFFFF	0x7FC00000
HTS	0x7F000000	0x7F1FFFFF	0x00000000
Hardware Info	0x7FF80000	0x7FFBFFFF	0x00000000

Step 5. Set the Programming Algorithm in the "TF FLASH PROGRAMMING" window to AMD 29LV128MH&L (8192 x 16) 4 DEVICES if it is not already set to this algorithm.

Step 6. Click on the "Erase and Program" button at the bottom of the "TF FLASH PROGRAMMING" window. A status window should pop up showing the status of the programming. When it is finished (100%), click on the "OK" button.

Step 7. Click on the "OK" button on the "TF FLASH PROGRAMMING" window.

Step 8. Enter "rst" at the "BKM" prompt of the "Terminal" window of any instance of visionClick that you have connected to P1.

Step 9. After the download is complete, remove power from the UUT.

APPENDIX B

TCAS 3000 MANUAL ALIGNMENT PROCEDURE

1 INTRODUCTION

Alignment and calibration of the TCAS 3000 Receiver and Transmitter is accomplished both at the module level (prior to installation in an End Item) and at the End Item level. Calibration at the module level allows easier access to soldering test select resistors and copper foil. Calibration at the End Item level allows the storage of calibration constants in the FLASH memory of the processor CCA.

The procedure described in this Appendix is to be performed at the module level. In order to perform an end item level calibration as described in Appendix C, the UUT must be assembled into an end item with software loaded per Appendix A.

NOTE: Do not attempt to transmit interrogations until after the RF alignment procedures in para. 3.2 (transmitter peak power and rise time adjustments) or para. 4. (transmitter spectrum filter alignment) have been performed to avoid possible transmitter damage.

~~The parameters in EEPROM have an error detection means, so as to detect data loss. A loss of calibration data could result in invalid TCAS operation.~~

2 MANUAL RECEIVER MODULE ALIGNMENT

The CCA dash number on which a reference designator is pertinent is typically included in the instructions unless the reference designator is a connector or plug. These are anticipated to remain the same across all new dash numbers of an assembly. If the specific dash number (of the assembly being tuned) is not reference it is permissible to cross-reference between assemblies of the same base number and identify the appropriate component.

2.1 Oscillator Frequency Adjustment

2.1.1 Overview

This step sets the oscillator frequency by adjusting a potentiometer screw on the Receiver CCA while transmitting full power. The screw is accessed through the edge of the cover over the oscillator. The potentiometer is A5R612 on a 7517945-904 or 7517945-905. A clockwise rotation of the screw will decrease the frequency of the unit. This step may also be performed at other stages of this procedure as well as during the final End Item calibration in Appendix C.

2.1.2 Setup

1. Connect the Power Supply and Transmitter Pair to the TCAS 3000 Power Supply Test Fixture as shown in Figure B-007.
2. The cable and padding loss needs to be accounted for in the measurements of the peak power meter. See the operating instructions of the power meter used for instructions.
3. Set the source power supply to 28 ±3 VDC or 115 ±6 VAC at 400 ±10Hz. (Note: the power supply will not function from 115VAC 400Hz unless a transformer such as 9000470-001 is installed to J1 of the 9003030-002)
4. Connect the 40dB pad to the RF input of the Spectrum Analyzer.
5. Select the following Spectrum Analyzer Settings:

- VBW = 3 kHz
- RBW = 1kHz
- Span 100 kHz
- Sweep = 50ms
- 10dB/div
- Ref = 0 dBm
- Atten = 10 dB
- Set the max hold function on

6. Turn on the TCAS 3000 Power Supply Test Fixture 'fixture power' switch.
7. Set the rotary switch on the TCAS 3000 Power Supply Test Fixture in the 'Bypass Trans Disable (RF off)' position.
8. Set the Receiver Transmit Path switches on the TCAS 3000 Power Supply Test Fixture to 0 degrees top.
9. Apply power to the Power Supply using the UUT 115VAC or 28VDC switch on the TCAS 3000 Power Supply Test Fixture, as appropriate.
10. Apply 50ohm 5W loads to the 0 degree Bottom, and the remaining Top ports. Un-terminated (minimum 5W) pads with a minimum attenuation of 10dB may be used.
11. Set the rotary switch on the TCAS 3000 Power Supply Test Fixture to the 'TX Long Pulses' position. This transmits a long (~31.5uS) pulse at a 50 pulse per second rate.
12. Allow the UUT to transmit enough pulses that the spectrum display becomes smooth. Identify the peak of the spectrum by performing a peak search on the spectrum analyzer. The peak **shall** be within 1030 ± 1kHz.
13. If the peak is not within the specified range, adjust A5R612. Refresh the spectrum analyzer display and wait until the spectrum on the display is smooth again and ID the new spectrum peak. Repeat this process until the oscillator frequency is within the specified range. Connect the 53 pin circular connector to the ARINC 615 front panel PDL connector, and apply power to the unit per figure B-1A.

~~2.9~~2.2 Receiver IF Filter Calibration

2.2.1 Overview

Calibration comprises pulse scaling, a filter alignment step, and a check of the self-test function.

The pulse-scaling alignment is used to set the gain that accumulates in each channel's chain of mixers, amplifiers and filters. Though pulses can be routed through either the wide or the narrow filters the pulse-scaling procedure does not use the route through the narrow-band filter, which is assumed to have a satisfactory characteristic when it meets its alignment requirements.

In the filter alignment step, each channel's frequency response, both through the wide-band and narrow-band routes, is fine-tuned within its pass band.

NOTE: Generally, wide-band receiver pulse performance measurements should precede filter alignment because initial receiver performance or degradation is easier to troubleshoot during pulse testing. Alignment (fine tuning) of the wide-band filters should not affect the wide-band pulse performance characteristics. However, if the band-pass characteristics are not normal because of component failures, or because of technician preference, filter band-pass tuning can be done initially, followed by the pulse performance measurements.

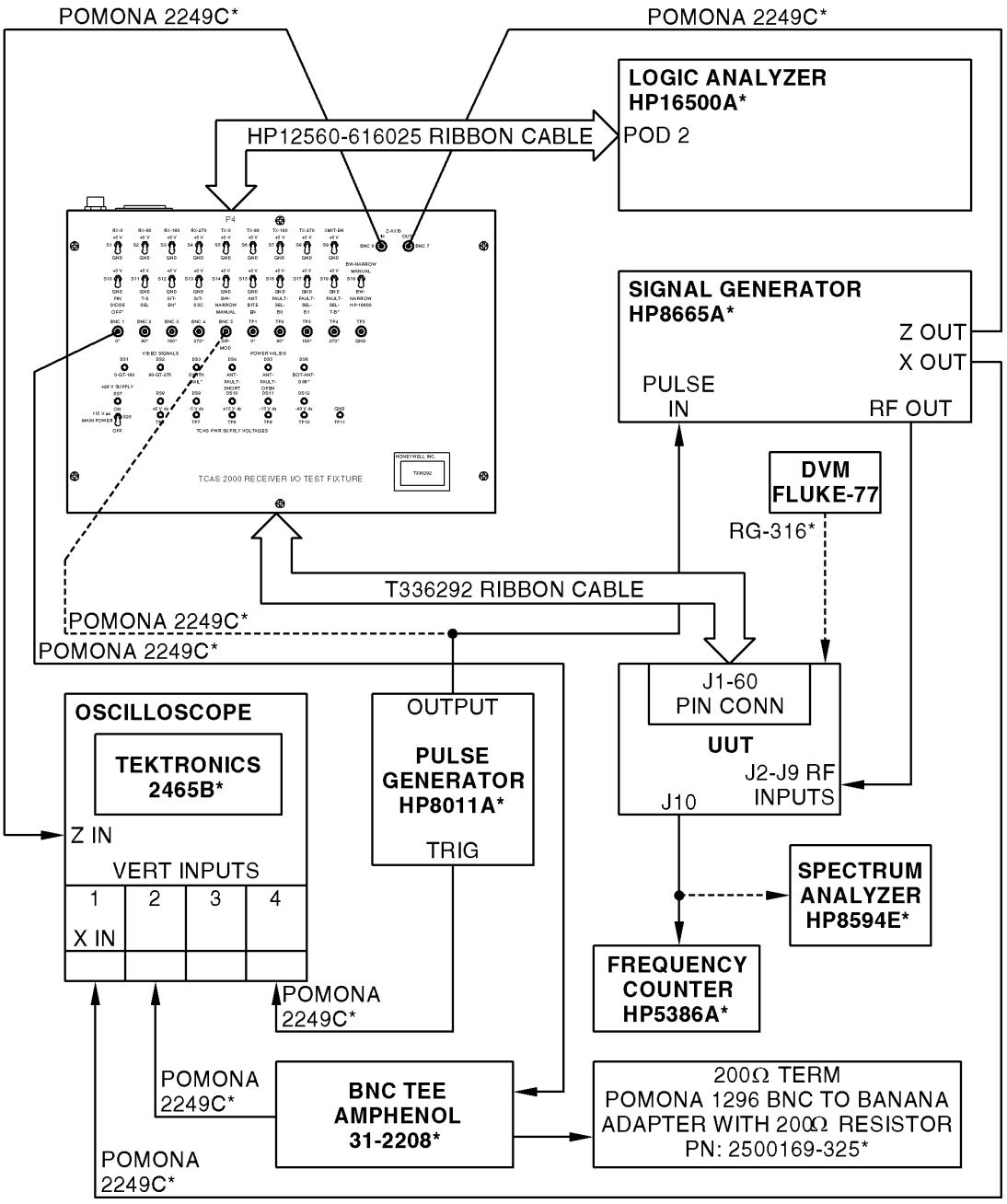
Self Test Amplitude alignment verifies the basic functional operation of the on-board 60 MHz source, modulation mixer, the splitter, and the directional couplers. This alignment step is optional as it is normally addressed at the unit level, and is intended to provide a method of calibration of the self-test function which is only required if PWB variations cause this function to be inconsistent.

Primary reference designators apply to 7517945-903. Reference designators inside parenthesis apply to 7517945-904 and 7517945-905.

2.2.2 Receiver IF Filter Alignment Test Equipment Setup

The receiver IF filter calibration is performed at the module level. The baseline test equipment setup is shown in Figure B-001 below:

1. Remove receiver covers if alignment is to be performed.
2. Make sure S20, MAIN POWER switch on the test fixture is in the OFF position.
3. Connect the J1 of the test fixture to J1 of the receiver. Carefully align the pins while mating the connector, noting the polarization pin orientation.
4. Set up the test equipment as shown in Figure B-001, except do not connect the cable between the T336292 Test Fixture Z-AXIS IN, BNC6, and the Oscilloscope Z-IN connection.
5. Set all test fixture switches as shown in Table B-001. Suggested test equipment settings are shown in Table B-001, which may be altered by the technician preference as experience is gained.



* Or equivalent

NOTE:
DVM used only for troubleshooting.

Figure B-001. Block Diagram for Receiver Test Set-up

Table B-001. Test Fixture and Test Equipment Settings

T336292 Test Fixture Settings	S1 (RX-0° *)	GND
	S2 (RX-90° *)	GND
	S3 (RX-180° *)	GND
	S4 (RX-270° *)	GND
	S5 (TX-0° *)	+5V
	S6 (TX-90° *)	+5V
	S7 (TX-180° *)	+5V
	S8 (TX-270° *)	+5V
	S9 (XMIT-EN*)	+5V
	S10 (PIN-DIODE-OFF*)	+5V
	S11 (T*-B-SEL)	GND
	S12 (S/T-EN*)	+5V
	S13 (S/T-OSC)	GND
	S14 (B/W-NARROW)	GND
	S15 (ANT-BITE-EN)	GND
	S16 (FAULT-SEL-B0)	GND
	S17 (FAULT-SEL-B1)	GND
	S18 (FAULT-SEL-T-B*)	GND
	S19 (BW NARROW-MANUAL/HP 16500)	MANUAL
Oscilloscope Settings: TEK 2465A*	Channel 1	Off
	Channel 2	0.1 V/div; reference ground 1 division above bottom grid.
	Channel 3	(not used)
	Time Base	200 ns/div
	Trigger	Auto; DC Coupled; Level: 0.5 V; Source: Channel 4; Slope: +; Vert: Channel 4
	Cursors	Horizontal, one cursor at GND reference, 2nd cursor set to measure peak pulse amplitude.
Signal Generator Settings: HP 8665A*	Pulse Modulation:	ON; EXT DC: ON
	Mode Select:	AUTO, ON, MODE 1: ON,
	Amplitude:	-77.2 dBm (calibrated @ UUT J2-J9 Inputs)
	Frequency:	1090.000 MHz
Pulse Generator Settings: HP 8011A*	Pulse Width:	500 ns (use vernier)
	Pulse Amplitude:	+2.5 V peak (into 50 ohm termination)
	Pulse Period:	20 us (use vernier)
* = or equivalent		

~~2.9.22.3~~ Initial Frequency Check and Pulse Performance Check

1. With the test equipment set up as in 2.2.2 (Receiver IF Filter Alignment Test Equipment), connect a coaxial cable from J10 of the receiver to the frequency counter.
2. Connect a coaxial cable from signal generator RF output to J2 (0 degree TOP).
3. Switch S20, MAIN POWER to the ON position.
4. Check L.O. frequency. It should read approximately 1030.000 MHz initially at room temperature. If not, adjust R623 (R612) until frequency is within the desired range. The frequency should be

checked again after the receiver has been powered on for 15 minutes and has stabilized. At this time the frequency should be 1030.000 ± 0.001 MHz.

5. An optional setup for frequency measurement is to use a Spectrum Analyzer as shown in Figure B-001. This gives the added ability to indirectly measure the L.O. output power in addition to the frequency. The output power from J10 should be between 5.5 and 10 dBm. Ensure that the loss of the cables used in the measurement setup are calibrated out.
6. Measure the Y1 tuning voltage at R139 (R143) p.1. The voltage should be between 7.0 Vdc and 9.5 Vdc. If needed, select an alternate value of C178 (C198) to achieve this.
7. Connect a coaxial cable to the 0 degree, BNC1 video output of the test fixture to channel 2 of the oscilloscope. The 200 ohm termination resistor must be attached with a BNC Tee at the scope input (Ch 2).
8. Execute the appropriate Logic Analyzer file from PS7517977 using the following commands:
    i. LOAD “DGPTDEF_A”
    ii. ALL; PATTERN GEN A
    iii. EXECUTE
    iv. SYSTEM; PATTERN GEN A
    v. RUN; SINGLE
9. If working properly the observed waveform will be one pulse with a minimum amplitude of 505 mV and a maximum amplitude of 593 mV when measured at the peak of the noise. Reselect R31 (R31) to lower value if the minimum level of 505 mV is not attained. Conversely raise the value of R31 (R31) if the maximum level of 593 mV is observed. A nominal amplitude of 544 mV is shown in Figure B-002. Note that the IF and Wide filter responses must be close to within specification for the pulse to appear as shown.
10. Move the signal generator cable from J2 to J3 (0 degree Bottom). The pulse should completely disappear. Change S11, T*-B-SEL switch to +5V. The pulse should reappear with the same amplitude as with J2. Return the T*-B-SEL switch to GND.
11. Move the signal generator cable and repeat the performance check for the 90, 180 and 270 channels using the respective switch settings and video output connectors on the test equipment. Change the respective test select resistors as required to obtain a nominal video amplitude. Reselect R98 (R97) for the 90 channel, R69 (R67) for the 180 channel and R137 (R141) for the 270 channel.

NOTE: Rerun single on Logic Analyzer if power to test fixture has been interrupted.

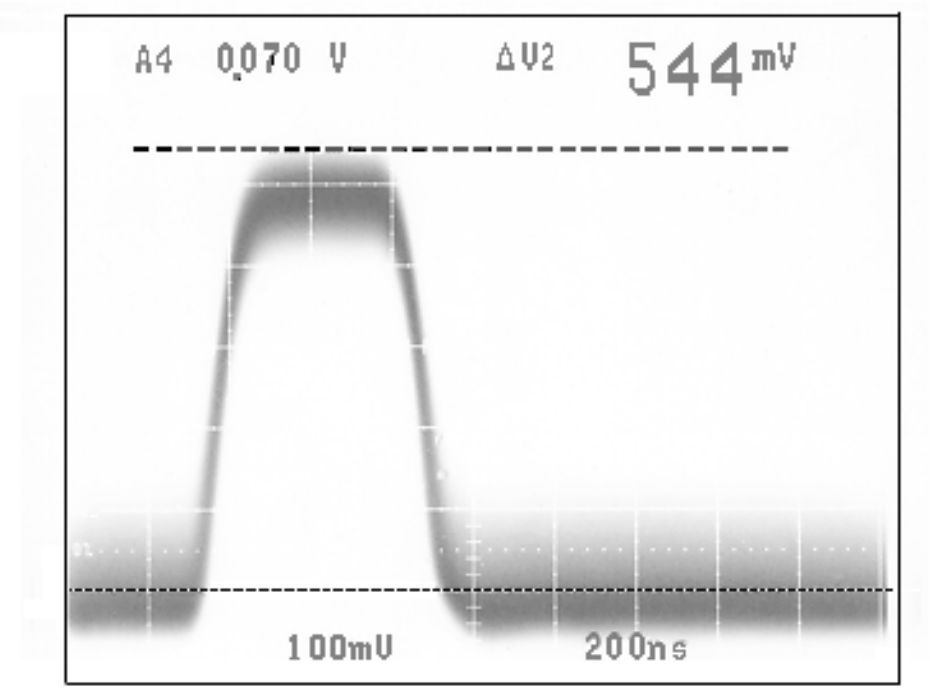


Figure B-002. Video Pulse Response @ -77.2 dBm - 1090 MHz

~~2.9.32.4~~ Wide-Band Filter Alignment

2.4.1 Setup and Adjustment

Reset the Oscilloscope as shown below:

Table B-002. Oscilloscope Settings for Wide/Narrow Band Filter Alignment

Channel 1 (X input)	1.0 V/Div
Channel 2	0.1 V/Div
Channel 3	(not used)
Time Base	X-Y (full CCW)
Trigger	Auto; DC Coupled
Level	0.5 V
Source	Channel 4
Slope	+

1. Move the Signal Generator RF output cable to J2 (0 degree Top). Move the video signal coax to BNC1 (0 degree).

2. Connect BNC6, Z-AXIS IN, to the oscilloscope's Z-INPUT.
3. Change the Signal Generator settings to 'MODULATION OFF' OFF, Amplitude = -60 dBm, SPECIAL: 112 (press 'ON' twice), Frequency Span = 10 MHz, Center Frequency Sweep = 1090 MHz, Sweep Time = 10 ms (press 'Auto' button).
4. Adjust the oscilloscope Channel 2 vertical position to obtain the swept output as shown in Figure B-003 below. The bright spots on the scope trace are frequency-selectable markers created by the (sweep) signal generator. (In X-Y mode, the Channel-1-vertical-position knob sets the horizontal placement.) The bright spots on the scope trace are frequency-selectable markers created by the (sweep) signal generator. (Note: you may have to hunt for the trace using the vertical position knobs for channel 1 and 2):

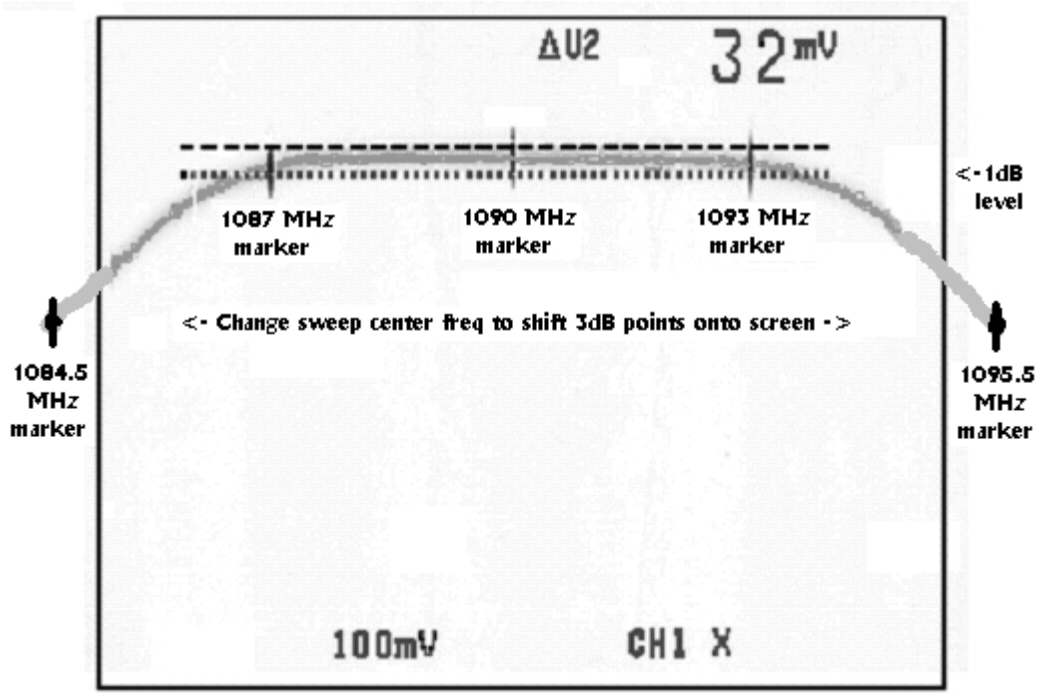


Figure B-003. Wide-Band Swept Video Response @ -60 dBm

5. The actual shape of the frequency response may vary. Move the center marker to the middle of the screen and adjust the vertical position so the swept response overlays the top cursor line.
6. Set the sweep generator markers for Marker 1:1087.0 MHz, Marker 2: 1090MHz, and Marker 3: 1093.0 MHz. Reposition the oscilloscope lower cursor to determine that the passband flatness is within 33 mV (1 dB – the logamp response is ~33mV/dB) between these two markers. If this requirement is not met, refer to Figure B-004 and Table B-003, which shows a typical filter configuration, indicating which components will change the observed response. Reselect allowable components per the applicable CCA drawing and the functions described in Figure B-004 and Table B-003 until the receiver meets the specification.

   Reprogram the swept center frequency to 1086 MHz and set marker 1 to 1084.5 MHz and measure response. Reassign the swept center frequency to 1094 MHz and set marker 3 to 1095.5 MHz and measure response. The response at these frequencies must be greater than 100 mV (3 dB) down from the response at 1090 MHz. In addition, balance the two responses so that they are within 33 mV (1 dB) of each other. Again refer to Figure B-004 and Table B-003

and choose selectable components per the applicable CCA drawing to bring the receiver into specification.

After adjusting the 3dB points, ensure that the passband flatness is remains within specification. Re-adjustment may be necessary to ensure that both passband flatness and the 3dB responses are maintained.

7. Repeat for the 90 degree, 180 degree and 270 degree channels.

NOTE: Use the top antenna connection for each channel.

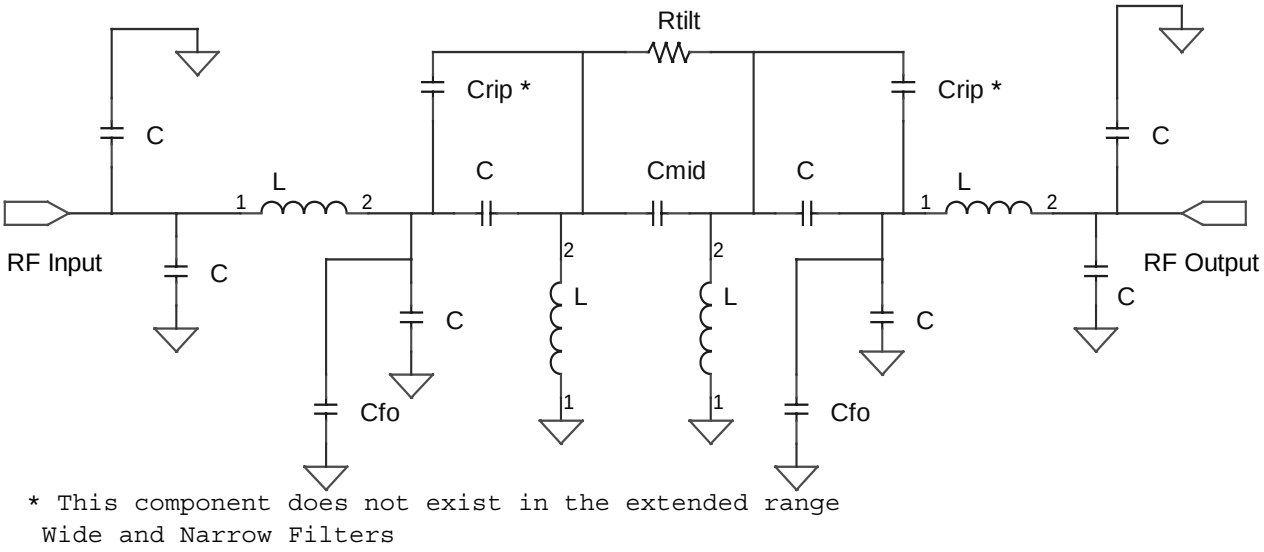


Figure B-004. General IF Bandpass Filter Tuning Schematic for All Receiver IF Filters

***** See the schematic and parts list for the specific reference designators corresponding to this figure and to the table that follows. They vary by channel and circuit card revision.

Table B-003. IF Bandpass Filter Tuning Key

COMP	DESCRIPTION
C	Fixed Value (Not selectable, change only if defective)
Lfo	Center Frequency adjustment (Larger L lowers frequency). Can also affect ripple and passband skew.
Lmatch	Bandwidth, ripple, and Center Frequency Adjustment
CF_O	Center Frequency Adjustment (Larger C lowers frequency) – First-stage IF Filter on Duroid Side – Wide-band IF Filter on FR4 Side – Narrow-band IF Filter on FR4 Side
C_{RIP}	Adjusts Center Frequency Sag & Excessive Bandwidth (Larger C lowers frequency, narrows bandwidth and reduces center sag) – First-stage IF Filter on Duroid Side
C_{MID}	Affects tilt of bandpass characteristic: – Wide-band IF Filter on FR4 Side – Narrow-band IF Filter on FR4 Side

R_{TILT}	Adjusts 1 dB Bandpass Tilt (Lower value R lowers low frequency side of pass-band amplitude): – First-stage IF Filter on Duroid Side – Wide-band IF Filter on FR4 Side Adjusts Gain And Frequency Centering (Lower value R lowers the center frequency and amplitude): – Narrow-Band IF Filter on FR4 Side

NOTE: It is recommended but not required to install CF_O and C_{RIP} as identical pairs. If the 7517945-90X drawing allows, certain locations may have no components installed. Reference the pertinent 7517945-9XX drawing to determine which components may be used to tune the filters as well as the allowed component values.

2.5 Narrow Band Filter Alignment

2.5.1 Test (continued from Wide Band Filter Alignment)

1. Move the Signal Generator RF output cable to J2 (0 degree Top). Move the video signal coax to BNC1 (0 degree).
2. Change S14 B/W-NARROW on the Test Fixture to +5V. The trace should be as shown in Figure B-005.
3. Change the marker frequencies to 1089 MHz and 1091 MHz on the signal generator.

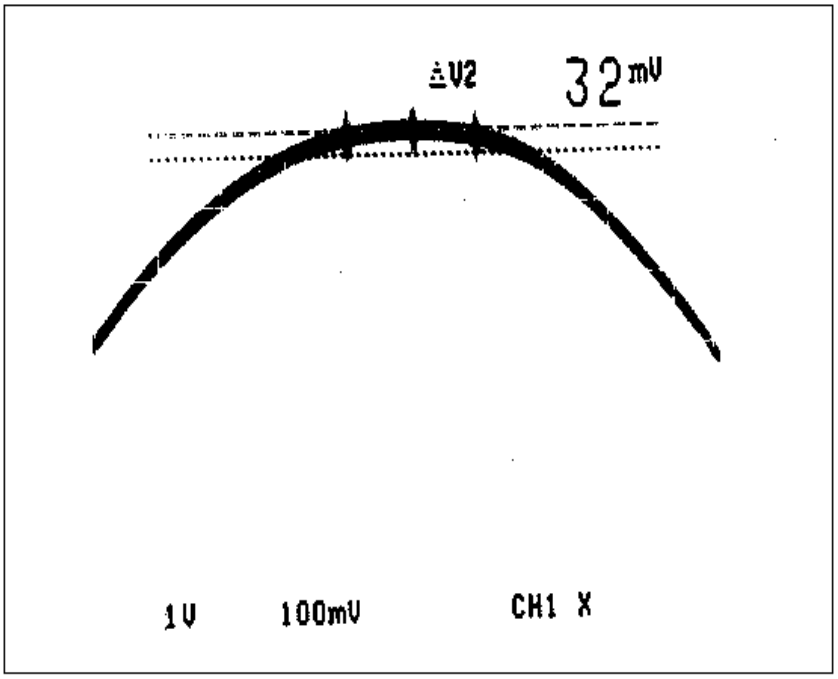


Figure B-005. Narrowband Swept Video Response @ -60 dBm - 1090 Mhz

4. The peak of the response should be centered at 1090 MHz within the ± 1 MHz markers, and the ± 1 MHz response markers should be at or less than 32 mV below the peak response. If these requirements are not met, add or change components according to Figure B-004 and Table B-003. Repeat for the 90 degree, 180 degree and 270 degree channels.
5. Position a cursor at the 1090 MHz response marker. Change S14, B/W-NARROW, on the Test Fixture to GND and position a second cursor at the 1090 MHz response marker. The difference between the wide-band and narrow-band filter responses at 1090 MHz should be less than 33 mV. The R_{TILT} resistor is used to set amplitude balance between the wide-band and narrow-band settings, however it does also affect the center frequency slightly, and must be considered when selecting the CF_O capacitors. If a change is required to balance the wide-band and narrow-band filter responses, sections 2.4 (Wide Band Filter Alignment) and 2.5 (Narrow Band Filter Alignment) must be repeated.
6. Rerun section 2.3 (Initial Frequency check and performance check) to verify proper operating frequency and video pulse amplitude.

2.6 Self Test Amplitude Balance

2.6.1 Setup and Test (setup continued from filter alignment)

1. Set the 8011A Pulse Generator to “COMPL ON”. Move the 8011A output cable from the signal generator’s pulse modulation input to the “BNC5, S/T-MOD*” input on the test fixture. Place a 50 ohm shunt load at the S/T Modulation input jack on the Test Fixture. Set S12 S/T-EN* to GND and S13 S/T-OSC to +5V on the test fixture. Adjust the Pulse Duration to 1 microsecond.
2. Set oscilloscope settings as shown in the initial setup. Set the signal generator to the initial settings, except select RF OFF.
3. Connect a coaxial cable to the BNC1, 0 degree video output of the test fixture to channel 2 of the oscilloscope.
4. Disconnect the coaxial cable from BNC6 on the Test Fixture. A pulse of approximately 1.50 V ± 0.3 V amplitude should be visible on the scope, as shown in Figure B-006. Note the voltage of the pulse peak.
5. Repeat for the 90 degree, 180 degree and 270 degree channels, taking note of the voltage of each pulse peak.
6. Check the relative amplitudes between the four channels. Reselect R9 (R12) for the 0 channel, R11 (R15) for the 180 channel, R121 (R125) for the 90 channel or R124 (R128) for the 270 channel to set the level and balance the four channels to within 165 mV of each other. The selection of an increased resistance value will lower the pulse amplitude. This adjustment is normally performed at the End Item level based on Receiver performance in the End Item. As such, this adjustment at the module level is optional.

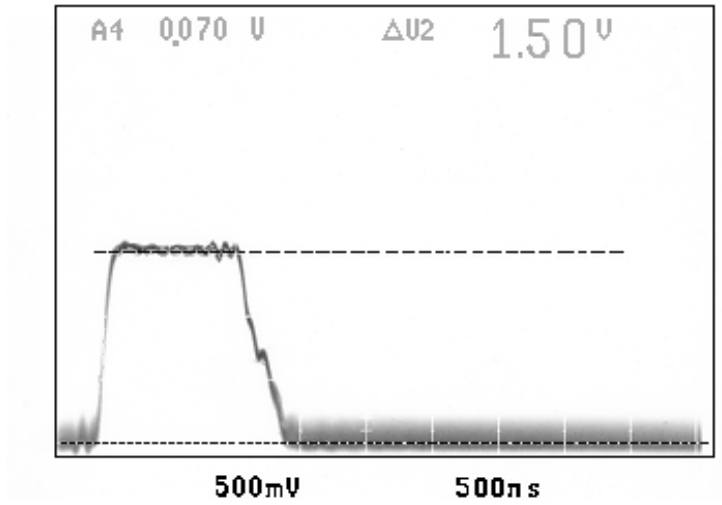


Figure B-006. Self Test Pulse Response

3 MANUAL TRANSMITTER MODULE ALIGNMENT

The CCA dash number on which a reference designator is pertinent is typically included in the instructions unless the reference designator is a connector or plug. These are anticipated to remain the same across all new dash numbers of a assembly. If the specific dash number (of the assembly being tuned) is not reference it is permissible to cross reference between assemblies of the same base number and identify the appropriate component.

3.1 Alignment Setup

1. Connect the Power Supply and Transmitter Pair to the TCAS 3000 Power Supply Test Fixture as shown in Figure B-007.
2. The cable and padding loss needs to be accounted for in the measurements of the peak power meter. See the operating instructions of the power meter used for instructions.
3. Set the source power supply to 28 ±3 VDC or 115 ±6 VAC at 400 ±10Hz. (Note: the power supply will not function from 115VAC 400Hz unless a transformer such as 9000470-001 is connected to J1 of the 9003030-002)
4. The receiver is intended to be the receiver with which the Power Supply and Transmitter Pair will be mated when they are installed within an End Item. It is possible to align a transmitter without a receiver (in which case the references to

Top and Bottom and ports are not applicable) but it may result in additional tuning when the transmitter is mated to a receiver in a unit.

5. This procedure is written around transmission from the 0 degree Top port of the Receiver. When transmitting from one of the 'Top' ports the remaining 3 'Top' ports and the 0 degree Bottom port **shall** each be terminated in 50ohm 5 watt or greater loads or in an un-terminated 5 watt or greater pad with a minimum attenuation of 10dB. These will both be referred to as 50ohm loads.

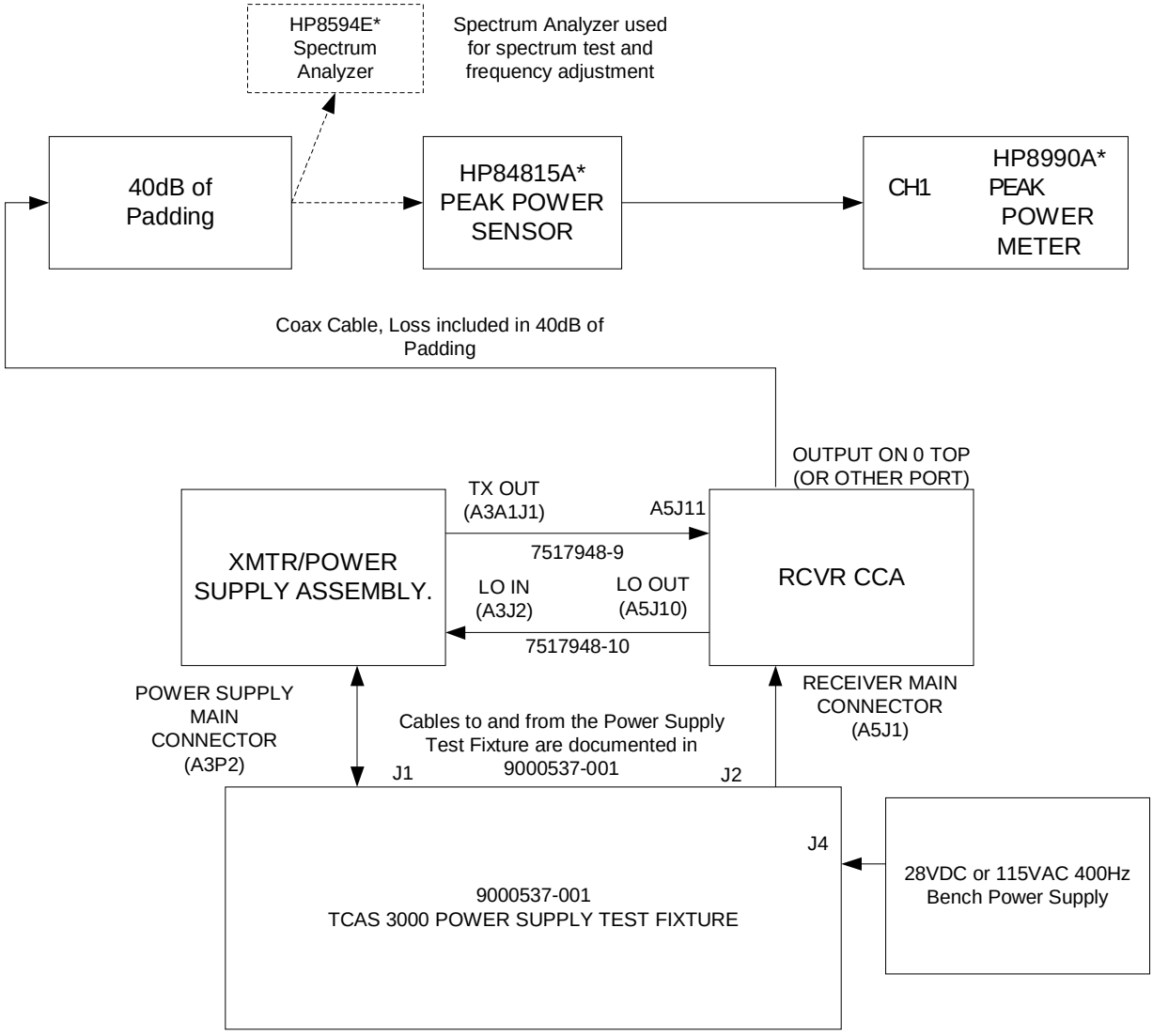


Figure B-007

*Or Equivalent

3.2 Transmitter Peak Power and Rise Time Adjustment

3.2.1 Overview

To reduce the risk of damaging the transmitter driver and final transistors upon initial power up and to ensure proper calibration of pulse width, the transmitter must be aligned for peak power and rise time prior to any further calibration. This section addresses aligning the peak power and rise times. The covers on the transmitter may be removed to aid in adjustment, but as the cover affects measurements accuracy is not assured until the covers are replaced.

CAUTION: VOLTAGES IN EXCESS OF 50V ARE PRESENT ON THE POWER SUPPLY, AND MAY BE PRESENT ON THE TRANSMITTER.

3.2.2 Tuning Procedure

1. Ensure that all of the TCAS 3000 Power Supply Test Fixture load switches within the dashed line are in the OFF position.
2. Set the Receiver Transmit Path Switches to 'Top', 0 degree 'ON', 90 degree '0ff', 180 degree 'OFF', and 270 degree 'OFF'. (This sets the receiver to direct the transmitted output to the 0 degree Top port. If two or more switches are set to 'ON' all transmission will be disabled so as to keep the transmitter from a non-standard configuration and minimize stress on the transmitter and on the PIN diode switches.)
3. Turn the rotary switch on the TCAS 3000 Power Supply Test Fixture to 'Bypass Trans Disable'
4. Turn on the source power supply
5. Apply 115VAC 60Hz to the Power Supply Test Fixture and Turn on the Fixture Power switch. This turns on the fan and applies power to the internal CPLD that provides the control signals.
6. Turn on the appropriate UUT power switch to apply power to the Power Supply. The Power Supply in turn applies power to the Transmitter and the Receiver.
7. Set all Whisper Shout Trim Switches to the 'OFF' position.
8. Turn the rotary switch on the TCAS 3000 Power Supply Test Fixture to the '0dB to –9dB Pulses' position.
9. Set the Peak Power Meter to display the first pulse (0dB attenuation) by itself. See the manual of your peak power meter for instructions. The time per division should be approximately 200nS/div.
10. Measure peak power out of the UUT. The power out of the UUT shall be 280 to 630 watts (54.5 to 58 dBm) when the power losses are calibrated out. If the measurement is being made without a receiver in the transmission path the power **shall** be 398 to 794 watts (56 and 59dBm). Adjust the transmitter as described in paragraph 3.2.3, Transmitter Power Alignment Guidance, as needed.
11. Measure the pulse rise and fall times (as measured at the 10 and 90% points of the pulse). This **shall** be less than 100ns. Adjust the transmitter as described in paragraph 3.2.3, Transmitter Power Alignment Guidance, as needed.
12. Recheck the peak power out of the UUT and ensure that the power output remains in specification. Adjust the transmitter as per steps 10 and 11 as necessary until both the peak power and rise/fall times are within specification.
13. Turn off the transmissions by turning the rotary switch to 'Bypass Trans Disable' and move the output cable from the 0 degree Top to each of the other 7 outputs in

succession. Ensure that the corresponding Top (if transmitting out a Bottom port) or Bottom (if transmitting out a Top port) port is terminated in 50ohms. Also ensure that the remaining Bottom ports (if transmitting out a Bottom port) or Top ports (if transmitting out a Top port) are terminated in 50ohms. Remember to turn the transmissions back on after the cable has been moved and the 50ohm loads attached correctly.

14. Verify that the peak power of the 0dB pulse is within 54.5 to 58 dBm (56 and 59dBm if the receiver is not included). If one of the outputs is much different from the others it may indicate either an issue with the Receiver or an interaction between the Transmitter and Receiver due to VSWR.
15. Turn the rotary switch on the TCAS Power Supply Test Fixture to the 'TX Long Pulses' position. This will cause the transmitter to output an approximately 31.0 to 31.5uS pulse once every 20ms.
16. Set the peak power meter so that the entire pulse may be viewed and ensure that the change in pulse power from beginning to end is less than 1dB.

3.2.3 Transmitter Power Alignment Guidance

With a Johanson tuning tool 8777 or equivalent, turn the tuning slug in each of the four trimmer capacitor (C126, C127, C128 and C129 on 7517935-910 or 7517935-912) approximately 10 turns counter clockwise or until the tuning slug is near the top of the trimmer capacitor barrel. Ensure that the remaining 7 UUT RF antenna ports are terminated in 50 Ω loads capable of dissipating at least 3W.

While displaying the 0dB pulse, adjust the trimmer capacitors clockwise in the following order for maximum power out of the transmitter: C129 (driver input), C128 (driver output), C127 (final output), C126 (final output). See A3A2 Transmitter CCA drawing 7517935-910 or 7517935-912 for capacitor locations.

If rise time is greater than 100 ns, adjust the trimmer capacitors in following order while monitoring both rise time and power output until both requirements are met: C126 (final output), C127 (final output), C128 (driver output) and C129 (driver input).

If rise times or peak power are not within specification, additional tuning of the transmitter can be achieved by soldering small pieces copper foil, as noted on the 7517935 drawing relevant to the Transmitter being aligned. Copper foil should be tinned prior to soldering to the PWB. Use a capacitive loading stick to determine the optimum tuning location before soldering copper foil to the PWB.

3.3 Whisper-Shout Adjustments

3.3.1 Overview

While transmitting ATCRBS in a unit the peak power of the transmitted RF power is varied. To ensure that the transmitter is able to adjust the power in 1dB steps the Whisper-Shout is evaluated and adjusted as necessary. It is easier to do this while the Transmitter Power Supply pair is out of a unit.

The TCAS 3000 Power Supply Test Fixture provides the proper control inputs to cause the transmitter to step the output power in 1dB ± 0.2 dB steps. The 1/2dB trim is provided so that, when installed in a unit, the whisper shout steps may be adjusted so that each step is within 1dB ± 0.2 dB of the adjacent steps. Within an End Item, whether or not the trim is applied to a particular step is stored in memory during calibration. To simulate this, and ensure that the transmitter will calibrate smoothly when installed in an End Item, the TCAS 3000 Power Supply Test Fixture has ten Whisper Shout Trim Switches that affect the attenuation steps listed below each switch.
During calibration it is possible that a step size may be too large or too small and there is no way to meet the 1.0 dB ± 0.2 dB step size requirement even when adjusted by using the Whisper Shout Trim Switches. This indicates that the transmitter will be unable to meet the requirement when installed in a unit. Test select resistors may be used to bring a particular step size into specification. First determine which of the five major attenuators needs to be adjusted (1 dB, 2 dB, 4 dB, 8 dB, or 16 dB). By looking at the step size data with the default values loaded, a trend may be noted. For example, if the 4 dB attenuator is too large, every time that step is switched in to create a larger whisper/shout step, the new step may be too large as well. Since all whisper/shout steps are created by a combination of the five major attenuator steps, correcting a lower attenuation step size may also fix higher attenuation steps.

3.3.2 Tuning Procedure

1. Peak power and Rise Time should be adjusted before performing this alignment.
2. Ensure that all of the TCAS 3000 Power Supply Test Fixture load switches within the dashed line are in the OFF position.
3. Turn the rotary switch on the TCAS 3000 Power Supply Test Fixture to ‘Bypass Trans Disable’
4. Set the Receiver Transmit Path Switches to ‘Top’, 0 degree ‘ON’, 90 degree ‘0ff’, 180 degree ‘OFF’, and 270 degree ‘OFF’. (This sets the receiver to direct the transmitted output to the 0 degree Top port. If two or more switches are set to ‘ON’ all transmission is disabled)
5. Ensure that all of the remaining ‘Top’ ports and the 0 degree ‘Bottom’ are terminated in 50 ohm loads.
6. Turn on the source power supply
7. Apply 115VAC 60Hz to the Power Supply Test Fixture and Turn on the Fixture Power switch. This turns on the fan and applies power to the internal CPLD that provides the control signals.
8. Turn on the appropriate UUT power switch to apply power to the Power Supply and Transmitter pair assembly. The Power Supply in turn applies power to the Transmitter and the Receiver.
9. Set all Whisper Shout Trim Switches to the ‘OFF’ position.
10. Turn the rotary switch on the TCAS 3000 Power Supply Test Fixture to ‘0dB to –9dB Pulses’ and the transmitter will automatically begin transmitting ten 1 microsecond pulses spaced 1 microsecond apart, at a duty cycle of approximately 50 times per second. The first pulse will have the minimum (0dB) attenuation and the remaining should each be 1dB lower than the preceding. This is viewed on the peak power meter. Refer to the manual of the peak power meter for operation instructions. It is recommended that at least 10 pulses be displayed on the screen with a power resolution of a maximum of 2dB/div so as to be able to measure the power differences.

11. The pulses **shall** be within 1 ± 0.2dB of each adjacent pulse. If not, they may be adjusted by choosing the appropriate Whisper Shout Trim Switch. For example, the –3dB pulse (the fourth pulse) may be attenuated by approximately 0.5dB by turning 'ON' the –3dB/-13dB/-23dB switch.

12. If the steps are not within 1 ±0.2dB even with the use of the Whisper Shout Trim Switches then it will be necessary to adjust the hardware using the test select resistors on the Transmitter. See paragraph 3.3.3, "Whisper-Shout Alignment Guidance", for guidance.

13. Repeat steps 9 through 12 with the rotary switch position changing from '0dB to –9dB Pulses' to '-9dB to –19dB Pulses'. If the power meter appears to momentarily glitch or show odd patterns while any switch is flipped on the TCAS 3000 Power Supply Test Fixture it is a normal artifact of the Test Fixture, not a problem with the Transmitter.

14. Repeat steps 9 through 12 with the rotary switch position changing from ''-9dB to –19dB Pulses' to. '-19dB to –29dB Pulses'. Note that the –9dB step has been included to provide overlap with the previous steps to facilitate alignment. Note also that the Whisper-Shout switch that modifies the –9dB step is the same that modifies the –19dB step.

15. Repeat steps 9 through 12 with the rotary switch position changing from '-19dB to –29dB Pulses' to '-28dB to –31dB Pulses'. Note the overlap of the –19dB step and the –28 and –29dB steps.

16. The over all linearity of the PIN diode attenuators may be observed by turning the rotary switch to '0dB to –31dB Pulses' and displaying all 32 pulses on the Peak Power Meter. This outputs all 32 pulses in a row at a duty cycle of approximately 50 times per second.

17. Turn the rotary switch on the TCAS 3000 Power Supply Test Fixture to 'Bypass Trans Disable (RF Off)'

18. Move the cable connection (from the receiver to the 40dB pad) from the 0 degree Top port to the 90 degree bottom. Ensure the remaining Bottom ports and the 90 degree Top Port have 50ohm loads. (Other ports may also be chosen for verification if desired, so long as the remaining ports are terminated correctly)

19. On the TCAS 3000 Power Supply Test Fixture set the Receiver Transmit Path Switches so that the correct port is chosen. (NOTE: IT IS VERY IMPORTANT THAT THESE SWITCHES ARE NOT SET TO TRANSMIT OUT OF A PORT WITH NO 50OHM LOAD)

20. Turn the rotary switch on the TCAS 3000 Power Supply Test Fixture to '0dB to –9dB Pulses', and ensure that the pulses remain within specification. Re-align the transmitter as necessary.

21. This concludes Module level Whisper Shout alignment.

3.3.3 Whisper-Shout Alignment Guidance

To help determine which attenuator may require a change to a test select resistor, an understanding of the fundamental operation of the whisper/shout attenuator is required. Figure B-008 below shows a block diagram of the whisper/shout circuit.

The whisper/shout circuit consists of pin diode switches that direct the transmitter power through various pi-pad attenuators. The pin diode attenuators themselves are switches that direct the transmitter power through the pi-pad or around it. The transmitter power

enters the whisper/shout attenuator and can be switched through one of two paths, the bypass path (which is the shortest), or the w/s path (which is longer).

The bypass path shares the 0/1 dB attenuator with the w/s path and is used for only the 0 and 1 dB whisper/shout steps. The w/s path consists of the 0/2 dB, 0/4 dB, 0/8 dB and the 0/16 dB attenuators before connecting with the bypass path before the 0/1 dB attenuator. Each of the five major attenuators can be switched between its low loss state (0 dB) or its attenuated state.

The whisper/shout was designed with two paths to reduce the overall insertion loss of the whisper/shout circuit in the 0 dB state. If all the attenuators were in series or a single path and switched to the 0 dB state, the overall insertion loss of the whisper/shout would be approximately 2.0 dB to 2.5 dB, since each attenuator has a minimum insertion loss of approximately 0.4 dB to 0.5 dB. By creating a second path for all the larger attenuation steps, four of the five attenuators can be bypassed, reducing insertion loss for the 0 dB step when the bypass path is utilized.

As a result, the through insertion loss of the whisper/shout has been minimized to approximately 1.2 dB. The insertion loss of the w/s path in its minimum insertion loss state is approximately 2.0 dB greater than the 0 dB bypass. As a result the w/s path in its minimum attenuation state is used as the 2 dB whisper/shout step. Table B-004 below shows the path and major attenuators that are used to make the default whisper/shout steps.

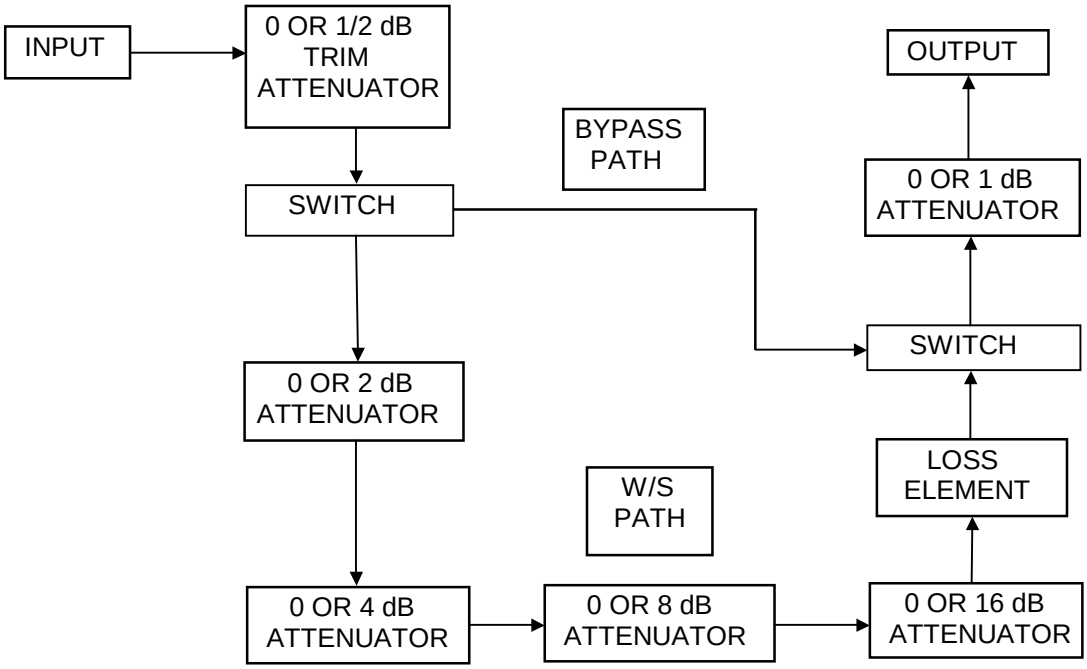


Figure B-008. Whisper/Shout Circuit Block Diagram

Table B-004. Default Path and Attenuators for Whisper/Shout Steps

Whisper/Shout Step	Path and Attenuators	Whisper/Shout Step	Path and Attenuators
0	Bypass (0)	16	W/S (8, 4, 2)
1	Bypass (1)	17	W/S (8, 4, 2, 1)
2	W/S (0)	18	W/S (16)
3	W/S (1)	19	W/S (16, 1)
4	W/S (2)	20	W/S (16, 2)
5	W/S (2, 1)	21	W/S (16, 2, 1)
6	W/S (4)	22	W/S (16, 4)
7	W/S (4, 1)	23	W/S (16, 4, 1)
8	W/S (4, 2)	24	W/S (16, 4, 2)
9	W/S (4, 2, 1)	25	W/S (16, 4, 2, 1)
10	W/S (8)	26	W/S (16, 8)
11	W/S (8, 1)	27	W/S (16, 8, 1)
12	W/S (8, 2)	28	W/S (16, 8, 2)
13	W/S (8, 2, 1)	29	W/S (16, 8, 2, 1)
14	W/S (8, 4)	30	W/S (16, 8, 4)
15	W/S (8, 4, 1)	31	W/S (16, 8, 4, 1)

Once the attenuation step that needs to be adjusted is identified, determine if the attenuation of that step needs to be increased or decreased. If more than one attenuation step appears to be out of specification, start with the lower value attenuation step first. Changing the attenuation is accomplished by changing the value of the series resistor of the pi pad attenuator of that step.

Note that variation among units may be such that certain units may not achieve the step size requirement with the default path and attenuators selected, even if test select resistors are used. In this case it is allowable to select any combination of paths, attenuators and allowable test select resistors in order to achieve the step size requirement. For example, whisper/shout step 17 may need the 16 dB attenuator only instead of the 1 dB, 2 dB, 4 dB and 8 dB attenuators, or it may need only the 2 dB, 4 dB and 8 dB attenuators.

Table B-005 below shows the typical installed value for the series resistor of each Whisper/Shout attenuator step as well as the allowable test select values. The change to the Whisper/Shout attenuation step for a given test select value is also shown. Note that Table B-005 is applicable to 7517935-910 only, and the reference designators and/or allowable test select values may change if a new Transmitter CCA is released or if a change order is written to the existing drawing. For a current list of installed resistors and allowable test selects refer to the 7517935 drawing that describes the Transmitter on which you are working.

Table B-005. Whisper/Shout Circuit Test Select Resistor Values

W/S Attenuator	REF DES	Test Select Value (Ω)	Attenuation Change
16	R36	70	Less Attenuation
16	R36	84	Less Attenuation
16	R36	92	Less Attenuation
16	R36	104	Installed Part
16	R36	110	More Attenuation
16	R36	117	More Attenuation
16	R36	133	More Attenuation

8	R35	28	Less Attenuation
8	R35	30	Less Attenuation
8	R35	32	Less Attenuation
8	R35	34	Less Attenuation
8	R35	36	Installed Part
8	R35	38	More Attenuation
8	R35	41	More Attenuation
4	R34	12	Less Attenuation
4	R34	14	Installed Part
4	R34	16	More Attenuation
2	R8	6	Less Attenuation
2	R8	7	Installed Part
2	R8	8	More Attenuation
1	R5	6	Installed Part
1	R5	7	More Attenuation
1	R5	8	More Attenuation
Trim	R2	70	More Attenuation
Trim	R2	92	More Attenuation
Trim	R2	104	More Attenuation
Trim	R2	110	More Attenuation
Trim	R2	117	Installed Part
Trim	R2	133	Less Attenuation
Trim	R2	150	Less Attenuation

The difference between whisper/shout steps 1 and 2 should generally be greater than 1.0 dB at room temperature to ensure that the unit will pass the temperature tests. This difference typically decreases at cold temperatures. The difference can be adjusted by changing the test select capacitor C130. To increase the difference, use a smaller value of capacitor. To decrease the difference, use a larger value of capacitor.

3.4 Transmitter Health Checks

3.4.1 Overview

While not required for calibration, the TCAS 3000 power supply allows for the easy checking of a few characteristics of the transmitter. These may be used to verify issues seen while installed after the cards are removed or to screen for issues prior to installing the assembly in an End Item. These characteristics include PIN diodes shorted, PIN diodes open, and DPSK modulation.

3.4.2 PIN Diode Short Test

1. Apply power to the TCAS 3000 Power Supply Test Fixture.
2. Apply 28VDC or 115VAC power to the Power Supply and Transmitter Module using the UUT 115VAC or 28VDC switch.

3. Ensure that one and only one of the receiver transmit path switches is in the 'ON' position. If two or more are 'ON' the CPLD internal to the Test Fixture shuts down all test functions.
4. Measure the DC voltage between the TCAS 3000 Power Supply Test Fixture test points 'Pin Short Mon' and 'GND'.
5. Place the rotary switch in the 'PIN Short Test' position.
6. The voltage should be less than 0.2VDC. If it is (nominally) 3.3V it indicates a fault in one of the whisper-shout PIN diodes on the transmitter.
7. Place the rotary switch in the 'PIN Open Test 1' position. This places half of the PIN diode drivers in a high state that mimics a PIN diode short. The DVM should read a nominal 3.3V.

3.4.3 PIN Diode Open Test

1. Apply power to the TCAS 3000 Power Supply Test Fixture.
2. Apply 28VDC or 115VAC power to the Power Supply and Transmitter Module using the UUT 115VAC or 28VDC switch.
3. Ensure that one and only one of the receiver transmit path switches is in the 'ON' position. If two or more are 'ON' the CPLD internal to the Test Fixture shuts down all test functions.
4. Measure the DC voltage between the TCAS 3000 Power Supply Test Fixture test points 'PIN Open Mon' and 'GND'.
5. Place the rotary switch in the 'PIN Open Test 1' position.
6. The voltage should be less than 0.2VDC. If it is (nominally) 3.3V it indicates a fault in the Whisper-Shout Trim PIN, or one of the diodes driven by PD3, PD4, PD9, PD10, PD11, and PD12.
7. Place the rotary switch in the 'PIN Open Test 2' position.
8. The voltage should be less than 0.2VDC. If it is (nominally) 3.3V it indicates a fault in one of the diodes driven by PD1, PD2, PD5, PD6, PD7, or PD8.

3.4.4 DPSK Modulation

1. Apply power to the TCAS 3000 Power Supply Test Fixture
2. Apply 28VDC or 115VAC power to the Power Supply and Transmitter Module using the UUT 115VAC or 28VDC switch.
3. Ensure that one and only one of the receiver transmit path switches is in the 'ON' position. If two or more are 'ON' the CPLD internal to the Test Fixture shuts down all test functions.
4. Ensure that the three remaining Top or Bottom ports are terminated with 50 ohm loads.
5. Place the rotary switch in the 'TX Long Pulses' position.
6. Connect a square wave generator with a 50 ohm output to the 'DPSK Mod Input' of the Power Supply Test Fixture connector J7. The square wave amplitude should be from ground (0VDC) to 3.2 ±0.1V. (To just ensure that the DPSK is working using a peak power meter, a 200kHz input will provide 6 chips – seen as 6 dips in the power output. To test the spectrum the worse case is transmitting all ones – which equates to a 4MHz input)

7. If a specific pattern is desired, the trigger output from J8 may be used to trigger the DPSK square wave generator so that the pattern is generated exactly while the transmitter transmits. This also stabilizes where the dips appear when viewed on a peak power meter.
8. The DPSK Modulated transmitted output may be viewed on the peak power meter, or the spectrum may be viewed on the spectrum analyzer.

4 TRANSMITTER SPECTRUM FILTER ALIGNMENT

Calibrate a Network Analyzer for S11 and S21 with the center frequency at 1.03 GHz and a span of 50 or 100 MHz. Install the Spectrum Filter Assembly (7517923) into the test fixture (T336413), connect the pin on A3A1E1 to the PWB on the test fixture and install the cover on the Spectrum Filter. If the test fixture has been modified to clamp the Spectrum Filter, then insert an uncovered Spectrum Filter in the fixture and clamp it in place.

Connect the output of the Spectrum Filter, A3A1J1 to the S22 input of the Network Analyzer. Connect the S11 port of the Network Analyzer to the input of the Spectrum Filter. Set the network analyzer so that the display appears as in figure B-010. Insert the tuning tool into the tuning access holes as shown in Figure B-009. Note that figure B-009 shows the Spectrum Filter installed in Transmitter module for reference purposes only. Adjust the tuning rods such that the filter response is similar to the Network Analyzer display as shown in Figure B-010.

NOTE 1: Proper application and cure of conformal coat will result in a shift in the passband frequencies. This is typically less than 3 MHz, but variation may be experienced. Prior to applying conformal coat to the ends of the resonators, the performance should be optimized at a frequency such that when the conformal coat is cured, the performance is optimized at 1030 MHz. As the technician gains experience, a different frequency may be used to ensure that after cure of conformal coat the specifications are met at 1030 MHz.

- Return loss (S11) shall be greater than or equal to 18 dB over the passband, 1030 ± 1 MHz after conformal coat cure. There shall be only one major lobe.
- Insertion loss (S21) should be minimum, less than or equal to 0.80 dB at the center frequency (1030 MHz after conformal coat cure).
- The 3 dB bandwidth shall be between 16 and 21 MHz.
- Insertion loss shall be greater than or equal to 12 dB at 1030 ± 20 MHz after conformal coat cure.

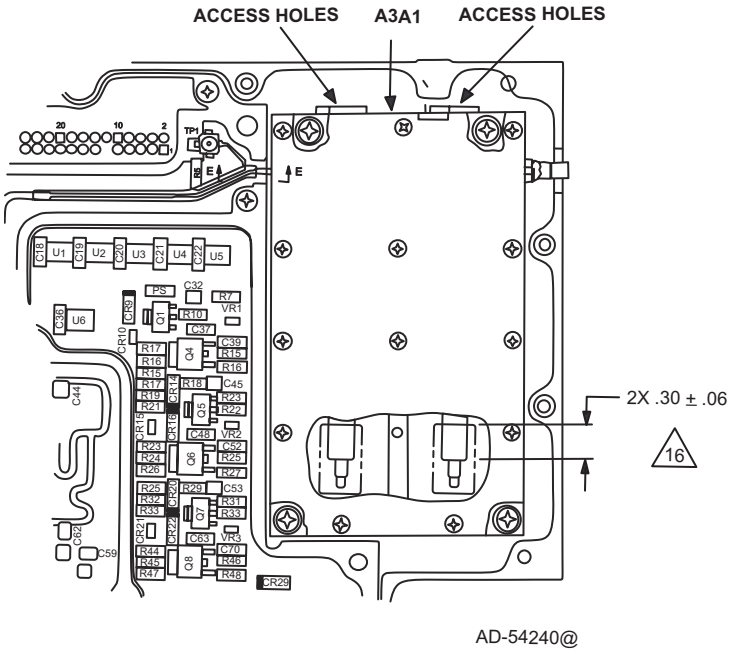


Figure B-09. Transmitter Assembly

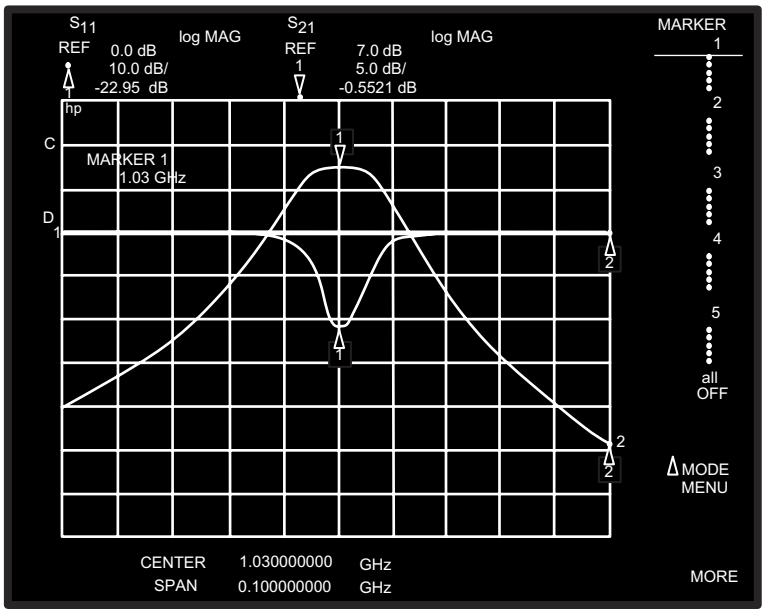


Figure B-010. Spectrum Filter Response

Once the Spectrum Filter is tuned, remove the Spectrum Filter cover (7517932-1) and apply conformal coat to the ends of the resonators as shown in Figure B-009 or refer to drawing 7517923. Readjust the Spectrum Filter before allowing the conformal coat to dry for 7 days or bake for 4 to 8 hours at 170 degrees F. After drying the conformal coat, verify the Spectrum Filter meets the specifications stated above. If the unit is not within specification, repeat tuning steps until the unit is within specification requirements.

APPENDIX C

TCAS 3000 AUTOMATIC CALIBRATION PROCEDURE

1 INTRODUCTION

The MTS can automate most of the UUT calibration process. When the autocalibration routine is selected, several test steps will be loaded which can be run independently or as a continuous sequence. At the beginning of each calibration step the previously stored calibration data is retrieved from the TCAS 3000 FLASH memory. Depending on the test selected, various measurements and calculations are made. If there are problems encountered during any step, notification is made to the operator. Finally, the CRC for the FLASH calibration memory is calculated and the values are written back to the TCAS 3000 calibration FLASH memory.

2 AUTOCALIBRATION PROCEDURE

2.1 Initialization

This procedure assumes that all of the required embedded images reside within the UUT.

2.1.1 Loading of Calibration Sequence

These steps will utilize the MTS test station.

Step 1. Insert the UUT into MTS UUT mount.

Step 2. On the desktop of the MTS PC, click on the shortcut icon for the MT9000469-001 software. This will launch the test program and bring up the operator interface.

Step 3. Log in with employee number and password.

Step 4. Go to File, Select, Open.

Step 5. Select the sequence file: calibrat.squ" from the File Open dialog of the Test Executive to initiate the autocalibration routine. Run autocalibration steps individually or as a continuous sequence as desired. The following paragraphs describe the function of each test step within the "calibrat.squ."

2.1.2 Sequence Step 01: Initialize

Execution of this step will apply power to the UUT and establish Rs232 communications. If desired, this step may be executed to allow the UUT to warm up to a stable internal temperature prior to continuing calibration.

Note: Execution of any other individual step within the calibration sequence will first apply power and establish communications with the UUT if not already done. The calibration function of that selected step will then automatically be performed.

2.1.3 Sequence Step 02: Default Cal

Execution of this step will automatically load default calibration values into the UUT. This is a relatively good starting point for all the calibration routines and may help to minimize the time required to select various calibration values calculated by the rest of the active calibration steps.

2.1.4 Sequence Step 03: Osc Freq Cal

This step places the MTS and UUT in a continuous transmit frequency measurement mode such that the transmit frequency can be changed by adjusting a potentiometer on the A5

RCVR I/O CCA while transmitting full power. If the operator is running the test from Single Pass or Test UUT, the program will automatically check the frequency to be 1030.000 +/- 0.001 MHz. If the frequency passes these limits, the program will continue. If the frequency does not pass these limits, the operator will be allowed to adjust the frequency. If the operator is running the test in Run Test mode, the operator will be allowed to adjust and accept the frequency.

The frequency adjustment potentiometer is A5R623 on the 7517945-903 CCA (A5R612 for the 7517945-904). The potentiometer can be accessed through a screw hole in the front cover of the TCAS 3000 unit. First remove the large Phillips head screw just above and toward the right side of the unit handle. Potentiometer A5R623 (A5R612) should now be accessible through the screw hole. A clockwise rotation of the potentiometer will decrease the frequency of the unit. While monitoring the frequency output, adjust the potentiometer until the frequency is 1030.000 +/- 0.001 MHz. Replace the Phillips head screw in the front cover of the TCAS 3000 unit and tighten to the appropriate torque requirement.

Note: f the unit has required a significant change in frequency, the UUT may need to repeat the measurements taken in Appendix B to verify that the transmitter peak power and rise times still meet the requirements. It is possible that the adjustment in frequency could slightly affect the peak power or rise time.

2.1.5 Sequence Step 04: Tx Pulse Width Cal

The transmit Pulse Width is automatically measured and set by this routine. No operator intervention is required. The result is stored in UUT FLASH memory.

2.1.6 Sequence Step 05: Tx SPR Cal

The transmit Sync Phase Reversal position is automatically measured and set by this routine. Continuous MODE S interrogations are transmitted by the UUT while being measured and adjusted by the MTS software. No operator intervention is required. The result is stored in UUT FLASH memory.

2.1.7 Sequence Step 06: Rx MTL & Slope Cal

This step sets the digital potentiometers for the Minimum Trigger Level (MTL) and slope (gain) for each of the 4 receiver channels of the UUT. No operator intervention is required. Each iteration of the routine tests percentage of received replies and composite video amplitude for a given input amplitude. The MTL is set to be 90% +/- 3% received replies with an input level at the ARINC 600 connector of -77.0 dBm. The slope is set such that the composite video amplitude is within 1.0 dB of the input amplitude at input amplitudes of -66.0 dBm, -48 dBm and -24 dBm. The slope setting is adjusted based on a weighted error function of all 3 amplitudes. In some cases, a stable combination can not be found. The routine will abort a channel if no combination can be found within 20 attempts. In such cases, a printout is provided with the results of the attempts. In all cases the most optimum setting combinations for all 4 receiver channels are stored in UUT FLASH memory.

2.1.8 Sequence Step 07: Tx Whisper/SHOUT Cal

This step automatically measures all 64 possible whisper/shout levels and selects the optimum combination of steps based on an error function comprised of both relative and absolute errors. The best fit of whisper/shout steps is then saved to UUT FLASH memory. No operator intervention is required. Because of the combinations and variations in this step, the results may be such that the UUT will not pass all manufacturing tests. In such a case, the routine will provide a printout of the actual power measurements and the

Whisper/Shout selections to assist in transmitter test-select resistor choices. Refer to Appendix B for detailed information explaining how to select the appropriate values of test-select resistors. In either case, the results are stored in UUT FLASH memory.

2.1.9 Sequence Step 08: SelfTest CV Cal

This step will generate self-test interrogations using the self-test oscillator on each channel (0,90,180,270) and compute the difference between the theoretical composite video values (-45 dBm) and the actual values. These values will then be scaled and stored as calibration factors in UUT Cal FLASH.

2.1.10 Sequence Step 09: Display Cal Data

The UUT Cal FLASH memory is read and displayed for recording and review. The results may be observed on the Test Executive screen and/or on the Test Report. No operator intervention is required.

APPENDIX D

TRD MACRO INSTRUCTIONS

1 MACRO INSTRUCTIONS

The following instructions are utilized by this document in a manner similar to the way a program uses functions which are called multiple times.

1.1 InitRegisters ( )

These steps will initialize the UUT Registers.

Step 1. Initialize the RF FPGA **Receiver Slope Calibration Adjustment Register** by first reading the cal values from the calibration table in the maintenance log and then writing to the RF FPGA register. Refer to the following algorithm:

FOR (*Address* = 0xff40002B THROUGH *Address* = 0xff400028)
{
Read Rcvr 270 through 0 degree Slope Adjust from the UUT cal table by executing the HTS command: "*RB P1 Address*". This will be done for each iteration of this loop.

Save the returned 2 character cal value to the string variable *RegVal*.

For each iteration of this loop, Concatenate the returned characters to the existing string *RegVal*. The final string will be 8 characters.

Set *Address* = *Address* – 0x1.
}

Write the Rcvr 270 through 0 degree Slope Adjust Values (*RegVal*) to the Receiver Slope Calibration Adjustment Register by executing the following HTS command:
WL P1 88003000 RegVal.

Step 2. Initialize the RF FPGA **Receiver MTL Calibration Adjustment Register** by first reading the cal values from the calibration table in the maintenance log and then writing to the RF FPGA register. Refer to the following algorithm:

FOR (*Address* = 0xff400027 THROUGH *Address* = 0xff400024)
{
Read Rcvr 270 through 0 degree MTL Adjust from the UUT cal table by executing the HTS command: "*RB P1 Address*". This will be done for each iteration of this loop.

Save the returned 2 character cal value to the string variable *RegVal*.

For each iteration of this loop, Concatenate the returned characters to the existing string *RegVal*. The final string will be 8 characters.

Set *Address* = *Address* – 0x1.
}

Write the Rcvr 270 through 0 degree MTL Adjust Values (*RegVal*) to the Receiver MTL Calibration Adjustment Register by executing the following HTS command:
WL P1 88003004 RegVal.

Step 3. Initialize the RF FPGA **Mode S and ATCRBS AOA Delay Register** by executing the following HTS command: "*WL P1 8800300C 00002ABC*".

Step 4. Initialize the RF FPGA **DMTL Offset And Sample And Hold Offsets Register** by executing the following HTS command: *"WL P1 88003010 151F232D* ".

Step 5. Initialize the RF FPGA **Enhanced Multi-Sample Mode S Configuration Register** by executing the following HTS command: "*WL P1 88003014 55230A05*".

Step 6. Initialize the RF FPGA **Squitter Listening Noise/Slope Setup Register** by executing the following HTS command: "*WL P1 88002004 10101500* ".

Step 7. Initialize the RF FPGA **Transmitter DPSK And Pulse Width Setup Register** by first reading the cal values from the calibration table in the maintenance log and then writing to the RF FPGA register. Refer to the following algorithm:

1. Read the Transmitter Pulse Width calibration value from the UUT cal table by executing the HTS command: "*RB P1 ff400021*" .
2. Save the returned 2 character cal value to the long (32 bit) integer variable **XmtrPw**
3. Read the Transmitter SPR Adjust calibration value from the UUT cal table by executing the HTS command: "*RB P1 ff400023*"
4. Save the returned 2 character cal value to the long (32 bit) integer variable **SprAdj**
5. Perform the following bitwise 'C' manipulation and assignment: **PwSprAdjRegVal** = ((**SprAdj** & 0x3f) << 8)] | (**XmtrPw** & 0x1F), where PwSprAdjRegVal is also defined as a long (32 bit) integer variable
6. Convert **PwSprAdjRegVal** to the string equivalent of its 8 char hex value and write this value to the Transmitter DPSK And Pulse Width Setup Register by executing the following HTS command: "*WL P1 88003008* ***PwSprAdjRegVal***"

Step 8. Turn the PIN Diode ON by executing the following HTS command: "*WL P1 F00B8000 1*".

1.2 GetSelfTestLimit (Limit)

These steps will compute the Receiver Self Test limits after reading the base values from UUT calibration memory. Where **Limit** is the desired value (Low/High) to be computed.

Step 1. If **Limit** = **LowLimit** perform the following steps:

1. Read the Receiver Self-Test Low Limit Threshold calibration value from the UUT cal table by executing the HTS command: "*RB P1 ff40002C*".
2. Save the returned 2 character cal value into the floating point variable **SF_LL,** then compute and return the result of the following:

   SF_LL = ((.2888 * **SF_LL** - 92.889) + 3.0

Step 2. If **Limit** = **HighLimit** perform the following steps:

1. Read the Receiver Self-Test High Limit Threshold calibration value from the UUT cal table by executing the HTS command: "*RB P1 ff40002D*".
2. Save the returned 2 character cal value into the floating point variable **SF_HL,** then compute and return the result of the following:

   SF_HL = ((.5778 * **SF_HL** - 92.889) - 3.0

1.3 InitModeSTxWrds (Len, W7, W8, W9, W10)

These steps will initialize words 1 through 10 of the UUT Xmit queue prior to generating a single Mode S interrogation. The input parameter, **Len,** is for setting a Short or Long P6 pulse. The input parameters **W7, W8, W9, W10** is the transmission data for Long/Short transmission.

Step 1. Initialize Word #1 of the Xmit queue for Long or Short MODE S interrogation, Top Ant, Suppression pulse enabled by executing one of the following HTS commands:

For **Len** = Long, execute "*WL P1 300000 37F12100*"
For **Len** = Short, execute "*WL P1 300000 37F10100*"

Step 2. Initialize Word #2 of the Xmit queue for Range Gate Stop, Range Time Delay by executing the following HTS command: "*WL P1 300004 10103001*".

Step 3. Initialize Word #3 of the Xmit queue for Mutual Suppression pulse, Noise Thresh, Noise Value by executing the following HTS command: "*WL P1 300008 00003010*".

Step 4. Initialize Word #4 of the Xmit queue for positive/negative slope value by executing the following HTS command: "*WL P1 30000C 1500B2E5*".

Step 5. Initialize Word #5 of the Xmit queue for pre/post interrogation delay by executing the following HTS command: "*WL P1 300010 0000A00F*".

Step 6. Initialize Word #6 of the Xmit queue to zero by executing the following HTS command: "*WL P1 300014 00000000*".

Step 7. Initialize Word #7 of the Xmit queue to **W7** by executing the following HTS command: "*WL P1 300018 **W7***".

Step 8. Initialize Word #8 of the Xmit queue to **W8** by executing the following HTS command: "*WL P1 30001C **W8***".

Step 9. Initialize Word #9 of the Xmit queue to **W9** by executing the following HTS command: "*WL P1 300020 **W9***".

Step 10. Initialize Word #10 of the Xmit queue to **W10** by executing the following HTS command: "*WL P1 300024 **W10***".

1.4 InitAtcTxWrds1Thru6 (Mode, Ant)

These steps will initialize words 1 through 6 of the UUT Xmit queue prior to generating a single ATCRBS interrogation. The input parameter **Mode** is the ATRCBS Mode (Mode C, Mode 2, Mode A). The input parameter **Ant** selects the top or bottom antenna.

Step 1. Initialize Word #1 of the Xmit queue for ATCRBS (MODE C or Mode A or Mode 2), Top Ant, Suppression pulse enabled by executing one of the following HTS commands:

For **Mode** = Mode_C, **Ant** = Top: execute "*WL P1 300000 37F00120*"
For **Mode** = Mode_2, **Ant** = Top: execute "*WL P1 300000 37F00140*"
For **Mode** = Mode_A, **Ant** = Top: execute "*WL P1 300000 37F00160*"

For **Mode** = Mode_C, **Ant** = Bot: execute "*WL P1 300000 37F00520*"
For **Mode** = Mode_2, **Ant** = Bot: execute "*WL P1 300000 37F00540*"
For **Mode** = Mode_A, **Ant** = Bot: execute "*WL P1 300000 37F00560*"

Step 2. Initialize Word #2 of the Xmit queue for Range Gate Stop, Range Time Delay by executing the following HTS command: "*WL P1 300004 10103001*".

Step 3. Initialize Word #3 of the Xmit queue for Mutual Suppression pulse, Noise Thresh, Noise Value by executing the following HTS command: "*WL P1 300008 00000001*".

Step 4. Initialize Word #4 of the Xmit queue for positive/negative slope value by executing the following HTS command: "*WL P1 30000C 15000000*".

Step 5. Initialize Word #5 of the Xmit queue for pre/post interrogation delay by executing the following HTS command: "*WL P1 300010 0000D007*".

Step 6. Initialize Word #6 of the Xmit queue to zero by executing the following HTS command: "*WL P1 300014 00000000*".

1.5 InitAtcTxWrds7Thru10 (S1_Att, S1_Ang, P1_Att, P1_Ang, P2A_Att, P2A_Ang, P2B_Att, P2B_Ang, P3_Att, P3_Ang, P4_Att, P4_Ang, P4_Pw)

These steps will initialize words 7 through 10 of the UUT Xmit queue prior to generating a single ATCRBS interrogation. The input parameters of this macro set the attenuation and angles of each pulse.

Step 1. If **S1_Att** < 0, initialize a 32 bit integer variable **S1_AttVal** = 0. If **S1_Att** ≥ 0 perform the following steps:

1. Read the Whisper/Shout step calibration value from the UUT cal table by executing the HTS command: "*RB P1 ff4000**S1_Att***", where **S1_Att** is the 2 char hex value for the specific byte location of the desired Whisper/Shout step calibration value.
2. Save the returned 2 character cal value to the 32 bit integer variable **S1_AttVal.**

Step 2. If **P1_Att** < 0, initialize a 32 bit integer variable **P1_AttVal** = 0. If **P1_Att** ≥ 0 perform the following steps:

1. Read the Whisper/Shout step calibration value from the UUT cal table by executing the HTS command: "*RB P1 ff4000**P1_Att***" , where **P1_Att** is the 2 char hex value for the specific byte location of the desired Whisper/Shout step calibration value.
2. Save the returned 2 character cal value to the 32 bit integer variable **P1_AttVal.**

Step 3. If **P2A_Att** < 0, initialize a 32 bit integer variable **P2A_AttVal** = 0. If **P2A_Att** ≥ 0 perform the following steps:

1. Read the Whisper/Shout step calibration value from the UUT cal table by executing the HTS command: "*RB P1 ff4000**P2A_Att***" , where **P2A_Att** is the 2 char hex value for the specific byte location of the desired Whisper/Shout step calibration value.
2. Save the returned 2 character cal value to the 32 bit integer variable **P2A_AttVal.**

Step 4. If **P2B_Att** < 0, initialize a 32 bit integer variable **P2B_AttVal** = 0. If **P2B_Att** ≥ 0 perform the following steps:

1. Read the Whisper/Shout step calibration value from the UUT cal table by executing the HTS command: "*RB P1 ff4000**P2B_Att***" , where **P2B_Att** is the 2 char hex value for the specific byte location of the desired Whisper/Shout step calibration value.
2. Save the returned 2 character cal value to the 32 bit integer variable **P2B_AttVal**.

Step 5. If **P3_Att** < 0, initialize a 32 bit integer variable **P3_AttVal** = 0. If **P3_Att** ≥ 0 perform the following steps:

1. Read the Whisper/Shout step calibration value from the UUT cal table by executing the HTS command: "*RB P1 ff4000**P3_Att***" , where **P3_Att** is the 2 char hex value for the specific byte location of the desired Whisper/Shout step calibration value.
2. Save the returned 2 character cal value to the 32 bit integer variable **P3_AttVal.**

Step 6. If **P4_Att** < 0, initialize a 32 bit integer variable **P4_AttVal** = 0. If **P4_Att** ≥ 0 perform the following steps:

1. Read the Whisper/Shout step calibration value from the UUT cal table by executing the HTS command: "*RB P1 ff4000**P4_Att***" , where **P4_Att** is the 2 char hex value for the specific byte location of the desired Whisper/Shout step calibration value.
2. Save the returned 2 character cal value to the 32 bit integer variable **P4_AttVal**.

Step 7. Perform the bitwise 'C' assignments & manipulations :

Word7Val = ((**P1_AttVal** << 4) | (**P1_Ang** << 12) | (**S1_AttVal** << 20) | (**S1_Ang** << 28))
Word8Val = ((**P2A_AttVal** << 4) | (**P2A_Ang** << 12) | (**P2B_AttVal** << 20) | (**P2B_Ang** << 28))
Word9Val = ((**P3_AttVal** << 4) | (**P3_Ang** << 12) | (**P4_AttVal** << 20) | (**P4_Ang** << 28))

Step 8. If **S1_Att ≥** 0 perform the bitwise 'C' manipulation: **Word7Val** |= 0x80000

Step 9. If **P1_Att ≥** 0 perform the bitwise 'C' manipulation: **Word7Val |=** 0x8

Step 10. If **P2A_Att ≥** 0 perform the bitwise 'C' manipulation: **Word8Val** |= 0x80000

Step 11. If **P2B_Att ≥** 0 perform the bitwise 'C' manipulation: **Word8Val |=** 0x8

Step 12. If **P3_Att ≥** 0 perform the bitwise 'C' manipulation: **Word9Val** |= 0x80000

Step 13. If **P4_Att ≥** 0 perform the bitwise 'C' manipulation: **Word9Val** |= (0x8 | (**P4_Pw** << 2))

Step 14. Convert the variables **Word7Val, Word8Val,** and **Word9Val** to Big Endian format and then to 8 character string representations of their hex Value.

Step 15. Initialize Word #7 of the Xmit queue for S1/P1 Pulses having the desired attenuation and angles by executing the HTS command "*WL P1 300018 **Word7Val***".

Step 16. Initialize Word #8 of the Xmit queue for P2A/P2B Pulses having the desired attenuation and angles by executing the HTS command "*WL P1 30001C **Word8Val***".

Step 17. Initialize Word #9 of the Xmit queue for P3/P4 Pulses having the desired attenuation and angles by executing the HTS command "*WL P1 300020 **Word9Val***".

Step 18. Initialize Word 10# of the Xmit queue to zero by executing the following HTS command: "*WL P1 300024 00000000*".

END OF DOCUMENT