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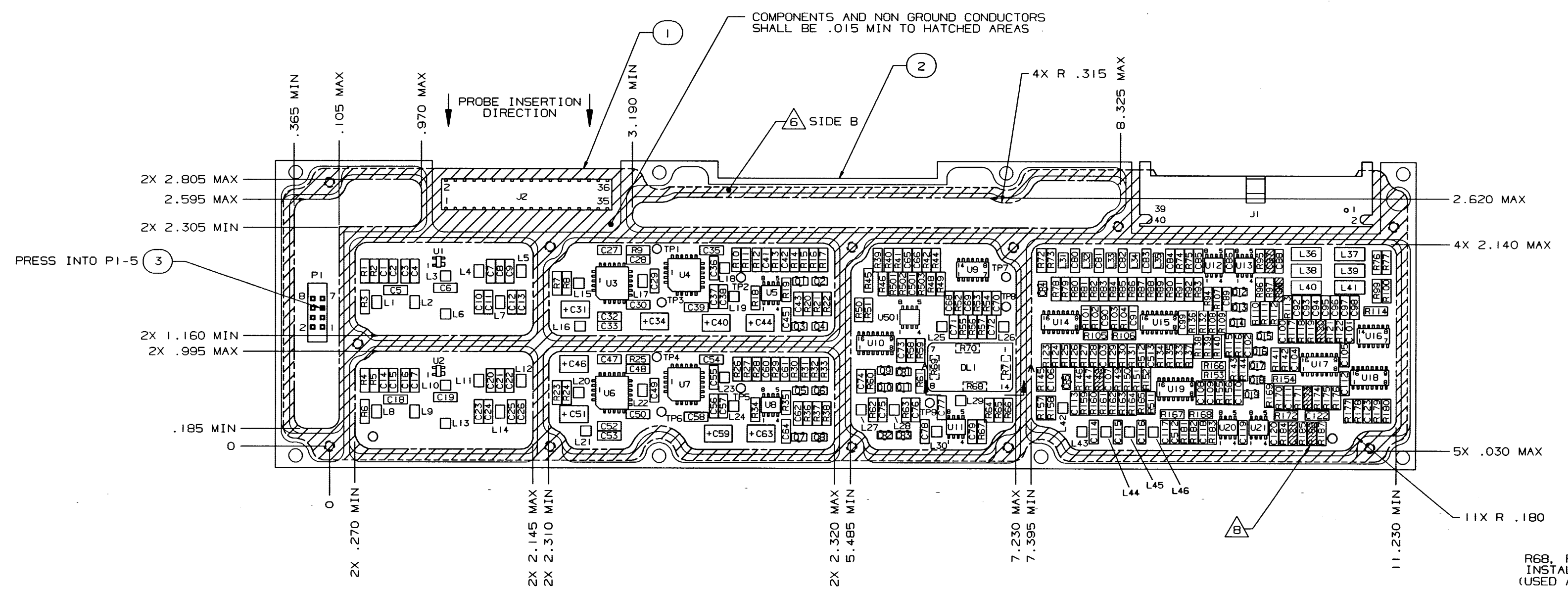
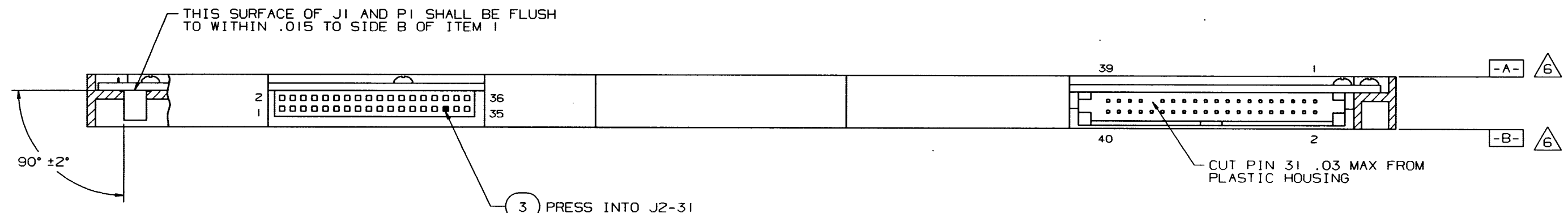
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
		INITIAL RELEASE	16OCT95	G. BEILER
	A	SH IDA REV. PL. AFFECTED. (02041 (U)) USE ALL PARTS IN-HOUSE. IN STOCK AND CURRENTLY ON ORDER (EFFECTIVITY IS NEXT BUY)	3MAY96	M. HORN P. ZALESKI
	B	SH IDA REV. PL. AFFECTED. (104102 (U)) USE ALL PARTS IN-HOUSE. IN STOCK AND CURRENTLY ON ORDER (EFFECTIVITY IS NEXT BUY)	104102 (U)	<i>[Signature]</i>

NOTES:

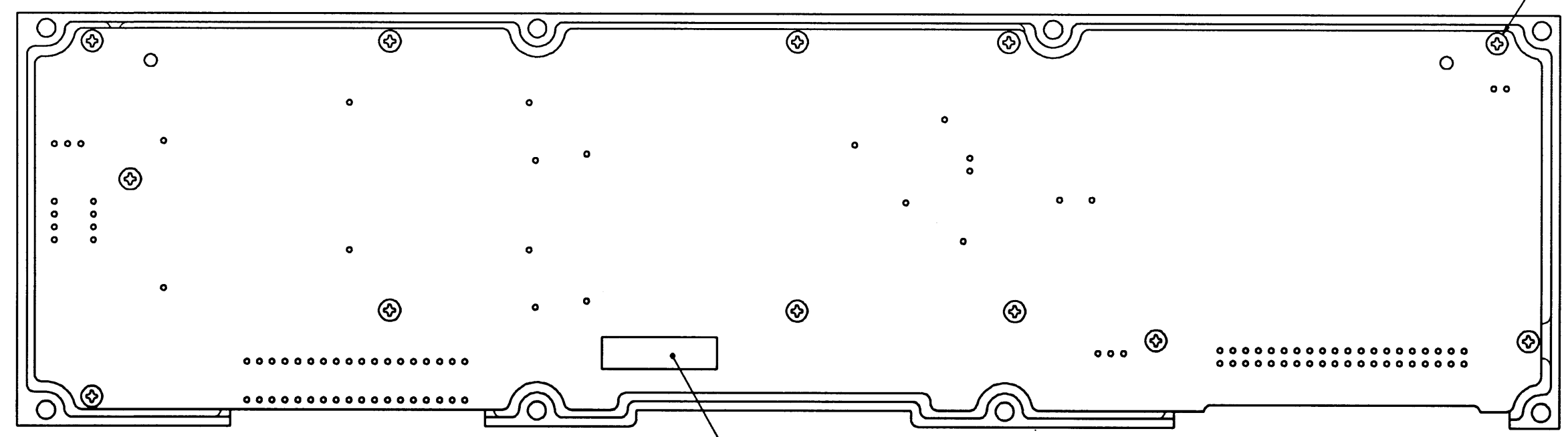
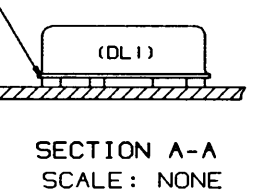
- ASSEMBLE PER ITEM 701.
- 
 THIS ASSEMBLY INCLUDES COMPONENTS WHICH ARE SUBJECT TO DAMAGE BY ELECTROSTATIC CHARGES; THEREFORE, ALL COMPONENTS SHALL BE HANDLED IN ACCORDANCE WITH GUIDELINES FOR ELECTROSTATIC DISCHARGE CONTROL.
- MAXIMUM COMPONENT HEIGHT SIDE B SHALL BE:
 CONDUCTIVE CASE .230
 NONCONDUCTIVE OR GROUNDED CASE .280 (EXCEPT J1 MAY BE .320 MAX).
- COMPONENT LEAD PROTRUSION SHALL BE .060 MAXIMUM: BARE COPPER PERMISSIBLE ON COMPONENT LEADS AT TRIMMED SURFACES.
- SQUARE PADS ON PRINTED WIRING BOARD INDICATE PIN 1.
- 
 CONFORMAL COAT CCA PER ITEM 702, EXCEPT SURFACES A AND B OF THE HOUSING (ITEM 2), J1 (PINS AND CAVITY), J2, AND P1. COATING ON THE HOUSING IS NOT REQUIRED.
- SOME COMPONENTS SHOWN OVERSIZE TO PROVIDE SPACE FOR DESIGNATORS.
- 
 SHADED COMPONENTS ARE NOT INSTALLED.

REV STATUS OF PARTS LIST SHALL BE SAME AS BASIC DRAWING NUMBER SEE SEPARATE PARTS LIST

<table border="1"> <tr> <td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td> </tr> <tr> <td colspan="25"></td> <td>A</td><td>B</td><td>REV</td><td>SHEET</td> </tr> <tr> <td colspan="25"></td> <td></td><td></td><td></td><td>INDEX</td> </tr> </table>										45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1																										A	B	REV	SHEET																													INDEX	CONTRACT XS-852 DRAWN BY R. RICHARDS DATE 06SEP95 DESIGNED BY R. PINGEL DATE 06SEP95 CHECKED BY E. THIESSEN DATE 06OCT95 APVD FOR MFG S. YATEEM DATE 06OCT95 APVD FOR DE O. MULLEN DATE 06OCT95 APVD FOR ENGRG M. HORN DATE 06OCT95 APVD FOR DATE FIRST USED ON 7510700		OPERATIONAL NOTE SIMILAR ASSEMBLY Honeywell COMMERCIAL FLIGHT SYSTEMS GROUP PHOENIX, ARIZONA TITLE CIRCUIT CARD ASSEMBLY-RECEIVER, A4 SIZE/CAGE CODE E155939 DRAWING NO. 7517440-904 REV B SCALE NONE UNIT WT 4 SHEET 1 OF 14	
45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1																																																																								
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MFG REF NO. DPA NO. A-16428 PRODUCT LINE NO. 3834 AW/PS ANALYSIS EB 7510800 REF DWG REF SPEC										MATL-PROCESS-FINISH MATL PROCESS FINISH										MILITARY DESIGNATION PROCESS, FINISH, SEE 00 40. ITEM CODE TYP EB699384 3 THIRD ANGLE PROJECTION DWG CLASS A APVD FOR DATE										INTERPRET DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982 UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES; TOLERANCES: 2 PL DEC ± .01 3 PL DEC ± .005 ANGLES ± 1°										APPLICATION 7517400 7510700 NEXT ASSY USED ON (SYS)																																																																												

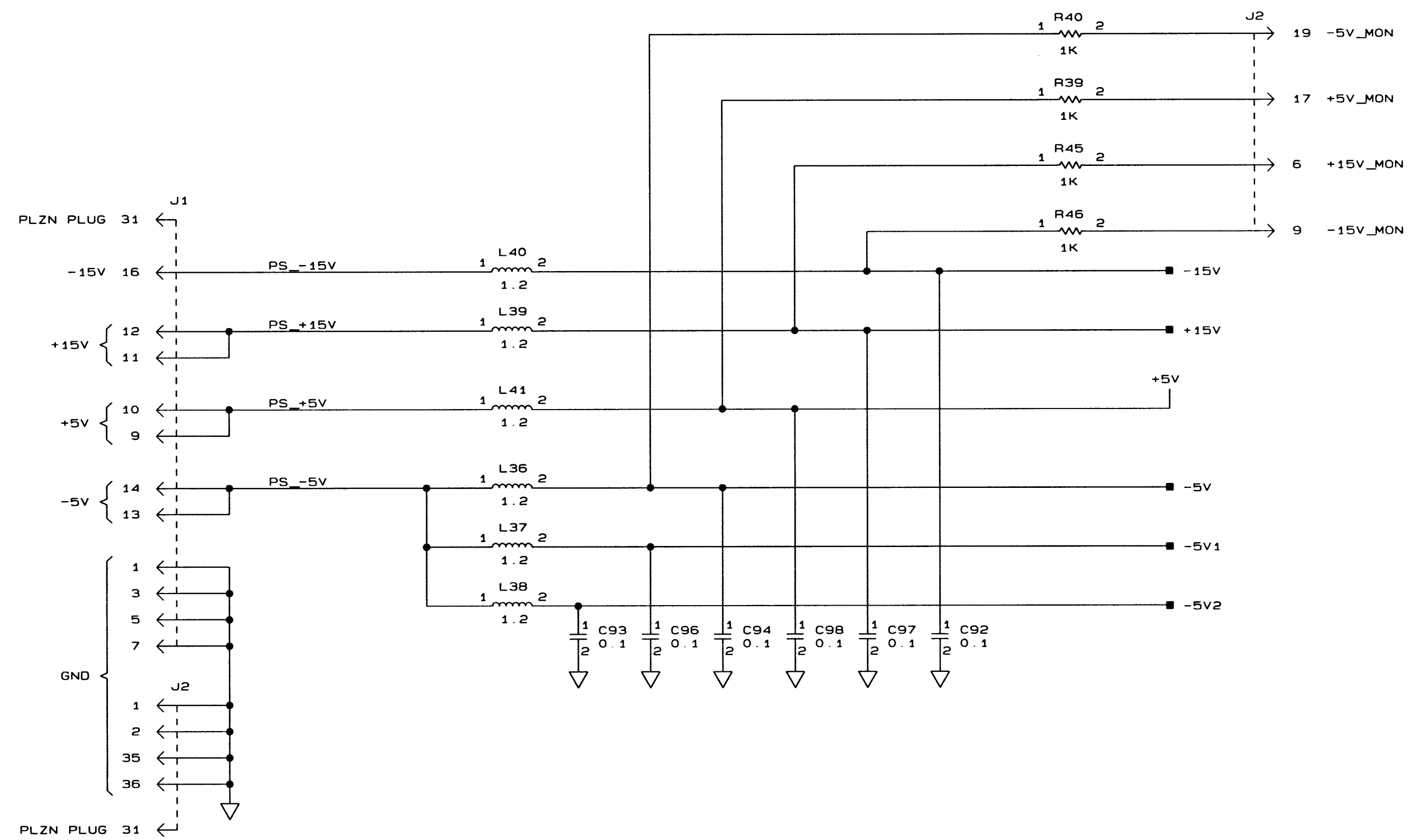


VIEWING SIDE B
COVER NOT SHOWN FOR CLARITY



VIEWING SIDE A

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



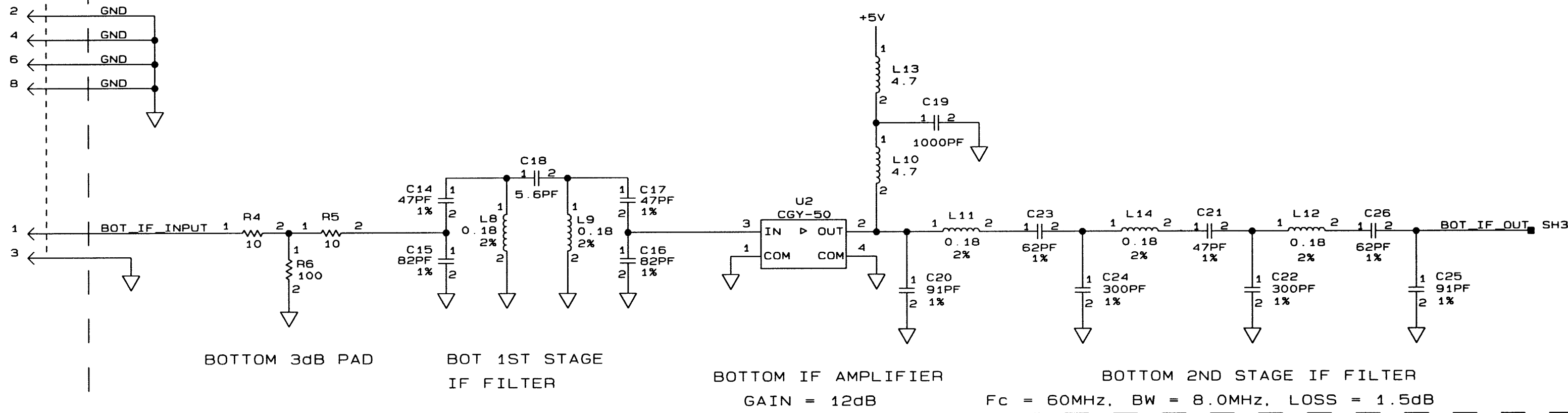
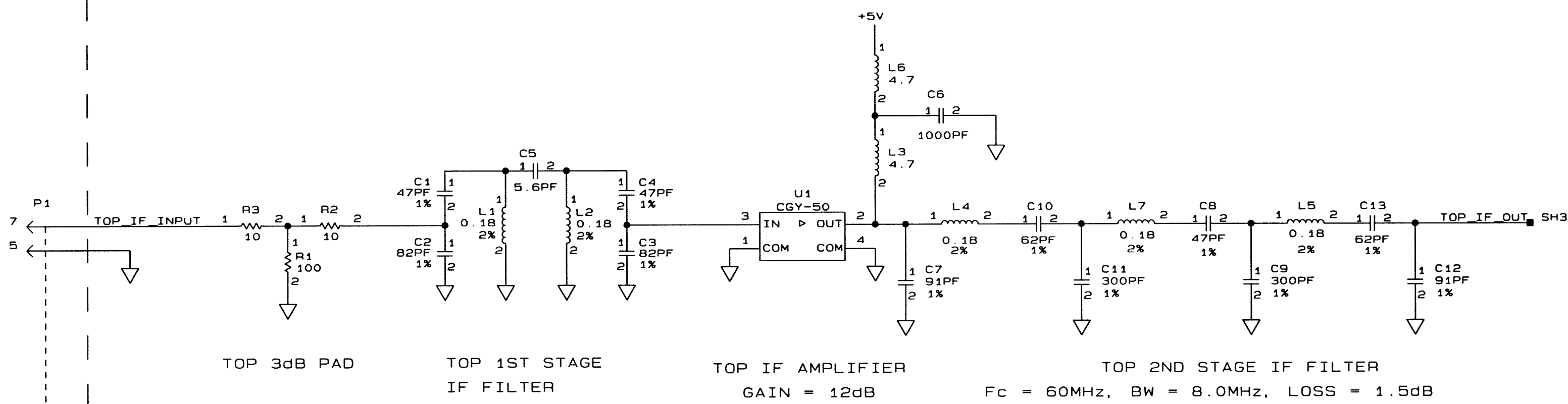
- NOTES:
 UNLESS OTHERWISE SPECIFIED:
 1. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 2. ALL RESISTANCE VALUES ARE IN OHMS.
 3. ALL INDUCTANCE VALUES ARE IN MICROHENRIES.
 4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN;
 FOR COMPLETE DESIGNATIONS PREFIX PART
 DESIGNATION WITH SUBASSEMBLY DESIGNATION.
 5. INTERPRET DRAWING PER ANSI Y32.2-1975 AND
 ANSI/IEEE STD 991-1986. LOGIC SYMBOLS
 CONFORM TO ANSI/IEEE STD 91-1984.
 6. RESISTORS R68-R71 ARE USED ONLY TO SPACE DL1
 OFF OF THE PWB. ELECTRICAL CONTACT BETWEEN
 ANY OF THESE RESISTORS AND DL1 IS PERMISSIBLE.

POWER LINE FILTERS
 SCHEMATIC DIAGRAM SHEET NO. 1 OF 12

COMPUTER GENERATED

Honeywell	SEE FIRST SHEET FOR CONTRACT NUMBER. USE OR DISCLOSURE OF INFORMATION ON THIS SHEET IS SUBJECT TO THE RESTRICTIONS ON THE FIRST SHEET OF THIS DOCUMENT.	SIZE	E	CAGE CODE	55939	DRAWING NO.	7517440-904	REV	
	SCALE							SHEET	3

7517440-904
 SHEET 3
 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100



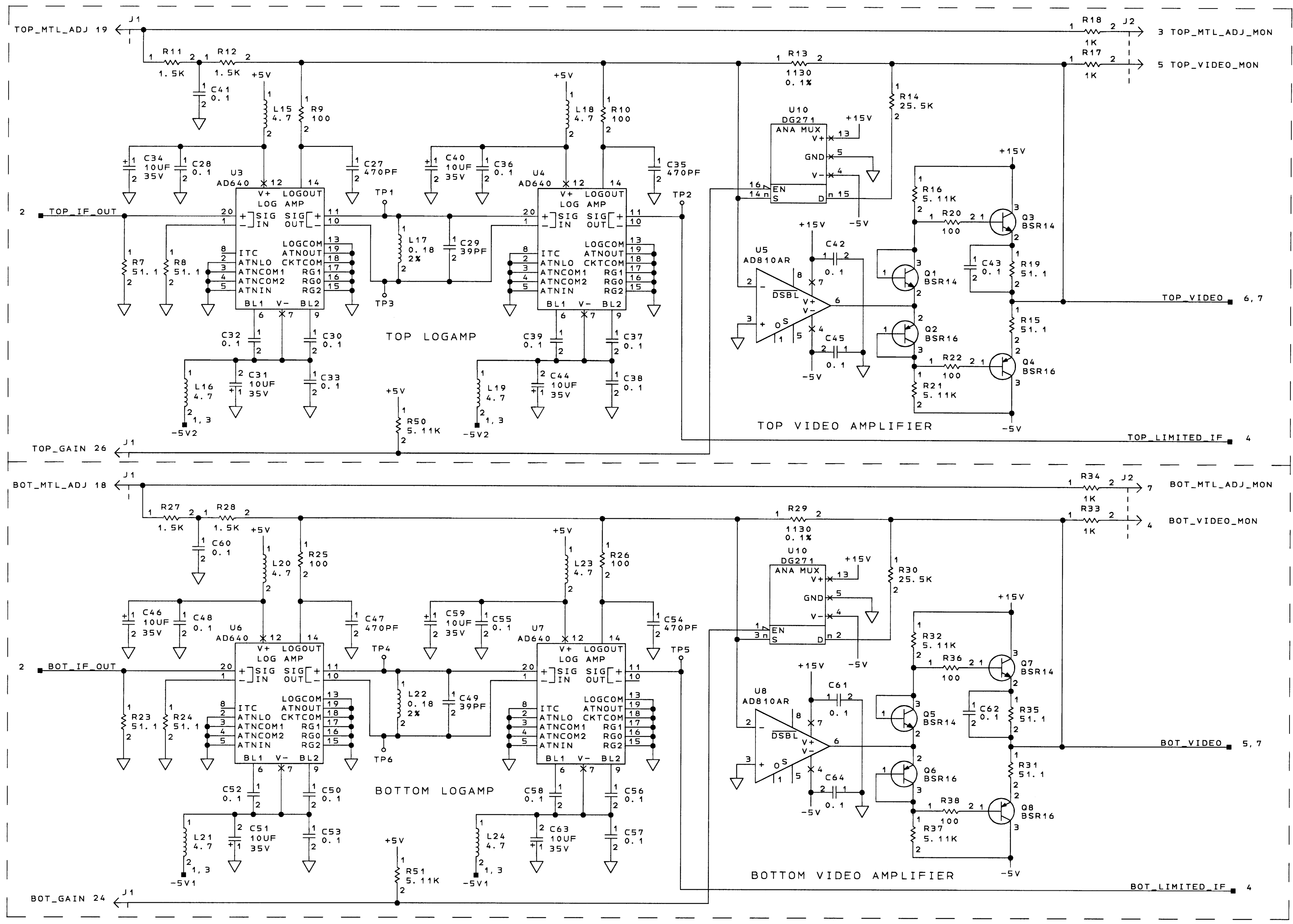
I.F. AMPLIFIER/FILTER - 60MHZ

TOP AND BOT IF AMPLIFIER AND IF FILTER

SCHMATIC DIAGRAM SHEET NO. 2

COMPUTER GENERATED

REV		DESCRIPTION	DATE	APPROVED
C4	F4	US AND UB WERE OP-160.	20 July 99	L. WISLER
		SEE DWG SH 1.	104102 (U)	



LOG AMPLIFIERS

TOP AND BOT LOG AMPS
TOP AND BOT VIDEO AMPS

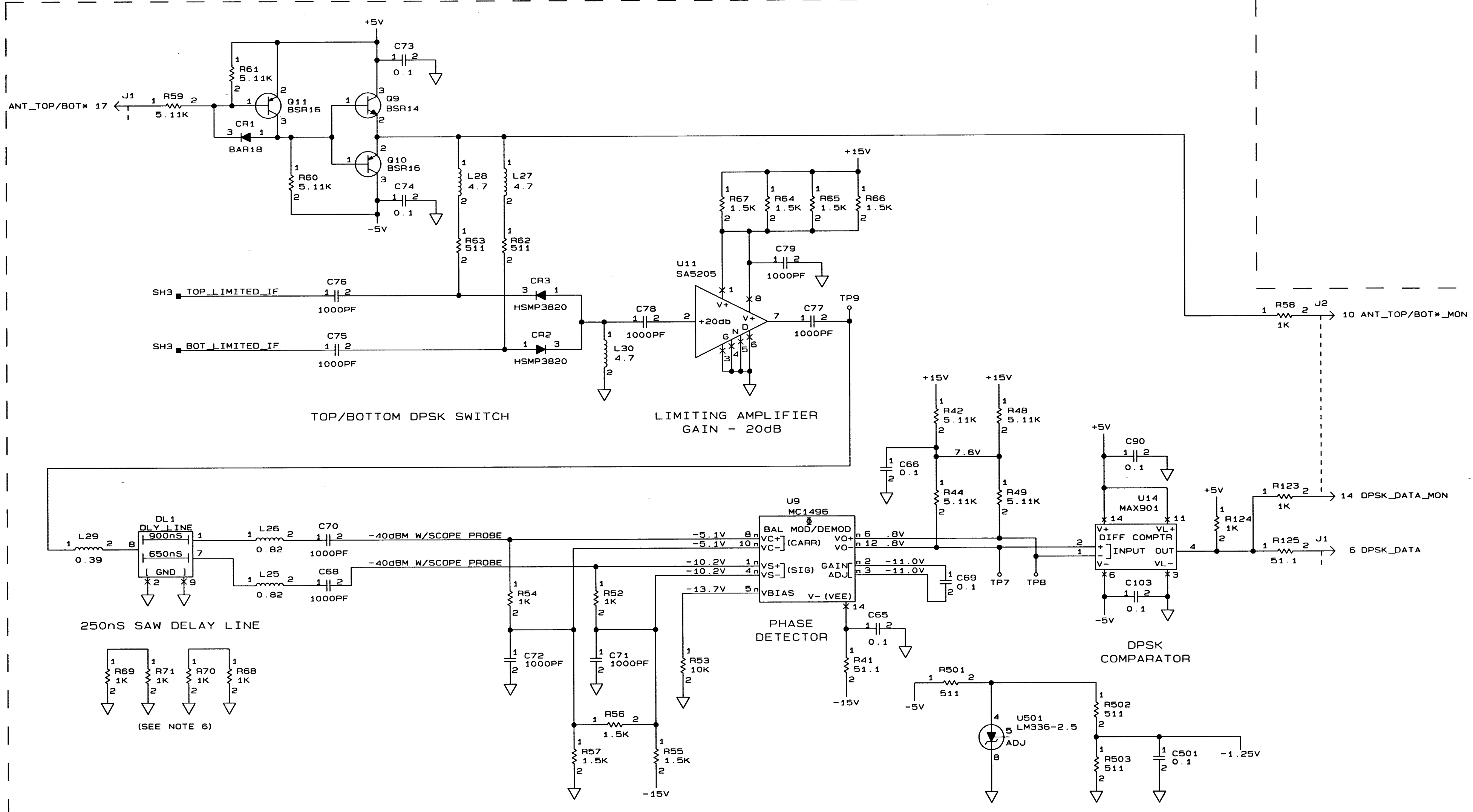
SCHEMATIC DIAGRAM SHEET NO. 3

COMPUTER GENERATED

Honeywell	SEE FIRST SHEET FOR CONTRACT NUMBER. USE OR DISCLOSURE OF INFORMATION ON THIS SHEET IS SUBJECT TO THE RESTRICTIONS ON THE FIRST SHEET OF THIS DOCUMENT.	SIZE	E 55939	DRAWING NO.	7517440-904	REV	B
	SCALE					SHEET	5

8331-841 (REV 4-88) HONEYWELL INC JAN 74, 1-1989
 7517440-904
 SHEET 5

ZONE	REV	DESCRIPTION	DATE	APPROVED
A		PARTS LIST DATA BASE CHANGE ONLY . 92041 (U) SEE DWG SHEET 1		<i>M. Moreau</i>

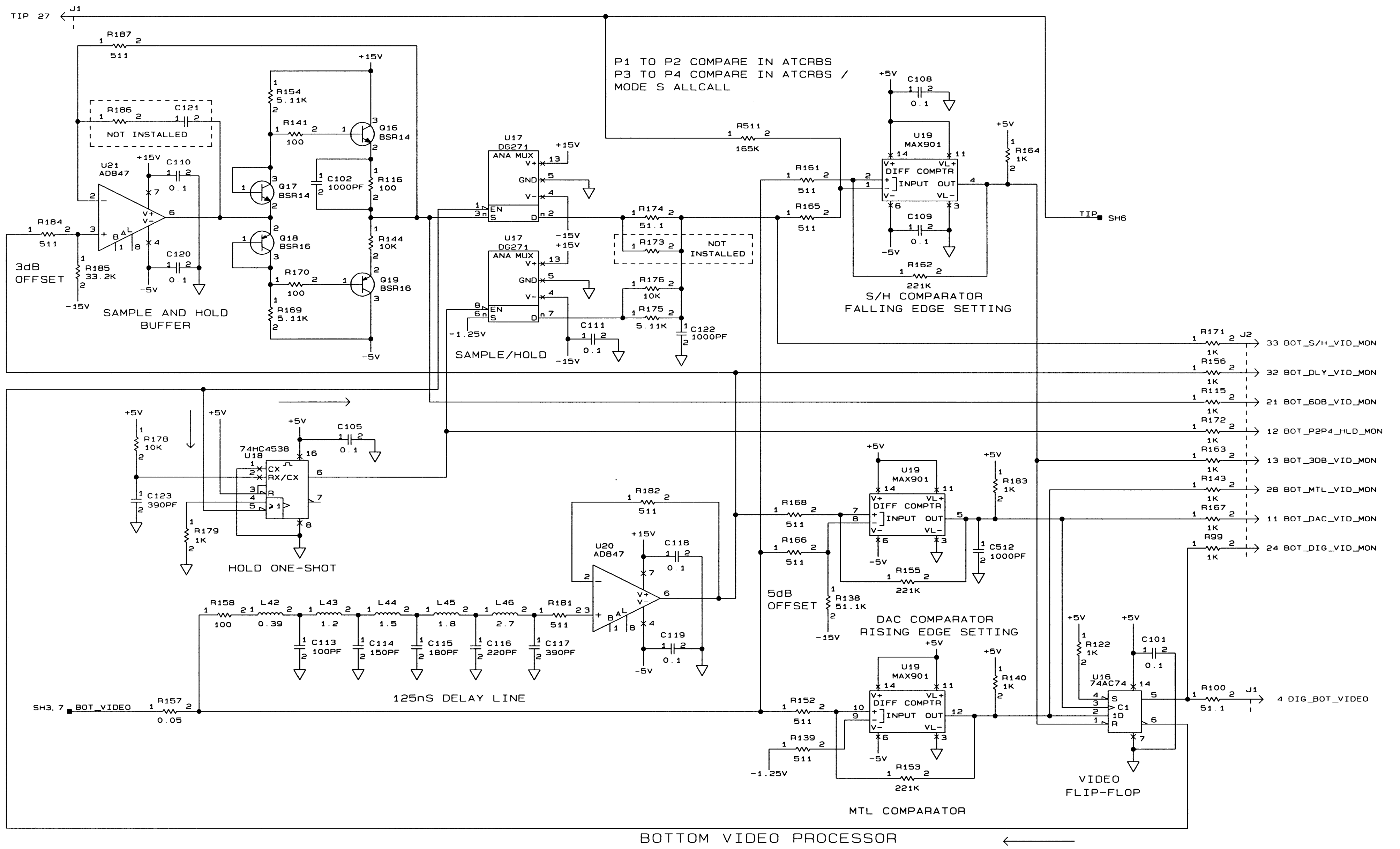


DPSK DEMODULATOR

TOP AND BOT
DPSK SWITCH/DPSK DEMODULATOR
SCHEMATIC DIAGRAM SHEET NO. 4

COMPUTER GENERATED

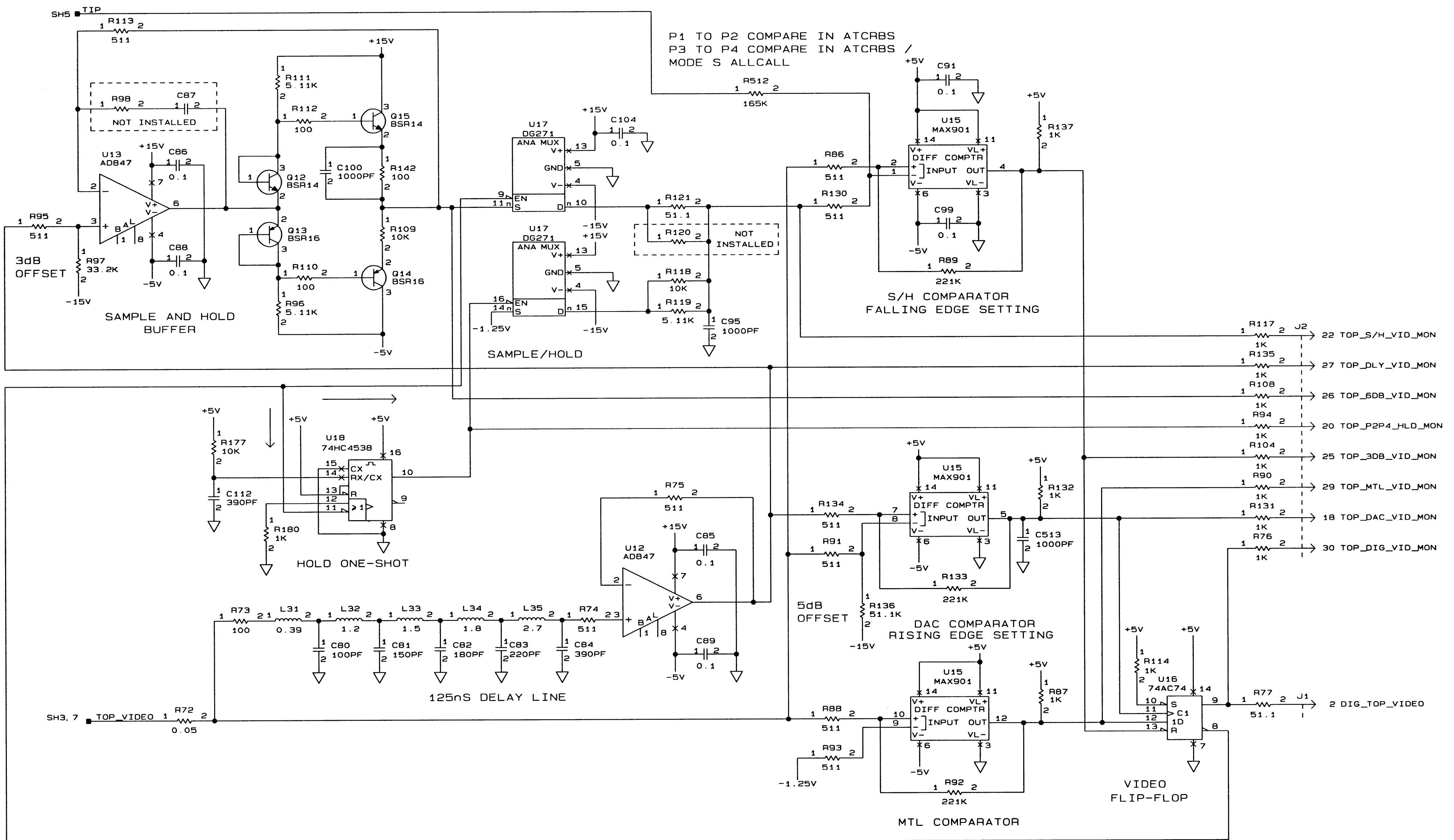
Honeywell	SEE FIRST SHEET FOR CONTRACT NUMBER. USE OR DISCLOSURE OF INFORMATION ON THIS SHEET IS SUBJECT TO THE RESTRICTIONS ON THE FIRST SHEET OF THIS DOCUMENT.	SIZE	E	CAGE CODE	55939	DRAWING NO.	7517440-904	REV	A
	SCALE		SHEET		6				



BOTTOM VIDEO PROCESSOR

BOT VIDEO PROCESSOR
SCHEMATIC DIAGRAM SHEET NO. 5

COMPUTER GENERATED



P1 TO P2 COMPARE IN ATCRBS
P3 TO P4 COMPARE IN ATCRBS /
MODE S ALLCALL

S/H COMPARATOR
FALLING EDGE SETTING

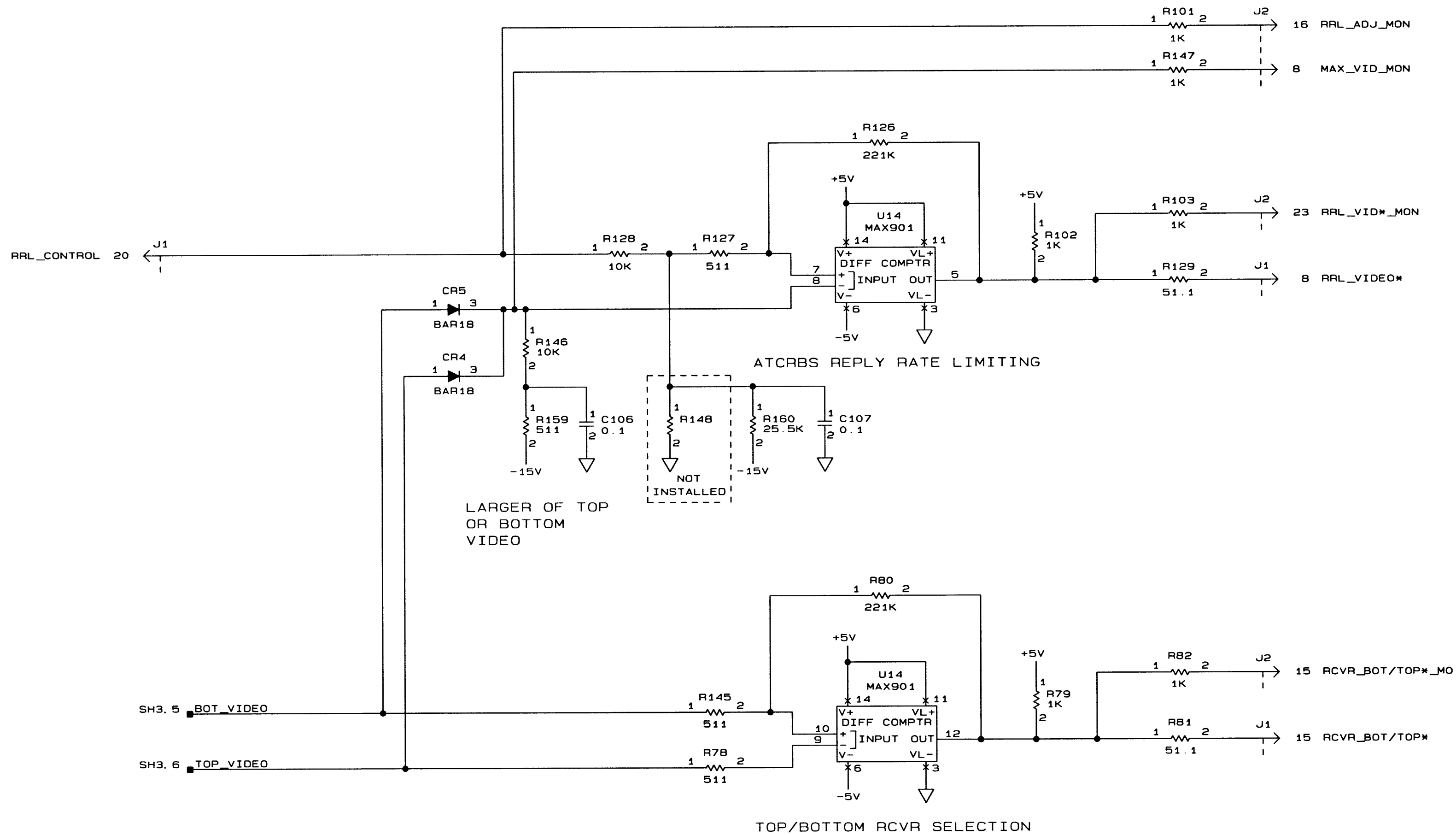
DAC COMPARATOR
RISING EDGE SETTING

VIDEO
FLIP-FLOP

TOP VIDEO PROCESSOR

TOP VIDEO PROCESSOR
SCHEMATIC DIAGRAM SHEET NO. 6

COMPUTER GENERATED



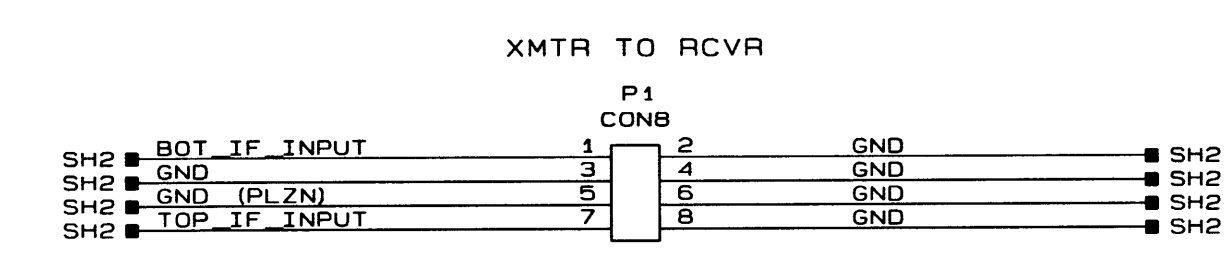
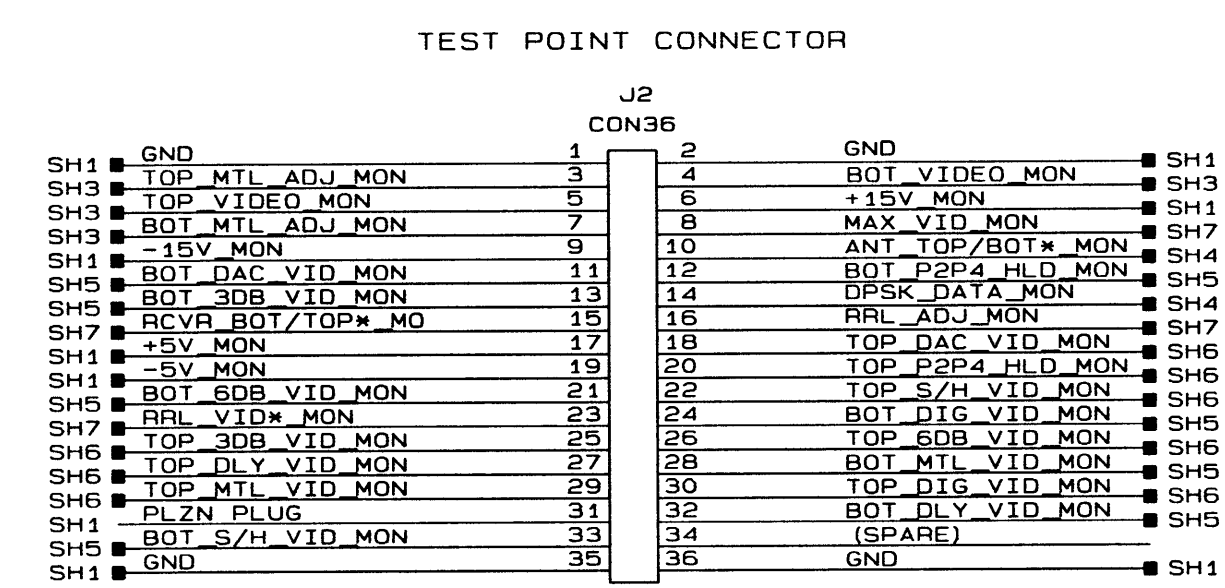
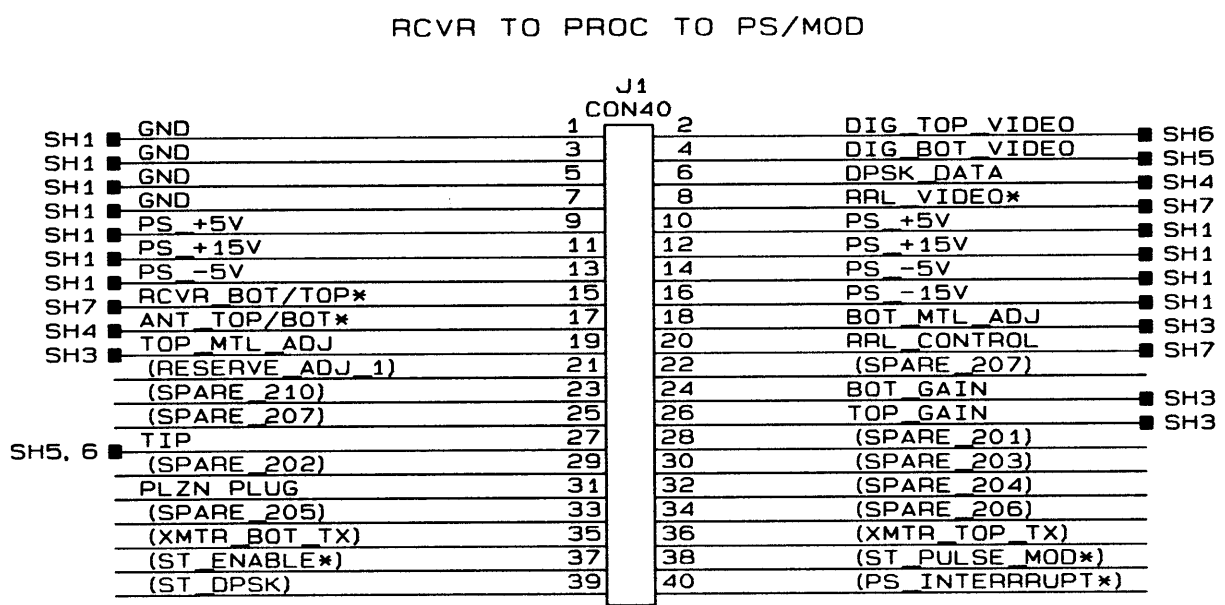
ATCRBS REPLY RATE LIMITING/TOP & BOT RCVR SELECTION

SCHEMATIC DIAGRAM SHEET NO. 7

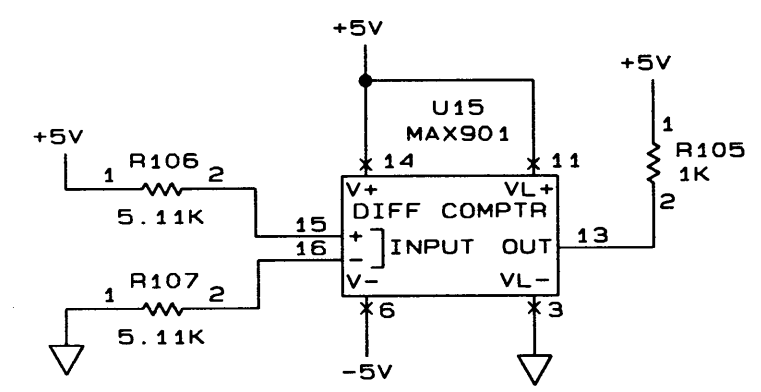
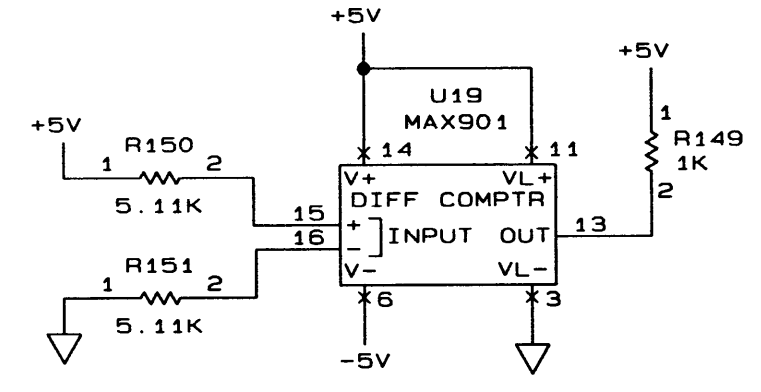
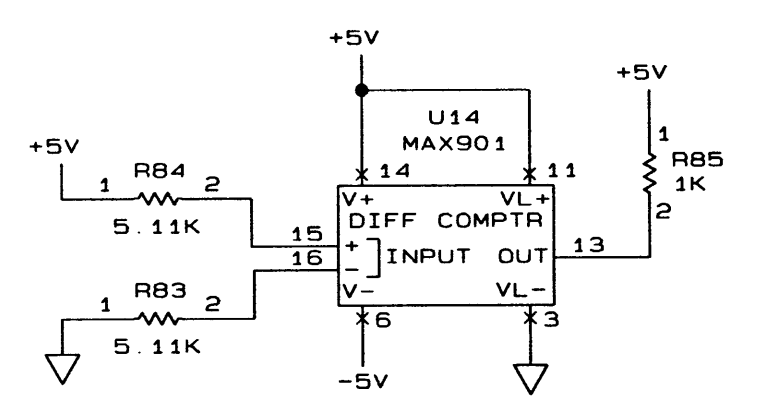
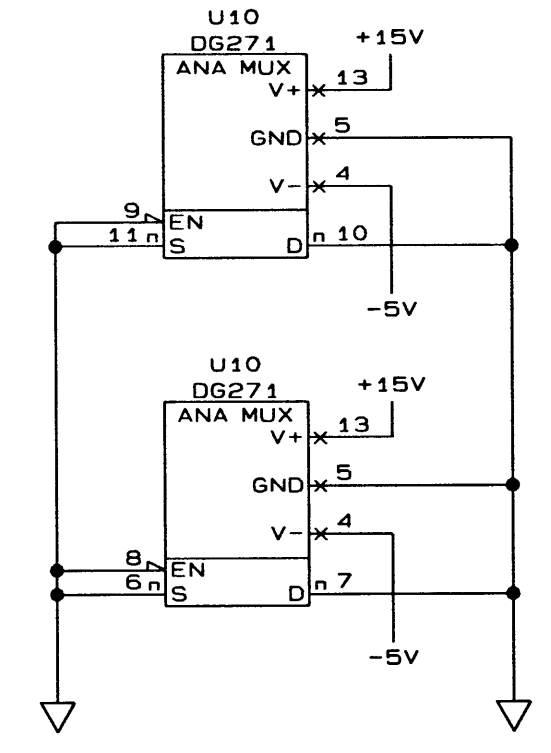
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	SCALE	—	E 55939	7517440-904	—

7517440-904 9



INTERCONNECT

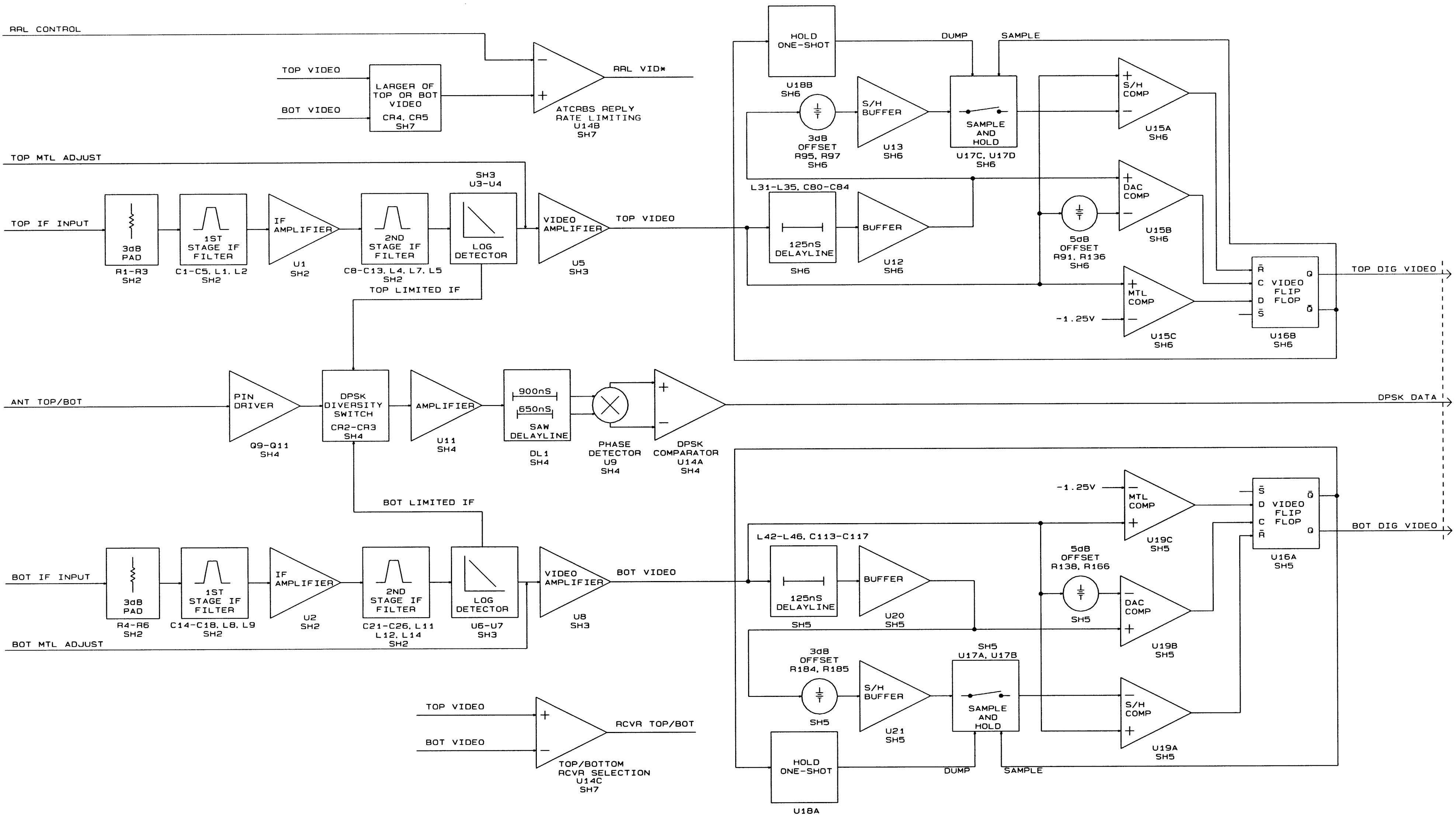


SPARES

CONNECTOR PIN SUMMARY
 AND SPARE COMPONENTS
 CAD REFERENCE/REQUIREMENT

SCHEMATIC DIAGRAM SHEET NO. 8

COMPUTER GENERATED



BLOCK DIAGRAM

DETAILED BLOCK DIAGRAM
SCHEMATIC DIAGRAM SHEET NO. 9

COMPUTER GENERATED

TEST POINT DESCRIPTIONS

TEST POINT	NAME	DESCRIPTION	VOLTAGE RANGE	LAYOUT LOCATION	SCHEMATIC LOCATION	WAVEFORM NUMBER
J2-1	GND	GND	—	—	—	—
J2-2	GND	GND	—	—	—	—
J2-3	TOP MTL ADJ	TOP MTL ADJUSTMENT VOLTAGE FROM PROCESSOR CCA	0.0 - 10.0 VDC	F6	SH3	N/A
J2-4	BOT VIDEO	BOTTOM RCVR VIDEO	STANDARD VIDEO *	F6	SH3	1. 2
J2-5	TOP VIDEO	TOP RCVR VIDEO	STANDARD VIDEO *	F6	SH3	1. 2
J2-6	+15V	+15 VOLT POWER SUPPLY MONITOR	+13.5V TO +16.5V	F6	SH1	N/A
J2-7	BOT MTL ADJ	BOTTOM MTL ADJUSTMENT VOLTAGE FROM PROCESSOR CCA	0.0 - 10.0 VDC	F6	SH3	N/A
J2-8	MAX VID	LARGER OF TOP AND BOTTOM VIDEO	STANDARD VIDEO *	F6	SH7	TBA
J2-9	-15V	-15 VOLT POWER SUPPLY MONITOR	-13.5V TO -16.5V	F6	SH1	N/A
J2-10	ANT TOP/BOT*	DPSK TOP/BOTTOM SELECT LOGIC FROM PROCESSOR CCA (LOGIC 1 = TOP)	0.8 - 3.5V LOGIC	F6	SH4	TBA
J2-11	BOT DAC VID	BOTTOM DELAY/ATTENUATE/COMPARE VIDEO (RISING EDGE = 6dB POINT ON DELAYED VIDEO)	0.8 - 3.5V LOGIC	F6	SH5	2
J2-12	BOT P2P4 HLD	BOTTOM P2/P4 HOLD ONE-SHOT OUTPUT (LOGIC 1 = HOLD)	0.8 - 3.5V LOGIC	F6	SH5	1
J2-13	BOT 3DB VID	BOTTOM S/H COMPARITOR OUTPUT	0.8 - 3.5V LOGIC	F6	SH5	5
J2-14	DPSK DATA	DPSK DATA TO PROCESSOR CCA (LOGIC 1 = PHASE CHANGE)	0.8 - 3.5V LOGIC	F6	SH4	3
J2-15	RCVR BOT/TOP*	RECEIVER TOP/BOTTOM SELECT LOGIC TO PROCESSOR (LOGIC 1 = BOTTOM SIG > TOP SIG)	0.8 - 3.5V LOGIC	F6	SH7	TBA
J2-16	RRL CONTROL	REPLY RATE LIMITING CONTROL FROM PROCESSOR CCA (LARGER VOLTAGE -> HIGHER MTL)	0.0 - 10.0 VDC	F6	SH7	N/A
J2-17	+5V	+5 VOLT POWER SUPPLY MONITOR	+4.75V TO +5.25V	F6	SH1	N/A
J2-18	TOP DAC VID	TOP DELAY/ATTENUATE/COMPARE VIDEO (RISING EDGE = 6dB POINT ON DELAYED VIDEO)	0.8 - 3.5V LOGIC	F6	SH6	2
J2-19	-5V	-5 VOLT POWER SUPPLY MONITOR	-4.50V TO -5.50V	F6	SH1	N/A
J2-20	TOP P2P4 HLD	TOP P2/P4 HOLD ONE-SHOT OUTPUT (LOGIC 1 = HOLD)	0.8 - 3.5V LOGIC	F6	SH6	1
J2-21	BOT 6DB VID	BOTTOM VIDEO OFFSET BY 6dB	STANDARD VIDEO *	F6	SH5	2
J2-22	TOP S/H VID	TOP SAMPLE/HELD VIDEO	STANDARD VIDEO *	F6	SH6	1
J2-23	RRL VID*	ATCRBS REPLY RATE LIMITED VIDEO (LOGIC 0 = VIDEO ABOVE ATCRBS RRL THRESHHOLD)	0.8 - 3.5V LOGIC	F6	SH7	TBA
J2-24	BOT DIG VID	BOTTOM VIDEO (LOGIC 1 = SIGNAL PRESENT)	0.8 - 3.5V LOGIC	F6	SH5	5
J2-25	TOP 3DB VID	TOP S/H COMPARITOR OUTPUT	0.8 - 3.5V LOGIC	F6	SH6	5
J2-26	TOP 6DB VID	TOP VIDEO OFFSET BY 6dB	STANDARD VIDEO *	F6	SH6	2
J2-27	TOP DLY VID	TOP DELAYED VIDEO	STANDARD VIDEO *	F6	SH6	2
J2-28	BOT MTL VID	BOTTOM MTL VIDEO (LOGIC 1 = SIGNAL ABOVE MTL)	0.8 - 3.5V LOGIC	F6	SH5	5
J2-29	TOP MTL VID	TOP MTL VIDEO (LOGIC 1 = SIGNAL ABOVE MTL)	0.8 - 3.5V LOGIC	F6	SH6	5
J2-30	TOP DIG VID	TOP VIDEO (LOGIC 1 = SIGNAL PRESENT)	0.8 - 3.5V LOGIC	F6	SH6	5
J2-31	POLARIZATION PLUG	POLARIZATION PLUG	—	—	—	—
J2-32	BOT DLY VID	BOTTOM DELAYED VIDEO	STANDARD VIDEO *	F6	SH5	TBA
J2-33	BOT S/H VID	BOTTOM SAMPLE/HELD VIDEO	STANDARD VIDEO *	F6	SH6	1
J2-34	SPARE	SPARE	—	—	—	—
J2-35	GND	GND	—	—	—	—
J2-36	GND	GND	—	—	—	—
TP1	TOP LOGAMP INTERSTAGE (+)	TOP LOGAMP INTERSTAGE (+)	TBD Vp-p (60MHZ)	F5	SH3	4
TP2	TOP LIMITED IF	LIMITER OUTPUT OF TOP LOGAMP	TBD Vp-p (60MHZ)	F5	SH3	TBA
TP3	TOP LOGAMP INTERSTAGE (-)	TOP LOGAMP INTERSTAGE (-)	TBD Vp-p (60MHZ)	F6	SH3	4
TP4	BOT LOGAMP INTERSTAGE (+)	BOTTOM LOGAMP INTERSTAGE (+)	TBD Vp-p (60MHZ)	E5	SH3	4
TP5	BOT LIMITED IF	LIMITER OUTPUT OF BOTTOM LOGAMP	TBD Vp-p (60MHZ)	E5	SH3	TBA
TP6	BOT LOGAMP INTERSTAGE (-)	BOTTOM LOGAMP INTERSTAGE (-)	TBD Vp-p (60MHZ)	E6	SH3	4
TP7	PHASE DETECTOR (-)	DPSK PHASE DETECTOR OUTPUT (-)	TBD Vp-p (60MHZ)	E6	SH3	4
TP8	PHASE DETECTOR (+)	DPSK PHASE DETECTOR OUTPUT (+)	TBD Vp-p	E4	SH4	3
TP9	DPSK LIMITER	OUTPUT OF DPSK AMPLIFIER	TBD Vp-p	E5	SH4	TBA
			TBD Vp-p (60MHZ)	E4	SH4	TBA

* STANDARD VIDEO : MTL = -1.25 VOLTS
GAIN = 50mV/dB

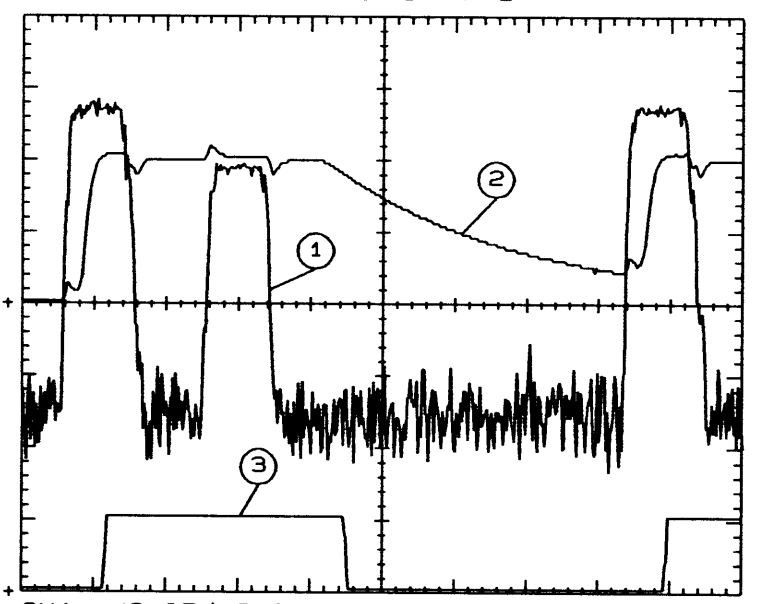
TEST POINT TABLE
SCHEMATIC DIAGRAM SHEET NO. 10

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7517440-904 12

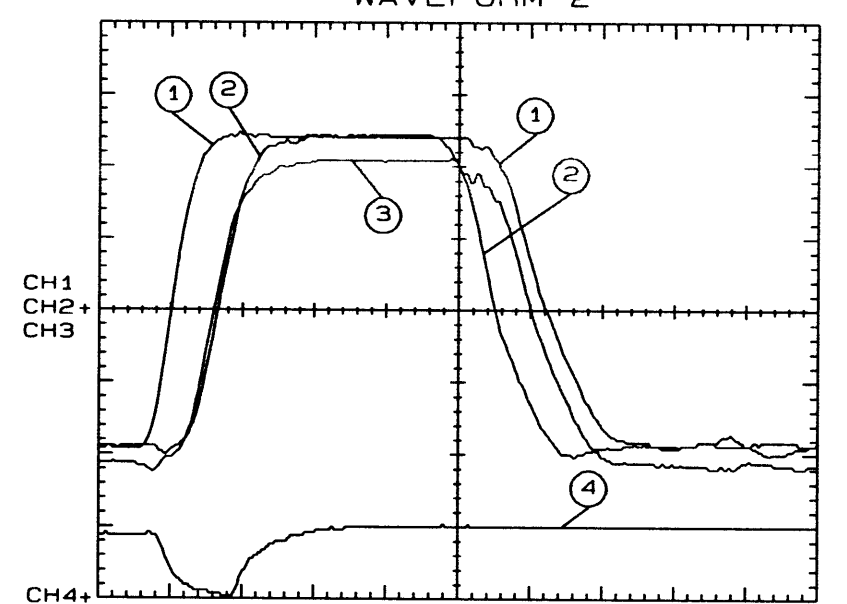
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

WAVEFORM 1



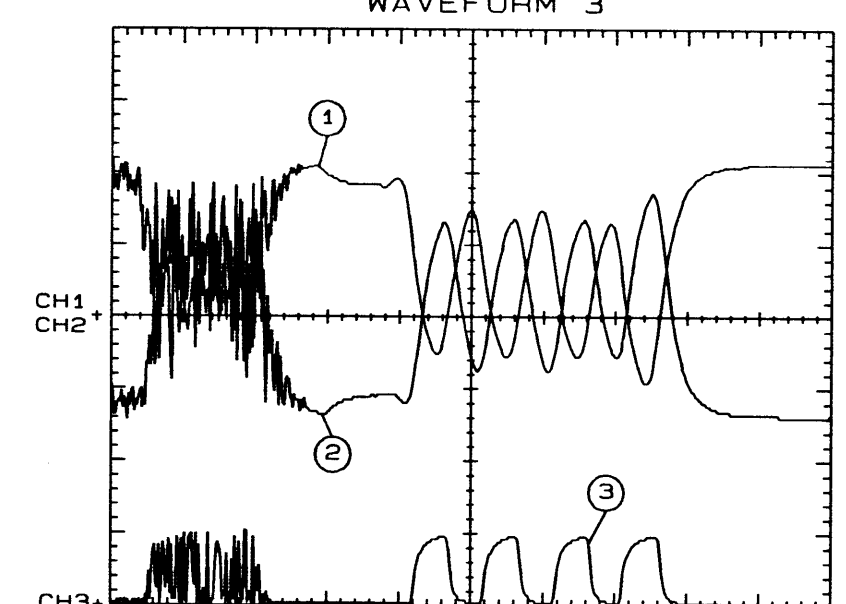
CH1, J2-05/J2-04, 0.5V/DIV, TOP/BOT VIDEO
 CH2, J2-22/J2-33, 0.5V/DIV, TOP/BOT S/H VIDEO
 CH3, J2-20/J2-33, 5.0V/DIV, TOP/BOT P2/P4 HOLD
 TIMEBASE : 1µS/DIV

WAVEFORM 2



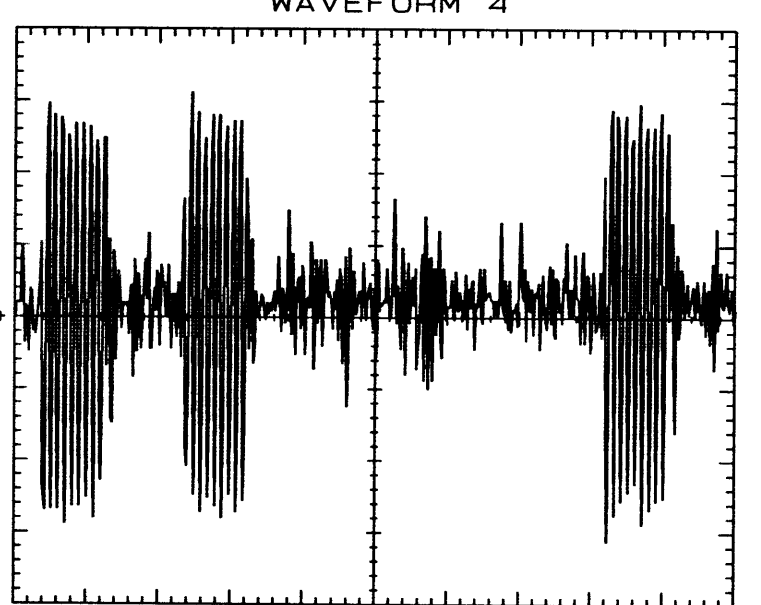
CH1, J2-05/J2-04, 0.5V/DIV, TOP/BOT VIDEO
 CH2, J2-27/J2-32, 0.5V/DIV, TOP/BOT DLY VIDEO
 CH3, J2-26/J2-21, 5.0V/DIV, TOP/BOT 60B VIDEO
 CH4, J2-18/J2-11, 5.0V/DIV, TOP/BOT DAC VIDEO
 TIMEBASE : 200ns/DIV

WAVEFORM 3



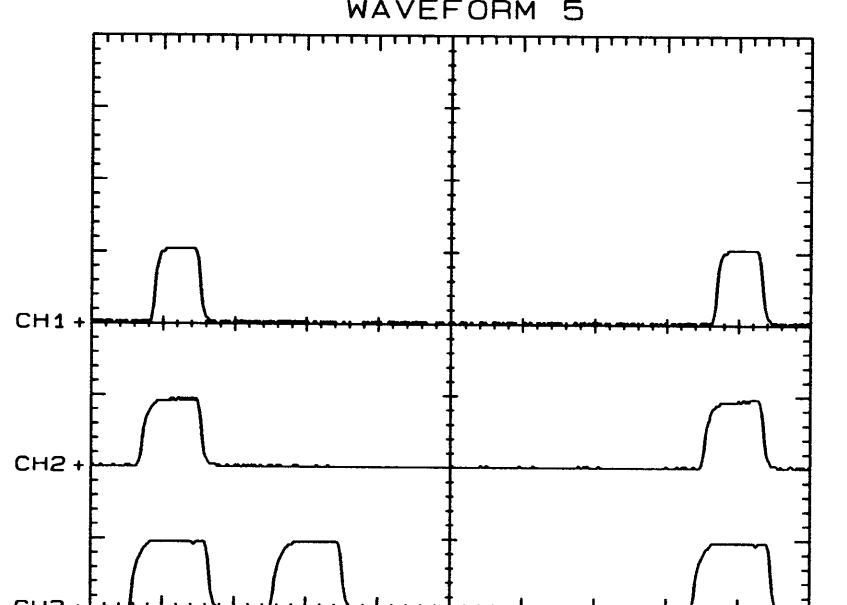
CH1, TP8, 1.0V/DIV, PHASE DET (+)
 CH2, TP7, 1.0V/DIV, PHASE DET (-)
 CH3, J2-14, 5.0V/DIV, DPSK DATA
 TIMEBASE : 500ns/DIV

WAVEFORM 4



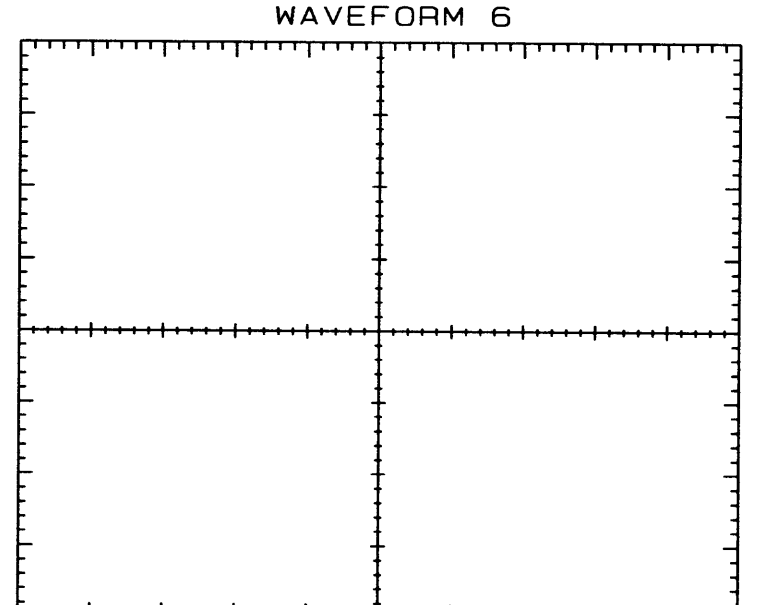
CH1, TP1/ETC, 20mV/DIV, LOGAMP INTERSTAGE
 SAME AS TP7, TP8, TP10
 TIMEBASE : 1µS/DIV
 SIGNAL LEVEL : -32dBm

WAVEFORM 5

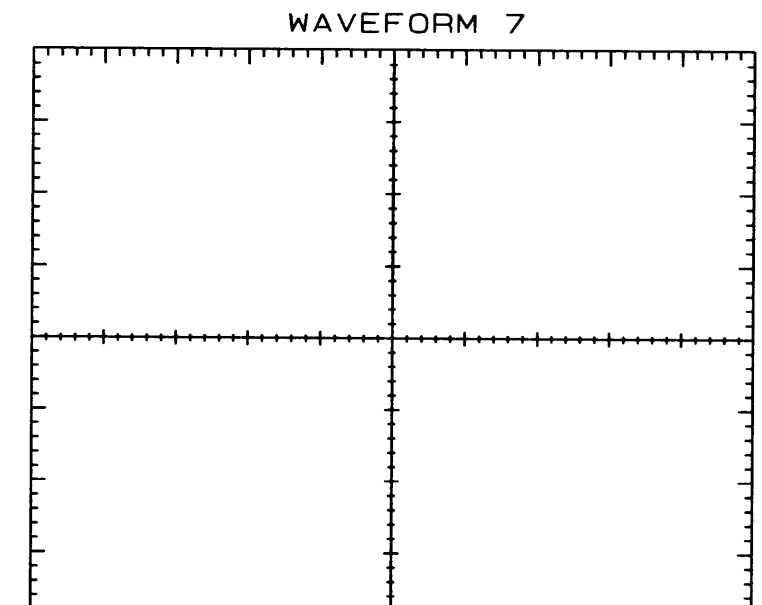


CH1, J2-30/J2-24, 5.0V/DIV, TOP/BOT DIG VIDEO
 CH2, J2-25/J2-13, 5.0V/DIV, TOP/BOT 30B VIDEO
 CH3, J2-28/J2-07, 5.0V/DIV, TOP/BOT MTL VIDEO
 TIMEBASE : 1µS/DIV

WAVEFORM 6



WAVEFORM 7

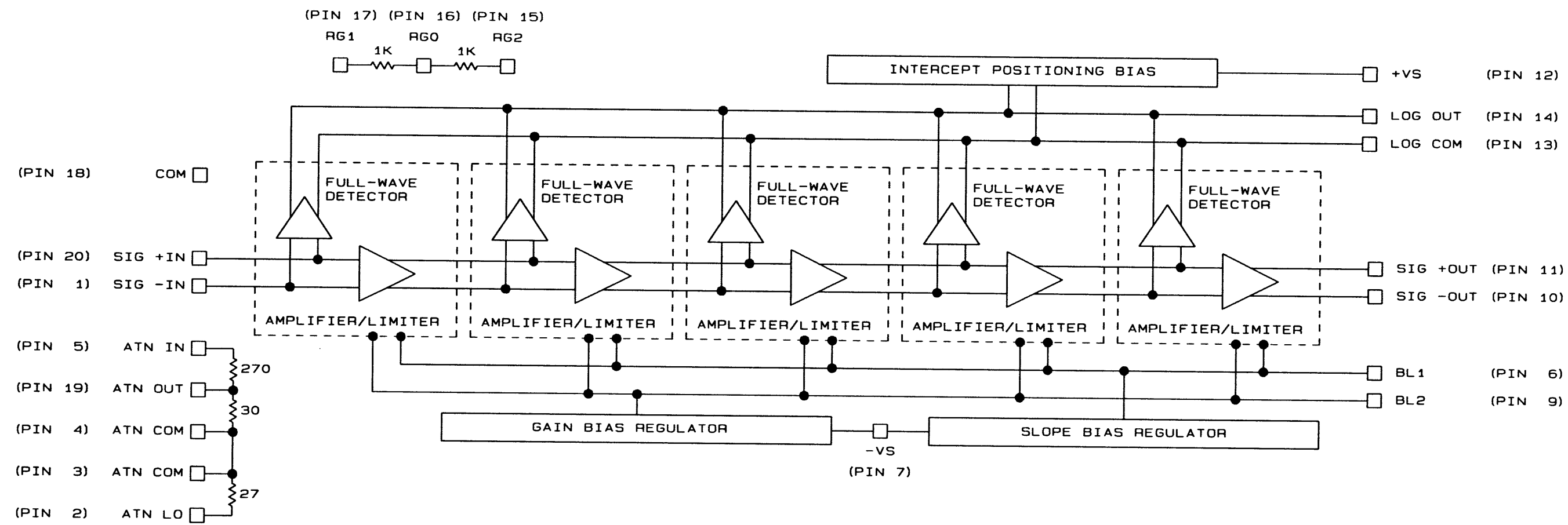


TEST POINT WAVEFORMS
 SCHEMATIC DIAGRAM SHEET NO. 11

COMPUTER GENERATED

7517440-904 13

REVISIONS			
ZONE	REV	DESCRIPTION	DATE



AD640 LOGAMP BLOCK DIAGRAM
 SCHEMATIC DIAGRAM SHEET NO. 12

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		SCALE					SHEET 14

7517440-904
 1 of 10 sheets
 SHEET 14