UAA3537G

Low power GSM/GPRS multi-band transceiver

Rev. 0.09 — 6 January 2005 **Preliminary Specification**

1. General description

The UAA3537 is a fully-integrated GSM hand-held transceiver

2. Features

- Multiple band application (850, 900, 1800 and 1900 MHz frequency bands).
- Low noise and wide dynamic range low IF receiver
- GPRS multi slot class 12 capable
- More than 3 dB on chip image rejection in receive
- More than 68 dB gain control range in receive
- Direct-up conversion in transmit
- Fully-integrated fractional-N RF-synthesizer with AFC control possibility
- Fully-integrated RF VCO with integrated supply regulator
- semi-integrated reference oscillator with integrated supply regulator
- Fully differential design to minimize cross-talk and spurs
- Functional down to 2.4 V and up to 3.0 V
- Three output to control RF frontend switches (pin diodes)
- 3-wire serial bus interface
- HVQFN40 package

3. Applications

- GSM 850 MHz, GSM 900 MHz, DCS 1800 MHz and PCS 1900 MHz hand-held transceiver.

4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply voltage	note 1	2.4		3.0	V
T_{amb}	operating ambient temperature		-30		70	°C

[1] for V_{CC} <2.7 V only functionality is guaranted, AC characteristics are not guaranted

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5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
UAA3537GHN	HVQFN40	micro leadframe package; 40 leads; body 6x 6x 0.85 mm	SOT618-1

6. Block diagram

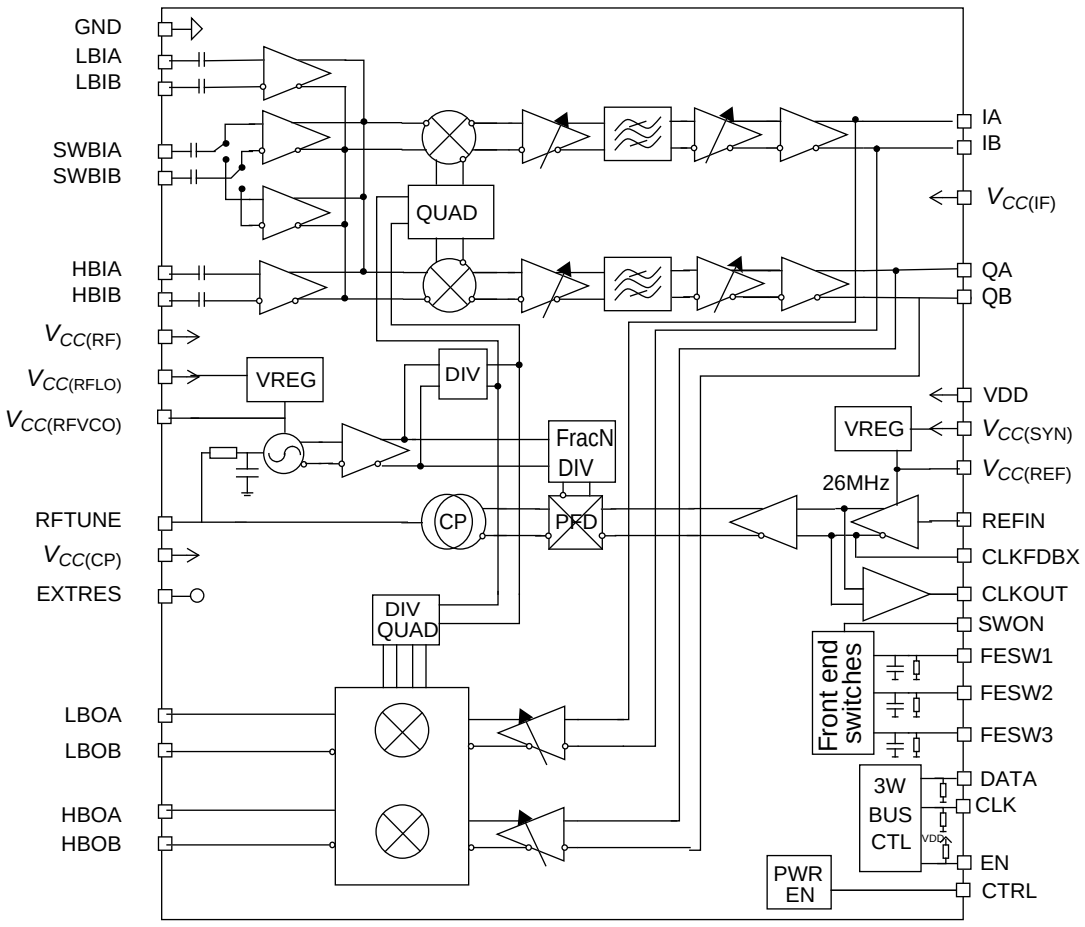


Fig 1. Block diagram.

7. Pinning information

7.1 Pinning

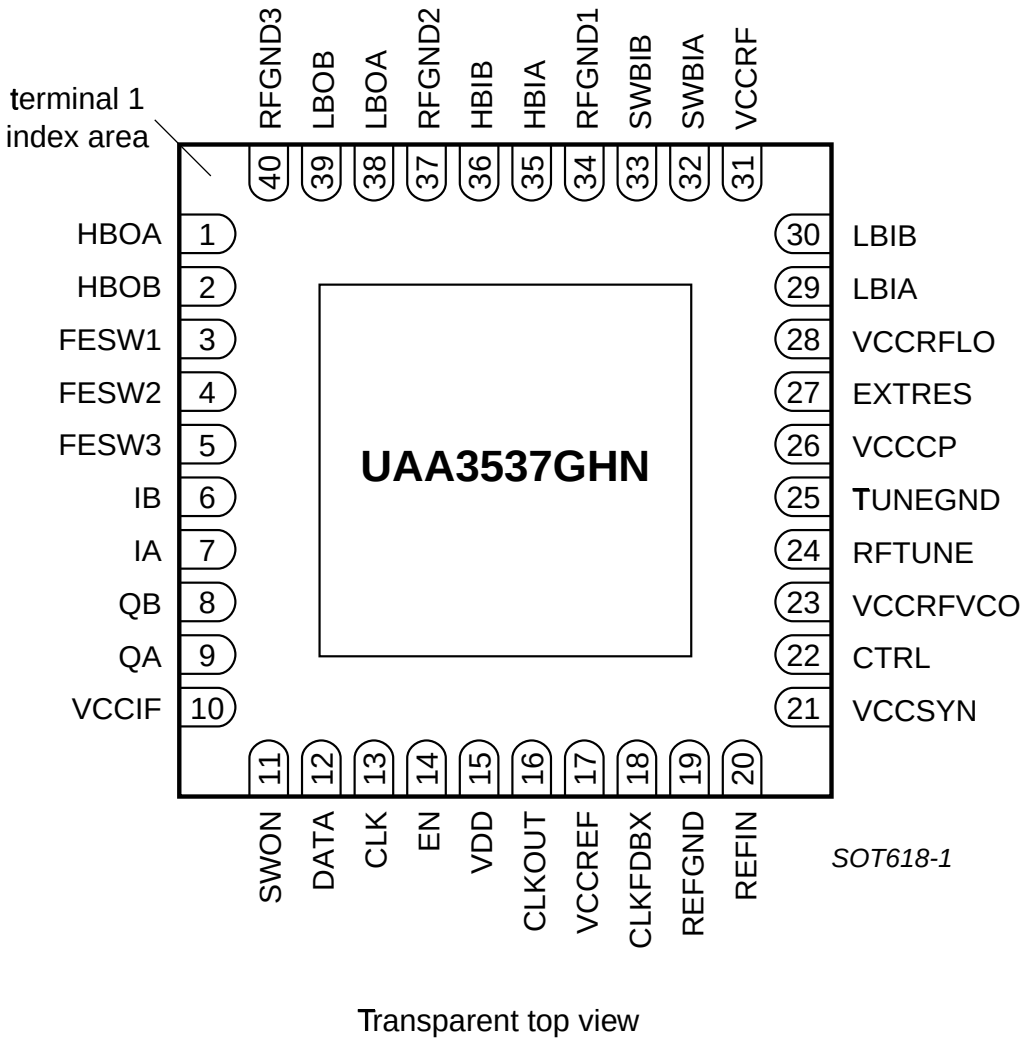


Fig 2. Pin configuration (Transparent top view)).

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
HBOA	1	DCS1800 and PCS1900 bands RF output
HBOB	2	DCS1800 and PCS1900 bands RF output
FESW1	3	front end switch control output
FESW2	4	front end switch control output
FESW3	5	front end switch control output
IB	6	baseband input-output; I path

Table 3: Pin description...*continued*

Symbol	Pin	Description
IA	7	baseband input-output; I path
QB	8	baseband input-output; Q path
QA	9	baseband input-output; Q path
$V_{CC(IF)}$	10	IF supply
SWON	11	front end switch control input
DATA	12	3-wire bus; DATA input
CLK	13	3-wire bus; CLK input
EN	14	3-wire bus; ENABLE control pin
VDD	15	digital supply
CLKOUT	16	reference oscillator output
$V_{CC(REF)}$	17	reference regulator output and reference supply
CLKFDBX	18	reference oscillator feedback
REFGND	19	GND for reference oscillator
REFIN	20	reference oscillator input
$V_{CC(SYN)}$	21	synthesizer and reference regulator supply
CTRL	22	global enable control pin
$V_{CC(RFVCO)}$	23	RFVCO regulator output and RF VCO supply
RFTUNE	24	tuning input of RF VCO
TUNEGND	25	ground for RF VCO tuning
$V_{CC(CP)}$	26	RF charge pump supply
EXTRES	27	reference resistor for RF PLL charge pump gains
$V_{CC(RFLO)}$	28	RF LO and RFVCO regulator supply
LBIA	29	receiver GSM850/900 RF input
LBIB	30	receiver GSM850/900 RF input
$V_{CC(RF)}$	31	RF front end and transmit part supply
SWBIA	32	receiver DCS1800/PCS1900 or GSM850/900 switched RF input
SWBIB	33	receiver DCS1800/PCS1900 or GSM850/900 switched RF input
RFGND1	34	ground for front end
HBIA	35	receiver DCS1800 or PCS1900 bands RF input
HBIB	36	receiver DCS1800 or PCS1900 bands RF input
RFGND2	37	ground for front end
LBOA	38	GSM850 and GSM900 RF output
LBOB	39	GSM850 and GSM900 RF output
RFGND3	40	ground for front end

8. Functional description

8.1 Receiver

The receiver consists of two distinct parts, the RF receiver front-end and the IF section. The RF receiver front-end amplifies the GSM850 (869-894) GSM900 (925-960 MHz), DCS1800 (1805-1880 MHz) or PCS1900 (1930-1990 MHz) aerial signal, converts the chosen channel down to a low IF of -100 kHz, and provides in addition more than 35 dB image suppression. Four LNAs are available on chip and can be configured to allow 3 bands (low, high and switched). The switched LNA will be used for roaming in different countries. Some selectivity is provided at this stage by an on-chip low-pass filter, and channel selectivity is provided by means of a high performance integrated band-pass filter. The IF section further amplifies the wanted channel, performs gain control to tune the output level to the desired value and rejects DC. This DC rejection is realised with an active high pass circuit and operates either continuously or keeps the acquired offset correction during the burst depending on the programming.

8.2 Transmitter

The transmitter is fully differential using a direct-up conversion architecture. It consists of a single side band power up mixer. Gain is set over 6 dB via the 3-wire serial programming bus. The fully-integrated VCO and the power mixer are designed to achieve LO suppression, quadrature phase error, quadrature amplitude balance and low noise floor specifications.

8.3 Local oscillator

The local oscillator (LO) signals required are provided by an on chip VCO for operation of the receive and transmit sections. The VCO is fully-integrated and self calibrating to reduce manufacturing tolerances. It consists of 64 differents frequency ranges that are selected internally depending on frequency programming. The frequencies of the RF VCO are set by an internal fractional-N synthesiser PLL circuit, which are programmable via a 3-wire serial bus. Comparison frequency is 26 MHz (24 Hz step programmability) derived from the 26 MHz reference signal which is generated from the semi-integrated reference oscillator. The quadrature phase RF LO signals required for IQ mixers are generated internally.

8.4 Reference Oscillator

An amplifier is integrated to build a crystal oscillator. Externally only a quartz and few passive components are needed. 26 MHz is the reference frequency. It is turned on when the supply voltage $V_{CC(SYN)}$ is applied. After buffering a reference clock of 26 MHz is supplied to the other parts of the system through the pin CLKOUT. An internal supply voltage regulator using $V_{CC(SYN)}$ as input supplies the reference oscillator and minimizes parasitic couplings and pushing. AFC can be done by the fractional-N synthesiser programming or via an external varactor. Additionally a coarse AFC control with a resolution of 8 bit is integrated via switchable capacitors. The programming of the coarse AFC capacitors is maintained during sleep mode as the

register memory is supplied via the continuous digital supply VDD. The reference signal (26 MHz) can alternatively be supplied from an external module (to pin REFIN). This module can be supplied through $V_{CC(REF)}$ pin.

8.5 Control

The circuit can be powered-up into four different modes, RX, TX, SYN or REF mode, depending on supply voltages applied, on the logic level at pin CTRL and on the 3-wire bus serial programming. In RX (TX) mode, all sections required for receive (transmit) are turned on. The SYN mode is used to power-up the synthesiser and the RF-VCO prior to the RX or TX mode. In the SYN mode, some internal LO buffers are also powered-up such that VCO pulling is minimized when switching on the receiver or the transmitter. The reference oscillator (REF mode) is turned on by applying the supply voltage. Additionally band selection is done using the 3-wire bus serial programming allowing the proper enabling of the LNAs

8.6 Control of front end switches

Three output are provided to drive RF switches of the phone, e.g. for switching between bands.

9. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
T_{stg}	storage temperature		-40	+150	°C
T_{amb}	operating ambient temperature		-30	+70	°C
P_{tot}	total power dissipation			500	mW
V_{CC}	analog supply voltage	on all V_{CC}, LBOA, LBOB, HBOA and HBOB	-0.3	3.3	V
V_{DD}	digital supply voltage	on V_{DD}	-0.3	2.75	V

10. Thermal characteristics

Table 5: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
Rth(j-a)	thermal resistance from junction to ambient with exposed diepad soldered on 4-layer PCB	in free air	25	K/W

11. Characteristics

Table 6: DC Characteristics

V_{CC} = 2.7V; V_{DD} = 1.8V; T_{amb} = 25 °C; unless otherwise stated

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pin $V_{CC(RF)}$, $V_{CC(IF)}$,$V_{CC(RFLO)}$, $V_{CC(SYN)}$, $V_{CC(CP)}$, LBOA, LBOB, HBOA and HBOB, V_{DD}						
V_{CC}	Analog supply range	note 1	2.4	2.8	3.0	V
V_{DD}	Digital supply range	note 2	1.3	1.8	2	V
I_{CCREF}	supply current REF mode	reference oscilator active ($V_{CC(SYN)}$ = 2.7V)	-	4.7	6.0	mA
I_{CCSYN}	supply current SYN mode	SYN mode active, SYNTX=0 SYN mode active, SYNTX=1	- -	31 42	40 52	mA
I_{CCRX}	supply current RX mode	RX and SYN mode active; FESW off	-	65	82	mA
$I_{CCTX;LB}$	Low band supply current TX mode	TX and SYN mode active; FESW off; G1TX1 = 0; BND2 = 0; note 4	-	120	145	mA
$I_{CCTX;HB}$	High band supply current TX mode	TX and SYN mode active; FESW off; G1TX1 = 1; BND2 = 1; note 4	-	110	135	mA
I_{IN_TX}	supply current on TX outputs (LBOA, LBOB, HBOA, HBOB)		-	34	-	mA
I_{IDDLE}	supply current in idle mode	V_{CC} = 0 or open, V_{DD} = 1.8V	-	10	30	µA
I_{DD}	digital supply current	SYN mode active	-	1	2	mA
Pins IA, IB, QA and QB						
V_{CM_IQ}	common mode IQ voltage range	$(V_{IA}+V_{IB})/2$ or $(V_{QA}+V_{QB})/2$; note 3	1.15	1.25	1.35	V
Pin $V_{CC(REF)}$						
$V_{CC(REF)}$	internal supply voltage of reference oscillator	$V_{CC(SYN)} \geq 2.7V$, $-30 \leq T_{amb} \leq 70°C$	2.3	2.4	2.5	V
I_{OUTREF}	output current		2	-	-	mA
Pin $V_{CC(RFVCO)}$						
$V_{CC(RFVCO)}$	internal supply voltage of RF VCO		-	2.0	-	V
Pin EXTRES						
V_{EXTRES}	reference voltage	R_{ext} = 3.3 kΩ (1%)	-	0.35	-	V
Pins REFIN, CLKFDBX, CLKOUT						
V_{REFIN}	intern. supplied DC input voltage		1.0	1.1	1.2	V
$V_{CLKFDBX}$	DC output voltage		1.5	1.8	2.1	V
V_{CLKOUT}	DC output voltage		-	$V_{CC(SYN)}$ -1.6	-	V
Pins FESW1, FESW2, FESW3						
V_{FESW}	output voltage	I_{SOURCE} = 10 mA	2.5	-	-	V

Table 6: DC Characteristics...*continued*

V_{CC} = 2.7V; V_{DD} = 1.8V; T_{amb} = 25 °C; unless otherwise stated

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{FESW}	Resistor to GND		-	10	-	kΩ
C_{FESW}	Capacitor to GND		-	10	-	pF
Digital input levels: pins EN, DATA, CLK, CTRL, SWON						
V_{IH}	logic HIGH level		0.8*VDD	-	VDD+0.3	V
V_{IL}	logic LOW level		-0.3	-	0.2*VDD	V
Pull up resistor: pin EN						
R_{UP}	Resistor to V_{DD}		-	1	-	MΩ
Pull Down resistors: pins DATA, CLK, CTRL, SWON						
R_{DOWN}	Resistor to GND		-	1	-	MΩ

[1] For V_{CC}<2.7 V only functionnality are guaranted, AC characteristics are not guaranted

[2] For VDD < 1.6V only data retention of the internal registers is guaranted

[3] RX mode: DC supplied from the IC
TX mode: DC supplied from external

[4] when FESW are on, current drawn from FESW pins will be supplied from $V_{CC(RF)°}$

Table 7: RF Receiver AC Characteristics

V_{CC} = 2.7V; Tamb = -30 to +70 °C; unless otherwise stated

Measured in a 50 Ω impedance system, including external input baluns and matching networks to 50 Ω,No DC applied on input pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pins LBIA and LBIB						
$f_{RFGSM\ 850}$	RF input frequency range GSM850 band		869	-	894	MHz
$f_{RFGSM\ 900}$	RF input frequency range GSM900 band		925	-	960	MHz
RIN	differential input resistance	parallel RC input model GSM900 band GSM850 band	-	 120 120	-	Ω
CIN	differential input capacitance	parallel RC input model GSM900 band GSM850 band	-	 1.75 1.4	-	pF
NF	noise figure; max AGC gain	notes 1 and 2	-	3.2	3.7	dB
GOFF	LNA off-state gain difference	bit LNA: 1 <-> 0;notes 1	-	45	-	dB
POFF	LNA off-state power handling	bit LNA = 0; notes 1 and 4	6	-	-	dBm
Pins HBIA and HBIB						
$f_{RF\ DCS1800}$	RF input frequency range DCS1800 band		1805	-	1880	MHz
$f_{RF\ PCS1900}$	RF input frequency range PCS1900 band		1930	-	1990	MHz
RIN	differential input resistance	parallel RC input model DCS1800 band PCS1900 band	-	 180 200	-	Ω
CIN	differential input capacitance	parallel RC input model DCS1800 band PCS1900 band	-	 1 0.5	-	pF
NF	noise figure; max AGC gain	notes 1 and 2	-	3.2	3.7	dB
GOFF	LNA off-state gain difference	bit LNA: 1 <-> 0;notes 1	-	45	-	dB
POFF	LNA off-state power handling	bit LNA = 0; notes 1 and 4	6	-	-	dBm
Pins SWBIA and SWBIB						
$f_{RF\ GSM850}$	RF input frequency range GSM850 band	LNA1 = 1; LNA2 = 0	869	-	894	MHz
$f_{RF\ GSM900}$	RF input frequency range GSM900 band	LNA1 = 1; LNA2 = 0	925	-	960	MHz
$f_{RF\ DCS1800}$	RF input frequency range DCS1800 band	LNA1 = 1; LNA2 = 1	1805	-	1880	MHz
$f_{RF\ PCS1900}$	RF input frequency range PCS1900 band	LNA1 = 1; LNA2 = 1	1930	-	1990	MHz

Table 7: RF Receiver AC Characteristics *...continued*

V_{CC} = 2.7V; Tamb = -30 to +70 °C; unless otherwise stated

Measured in a 50 Ω impedance system, including external input baluns and matching networks to 50 Ω,No DC applied on input pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RIN_{LB}	differential input resistance for GSM850/GSM900 bands	parallel RC input model; LNA1 = 1; LNA2 = 0 GSM900band GSM850 band	-	 110 110	-	Ω
RIN_{HB}	differential input resistance for DCS1800/PCS1900 bands	parallel RC input model; LNA1 = 1; LNA2 = 1 DCS1800 band PCS1900 band	-	 100 100	-	Ω
CIN_{LB}	differential input capacitance for GSM850/GSM900 bands	parallel RC input model; LNA1 = 1; LNA2 = 0 GSM900 band GSM850 band	-	 1.6 1.5	-	pF
CIN_{HB}	differential input capacitance for DCS1800/PCS1900 bands	parallel RC input model; LNA1 = 1; LNA2 = 1 DCS1800 band PCS1900 band	-	 1.9 1.9	-	pF
NF_{LB}	noise figure; max AGC gain for GSM850/GSM900 bands	LNA1 = 1; LNA2 = 0; notes 1 and 2	-	3.7	4.2	dB
NF_{HB}	noise figure; max AGC gain for DCS1800/PCS1900 bands	LNA1 = 1; LNA2 = 1; notes 1 and 2	-	3.7	4.2	dB
GOFF	LNA off-state gain difference	bit LNA: 1 <-> 0;note 1	-	45	-	dB
$POFF_{LB}$	LNA off-state power handling	LNA1 = 1; LNA2 = 0, bit LNA = 0; notes 1 and 4	6	-	-	dBm
$POFF_{HB}$	LNA off-state power handling	LNA1 = 1; LNA2 = 1, bit LNA = 0; notes 1 and 4	6	-	-	dBm
Pins LBIA, LBIB, SWBIA, SWBIB, HBIA and HBIB						
S11	input power matching	note 2	-	-15	-10	dB
$SPUR_{IN}$	spurious power level at RF input	in 800 to 1000 MHz band	-	-	-57	dBm
		in 1800 to 2000 MHz band	-	-	-50	dBm
		out of preceding bands	-	-	-45	dBm
CP1	1 dB input compression point; minimum AGC gain	Tamb = 25 °C; note 1	-24	-	-	dBm
IP3	input referred 3rd order intercept; maximum AGC gain	Tamb = 25 °C; note 1, 5	-18	-	-	dBm
IP2	input referred 2nd order intercept; max. AGC gain (AGC1)	Tamb = 25 °C;note 6	40	50	-	dBm

Table 7: RF Receiver AC Characteristics *...continued*

V_{CC} = 2.7V; Tamb = -30 to +70 °C; unless otherwise stated

Measured in a 50 Ω impedance system, including external input baluns and matching networks to 50 Ω,No DC applied on input pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Blocking_{LB}$	C/N ratio at blocking for GSM850/900 bands	Tamb = 25 °C; Δf = 3 MHz; Pw = -101dBm; Pint = -25dBm; note 1	9	-	-	dB
$Blocking_{HB}$	C/N ratio at blocking for DCS1800 and PCS1900 bands	Tamb = 25 °C; Δf = 3 MHz; Pw = -101dBm; Pint = -28dBm; note 1	9	-	-	dB
IMrej	image rejection	ΔfIF = 200 kHz; SBD = 0; Tamb = 25 °C; note 1	35	45	-	dB
ΔGvRF	gain mismatch between operation of different bands	notes 1 and 3	-	-	2.5	dB
Pins IA, IB, QA and QB (RX mode)						
Gv_{MIN}	voltage conversion gain	AGC gain set to minimum; notes 1 and 3	22	28	34	dB
Gv_{MAX}	voltage conversion gain	AGC gain set to maximum; notes 1 and 3	92	96	100	dB
ΔGvBW	gain difference between narrow and wide bandwidth mode	RXBW 0<->1	-0.5	0	0.5	dB
Gv_{STEP}	voltage conversion gain step	note 3	-	4	-	dB
ΔGvIQ	gain mismatch I and Q paths	note 3	-	-	0.5	dB
AGC_{lin}	gain control linearity	note 2; Fig 3 a)	-2	-	2	dB
		over any 20 dB gain range; Fig 3 b)	-0.5	-	0.5	dB
V_{OUT}	maximum output voltage per pin	RL = 100 kΩ differential; CL =10pF differential; Pw<-34 dBm; THD < 3%	0.75	-	-	V_{pk}
V_{ODM_RXIQ}	maximum differential output voltage	(I-IB) or (Q-QB) RL = 100 kΩ differential; CL =10pF differential; Pw<-34 dBm; THD < 3%	1.5	-	-	V_{pkdiff}
DC_{offset}	differential output offset voltage	150µs after RXON activation	-300	-	300	mV
DC drift	differential output offset voltage drift	STOPSETL = 1; see Fig. 5 RX AGC = AGC1 (table 32) RX AGC = AGC2 RX AGC = AGC3 RX AGC = AGC4 RX AGC = AGC5 RX AGC = AGC6 or AGC7 other RX AGC steps	-	 7 5 3 2 1 0.5 0.2	 15 11 7 4 3 2 1	mV/ms
HP-3dB	-3dB high pass corner frequency (DC notch)		4	6	8	kHz

Table 7: RF Receiver AC Characteristics...*continued*

V_{CC} = 2.7V; Tamb = -30 to +70 °C; unless otherwise stated

Measured in a 50 Ω impedance system, including external input baluns and matching networks to 50 Ω,No DC applied on input pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BW-3dB	-3dB LOW IF filter bandwidth for narrow bandwidth mode	-100 kHz center frequency ; RXBW =0	220	240	260	kHz
BW-3dB$_{HI}$	-3dB LOW IF filter bandwidth for wide bandwith mode	-100 kHz center frequency ; RXBW =1	275	305	335	kHz
LP-3dB	-3dB low pass corner frequency of mixer output		-	470	-	kHz
Δτgd	group delay variation	-170 kHz < f_{OUT} < -30 kHz	-	1.5	2	µs
Att$_{narrowband}$	LOW IF filter attenuation (5th order)n narrow bandwidth mode	f_{OUT} = -100 kHz ± 200 kHz	17	31	-	dB
		f_{OUT} = -100 kHz ± 400 kHz	54	64	-	dB
		f_{OUT} = -100 kHz ± 600 kHz	73	82	-	dB
Att$_{wideband}$	LOW IF filter attenuation (5th order) in wide bandwidth mode	f_{OUT} = -100 kHz ± 200 kHz	10	19	-	dB
		f_{OUT} = -100 kHz ± 400 kHz	45	54	-	dB
		f_{OUT} = -100 kHz ± 600 kHz	64	73	-	dB

[1] measured and guaranted on evaluation board

[2] this value includes printed circuit board and balun losses

[3] Voltage gain defined as the differential base band RMS output voltage (either at pins IA and IB or QA and QB measured in standard load) divided by the RMS input voltage at the RF baluns.

[4] No degradation of the LNA inputs. See application note (AN 040616/AE) for phase error degradation caused by TX power coupling to RX inputs

[5] IP3 related to an IM3 measurement with two tones at 800 and 1600 kHz offset.

[6] IP2 related to an IM2 measurement with two tones at 6 and 6.1 MHz offset.

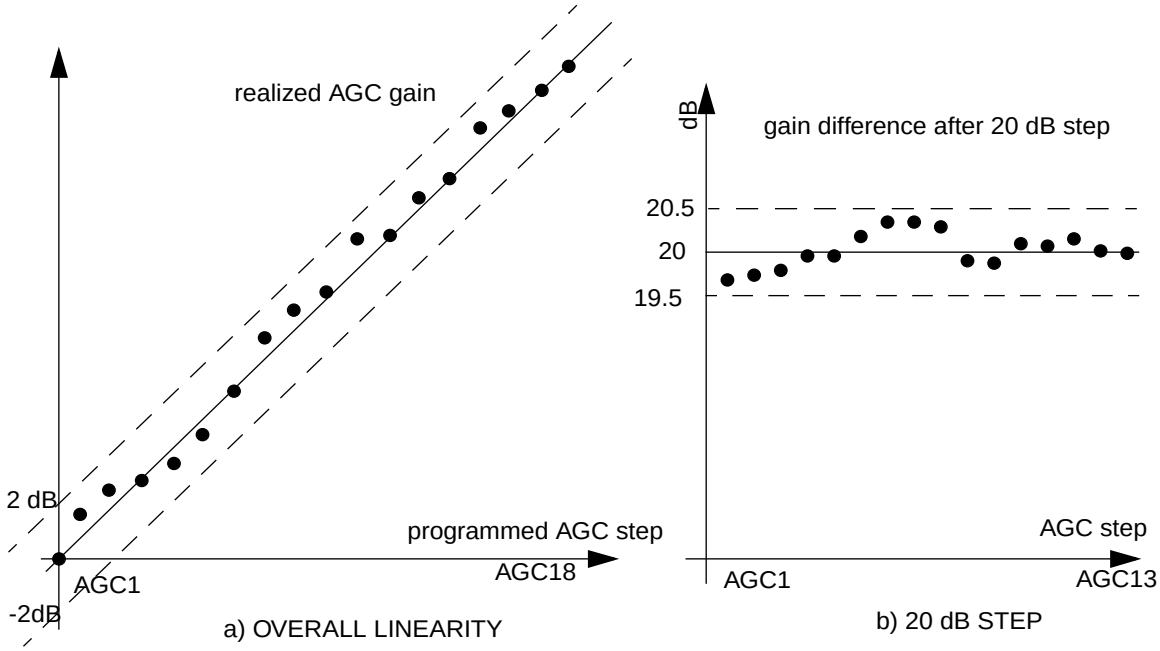


Fig 3. AGC linearity

Table 8: Transmit section AC Characteristics

V_{CC} = 2.7V; Tamb = -30 to +70 °C; unless otherwise stated

Vmod = 0.5 Vpk; fmod = 67.7kHz; I and Q signals matched; unless otherwise stated

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Pins IA, IB, QA and QB (mode TX)							
f_{mod}	modulation frequency range	3 dB 2nd order low pass cutoff frequency		0.5	-	-	MHz
$\Delta\tau gd$	group delay variation	30 kHz < f_{mod} < 170 kHz		-	1.5	2	µs
V_{mod}	modulation level	single ended; peak value		-	0.5	0.55	V_{pk}
V_{I_TXIQ}	input signal amplitude	differential		-	1	1.1	V_{diff}
R_{IN}	dynamic input resistance	single ended		-	25	-	kΩ
IQ Modulator; f_{mod} = 67.7 kHz; pins LBOA, LBOB, HBOA, HBOB							
$P_{out;LB}$	Low band output peak power	Tamb= 25°C	note 1	5.4	7	8.6	dBm
$P_{out;HB}$	High band output peak power	Tamb= 25°C	note 1	1.4	3	4.6	dBm
ΔP_{out}	output peak power variation vs Temp		note 1	-0.4	-	0.4	dB
$\Phi NOISE;_{LB}$	phase noise output power density in GSM850/GSM900 bands	Tamb=25°C; Δf = 400 kHz; note 1, 2		-	-122	-120	dBc/Hz
		Tamb=25°C; Δf = 1.8 MHz; note 1, 2		-	-126	-124	dBc/Hz
		Tamb=25°C; Δf = 20 MHz; note 1, 2		-	-162	-	dBc/Hz
		Tamb=25°C; Δf = 30 MHz; note 1, 2		-	-164	-163	dBc/Hz
$\Phi NOISE;_{HB}$	phase noise output power density in DCS1800/PCS1900 bands	Tamb=25°C; Δf = 400 kHz; note 1, 2		-	-118	-116	dBc/Hz
		Tamb=25°C; Δf = 1.8 MHz; note 1, 2		-	-123	-121	dBc/Hz
		Tamb=25°C; Δf = 20 MHz; note 1, 2		-	-	-154	dBc/Hz
$AM_{Noise;LB}$	AM noise output power density in GSM850/900 bands	Tamb=25°C; Δf = 20 MHz; note 1		-	-170	-	dBc/Hz
$AM_{Noise;HB}$	AM noise output power density in DCS1800/PCS1900 bands	Tamb=25°C; Δf = 20 MHz; note 1		-	-162	-	dBc/Hz
$CREJ;_{LB}$	Low band carrier rejection	f = (Fc + fmod) +/- fmod ; note1, 3		-	-37	-30	dBc
$CREJ;_{HB}$	High band carrier rejection	f = (Fc + fmod) +/- fmod ; note1, 3		-	-35	-28	dBc
$IM_{OUT;LB}$	image level	f = (Fc + fmod) +/- 2 * fmod; note 1		-	-45	-37	dBc
$IM_{OUT;HB}$	image level	f = (Fc + fmod) +/- 2 * fmod; note 1		-	-45	-37	dBc

Table 8: Transmit section AC Characteristics *...continued*

V_{CC} = 2.7V; Tamb = -30 to +70 °C; unless otherwise stated

Vmod = 0.5 Vpk; fmod = 67.7kHz; I and Q signals matched; unless otherwise stated

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$SPUR_{3fmLB}$	Low band spurious level at 3*fmod offset from wanted	f = (Fc + fmod) +/- 3* fmod; note 1	-	-50	-45	dBc
$SPUR_{3fmHB}$	low band spurious level at 3*fmod offset from wanted	f = (Fc + fmod) +/- 3* fmod; note 1	-	-50	-45	dBc
$SPUR_{4fmLB}$	spurious level at 4*fmod offset from wanted	f = (Fc + fmod) +/- 4 * fmod; note 1	-	-44	-42	dBc
$SPUR_{4fmHB}$	spurious level at 4*fmod offset from wanted	f = (Fc + fmod) +/- 4 * fmod; note 1	-	-44	-42	dBc
$Spur_{otherLB}$	Low band spurious level at other frequencies	abs(f-(Fc+fmod))>=300kHz; f < 1.5 GHz; note 1	-	-	-70	dBc
$Spur_{otherHB}$	High band spurious level at other frequencies	abs(f-(Fc+fmod))>=300kHz; f < 2.5 GHz; note 1	-	-	-70	dBc
$Harm_{LB}$	Low band harmonics level	G1TX1 = 0; note 1 2*Fc 3*Fc	-	-	 -20 -10	dBc
$Harm_{HB}$	High band harmonics level	G1TX1 = 1; note 1 2*Fc 3*Fc	-	-	 -20 -15	dBc
$TX_{load,LB}$	Low band Output load		-	160	-	Ω
$TX_{load,HB}$	High Band Output load		-	200	-	Ω

[1] Measured at balun output

[2] Measured according to ETSI specification.

[3] lead to phase error rms better than 3.5° in HB and 3° in LB at antenna output on reference design Sy.Sol 5100.

Table 9: Synthesiser and VCO

V_{CC} = 2.7V; Tamb = -30 to +70 °C; unless otherwise stated

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RF-synthesizer						
f_{RFLO}	synthesizer frequency range		3294	-	3982	MHz
f_{comp}	comparison frequency		-	26	-	MHz
f_{step}	frequency step programmability	fcomp = 26 MHz at f_{RFLO}	-	24.8	-	Hz
Φnoise	close-in phase noise	f =f_{RFLO} ± 2 kHz; note 1	-	-86	-78	dBc/Hz
Pspur	spur levels	Δf > 400kHz	-	-	-70	dBc
ICP	Charge pump current range	sink or source; Rext=3.3 kΩ (1%); over VCP range;	-	200	-	µA
KΦ	phase frequency detector gain	for ICP = 0.2 mA	-	32	-	µA/rad
VCP	charge pump output voltage	ICP within range specified	0.4	-	$V_{CC(CP)}$ - 0.4	V
fractional-N synthesizer (f_{LO} = f_{comp}*(N+ 2*K_{frac}); K_{frac} = K/2exp21 + 1/2exp22)						
N	integer divider ratio	fcomp=26MHz	126	-	155	
Kfrac	fractional divider ratio	exception see note	0.25	-	0.75	
Integrated RF oscillator pin RFTUNE						
Gvco	VCO gain	Vtune= 1.4 V	-	32	-	MHz/V
$ΔG_{(VCO*KΦ)}$	VCO gain times Chpump gain variation	after VCO calibration	3200	6400	9600	A/Vs
Rtune	RFTUNE series resistor inside the IC		-	15	-	kΩ
Ctune	parallel capacitor at VCO tuning input to ground inside the IC		-	46	-	pF
Vtune	tuning voltage range		0.4	-	V_{CC} -0.4	V
$Δf_{VCC}$	pushing	TX mode, SYNTX = 1 RX mode, SYNTX = 0	-	-	5 10	MHz/V
$T_{VCO\ cal}$	VCO calibration time	after synthesizer activation	-	32	-	µs
Low noise crystal oscillator; pins REFIN, CLKFDBX						
f_{REF}	reference frequency		-	26	-	MHz
R_{REFIN}	input resistance	fREF = 26 MHz	-	2.7	-	kΩ
C_{REFIN}	input capacitance	fREF = 26 MHz	-	0.8	-	pF
$R_{CLKFDBX}$	output resistance	f = 26 MHz; CAFC0/.../7 =0 f = 26 MHz; CAFC0/.../7 =1	-	900 600	-	Ω
G_v	small signal voltage gain (REFIN, CLKFDBX)	f=2.6MHz; CAFC 0/.../7 = 1; Pin < -42 dBm; note 2	-	26	-	dB
$V_{IN(REFIN)}$	input voltage level	note 1	300	-	-	mVpp
$V_{CLKFDBX}$	limiting output voltage swing	note 1	-	1500	-	mVpp

Table 9: Synthesiser and VCO *...continued*

V_{CC} = 2.7V; Tamb = -30 to +70 °C; unless otherwise stated

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$SPUR_{OUT}$	Spurious emission	f = 2*fref, note 1	-	-	-20	dBc
	Spurious emission	non harmonics, note 1	-	-	-70	dBc
Coarse AFC						
$C_{CAFC,LO}$	CLKFDBX output capacitance LO	CAFC 0/.../7 = 0	13.5	15.5	17.5	pF
$C_{CAFC,HI}$	CLKFDBX output capacitance HI	CAFC 0/.../7 = 1	30	36	42	pF
$C_{CAFC,LSB}$	LSB of coarse AFC capacitor	CAFC 1/.../7 = 0 CAFC0 0 <-> 1	61	80	96	fF
$f_{step,XO}$	CAFC monotonicity	CAFC -> CAFC-1, note 1	0.1	7	26	Hz
Low noise crystal oscillator amplifier output signal CLKOUT						
f_{CLKOUT}	output frequency		-	26	-	MHz
R_{CLKOUT}	output resistance		-	200	-	Ω
V_{CLKOUT}	limiting output voltage swing	note 1, note 3	0.75	1	1.5	Vpp
D_{CLKOUT}	duty cycle	note 1	40	-	60	%
Φnoise-BB	CLKOUT phase noise	Δf = 2 kHz, note 1, 3	-	-	-118	dBc/Hz
$Jitter_{XO}$	time jitter at CLKOUT	notes 1, 3, 4; RMS value	-	-	60	ps rms
Greverse	reverse isolation	to pin CLKFDBX; BW<100MHz; note1	20	50	-	dB
$S_{CLKOUT,pos}$	positive slew rate	between VDC - 50mV and VDC + 50mV; notes 1, 3	60	-	-	mV/ns
$\Delta f_{ref,\ CAFC}$	residual frequency error	after coarse AFC alignment, T_{amb} = 25 °C, quartz specified with max ± 10 ppm, note 1	-0.5	-	0.5	ppm
Δf/f (T)	frequency stability as a function of temperature	over full temperature range, quartz specified with max. +/- 20ppm, note 1	-24	-	24	ppm
Δf/f (t)	frequency stability as a function of time	Cumulative contribution related to the IC over 10 years,T=25 ℃, note 1	-2	-	2	ppm

[1] These performance are measured and guaranted on evaluation board. The 26 MHz quartz is outside the IC. C_{load_quartz} = 10 pF

[2] Gain value is also valid for 26MHz not taking into account loading by C_{CAFC} and external capacitor

[3] $C_{load,\ CLKOUT}$ = 20pF

[4] based on phase noise measurement

[5] 4 extra value are allowed for K : 80659, 209715, 1887436, 2016492

Table 10: Timing specifications

V_{CC} = 2.7V; T_{amb} = -30 to +70 °C; unless otherwise stated

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{REF,ON}$	Turn on time of Reference oscillator	to 0.1ppm of final frequency; notes 1	-	-	4.6	ms
$t_{SYN,ON}$	Turn on time of RF synthesiser	to 0.1ppm of final value of fRX,out; notes 1, 2, 3	-	-	200	µs
$t_{RX,ON}$	RX DC settling time	V(IA-IB) to 50mV from final DC value; notes 1, 4; STOPSETL=0; FASTSETL=0	-	-	200	µs
$t_{TX,ON}$	TX settling time		-	-	73	µs

[1] These performances are measured and guaranted on evaluation board.

[2] Only valid after crystal oscillator has locked

[3] Measured acc. GSM specification.

[4] A new RXDC settling is provoked when changing AGC bits G2, G3, G4 or G5. No change of RXDC settling will occur after changing AGC bits G0 and G1.

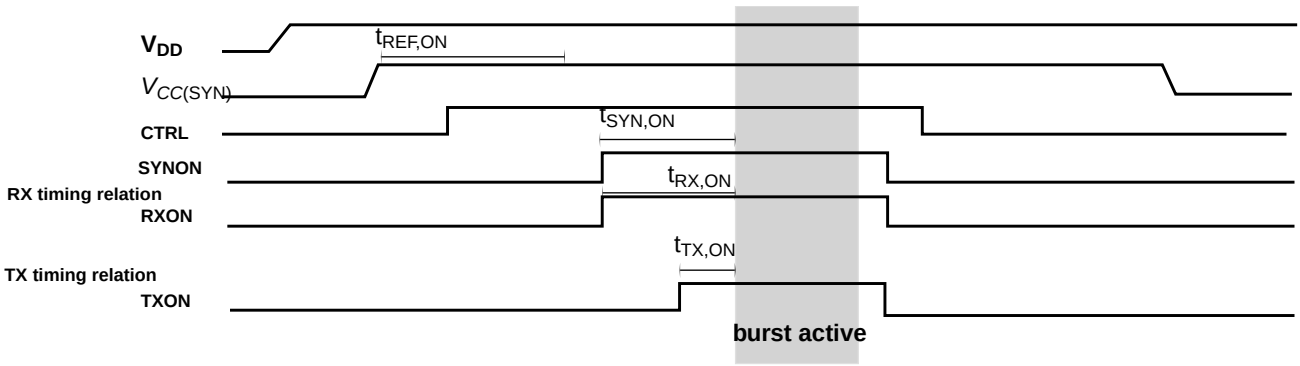


Fig 4. Timing diagram

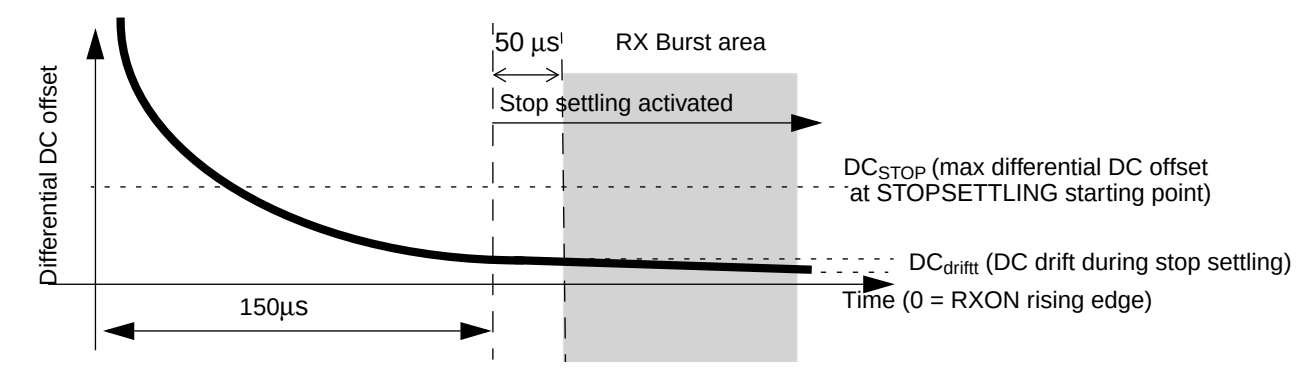


Fig 5. StopSettling Timing diagram

Table 11: Serial bus timing Characteristics

V_{DD} = 1.6 to 2V; T_{amb} = -30 to +70 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Serial programming clock; pin CLK						
tr, tf	input rise and fall times		-	-	8	ns
tcy	clock period		67	-	-	ns
twclk	clock pulse width		20	-	-	ns
Enable programming; pin EN						
t_{START}	delay to rising clock edge		15	-	-	ns
t_{END}	delay from last falling clock edge		15	-	-	ns
t_W	minimum inactive pulse width		60	-	-	ns
Register serial input data; pin DATA						
$t_{SU;DATA}$	input data to clock set-up time		15	-	-	ns
$t_{HD;DATA}$	input data to clock hold time		22	-	-	ns

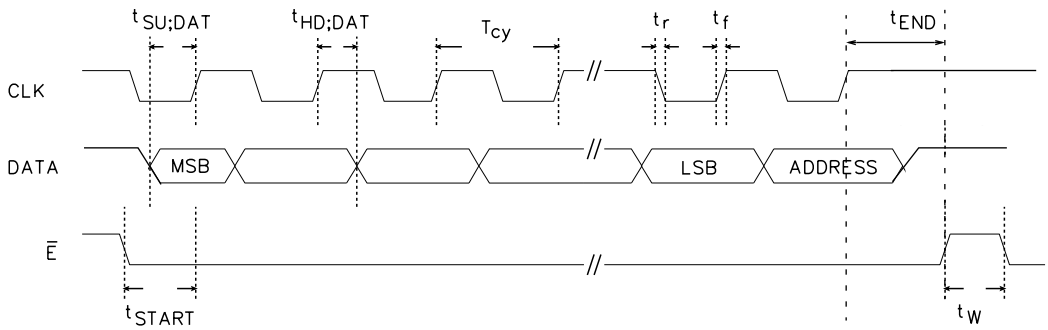


Fig 6. Serial bus timing diagram.

12. Power supply concept

Four different voltage supplies are needed

1. Digital supply (V_{DD}) for digital inputs, for digital parts. In order to save AFC programming this supply must be kept turned on during sleep mode.
2. for the charge pump block ($V_{CC(CP)}$): supply can be turned off in sleep mode
3. for TX and RX path ($V_{CC(RFLO)}$): supply can be turned off in sleep mode
4. for the reference oscillator ($V_{CC(SYN)}$): supply has to be turned off in sleep mode to turn off the reference oscillator

the following power supply concept is proposed:

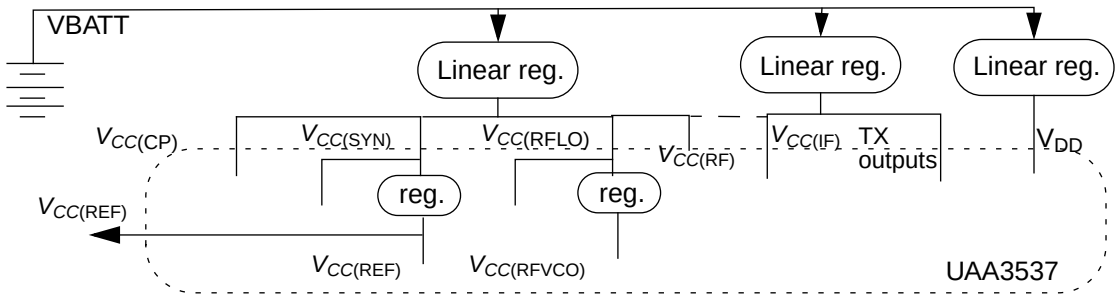


Fig 7. Power supply concept

note: $V_{CC(RF)}$ can be connected either to one or the other regulator (depending on the power regulator capability).

13. Operating Mode

13.1 Basic operating modes

The circuit can be powered up into different modes depending on the logic level applied at pin CTRL, on supply voltage applied and on the control bits SYNON, RXON, TXON of the 3-wire bus. This defines six main modes called IDLE, REF, DISABLE, SYN, RX and TX mode.

Table 12: Operation mode

MODE	PIN CTRL	BIT SYNON	BIT RXON	BIT TXON	$V_{CC(SYN)}$
IDLE	X	0	0	0	OFF
REF	X	0	0	0	ON
DISABLE	0	X	X	X	ON
SYN	1	1	0	0	ON
RX	1	1	1	0	ON
TX	1	1	0	1	ON

Table 13: Mode description

MODE	DESCRIPTION
IDLE	Reference, synthesiser, receiver and transmitter are OFF
REF	Only Reference oscillator is ON
DISABLE	Transceiver is disabled reference is ON if $VCC_{(SYN)}$ is ON
SYN	Synthesiser is ON; note 1
RX	Receiver is ON; note 2
TX	Transmitter is ON

[1] The synthesizer includes the LO buffers common also to the receive and transmit sections.

[2] When the receiver is on, it is possible to switch off the low noise amplifier. Refer to receiver control described below.

TX, RX or SYN mode can be disabled by means of the CTRL bit. In fact, internally CTRL bit is combined by logic AND to 3-wire bus TXON, RXON and SYNON bits and so override the operating mode. The goal of the CTRL pin is to handle the DTX and DRX GSM operation. When CTRL pin goes low, only the current mode (TX or RX) is disabled (DISABLE mode) and no internal register are reseted.

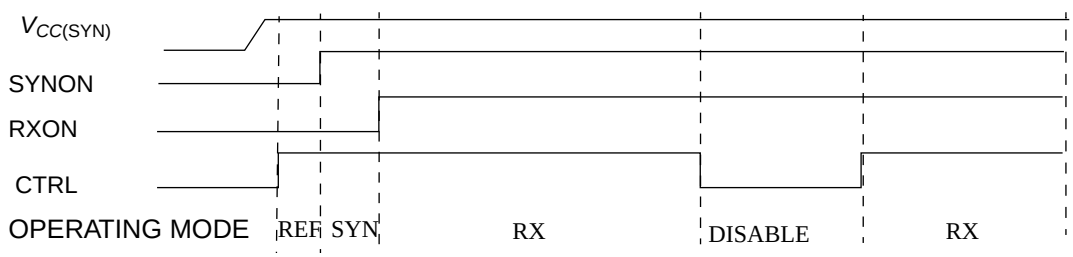


Fig 8. CTRL bit usage, example for RX mode

13.2 Transmit I/Q polarity control

The polarity of the I/Q signal for TX clock can be changed. The selection of these two modes is accomplished by means of the bit IQPOL.

Table 14: TX I/Q polarity

IQPOL BIT STATUS	MODE OF OPERATION
0	Q signal 90 degree before I
1	I signal 90 degree before Q

13.3 Front end switch control

There are three output pins FESW1, FESW2 and FESW3 that can supply current. They are controlled by means of the bit FESW1H, FESW2H, FESW3H, FESW1L, FESW2L and FESW3L combined with the control pin SWON. This allows to program a changed state to the control register and activate it later on by changing the logic state at the control pin SWON.

The switch status depends on the control bits FESWxx according to the table below

Table 15: Front end switch status

FESWxH BIT STATUS	FESWxL BIT STATUS	SWON PIN STATUS	STATUS AT FESWx PIN
X	0	0	pull down to GND
X	1	0	source current supplied
0	X	1	pull down to GND
1	X	1	source current supplied

13.4 Receiver LNAs control

The receiver includes 4 LNAs. One LNA (LBLNA) is connected to LBIA and LBIB inputs, one LNA (HBLNA) is connected to HBIA and HBIB inputs and two LNAs (SW1LNA and SW2LNA) are connected to the same inputs (SWBIA & SWBIB). LBLNA can cover GSM 850 & 900 MHz bands, HBLNA can cover DCS1800 & PCS1900 bands, SW1LNA can cover GSM 850 and 900 bands and SW2LNA can cover DCS1800 and PCS1900 bands. Only one out of those four LNA will operate at one time depending on the LNA1 and LNA2 bits status according to the table below.

Table 16: switched LNA status

LNA1 BIT STATUS	LNA 2 BIT STATUS	OPERATING LNA (covered bands)
0	0	LBLNA (GSM 850 or 900)
1	0	SW1LNA (GSM 850 or 900)
1	1	SW2LNA (DCS1800 or PCS1900)
0	1	HBLNA (DCS1800 or PCS1900)

13.5 Receiver power status control

When the receiver is on, it is possible to switch off the low noise amplifier separately by the mean of the bit LNA.

Table 17: LNA status

LNA BIT STATUS	POWER STATUS OF THE LNA
0	OFF
1	ON

13.6 Sideband select status control

The receiver includes an image rejection front end which allows the use of a RF LO 100 kHz below the RF input frequency (infradyne) or 100 kHz above the RF input frequency (supradyne), between these two states the proper image should be selected for rejection. The selection of these two modes is accomplished by means of the bit SDB according to the table below.

Table 18: Sideband select

SDB BIT STATUS	MODE OF OPERATION
0	supradyne
1	infradyne

13.7 RXIF filter bandwidth control

The bandwidth of the RXIF bandpass filter can be switched between 240 and 300kHz.

THe RXIF filter band pass depends on the control bit RXBW according to the table below

Table 19: RXIF bandwidth

RXBW BIT STATUS	MODE OF OPERATION
0	240 kHz bandwidth
1	300 kHz bandwidth

13.8 Fast settling mode

The RXIF part contains an active DC compensation (DC notch) that needs significant settling time. To speed it up a fast settling mode is implemented with a higher bandwidth of the notch. Afterwards it has to be set back again to normal settling. The mode is controlled by the bit FASTSETL.

Table 20: Fast settling control

FASTSETL BIT STATUS	MODE OF OPREATION	BANDWIDTH OF DC NOTCH
0	normal settling	6 kHz
1	fast settling	24 kHz

13.9 Stop settling mode

The active DC compensation (DC notch) of the RXIF part can be switched to static DC compensation. After switching to stop settling mode the achieved differential offsets at the I/Q output pins are kept stable during the burst. It is controlled by the bit STOPSETL.

Table 21: Stop settling control

STOPSETL BIT STATUS	MODE OF OPERATION
0	Dynamic DC compensation
1	Static DC compensation

13.10 Notch remove mode

The active DC compensation (DC notch) of the RXIF part can be disconnected for test purpose. It is controlled by the bit NTCHREM according to the table below.

Table 22: Notch remove control

NTCH REM BIT STATUS	MODE OF OPERATION
0	Notch connected
1	Notch disconnected

13.11 Band status control

The receiver includes four RF front end (3 band capable) and their RF LO section. For GSM 850 and 900 the RF LO signal is divided by four. For DCS1800 and PCS1900 the RF LO signal is divided by two. The selection of the different bands is accomplished by means of the bit BND1/BND2 according to the table below.

Table 23: Band select control

BND1 BIT STATUS	BND2 BIT STATUS	MODE OF OPERATION
0	0	GSM850
1	0	GSM900
0	1	DCS1800
1	1	PCS1900

13.12 Coarse AFC control

The coarse AFC capacitors of the reference oscillator are controlled via the binary weighted bits CAFC 0/1/2/3/4/5/6/7. Their weight is defined according to the table below.

Table 24: Coarse AFC control

NAME OF THE BIT	VALUE OF THE BIT
CAFC0	LSB
CAFC7	MSB

This register is supplied by V_{DD}, so coarse AFC programing is kept (especially during sleep mode) by means of a continuous V_{DD}.

13.13 Synthesiser mode status

To avoid pulling on the VCO, a part of the LO path is enabled during SYN mode. To save power, during SYN mode only the RX or TX path is powered depending on the next state of the transceiver (transmit or receive). The selection of those two synthesiser mode is accomplished by means of the SYNTX bit.

Table 25: Synthesiser mode control

SYNTX BIT STATUS	MODE OF OPERATION
0	synthesiser in RX operation
1	synthesiser in TX operation

14. Programming

14.1 Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and EN (enable). The data sent to the device is loaded in bursts framed by EN. Programming clock edges are ignored until EN goes active LOW. The programmed information is loaded into the addressed latch when EN returns inactive HIGH. This is allowed when CLK is in either state without causing any consequences to the register data. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programming data even during power-down of the synthesizer.

14.2 Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The address bits are decoded on the rising edge of EN. This produces an internal load pulse to store the data in the addressed latch. To ensure that data is correctly loaded on first power-up, EN should be held LOW and only taken HIGH after having programmed an appropriate register. To avoid erroneous divider ratios, the pulse is inhibited during the period when data is read by the frequency dividers. This condition is guaranteed by respecting a minimum EN pulse width after data transfer.

14.3 Reset concept

Two reset signals are generated internally. First when V_{DD} rises, secondly when $V_{CC(SYN)}$ rises. When first reset signal occurs, all registers are preset according to the following table (RESET V_{DD} column). When second reset signal occurs, all registers except the AFC register are preset according to the following tables (RESET $V_{CC(SYN)}$ column). This allows the coarse AFC programming to be kept as long as V_{DD} is present.

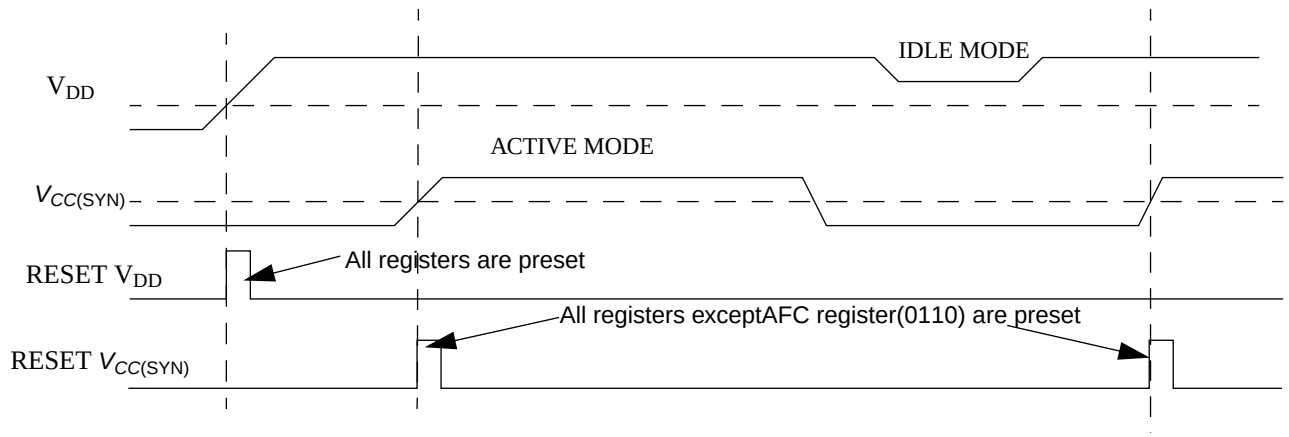


Fig 9. Reset concept

14.4 Register bit allocation

Table 26: AFC Register “0110”

BIT	SYMBOL	RESET V_{DD}	RESET $V_{CC(SYN)}$	DESCRIPTION
16	1	1	1	reserved
15	0	0	0	not used
14	0	0	0	reserved
13	0	0	0	reserved
12	1	1	none	reserved
11	0	0	none	reserved
10	CAFC 7	1	none	Coarse AFC MSB
9	CAFC 6	0	none	
8	CAFC 5	0	none	
7	CAFC 4	0	none	
6	CAFC 3	0	none	
5	CAFC 2	0	none	
4	CAFC 1	0	none	
3	CAFC 0	0	none	Coarse AFC LSB
2	0	0	0	not used
1	1	1	none	reserved
0	1	1	1	reserved

Table 27: Synthesiser Register “ 0101“

BIT	SYMBOL	RESET V_{DD}	RESET $V_{CC(SYN)}$	DESCRIPTION
16	RFK20	0	0	Synthesiser Fractional bit
15	RFK19	1	1	Synthesiser Fractional bit
14	RFK18	1	1	Synthesiser Fractional bit
13	RFK17	0	0	Synthesiser Fractional bit
12	RFK16	0	0	Synthesiser Fractional bit
11	RFK15	0	0	Synthesiser Fractional bit
10	RFK14	1	1	Synthesiser Fractional bit
9	RFK13	0	0	Synthesiser Fractional bit
8	RFK12	0	0	Synthesiser Fractional bit
7	RFK11	1	1	Synthesiser Fractional bit
6	RFK10	1	1	Synthesiser Fractional bit
5	RFK9	1	1	Synthesiser Fractional bit
4	RFK8	0	0	Synthesiser Fractional bit
3	RFK7	1	1	Synthesiser Fractional bit
2	BND2	0	0	Band Select bit
1	BND1	1	1	Band select bit
0	0	0	0	not used

Table 28: Synthesiser Register " 0100"

BIT	SYMBOL	RESET V_{DD}	RESET $V_{CC(SYN)}$	DESCRIPTION
16	RFK6	1	1	Synthesiser Fractional bit
15	RFK5	0	0	Synthesiser Fractional bit
14	RFK4	0	0	Synthesiser Fractional bit
13	RFK3	0	0	Synthesiser Fractional bit
12	RFK2	1	1	Synthesiser Fractional bit
11	RFK1	0	0	Synthesiser Fractional bit
10	RFK0	0	0	Synthesiser Fractional bit
9	RFK-1	1	1	Synthesiser Fractional bit
8	RFN7	1	1	Synthesiser Integer bit
7	RFN6	0	0	Synthesiser Integer bit
6	RFN5	0	0	Synthesiser Integer bit
5	RFN4	1	1	Synthesiser Integer bit
4	RFN3	0	0	Synthesiser Integer bit
3	RFN2	0	0	Synthesiser Integer bit
2	RFN1	0	0	Synthesiser Integer bit
1	RFN0	1	1	Synthesiser Integer bit
0	RFK-2	0	0	reserved

Table 29: Receiver settings Register " 0011"

BIT	SYMBOL	RESET V_{DD}	RESET $V_{CC(SYN)}$	DESCRIPTION
16	NTCH REM	0	0	DC notch remove
15	STOP SETL	0	0	Stop settling
14	FAST SETL	0	0	Fast settling
13	RXBW	0	0	Bandwidth selection
12	SBD	0	0	Sideband selection
11	LNA2	0	0	LNA select
10	LNA1	0	0	LNA select
9	LNA	1	1	LNA power
8	G5	1	1	RX AGC bit
7	G4	1	1	RX AGC bit
6	G3	1	1	RX AGC bit
5	G2	1	1	RX AGC bit
4	G1	1	1	RX AGC bit
3	G0	1	1	RX AGC bit
2	0	0	0	not used
1	0	0	0	not used
0	0	0	0	reserved

Table 30: Transmitter settings Register " 0010"

BIT	SYMBOL	RESET V_{DD}	RESET $V_{CC(SYN)}$	DESCRIPTION
16	IQPOL	1	1	IQ polarity (TX)
15	0	0	0	reserved
14	G1TX1	0	0	TX Attenuation setting
13	0	0	0	reserved
12	0	0	0	reserved
11	0	0	0	reserved
10	0	0	0	reserved
9	0	0	0	reserved
8	0	0	0	reserved
7	0	0	0	reserved
6	0	0	0	not used
5	0	0	0	not used
4	0	0	0	reserved
3	1	1	1	reserved
2	0	0	0	reserved
1	0	0	0	reserved
0	0	0	0	reserved

Table 31: Transceiver settings Register " 0001"

BIT	SYMBOL	RESET V_{DD}	RESET $V_{CC(SYN)}$	DESCRIPTION
16	FESW3H	0	0	FESW control
15	FESW3L	0	0	FESW control
14	FESW2H	0	0	FESW control
13	FESW2L	0	0	FESW control
12	FESW1H	0	0	FESW control
11	FESW1L	0	0	FESW control
10	1	1	1	reserved
9	1	1	1	reserved
8	1	1	1	reserved
7	1	1	1	reserved
6	1	1	1	reserved
5	1	1	1	reserved
4	1	1	1	reserved
3	SYNTX	0	0	Synthesiser mode (TX or RX)
2	TXON	0	0	TX mode control
1	RXON	0	0	RX mode control
0	SYNON	0	0	SYN mode control

15. AGC

Table 32: RX AGC gain look up table; 1

G53	G43	G3	G2	G1	G0	GAIN STEP	ATTENUATION FROM MAX GAIN (dB)2
1	1	1	1	1	1	AGC1	0
1	1	1	1	1	0	AGC2	4
1	1	1	1	0	1	AGC3	8
1	1	1	1	0	0	AGC4	12
1	0	1	1	0	1	AGC5	16
1	0	1	1	0	0	AGC6	20
0	1	1	1	0	1	AGC7	24
0	1	1	1	0	0	AGC8	28
0	1	0	1	1	1	AGC9	32
0	1	0	1	1	0	AGC10	36
0	0	0	1	1	1	AGC11	40
0	0	0	1	1	0	AGC12	44
0	0	1	0	0	1	AGC13	48
0	0	1	0	0	0	AGC14	52
0	0	0	0	1	1	AGC15	56
0	0	0	0	1	0	AGC16	60
0	0	0	0	0	1	AGC17	64
0	0	0	0	0	0	AGC18	68

[1] All code not included in table are forbidden

[2] This is voltage gain attenuation for complete receiver

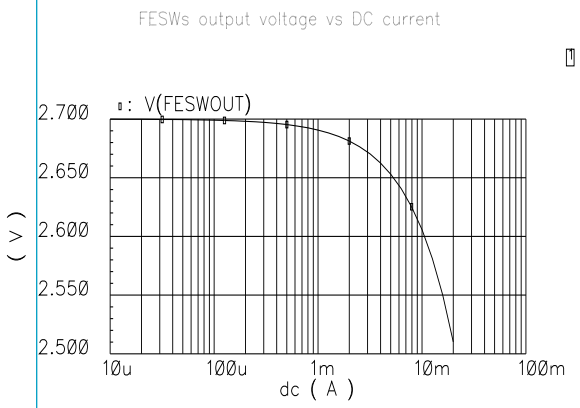
[3] Steps in front of the bandpass filter

Table 33: TX AGC gain look up table.

G1TX1	ATTENUATION FROM MAX GAIN (dB)1
0	0
1	4

[1] This is power attenuation for the complete transmit chain

16. Typical performance characteristics



FESW outputs V(I) curve

Fig 10. Typical performance characteristics

17. Application information

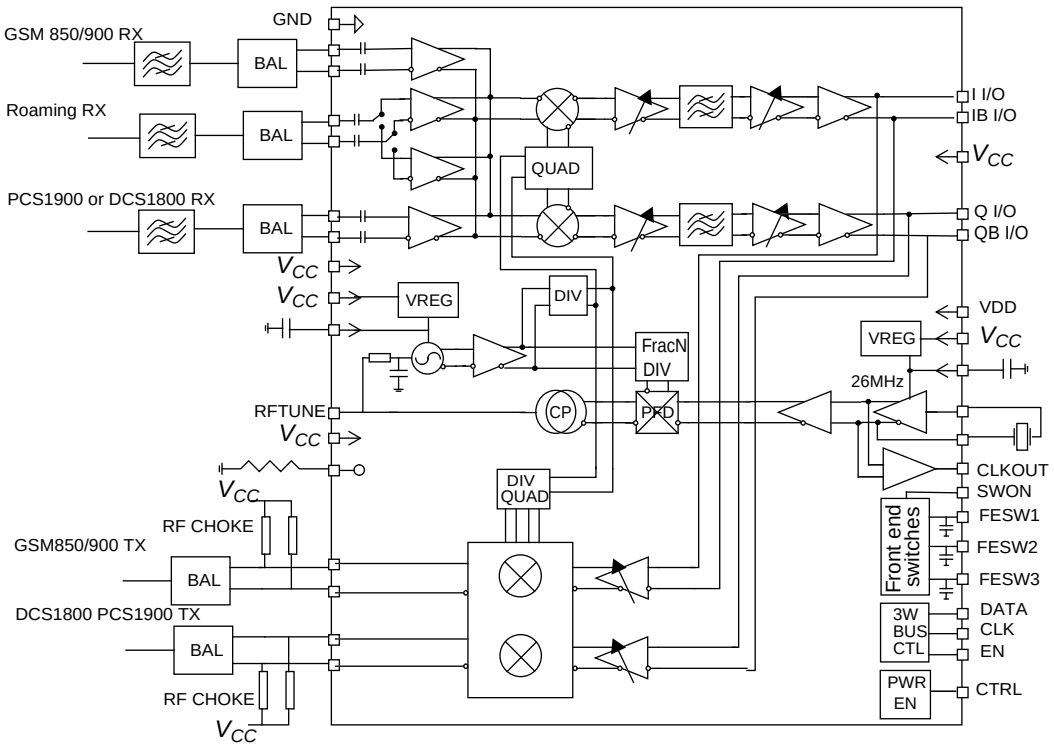
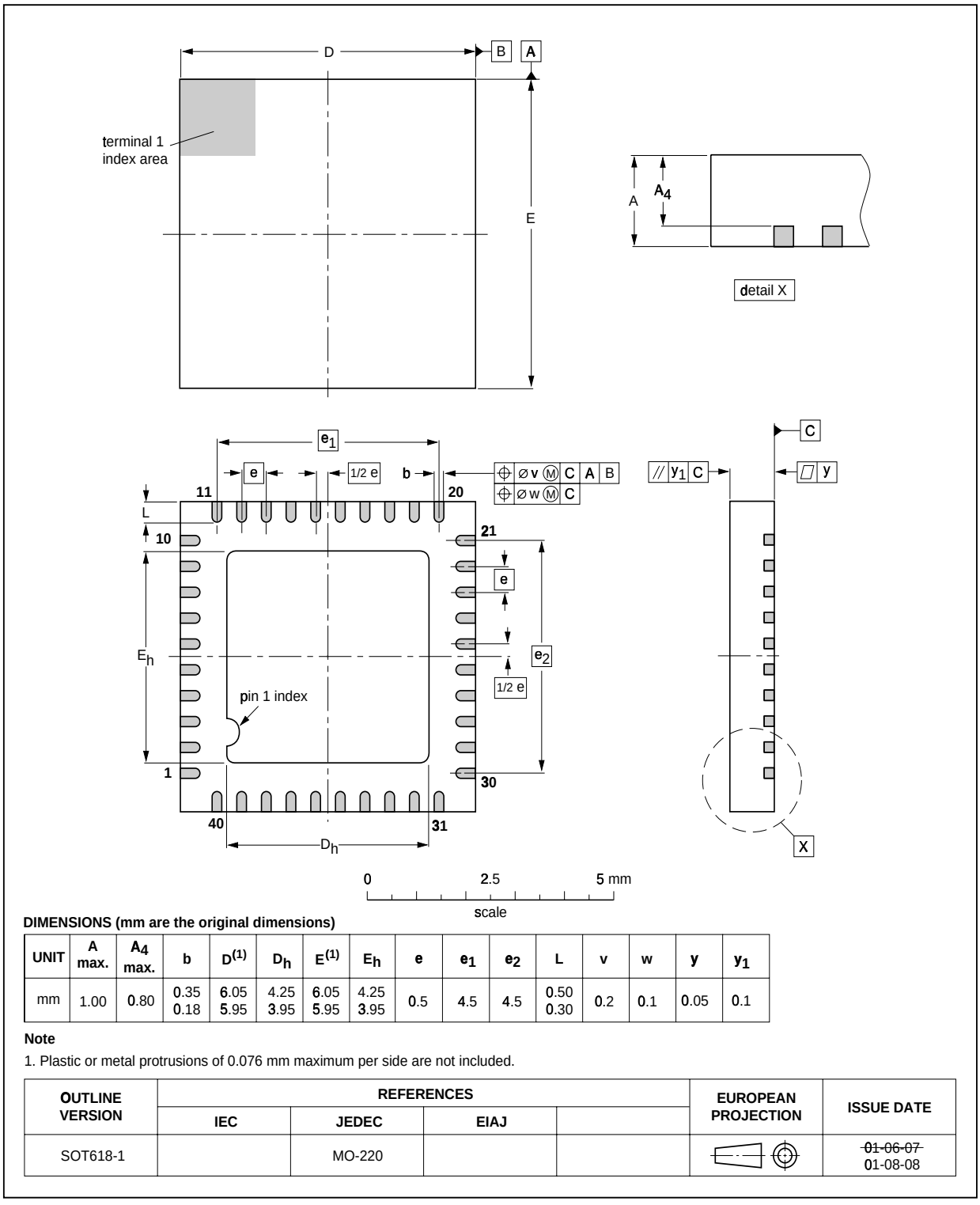


Fig 11. Application diagram.

18. Package outline

HVQFN40: plastic, heatsink very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm **SOT618-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_4 max.	b	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1.00	0.80	0.35 0.18	6.05 5.95	4.25 3.95	6.05 5.95	4.25 3.95	0.5	4.5	4.5	0.50 0.30	0.2	0.1	0.05	0.1

Note

1. Plastic or metal protrusions of 0.076 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT618-1		MO-220				~~01-06-07~~ 01-08-08

Fig 12. Package outline.

19. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe, it is desirable to take normal precautions appropriate to handling integrated circuits. Details on Electrostatic Discharge (ESD) can be found in the *Quality Reference Handbook*. The handbook can be ordered using the code 9397 750 02391.

20. Soldering

20.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

20.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C small/thin packages.

20.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

20.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

20.5 Package related soldering information

Table 34: Suitability of surface mount IC packages for wave and reflow soldering methods

Package	Soldering method	
	Wave	Reflow [1]
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable [2]	suitable
PLCC [3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [3] [4]	suitable
SSOP, TSSOP, VSO	not recommended [5]	suitable

[1] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[2] These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).

[3] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[4] Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[5] Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

21. Revision history

Table 35: Revision history

Rev	Date	CPCN	Description
0.01	4 Sep. 01		Creation
0.02	9 Oct. 01		Change package
0.03	5 Nov. 01		Specification review basis
0.04	10 Jan. 02		Corrected specification after review
0.05	5 Apr. 02		Corrected specification afer review (Apr. 04 2002)
0.06	23 Jan. 03		Updated specification
0.07	20 Nov. 03		Updated specification
0.08	04 Dec. 03		Updated specification
0.09	05 Jan. 04		Preliminary specification