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Flaircomm Microelectronics, Inc.

Bluetooth Module
FLC-BTM901
Datasheet

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Release Record

Version	Release Date	Comments
V1.0	September 20, 2019	Release
V1.1	December 26, 2019	Increase the description of BTM901IQ2C/D module

CONTENTS

TABLES AND FIGURES

1 Introduction

FLC-BTM901 is a system on-chip (SoC) with on-chip Bluetooth, audio and programmable application module. It includes high-performance, analog, and digital audio codecs, Class-AB and Class-D headphone drivers, advanced power management, Li-ion battery charger, light-emitting diode (LED) drivers, universal asynchronous receiver transmitter (UART), and programmable input/output (PIO). A range of audio processing capabilities are provided from ROM which are configurable in fully flexible audio graphs.

1.1 Naming Declaration

Product Revision	Description	Availability
A	Without internal antenna	Yes
B	With an internal antenna	Yes
C	With SD interface, without internal antenna	Yes
D	With SD interface, with an internal antenna	Yes

Table 1：Naming Declaration

1.2 Block Diagram

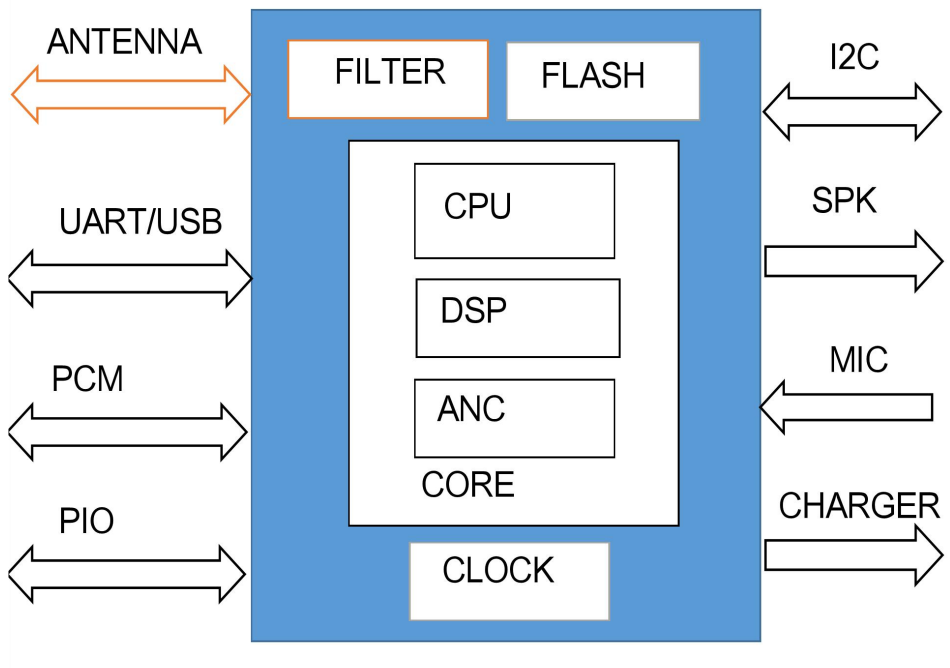


Figure 1: BTM901 Block Diagram

- Bluetooth ® V5.1
- Dual 120 MHz audio DSPs
- Firmware Processor for system
- 64M QSPI flash
- Advanced audio algorithms
- High-performance 24‑bit stereo audio interface
- Digital and analog microphone interfaces
- Active Noise Cancellation: Feedforward, Feedback, Hybrid
- UART , PCM
- Integrated PMU: Dual SMPS for system/digital circuits, Integrated Li-ion battery charger
- AIO,PIO

1.3 Applications

bluetooth headset

bluetooth speaker

vehicular audio system

2 General Specification

Bluetooth Specification	
Standard	Bluetooth 5.1 BR/EDR+BLE
Frequency Band	2.402GHz ~ 2.480GHz
System Clock	32MHz
Interface	UART,PIO, AIO, PCM，USB,I2C
Sensitivity	-94dBm@0.1%BER
RF TX Power	8dBm
Power	
Power Supply Voltage	2.8 ~ 6.5V DC
Output Voltage (Deep Sleep)	0.8-0.95V DC
Operating Environment	
Temperature	-40ºC to +85ºC
Dimension and Weight	
BTM901	20.8*11.8*2.8mm

Table 2:General Specification

3 Pin Configuration

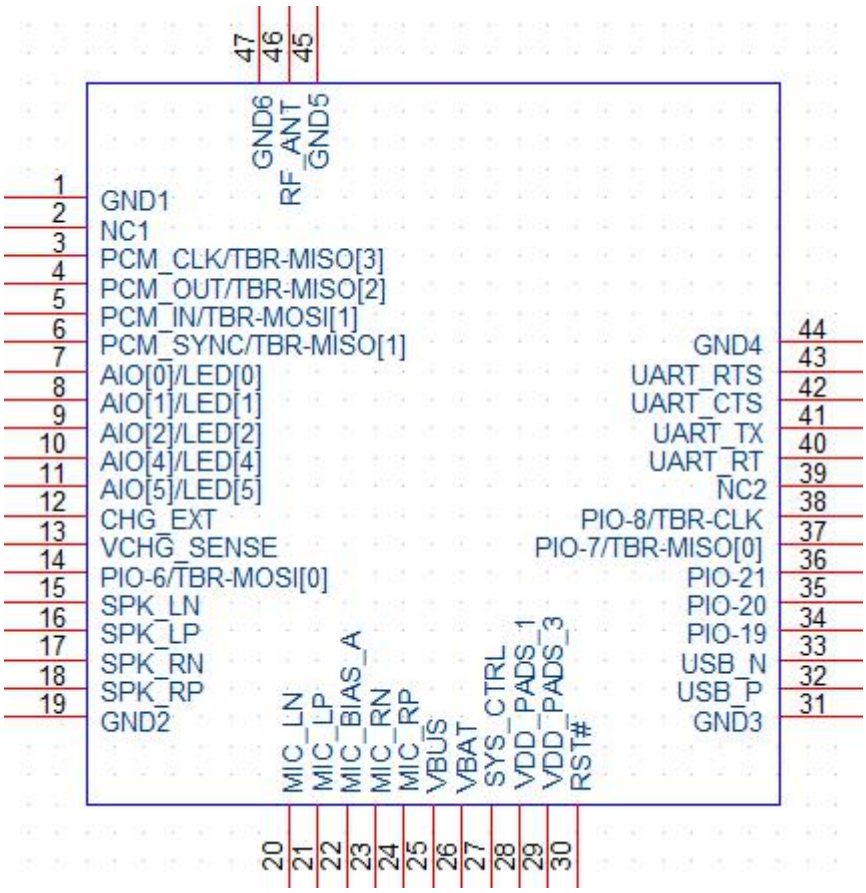


Figure 2:Pin Configuration of BTM901IQ2A/IQ2B

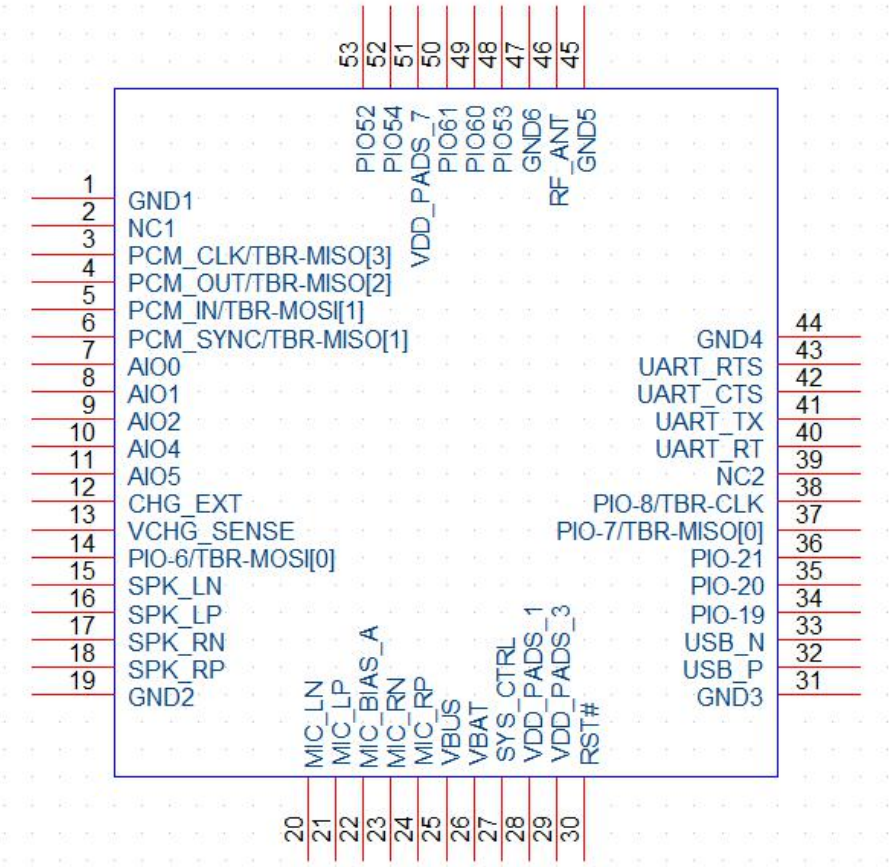


Figure 3：Pin Configuration of BTM901IQ2C/IQ2D

4 Pin Definition

4.1 BTM901 Pin Definition:

PIN	Symbol	PIN Type	Description
1	GND1	Power	Ground
2	NC1	NC	NC
3	PCM_CLK/TBR-MISO[3]	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 2. Alternative function:PCM_CLK TBR_MISO[3]
4	PCM_OUT/TBR-MISO[2]	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 3. Alternative function: PCM_OUT TBR_MISO[2]
5	PCM_IN/TBR-MOSI[1]	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 4. Alternative function: PCM_IN TBR_MOSI[1]
6	PCM_SYNC/TBR-MISO[1]	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 5. Alternative function: PCM_SYNC TBR_MISO[1]
7	AIO[0]/LED[0]	Analog or digital input/ open drain output.	General-purpose analog/digital input or open drain LED output.
8	AIO[1]/LED[1]	Analog or digital input/ open drain output.	General-purpose analog/digital input or open drain LED output.
9	AIO[2]/LED[2	Analog or digital input/ open drain output.	General-purpose analog/digital input or open drain LED output.
10	AIO[4]/LED[4]	Analog or digital input/ open drain output.	General-purpose analog/digital input or open drain LED output.
11	AIO[5]/LED[5]	Analog or digital input/ open drain output.	General-purpose analog/digital input or open drain LED output.
12	CHG_EXT	Analog	External charger transistor current control.
13	VCHG_SENSE	Analog	Battery voltage sense input.
14	PIO-6/TBR-MOSI[0]	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 6. Alternative function: TBR_MOSIO[0]

15	SPK_LN	Analog	Headphone/speaker differential left output, negative. Alternative function: Differential left line output, negative
16	SPK_LP	Analog	Headphone/speaker differential left output, positive. Alternative function: Differential left line output, positive
17	SPK_RN	Analog	Headphone/speaker differential right output, negative. Alternative function: Differential right line output, negative
18	SPK_RP	Analog	Headphone/speaker differential right output, positive. Alternative function: Differential right line output, positive
19	GND2	Power	Ground
20	MIC_LN	Analog	Microphone differential left input, negative. Alternative function: Differential audio line input left, negative
21	MIC_LP	Analog	Microphone differential left input, positive. Alternative function: Differential audio line input left, positive
22	MIC_BIAS_A	Analog	Mic bias output.
23	MIC_RN	Analog	Microphone differential right input, negative. Alternative function: Differential audio line input right, negative
24	MIC_RP	Analog	Microphone differential 2 input, positive. Alternative function: Differential audio line input right, positive
25	VBUS	Power	USB voltage input.
26	VBAT	Power	Battery voltage input.

27	SYS_CTRL	Digital Input	Boots device in response to a button press when power is still present from battery and/or charger but software has placed the device in the OFF or DORMANT state.
28	VDD_PADS_1	Power	1.8 V/3.3 V PIO supply.
29	VDD_PADS_3	Power	1.8 V/3.3 V PIO supply.
30	RST#	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Automatically defaults to RESET# mode when the device is unpowered, or in off modes. Reconfigurable as a PIO after boot. Alternative function: Programmable I/O line 1.
31	GND3	Power	Ground
32	USB_N	Digital	USB Full Speed device D- I/O. IEC-61000-4-2 (device level) ESD Protection
33	USB_P	Digital	USB Full Speed device D+ I/O. IEC-61000-4-2 (device level) ESD Protection
34	PIO-19	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 19.
35	PIO-20	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 20.
36	PIO-21	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 21.
37	PIO-7/TBR-MISO[0]	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 7. Alternative function: TBR_MISO[0]
38	PIO-8/TBR-CLK	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 8. Alternative function: TBR_CLK

39	NC2	NC	NC
40	UART_RX	D Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 18. Alternative function: UATR_RX
41	UART_TX	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 17. Alternative function: UART_TX
42	UART_CTS	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 16. Alternative function: UART_CTS
43	UART_RTS	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 15. Alternative function: UART_RTS
44	GND4	Power	Ground
45	GND5	Power	Ground
46	RF_ANT	RF	Bluetooth transmit/receive.
47	GND	Power	Ground
48	PIO53	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 53. Alternative function: SDIO_CMD
49	PIO60	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 60.
50	PIO61	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 61.
51	VDD_PADS_7	Power	1.8 V/3.3 V PIO supply.

52	PIO54	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 53. Alternative function: SDIO_D0
53	PIO52	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 53. Alternative function: SDIO_CLK

Table 3: BTM901 Pin Definition

NOTE :
Only BTM901IQ2C/BTM901IQ2D has pin48-53.

There is an internal 10 μA current source that can be connected to a thermistor typically for battery temperature monitoring. Any LED/IO can be multiplexed to this current source.

5 Device Details

5.1 Audio Subsystem

■ Dual 32-bit Kalimba audio digital signal processor (DSP) cores with flexible clocking from 2 MHz to 120 MHz to allow optimization and trade-off performance vs. power consumption

■ DSPs execute code from ROM and from program RAM, original equipment manufacturer (OEM) and third party developed features can run from program RAM

■ 80 KB program RAM

■ 256 KB data RAM

■ 5 Mb ROM

5.2 Application Subsystem

■ Dual-core application subsystem 32/80 MHz operation

■ 32-bit Firmware Processor:

■ Reserved for system use

■ Runs Bluetooth upper stack, profiles, house-keeping code

■ 32-bit Developer Processor:

■ Runs developer applications

■ Both cores execute code from external flash memory using QSPI clocked at 32 MHz or 80 MHz

■ On-chip caches per core allow for optimized performance and power consumption

5.3 Bluetooth Subsystem

■ Qualified to Bluetooth v5.1 specification including 2 Mbps Bluetooth low energy (Production parts)

■ Single ended antenna connection with on-chip balun and Tx/Rx switch

■ Bluetooth, Bluetooth low energy, and mixed topologies supported

■ Class 1 support

5.4 Li-ion Battery Charger

■ Integrated battery charger supporting internal mode (up to 200 mA) and external mode (up to 1.8 A)

■ Variable float (or termination) voltage adjustable in 50 mV steps from 3.65 V to 4.4 V

■ Thermal monitoring and management are implementable in application software

■ Pre-charge to fast charge transition configurable at 2.5 V, 2.9 V, 3.0 V, and 3.1 V

5.5 Power Management

■ Integrated power management unit (PMU) to minimize external components

■ BTM901 runs directly from a Li-ion, USB, or external supply (2.8 V to 6.5 V)

■ Auto-switching between battery and USB (or other) charging source

■ Power islands employed to optimize power consumption for variety of use-cases

■ Dual switch-mode power supply: Automatic mode selection to minimize power consumption

5.6 Audio Engine And Digital Audio Interfaces

■ 24-bit I²S interface with 1 input and 3 output channels

■ Programmable audio master clock (MCLK)

■ Sony/Philips digital interface (SPDIF): 2, configurable as input or output

■ Stereo analog outputs configurable as differential Class- AB headphone outputs or differential high efficiency Class-D outputs:

□ A signal-to-noise ratio (SNR) differential: 98 dBA typ.

□ A total harmonic distortion plus noise (THD+N) differential, 32 Ω load: -85 dB typ.

■ Dual analog inputs configurable as single ended line inputs or, unbalanced or balanced analog microphone inputs:

□ SNR single-ended: 96 dBA typ.

□ THD+N single-ended: -85 dB typ.

■ 1 microphone bias (single bias shared by the two channels):

□ Crosstalk attenuation between two inputs using recommended application circuit: 65 dB

■ Digital microphone inputs with capability to interface up to 6 digital microphones

■ Both analog-to-digital converter (ADC)s and digital-to- analog converter (DAC)s

support sample rates of 8, 16, 32, 44.1, 48, 96 kHz. DACs also support 192 kHz.

6 Bluetooth Subsystem

The Bluetooth subsystem is a dual-mode radio supporting concurrent classic and Bluetooth low energy operation. It is fully qualified to the Bluetooth v5.1 specification. It has:

- 32 MHz processor running Bluetooth firmware
- Bluetooth packet processing engine and modem
- A single power domain under control of the System Manager subsystem
- Power and clocks automatically removed to reduce power when the Bluetooth radio is not operating

6.1 Bluetooth v5.1

BTM901 supports Bluetooth v5.1 including Bluetooth low energy 2 Mbps.

6.2 Bluetooth Radio

The Bluetooth radio consists of a single RF I/O port shared for receive and transmit. The RF port impedance is 50 Ω.

6.3 Receiver

The receiver consists of an LNA that boosts the incoming RF signal. The passive mixer down-converts the wanted signal and splits the wanted output between I and Q quadrature-related channels. Passive low pass filtering at the output of the mixer attenuates out of band signals while allowing the wanted signal to pass through. This helps to avoid saturating the ADC input.

LNA, Mixer, and ADC gains are automatically controlled by the AGC and are based on saturation detection and wideband RSSI detection indications from the RF front end.
The receive ADC is a continuous time second order sigma-delta architecture

6.4 Transmitter

The transmitter is implemented using a polar transmit architecture. There are separate paths for phase and amplitude modulated data. The phase modulation (PM) path is used for basic rate modulation. The phase modulation and amplitude modulation is used for enhanced data rate modulation (EDR2 and EDR3).

The advantage of using a polar transmit architecture is that a nonlinear PA is usable. The PA is a Class-D design and therefore provides high-power efficiency compared to previous generation devices.

7 System Power States

In a system-wide low-power state, software moves between these static power states to reduce total system power.

7.1 No Power State

When the BTM901 has no power at all, it is in the No Power state. When power is present, for example on battery attach, the BTM901 automatically boots and moves to Active state.

7.2 Active State No Power State

In Active state, the BTM901 clocks and power supplies are running, and all functions of the BTM901 are available.

7.3 Shallow Sleep State

Shallow Sleep state is functionally the same as the Active state. However, individual subsystems can autonomously enter Shallow Sleep state to conserve power. In Shallow Sleep state, a subsystem can turn off or reduce the frequency of clocks and/or power down memories.

7.4 Deep Sleep State

In Deep Sleep state, the main digital power rail is in state retention. To reduce leakage the digital

voltage is typically reduced to 0.85 V. The main digital clocks are stopped and a limited number of device features remain active, including:

- Boot Manager
- LED PWM drivers
- PIO controller

BTM901 extensively uses digital power islands. Deep Sleep state current varies significantly depending on which functions are active or in state retention.

The following events can move BTM901 to Active state (selectable via software) from Deep Sleep state:

- A rising edge on SYS_CTRL
- A rising edge or a falling edge on VCHG

- Activity on any PIO
- Activity on any digital interface
- A timer
- Digital activity on any LED pads (when configured as a digital input)
- Activity on the debug interfaces
- USB device resume

7.5 Dormant State

In Dormant state, the PMU is enabled in an ultralow power mode. The main digital supply is off.

This configuration reduces power consumption but limits available device features.

In Dormant state, the following inputs can transition the IC to the Active state (selectable via software):

- A rising edge on SYS_CTRL
- A rising edge or a falling edge on VCHG
- Activity on any PIO[8:1]
- A timer

NOTE Time accuracy in Dormant state is limited to ±20 %

- Digital activity on any LED pad (when configured as digital inputs)

7.6 Off State

The Off state is different to No Power state because the BTM901 has power attached from VBAT. In this state the following events boot the chip and transition it to Active state:

- A rising edge on SYS_CTRL held high for 20 ms
- A rising edge on VCHG held high for 20 ms

NOTE: The device cannot power off with VCHG attached. Dormant state is the lowest possible power state when voltage is present on the VCHG input.

7.7 Transition Between Static Power States

Transition into Shallow Sleep and Deep Sleep states is automatic, with the system constantly entering the lowest power mode. Transition into the Dormant and Off states is under the control of the application software.

7.8 Power Islands

To reduce digital leakage the Bluetooth, Audio, and Applications subsystems are contained within separate power islands. When these subsystems are enabled, the power is applied automatically.

8 Host Interfaces Subsystem

Host interfaces within the Host Interfaces subsystem are shared by other BTM901 subsystems, for example Applications subsystem, Bluetooth subsystem, and Audio subsystem. Host interface sharing ensures that subsystems have access to the required interfaces as if they had their own dedicated host interface, and makes efficient use of a single host interface. These host interfaces can operate concurrently. The System Manager allocates host interface resources to individual subsystems as required. Each subsystem serviced by the Host Interface Subsystem has its own memory management unit (MMU), which is accessed directly by the Host Interface Subsystem via the transaction bus. Interrupts are routed to the correct subsystem.

8.1 Host Interfaces Subsystem Features

BTM901 supports the following Host Interfaces:

- ■ USB Device
  - □ Full Speed (12 Mbps)
  - □ Multiple IN and OUT endpoints, allocable individually
  - □ Charging support
- ■ UART
  - □ Supports H4 and BCSP HCI interfaces or raw UART to application
- ■ 2 x Bit Serializers that are configurable independently as
  - □ I²C Master
  - □ SPI Master

These host interfaces can operate concurrently, subject to pin multiplexing constraints, between the UART, SPI, and I²C. Host Interface signals for UART, SPI and I²C go via a PIO mux with a further multiplexing implemented at the top level to the PIOs. The Host Interface subsystem must be selected as the controlling subsystem for the relevant PIOs.

9 Applications Subsystem

The Applications subsystem is a processor-based subsystem that provides on-chip Bluetooth high-level protocol stack functionality and customer programmability.

The Applications subsystem controls several peripheral interfaces:

- Some other chip resources are programmable. For example, PIO controllers.
- Interfaces such as USB Device, UART, I²C, SPI.

9.1 Application Subsystem Features

Application subsystem features include:

- 2 x 32 MHz central processing unit (CPU) cores using Kalimba DSP architecture
  - 32‑bit reduced instruction set computer (RISC) core with DSP features, integrated for optimal control code execution
  - Sleep mode, interrupt controller, timers, zero overhead looping
  - Private data RAM, 32 KB on Developer processor
  - 2-way cache 16 KB on Developer processor
  - 8 KB of tightly coupled memory on Developer processor
  - Debug features such as hardware breakpoints, single step, PC trace, code instrumentation message support
- 32 KB shared buffer RAM
- A direct memory access (DMA) controller core with acceleration for data encryption and comparison, access to QSPI flash and remote subsystems
- Demand-paged buffer management hardware providing efficient use of shared memory by local and remote masters
- QSPI data path unit with support for flash at 32 MHz single data rate (SDR), inline decryption, smart multimaster arbitration
- Multiple remote subsystem interfaces for messaging, control, and data transfer between the various radio and audio subsystems

The Applications subsystem is powered and brought out of reset by the System Manager and starts up automatically when clocked.

The subsystem has a single power-island. Each RAM instance is controlled independently to optimize power.

10 Audio Subsystem

10.1 Audio Subsystem Features

Audio subsystem features include:

- CPU clock options:
  - 120/80/32 MHz for audio processing
- Program ROM: 5 Mb
- Program RAM/cache: 80 KB
- Data RAM size: 256 KB
- Analog DAC: Stereo analog outputs configurable as differential Class-AB audio outputs or differential high efficiency Class-D
- Analog ADC: Stereo analog inputs configurable as single ended line inputs, or unbalanced, or balanced analog microphone inputs
- I²S/PCM interface
  - One interface, 24‑bit
  - Supports 8, 16, 32, 44.1, 48, 96, 192 kHz sample rates
- SPDIF interfaces
  - 2, configurable as input or output
  - Supports 8, 16, 32, 44.1, 48, 96, 192 kHz sample rates
- Audio MCLK: Programmable, available on PIO[15]
- Audio engine
  - 2 Codec output channels, supporting 8, 16, 32, 44.1, 48, 96, 192 kHz sample rates
  - 6 Codec input channels supporting 8, 16, 32, 44.1, 48, 96 kHz sample rates
- Digital mics
  - 6 mono/3 stereo
  - Supports 500 kHz, 1, 2, 4 MHz clock frequencies
- Active Noise Cancellation: Hybrid, Feedforward, and Feedback modes

10.2 Dual Core Kalimba

The audio subsystem has identical 2 x 32‑bit, clocked up to 120 MHz dual Kalimba cores. Each core has its own set of timers, interrupt controllers, and caches. Caches are implemented in program RAM. Both Kalimba cores have identical memory maps that

enable them to see all RAMs, NVM interfaces, and buffers in remote subsystems and shared peripherals, such as codec and buffer access controller. Kymera framework runs on the audio core to communicate with the rest of the device.

10.3 Program ROM

The Audio subsystem has a 5 Mb ROM.

10.4 Program RAM And Caches

The Audio subsystem has 80 KB of program RAM implemented as 10 banks of 8 KB each. Caches are implemented in Program RAM.

Access for each bank is arbitrated individually. By default, each CPU has full access to entire RAM, but access permissions can be set up at a bank level. Each CPU supports:

- Direct mapped mode
- 2-way set-associative mode (full and half capacity)

10.5 Data RAM

The Audio subsystem has 256 KB of DM RAM divided into eight banks of 32 KB each. All RAM banks are equally accessible by the CPUs.

Data RAM is directly accessible to the audio engine for audio streaming and for remote access.

10.6 Buffer Access Controller

The BAC enables remote subsystems to access audio buffers and data RAM. The BAC implements operations to manipulate audio buffer data to save DSP MIPs. Audio engine streams data in and out of buffer RAM through the BAC.

10.7 Audio Engine

The Audio subsystem implements 6 inputs and 2 outputs codec channels to service the digital and analog audio interfaces. The subsystem also implements Active Noise Cancellation hardware.

10.7.1 Active Noise Cancellation

The following Active Noise Cancellation (ANC) modes are supported using Digital Mics or Analog Mics:

- Hybrid ANC

- Feedforward ANC
- Feedback ANC

11 Audio Subsystem

11.1 Analog Audio Interfaces

BTM901 analog interfaces include:

- Line/Mic inputs
- Line/Headphone outputs

11.1.1 Line/Mic Inputs

BTM901 has two high-quality audio input ADCs (HQADC), primarily intended for line input use, but also suitable for other applications that support mixed differential and single ended use cases. The ADC is 24- bit, and capable of sample rates from 8 kHz to 96 kHz. The HQADC is configurable, with an internal switch arrangement. VAG is a virtual ground reference. The software API allows for direct control of the nine switches, or a simpler control, supporting three standard modes:

- Stereo differential input (switch value 0xC6)
- Stereo single ended input, using the P inputs (switch value 0xA5)
- Stereo single ended input, using the N inputs (switch value 0x14A)

Inputs should be AC coupled, typically with a 2u2 capacitor. This capacitor value can be reduced at the expense of low frequency response attenuation.

Each ADC channel receives a differential/single-ended input and generates a 3- bit Delta-Sigma modulated output that goes to the decimation filter block in the digits. The ADC serves both line and mic modes. Both channels have independent references, and most control signals are also independent.

The input is fed into a programmable gain amplifier. The audio output from the pre-amplifier stage is always differential and has a maximum amplitude of 2.4 Vpp. The pre-amplifier can support single ended and differential inputs at the same input amplitude. At 0 dB gain the maximum input is 2.4 Vpp, see Table 4.

Analog system gain (dB)	Input impedance (kΩ)	Input amplitude (mVpp, differential, and single ended)
0	20	2400
3	20	1699
6	20	1203
9	20	852

12	20	603
15	20	427
18	20	302
21	20	214
24	20	151
27	10	107
30	10	76
33	10	54
36	10	38
39	10	27

Table 4:High-quality ADC Analog Gain vs. Input Impedance And Input Amplitude

If the audio signal is single ended, the input goes ~300 mV below ground and ~300 mV above the 1.8 V audio power supply rail. The input impedance is 20 kΩ with gains 0 dB to 24 dB, and 10 kΩ at higher gains. A gain of 0 dB is typically used for line-input while higher gain settings are used when a low-level MIC signal is sampled. Both channel's ADCs are driven with 8 MHz clock and produces the digital output with the same rate.

Inputs should be AC coupled, typically with a 2.2 μF capacitor. This capacitor value can be reduced at the expense of low frequency response attenuation.

The ADC clocks are derived from a 32 MHz low jitter reference clock.

BTM901 has a microphone bias source, capable of biasing two external analog microphones at a load current of up to 3 mA.

11.1.2 Line/Headphone Outputs

Two high-quality audio output DACs (HQDAC) drive stereo low impedance differential loads (BTL headphones) or Line out.

DAC clocks are derived from a 32 MHz low jitter reference clock.

The HQ-DACs support two modes of operation. Class-D is a high efficiency, switching mode amplifier. The secondary Class-AB is a linear amplifier, and consumes more power.

BTM901 also has a low-power mode, where the entire analog loop can be disabled and a digital PWM bit- stream can drive the Class-D amplifier directly. This low-power mode can be used to trade off performance vs. power consumption.

Mode	Description
Class-D	Enables a lower power consumption for the headset. 3-state BD modulation enables a filter-free configuration. Directly driven from the digital circuitry. Most of the analog portion is powered-down. Drives differential headphone loads of 16/32 Ω
Class-AB	Enables either headphone or speaker applications. Can drive the same headphone outputs instead of switching to Class-D. Typically, useful for driving high impedance loads such as differential line out, or analog input power amp.

Table 5:Headset Output Driver Modes

11.2 Digital Audio Interfaces

Audio digital interfaces include:

- Digital microphone inputs
- Standard I²S/PCM interface
- SPDIF interface
- Audio MCLK

11.2.1 Digital Microphone Inputs

Up to six channels of digital microphone inputs are supported. These are grouped as three pairs. Most digital mics can be configured to enable two microphones to share a single data line. BTM901 supports this mode. It is achieved by one microphone outputting data on the rising clock edge and the other outputting data on the falling edge of the clock, while otherwise tri-stating their output.

Four digital mic clock frequencies can be generated, configurable at 500 kHz, 1 MHz, 2 MHz and 4 MHz. The digital mic function can be assigned to PIOs, see Related Information.

11.2.2 Standard I²S/PCM Interface

BTM901 provides a standard I²S/PCM interface capable of operating at up to a 192 kHz sample rate. The I²S/PCM port is highly configurable, and has the following options:

- Master (generate CLK and WS) or Slave (receive CLK and WS)
- Word Select polarity
- Left or right justification
- Sign extension / zero pad
- Optional 1‑bit period delay on WS to start of channel data
- 13/16/24-bit per sample

- Up to four slots per frame

NOTE: In multislot operation with 3 or 4 slots per frame, data padding to 32 bits within slots is not possible.

11.2.3 LI²S/PCM Master Mode Timing Diagram

Symbol	Parameter	Min	Typ	Max	Unit
$t_{dmclksynch}$	Delay time from I2S_CLK high to I2S_SYNC high	—	—	20	ns
$t_{dmclkpout}$	2Delay time from I2S_CLK high to valid I2S_OUT	—	—	20	ns
$t_{dmclkhsyncl}$	Delay time from I2S_CLK high to I2S_SYNC low	—	—	20	ns
$t_{dmclklpoutz}$	Delay time from I2S_CLK low to I2S_OUT high impedance	—	—	20	ns
$t_{dmclkhpoutz}$	Delay time from I2S_CLK high to I2S_OUT high impedance	—	—	20	ns
$t_{supinclkl}$	Set-up time for I2S_IN valid to I2S_CLK low	—	—	20	ns
$t_{hpinclkl}$	Hold time for I2S_CLK low to I2S_IN invalid	—	—	—	ns

Table 6: I²S/Pcm Master Mode Timing Diagram Symbols

11.2.4 SPDIF Interface

SPDIF (IEC 60958) is a digital audio interface. It uses biphase coding to minimize the DC content of the transmitted signal, and enables the receiver to decode clock information from the transmitted signal. BTM901 has up to two SPDIF interfaces configurable as input or output. These interfaces are compatible with IEC 60958-1, IEC 60958-3, IEC 60958-4, and AES/EBU standards.

Signals are input/output via PIO and typically require external line drivers (for 75 Ω cabling) or optical transceivers (‘Toslink’). Any PIO is assignable for SPDIF use.

11.2.5 Audio MCLK

BTM901 has two internal clock sources for audio interfaces. A standard 120 MHz clock (divided down), or an independent PLL (MPLL) that is useable as an alternate MCLK frequency clock source for the I²S/PCM and SPDIF ports. When it cannot be generated directly from the 120 MHz clock, the MPLL can be output on a PIO for use by an external codec where low jitter I²S/PCM and SPDIF performance is required.

Table 7 lists the output frequencies that the MPLL can generate.

The MPLL increases system power consumption and therefore only used when necessary.

MCLK frequency (Hz)	Sample rate (kHz)		
	MCLK divided by 128	MCLK divided by 256	MCLK divided by 384
1,024,000	8	—	—
2,048,000	16	8	—
3,074,000	24		8
4,096,000	32	16	—
5,644,800	44.1	—	—
6,144,000	48	24	16
8,192,000	—	32	—
9,216,000	—	—	24
11,289,600	88.2	44.1	
12,288,000	96	48	32
16,934,400	—	—	44.1
18,432,000	—	—	48
22,579,200	176.4	88.2	—
24,576,000	192	96	—
33,868,800	—	—	88.2
36,864,000	—	—	96
45,158,400	—	176.4	—
49,152,000	—	192	—
67,737,600	—	—	176.4
73,728,000	—	—	192

Table 7:Audio MCLK Clock Output Frequencies

12 Peripheral Interfaces

12.1 PIO

BTM901 has the following digital I/O pads:

- 15 PIO pads
- 5 x pads intended for LED operation: AIO[5:4, 2:0]
- 1 x Reset (active low) pad: RES#
- 1 x Power-on signaling: SYS_CTRL, usable as an input after boot.
- USB device I/O: If not used for USB purposes, this port is usable as digital I/O

12.2 Standard I/O

The standard digital I/O pins (PIO) on BTM901 are split into separate pad domains. Each VDD_PADS domain can be separately powered, from 1.7 V to 3.6 V. The VDD_PADS of a particular pin should be powered before voltages are supplied to PIO powered by that domain otherwise back powering can occur through the ESD protection in the pad.

PIO can be programmed to have a pull-up or pull down with two strengths (weak and strong). PIO can also be programmed with a sticky function where they are strongly pulled to their current input state. PIO have a reset pull state, after reset the pulls can be re-configured by software.

PIO also have a programmable drive strength capability of 2, 4, 8, or 12 mA.

All PIO are readable by all subsystems, but for write access are assigned by software to particular subsystem control. PIO inputs are via Schmitt triggers.

12.3 Pad Multiplexing

A BTM901 pad’s function is chosen at runtime from multiple potential functions, using multiplexing.

In the input direction, signals driven into the chip, all PIOs are distributed to each subsystem and visible on the PIO status bus. It is the subsystem's responsibility to select I/Os of interest for a particular application.

In the output direction, the System Manager has overall control of PIO allocation and control. When a PIO is allocated to a particular subsystem, the output is propagated combinationally from the subsystem to the pad. That is, there are no registers between the subsystem and the pad.

The LED pins and some other peripheral I/O states can be read as virtual PIO,see Table

8.

Function	PIO
SYS_CTRL	PIO[0]
LED[5:4, 2:0]	PIO[71:70, 68:66]
USB_DN	IO[63]
USB_DP	PIO[62]

Table 8:Virtual PIO

12.4 RESET# reset Pin

The BTM901 digital reset pin (RES#) is an active low reset signal. PIO[1] defaults to RESET# upon boot.

The pin is active low and on-chip glitch filtering avoids the need to filter out any spurious noise that may cause unintended resets. The RESET# pin has a fixed strong pull-up to VDD_BYP, and therefore can be left unconnected. The input is asynchronous, and is pulse extended within BTM901 to ensure a full reset.

BTM901 contains internal Reset Protection functionality to automatically keep the power rails enabled and enable the system to restart after unintended reset (such as a severe ESD event). Therefore for short assertions of RESET# the device does not turn off due to Reset Protection functionality.

Assertion of RESET# beyond the Reset Protection timeout (typically greater than ~1.8 s) causes the device to power down. BTM901 then requires a SYS_CTRL assertion or VCHG attach to restart.

NOTE: BTM901 is always powered if VCHG is present. It does not power down if RESET# is asserted while VCHG remains present.

BTM901 is powered down via software-controlled methods rather than external assertion of RESET#.

Holding RESET# low continuously is not the lowest BTM901 power state, because pull downs are enabled on VCHG and VDD_BYP in this state.

After boot, PIO[1] is configurable as a digital PIO.

12.5 SYS_CTRL Pin

SYS_CTRL is an input pin that acts as a power on signal for the internal regulators. It can also be used as an input (appears to software as virtual PIO[0]) or as a multifunction button.

From the OFF state, SYS_CTRL must be asserted for >20 ms to start power up.

SYS_CTRL is VBAT tolerant (4.8 V max), and typically connected via a button to VBAT. SYS_CTRL has no internal pull resistor, and requires an external pull-down if left undriven.

SYS_CTRL can be logically disconnected from the power on signal for internal regulators by software. Therefore, for example, once booted, software takes control of the internal regulators and the state of SYS_CTRL is ignored by the regulators.

12.6 LED Pads

BTM901 contains six LED pads that are configurable in four different operating modes:

1. LED Driver: This mode is designed for driving LEDs. The pad operates as an open-drain pad, tolerable of voltages up to 7.0 V. Therefore the cathode of the LED should be connected to the BTM901 LED pad. Each pad is rated to sink up to 50 mA of current.

2. Digital / Button input: This mode is designed for slow input signals, typically buttons. It is not designed for fast switching digital inputs like SPI. For these types of inputs, use the standard PIOs. In this mode, an internal weak pull-down can be enabled. Typically this is used for active high button signals to ensure that the input returns to 0 when the button is released. The pads are 7.0 V tolerant and the logic 1 threshold is typically 1 V. In digital input mode, the logic inputs can be read by the software as virtual PIO[71:70, 68:66].

3. Analog input: In this mode, the LED pad is used as an analog input port. The pad voltage is routable to a 10‑bit auxiliary ADC. In analog input mode, the input range is 0 to VDD_1V8_LDO.

4. Disabled: This is the default state for LED pads, where the pad is 7.0 V tolerant and a high impedance with no pull-down.

12.7 LED Controllers

BTM901 has PWM-based LED controllers controlled by the Applications subsystem. They are usable for driving the LED pads or other PIOs.

It is possible for an application to configure the LED flash rate and ramp time.

Once configured, the LED flash and ramp rate are fully hardware controlled within the LED/PWM module. It is possible to synchronize any number of the LED drivers together. Together with the hardware flash/ramp, this is usable for generating color change sequences on RGB LEDs.

LED outputs are able to operate in Deep Sleep state, but not in Dormant state.

Each PWM block provides a set of 12 virtual PIOs. The configuration is the same whether the PWM controller is driving a PIO or an LED pad.

Table 9 shows the LED controller pattern for BTM901

LED_PWM Number	PIO											
LED_PWM[0]	PIO[0]	PIO[6]	—	PIO[18]	—	—	—	—	—	—	—	PIO[66]
LED_PWM[1]	PIO[1]	PIO[7]	—	PIO[19]	—	—	—	—	—	—	—	PIO[67]
LED_PWM[2]	PIO[2]	PIO[8]	—	PIO[20]	—	—	—	—	—	—	—	PIO[68]
LED_PWM[4]	PIO[4]	—	PIO[16]	—	—	—	—	—	—	—	—	PIO[70]
LED_PWM[5]	PIO[5]	—	PIO[17]	—	—	—	—	—	—	—	—	PIO[71]

Table 9: LED Controller Pattern

NOTE Not all PIOs may be usable with the PWM generator due to other functions being assigned by an OEM.

Table 10 shows how each LED_PWM maps to a specific PIO and LED_PAD on BTM901.

LED_PWM Number	=	PIO Number	=	LED_PAD Number
LED_PWM[0]	=	PIO[66]	=	LED_PAD[0]]
LED_PWM[1]	=	PIO[67]	=	LED_PAD[1]
LED_PWM[2]	=	PIO[68]	=	LED_PAD[2]
LED_PWM[04]	=	PIO[70]	=	LED_PAD[4]
LED_PWM[05]	=	PIO[71]	=	LED_PAD[5]

Table 10: LED_PWM to PIO to LED_PAD Mapping

12.8 USB Interface

BTM901 has a USB device interface: An upstream port, for connection to a host Phone/PC or battery charging adaptor.

12.8.1 USB Device Port

The device port is a USB2.0 Full Speed (12 Mb/s) port. Typically BTM901 enumerates as a compound device with a hub with the enabled audio source / sink / HID / mass storage device appearing behind this hub.

The DP 1.5 k pull-up is integrated in BTM901. No series resistors are required on the USB data lines. BTM901 contains integrated ESD protection on the data lines to IEC 61000-4-2 (device level). In normal applications, no external ESD protection is required.

Extra ESD protection is not required on VCHG (VBUS) because BTM901 meets the USB certification requirements of a minimum of 1uF, and a maximum of 10 μF being present on VCHG (VBUS).

The VCHG input of BTM901 is tolerant of a constant 6.5 V and transients up to 7.0 V. If extra overvoltage protection is required, external clamping protection devices can be used.

12.9 USB Charger Detection

BTM901 supports charger detection to the USB BCv1.2 standard.

It provides Data Contact Detection (DCD) using an internal current source, and provides:

- Detection of standard downstream ports (SDP)
- Charging downstream ports (CDP)
- Dedicated downstream ports (DCP)

The voltage on the USB data lines can be read by the 10‑bit auxiliary ADC. This allows detection of proprietary chargers that voltage bias USB the data lines.

For USB C type connectors, the LED pins can be used to detect the voltage on the CC line pins to detect the charge current capabilities of the upstream device.

13 System Manager

The System Manager runs from ROM and controls the allocation of the resources in the system and coordinates firmware operation using message-passing and interaction with the other subsystems.

Chip-level sleep modes are coordinated by the System Manager. Each subsystem indicates to the System Manager that they are asleep. System Manager can individually disable clocks and/or power to subsystems in turn to minimize device power.

13.1 System Timer

The System Manager maintains a 1 MHz system timer, which is distributed to the subsystems in the hardware using the transaction bus. The system time has 20 ppm, 250 ppm, and 20% modes to optimize current in low-power states.

14 PMU Subsystem

The power management unit (PMU) subsystem is designed to support Li-ion batteries, integrating a charger with Instant-On support. Instant-On enables BTM901 to operate regardless of the state of the battery, or even when the battery is removed.

14.1 Li-ion Charger

TheBTM901 Li-ion charger is designed to support small to large batteries (several Amp hours). It is connectable in one of two modes:

■ Internal configuration: Supporting charge rates of 2 mA to 200 mA with no external components required.

■ External configuration: Supporting charge rates of 200 mA to 1800 mA with the addition of one PNP pass device and external resistor.

14.2 General Charger Operation

The charger system has five main operating states. The current charger status can be read by application software.

14.2.1 Trickle Charge

This mode is entered when VBAT is sensed in the range 0 to Vpre. This is encountered only with a deeply discharged battery (below Vpre threshold, point (A)), or when the cell's battery protection circuit has opened, temporarily disconnecting the cell. It is used to pass a small charging current to safely charge a cell, and also cause a cell battery protection circuit to reset.

The hysteresis on Trickle charge into Pre-Charge is typically 100 mV.

During Trickle charge, BTM901 controls charge current internally. The external pass transistor is not used.

Parameter	Description	Min	Typ	Max
Vpre threshold (A)	Voltage at which the charger transitions out of Trickle charge into Pre-charge.	2.0 V	2.1 V	2.2 V
Itrick	Trickle charge current.	1 mA	-	50 mA

Table 11:Parameters In Trickle Charge

14.2.2 Pre-charge

This mode is entered when VBAT is sensed in the range Vpre to Vfast. In this range, it is not recommended to charge the cell at maximum rate, but a faster charge rate than that

of Trickle charge is allowable. Typically this is ~10 % to 20 % of the Fast charge rate. The Vfast threshold, point (B) is programmable.

The hysteresis on the Vfast transition from Pre-Charge to Fast charge is typically 200 mV.

During Pre-Charge, BTM901 controls the charge current internally and the external pass transistor is not used.

Parameter	Description	Min	Typ	Max
Vfast threshold (B)	Voltage at which the charger transitions out of Pre-charge into Fast charge.	0 = 2.8 V 1 = 2.9 V 2 = 3.0 V 3 = 2.4 V	0 = 2.9 V 1 = 3.0 V 2 = 3.1 V 3 = 2.5 V	0 = 3.0 V 1 = 3.1 V 2 = 3.2 V 3 = 2.6 V
Ipre	Pre-charge current.	2 mA	-	200 mA

Table 12:Parameters In Pre-Charge

14.2.3 Fast Charge

Fast charge has two parts:

■ Constant current: Entered when VBAT is sensed in the range Vfast to Vfloat point (C). This is the maximum charge rate, and should be set according to the battery manufacturers Data Sheet.

■ Constant voltage: When Vfloat is reached the cell voltage is maintained at Vfloat, and the current slowly reduces until the termination point (E) is reached where charging ceases, and the charger transitions to Standby mode.

Vfloat can be configured from 3.65 V to 4.40 V in 5 mV increments. This allows use of cells with different Vfloat values, or cell life extension by reducing Vfloat. Vfloat can also be altered depending on temperature change, for cell life protection.

The current termination point (E) can be adversely influenced by dynamic changes in VBAT load current, or to a lesser extent changes in VCHG voltage.

The current termination point (E) can be adversely influenced by dynamic changes in VBAT load current, or to a lesser extent changes in VCHG voltage.

Parameter	Description	Min	Typ	Max
Ifast	Ifast Fast charge current (Internal mode).	2 mA	-	200 mA
Ifast	Ifast Fast charge current (External mode).	2 mA	-	1.8 A
Termination point(E)	Transition from fast charge (constant voltage) to Standby. Expressed as % of Ifast.	-	0 = 10 1 = 20 2 = 30 3 = 40	-

Table 13:Parameters In Fast Charge

14.2.4 Standby Mode

Once the charge current has fallen and the charger is terminated, the system enters Standby mode. In Standby mode, the charger does not charge. It continues to monitor the battery voltage. If the voltage falls back below Vfloat by more than a configurable threshold Vhyst, point (D), then the charger re-enters Fast charge mode. Vhyst is expressed as a percentage of Vfloat.

In this way, the charger system maintains the cell near full charge while prolonging cell life.

Parameter	Description	Min	Typ	Max
Vhyst threshold (D)	Percentage of Vfloat at which the charger moves from Standby back to Fast charge.	0 = 0.006 1 = 0.018 2 = 0.030 3 = 0.042	0 = 0.012 1 = 0.024 2 = 0.036 3 = 0.048	0 = 0.018 1 = 0.030 2 = 0.042 3 = 0.054

Table 14: Parameters In Standby Mode

14.2.5 Battery Protection

Deeply discharging a Li-ion battery for a long time can cause irreversible damage, leading to excessive heating on a subsequent charger cycle.

To prevent this, customer application software should turn off the device at ~3.0 V. Typically cells have ~5 % usable capacity left at this point.

QTIL strongly recommends that all applications include a battery protection IC, normally built into the battery pack itself, as a secondary level of protection. This protection typically disconnects the battery cell if the voltage drops too low, or goes too high, and protects against overcurrent in the connections between BTM901 and the cell itself.

14.2.6 Temperature Measurement During Charging

Application layer software can be used to monitor the battery temperature using an NTC thermistor, typically mounted in contact with the cell. This information can then be used to disable charging or alter the charge current at extremes of temperature.

For temperature measurement, software can be configured to drive an enable signal to a potential divider, which consists of an external 10K resistor and 10K NTC in series. A PIO is used to provide a switched 1.8 V nominal supply to the external 10K resistor; this minimizes the external consumption. An LED pad would be required as a sense line from the 10K NTC thermistor.

14.3 Charging Modes

The BTM901P charger is designed to work in one of two modes:

■ Headset mode: Delivers a known current into the battery with the system (IC + all external components) running directly from VCHG.

■ Speaker mode: Limits the current taken from the VCHG port to a known value. In this mode, the system can take peak currents from the battery during charging, and as long as the average current into the battery is higher than the average current taken from the battery the system charges.

14.4 Charger With External Transistor

Charger with external transistor uses a single external PNP pass transistor is used for fast charge. BTM901 senses the charging current by measuring the voltage drop across an external sense resistor (between the VCHG and VCHG_SENSE pins) and controls the base current of the PNP transistor. At the higher currents available when charging with an external pass transistor, the routing of VBAT_SENSE becomes more critical. The VBAT_SENSE pin should be routed separately back to the battery itself to ensure that the cell voltage is sensed correctly and not influenced by volt drops in PCB tracks.

14.4.1 Selection of Sense Resistor Value

At maximum charge current setting, the sense resistor R sense should be chosen to give 100 mV voltage between the VCHG and VCHG_SENSE pins. For example, a 100 mΩ R sense resistor gives a max charge current of 1 A, while a 68 mΩ R sense resistor gives a max charge current of 1.5 A.

The fast charge current is configurable for charge currents equivalent to 5 mV steps over the range of 25 mV to 100 mV across R sense . Ensure that the sense resistor is suitably rated to dissipate heat generated within it. QTIL recommends 1% or lower tolerance R sense resistors to ensure accurate charge current measurement.

14.4.2 Selection of PNP Transistor

The PNP transistor should have an Hfe lower than 700. Do not use high gain or Darlington type transistors. Ensure that the transistor and heatsinking are suitably rated to dissipate generated heat at maximum charge current. Select an Hfe to keep the base current in normal operating modes in the range 0 mA to 40 mA. In low VCHG conditions, the base current may exceed this and BTM901 controls the base current to a safe limit.

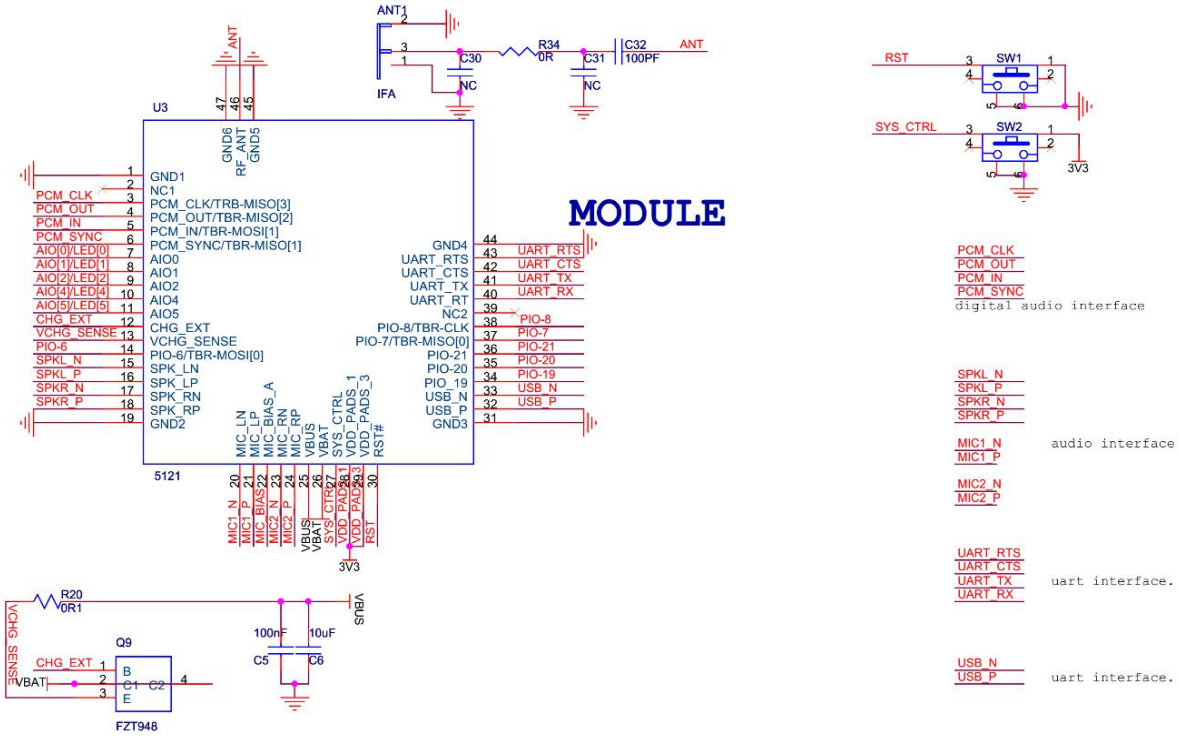
NOTE The base current of the PNP transistor is drawn from VCHG. Account for this if VCHG current has to be limited to a set maximum.

15 Bluetooth Performance Specification

Parameter	Condition	Min	Typ	Max	Unit
Bluetooth BR, EDR, BLE operation frequency range		2400		2483.5	MHz
Bluetooth BR, EDR channel spacing			1		MHz
BLE channel spacing			2		MHz
Bluetooth BR, EDR, BLE input impedance			50		Ω
BR RF output power			8		dBm
BLE RF output power			8		dBm
Bluetooth BR sensitivity			-94		dBm
Bluetooth EDR sensitivity			-86		dBm
BLE sensitivity-1Ms/s			-96		dBm
BR initial carrier frequency tolerance			±20		KHz

Table 15: Bluetooth Performance at 20°C

16 Reference Design



17 Recommended Reflow Profile

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

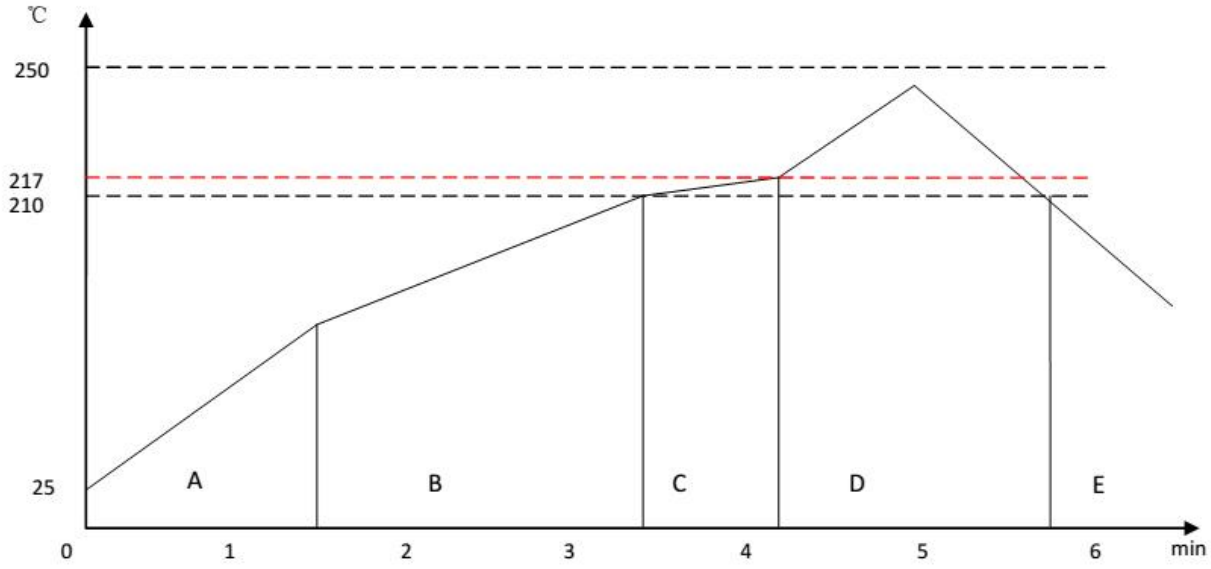


Figure 4: Recommended Reflow Profile

Pre-heat zone (A) —This zone raises the temperature at a controlled rate, typically 0.5 –2 ℃/s. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 ℃. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re -oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. The temperature is recommended to be 150℃to 210℃ for 60 to 120 second for this zone.

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217℃ for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint.

The recommended peak temperature (Tp) is 230 ~ 250℃. The soldering time should be 30 to 90 second when the temperature is above 217℃.

Cooling Zone (E) —The cooling ate should be fast, to keep the solder grains small which will give a longer lasting joint. Typical cooling rate should be 4 ℃.

18 Mechanical Characteristic

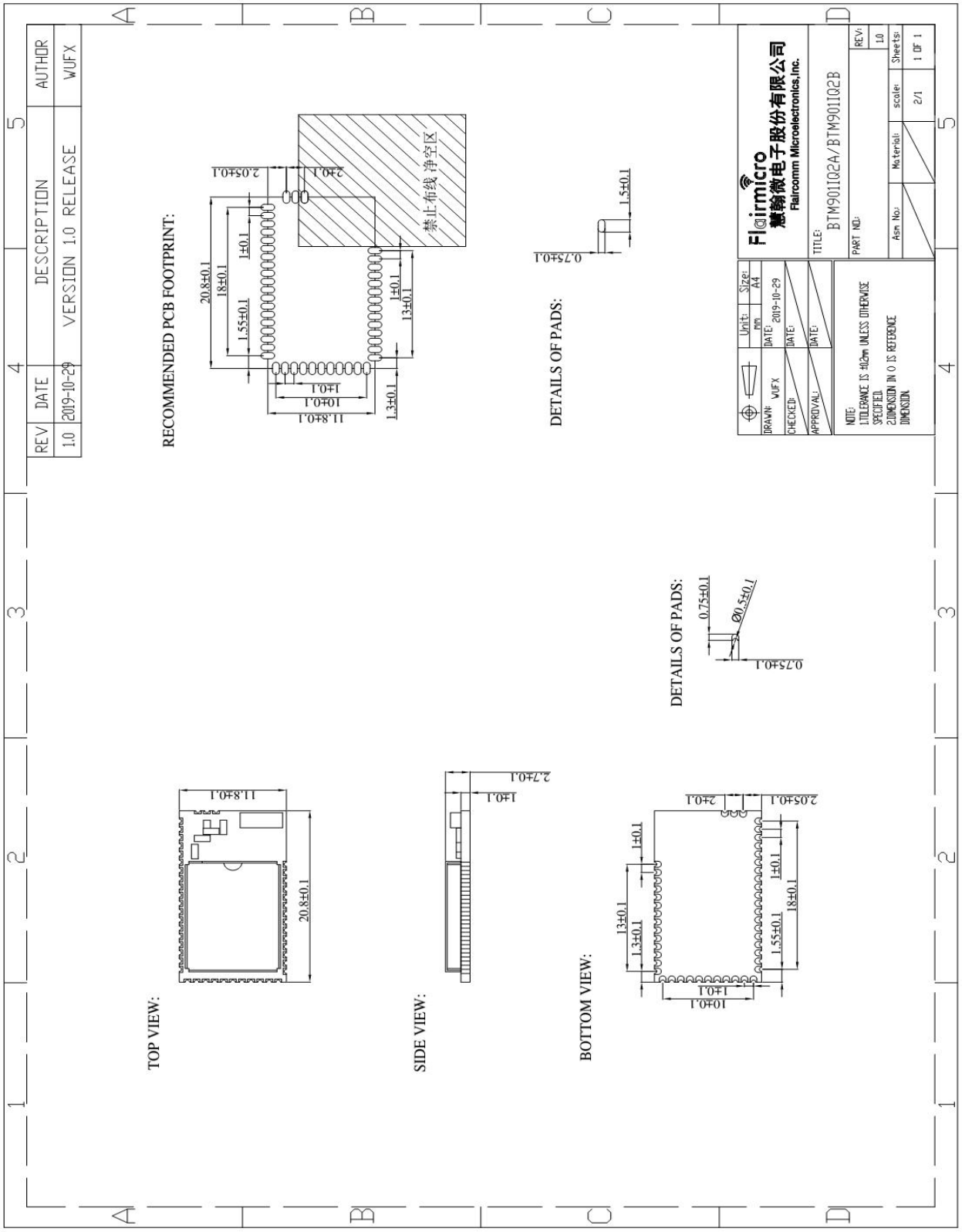


Figure 5：BTM901IQ2A/IQ2B

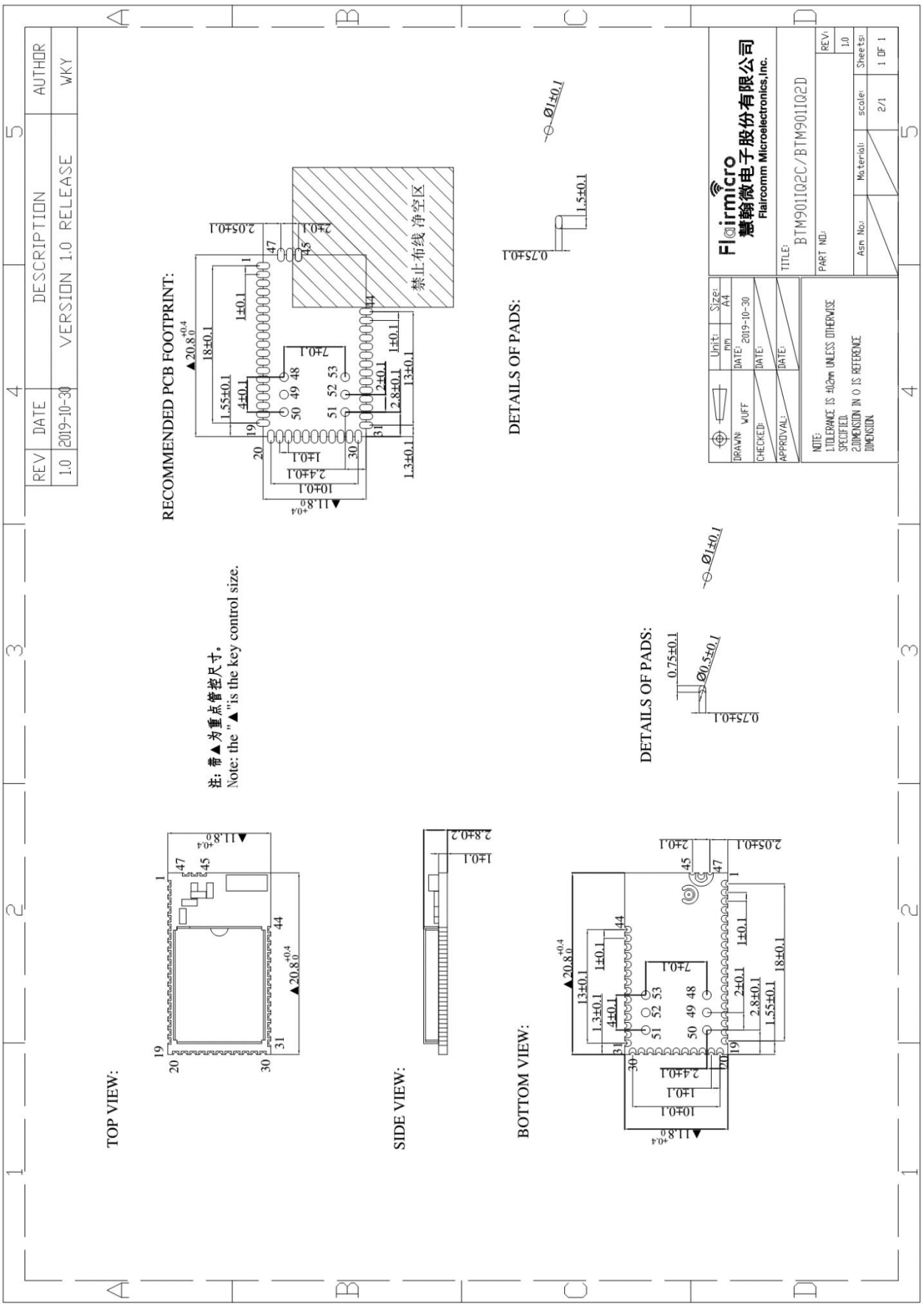


Figure 6：BTM901IQ2C/IQ2D

19 Recommended PCB Layout and Mounting Pattern

A very important factor in achieving maximum Bluetooth performance is the placement of a module with on-board antenna designs onto the carrier board and corresponding PCB layout. There should be no any trace, ground and vias in the area of the carrier board underneath the module's on-board antenna section as indicated in Figure 4. Antenna portion of the module must be placed at least 15mm away from any metal part and the antenna should not be covered by any piece of metal. The antenna of the module MUST be kept as far from potential noise sources as possible and special care must also be taken with placing the module in proximity to circuitry that can emit heat. The RF part of the module is very sensitive to temperature and sudden changes can have an adverse impact on performance.

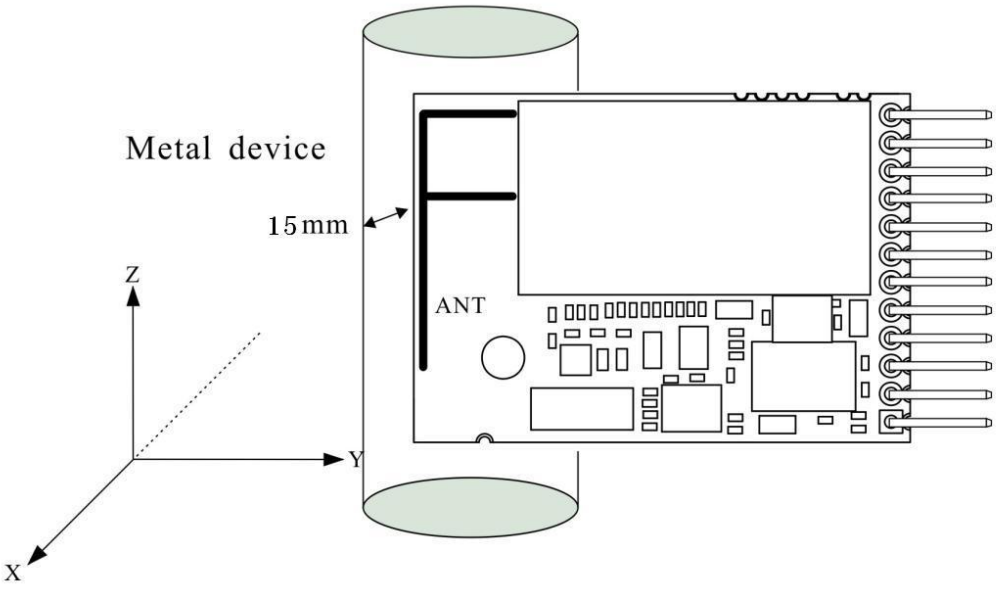


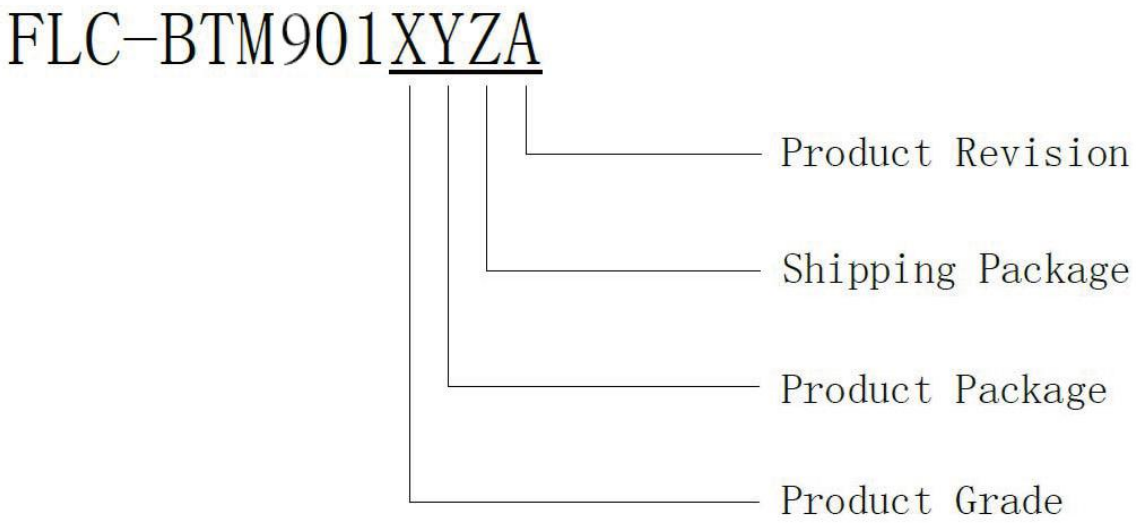
Figure 7：Leave 15mm Clearance Space from the Module Built-in Antenna

20 Ordering Information

20.1 Product Packaging Information

TBD

20.2 Ordering Information



20.2.1 Product Revision

Product Revision	Description	Availability
A	Without internal antenna	Yes
B	With an internal antenna	Yes
C	With SD interface, without internal antenna	Yes
D	With SD interface, with an internal antenna	Yes

Table 16: Product Revision

20.2.2 Shipping Package

Shipping Package	Description	Quantity	Availability
0	Foam Tray	—	No
1	Plastic Tray	100x10x3 = 3000	Yes
2	Tape	1000x5 = 5000	Yes

Table 17: Shipping Package

20.2.3 Product Package

Product Package	Description	Availability
Q	QFN	YES
L	LGA	NO
B	BGA	NO
C	Connector	NO

Table 18: Product Package

20.2.4 Product Grade

Product Grade	Description	Availability
C	Consumer	Refer to Table 15
I	Industrial	Refer to Table 15
V	Automobile After-Market	Refer to Table 15
A	Automobile Before-Market	Refer to Table 15

Table 19:Product Grade

21 Cautions &Warnings

21.1 FCC Statement

FCC standards: FCC CFR Title 47 Part 15 Subpart C Section 15.247 Ceramic Antenna with gain 0.5dBi(BT/BLE)

FCC Regulatory Compliance:
This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:
(1)this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.
If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures: -- Reorient or relocate the receiving antenna. -- Increase the separation between the equipment and receiver. -- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
-- Consult the dealer or an experienced radio/TV technician for help.
Warning: changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

If power exceeds the limit and the distance(Over 20cm distance in actual use between the device and user) is compliance with the requirement

RF Exposure Compliance:
This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the radiator and any part of your body.

Notice to OEM integrator
If the FCC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. The end product shall haves the words “Contains Transmitter Module FCC ID: P4I-BTM901”.
The device must be professionally installed.
The intended use is generally not for the general public. It is generally for industry/ commercial use.
The connector is within the transmitter enclosure and can only be accessed by disassembly of the transmitter that is not normally required. The user has no access to the connector.
Installation must be controlled. Installation requires special training.

Any company of the host device which installs this modular with unlimited modular approval should perform the test of radiated & conducted emission and spurious emission, etc. according to FCC part 15C: 15.247 and15.209 & 15.207, 15B Class B requirement, only if the tests result comply with FCC part 15C: 15.247 and 15.209 & 15.207, 15B Class B requirement, then the host can be sole legally.

When the module is installed inside another device, the user manual of the hose contain below
1) This device may not cause harmful interference.
2) This device must accept any interference received, including interference that may cause undesired operation

21.2 RF Warning Statement

The device has been evaluated to meet general RF exposure requirement. The device can be used in portable exposure condition without restriction.

21.3 IC Statement

This device complies with Industry Canada’s licence-exempt RSSs. Operation is subject to the following two conditions:

(1) This device may not cause interference; and
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Ce dispositif est conforme à la norme RSSs d'Industrie Canada applicable aux appareils radio exempts de licence. Son fonctionnement est sujet aux deux conditions suivantes:
(1) le dispositif ne doit pas produire de brouillage préjudiciable, et
(2) ce dispositif doit accepter tout brouillage reçu, y compris un brouillage susceptible de provoquer un fonctionnement indésirable.

Radiation Exposure Statement:
This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 15mm between the radiator & your body.

Déclaration d'exposition aux radiations:
Cet équipement est conforme aux limites d'exposition aux rayonnements IC établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 15mm de distance entre la source de rayonnement et votre corps.

21.4 FLC-BTM901 Label Instructions

The FLC-BTM901 module is designed to comply with the FCC statements.

The packaging of host system that uses BTM901 should display a label indicating the information as follows:

Contains

FCC ID: P4I-BTM901

Model: FLC-BTM901
(Series models: FLC-BTM901IQ2A/ FLC-BTM901IQ2B/
FLC-BTM901IQ2C/ FLC-BTM901IQ2D)

Any similar wording that expresses the same meaning may also be used.

21.5 FLC-BTM901 Antenna Statement

Note: In this section, “A” and “B” and “C” and “D” in “BTM901A” and “BTM901B” and “BTM901C” and “BTM901D” refer to Product Revision. Please see Section 20.2.1 for reference.

21.5.1 BTM901A and BTM901C (Without Antenna)

There is no built-in antenna in BTM901A and BTM901C. In order to make the product compliant with the FCC standard, the applicable antennas which designers choose should be similar to the antenna in BTM901B and BTM901D in specifications and radiation patterns. And the gain should be less than the peak gain of the antenna in BTM901B and BTM901D. If designers choose a different antenna, additional testing and

equipment authorization are needed to ensure the compliance with FCC statement.

21.5.2 BTM901B and BTM901D (With Antenna)

Antenna specifications of BTM901B and BTM901D are listed in the following table:

Part Number	Frequency Range (MHz)	Peak Gain （XZ-V）	Average Gain （XZ-V）	VSWR	Impedance
AT3216-B2R7HAA_	2400 ~ 2500	0.5 dBi typ.	-0.5 dBi typ.	2 max.	50 Ω

Table 20: Antenna Specifications

Operating Temperature Range:-40 ~ +85 ℃
Storage Temperature Range: -40 ~ +85 ℃

Power Capacity: 3W max.

The following figures show the Radiation Patterns of the antenna in BTM901B and BTM901D.

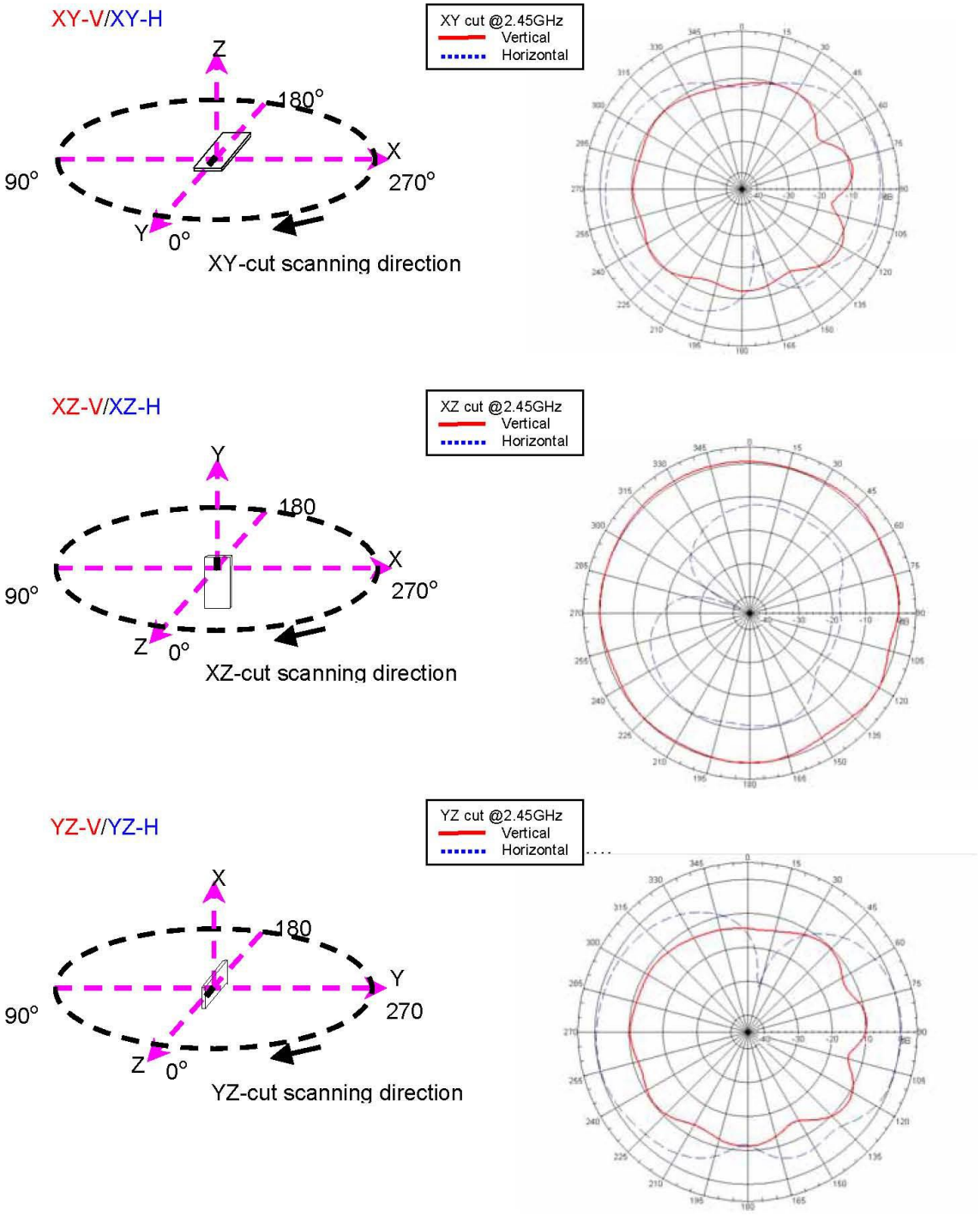


Figure 8: Radiation Patterns of Antenna

CE Statement

Herby,Flaircomm Microelectronics, Inc. declares that this Bluetooth Module，FLC-BTM901 is in compliance with the essential requirements and other relevant provisions of Directive 2014/53/EU.
In accordance with Article 10(2) and Article 10(10), this product allowed to be used in all EU member states.

Use the Bluetooth Module in the environment with the temperature between -40℃ and 85℃

Operating frequency：For BT/BLE: 2402MHz~2480MHz
Max output power: BT: 0.0024W BLE: 0.0026W

Manufacturer：Flaircomm Microelectronics, Inc.
Address：7F, Guomai Building, 116 East JiangBin Ave, Fuzhou, Fujian, China
Tel: +86-591-88833388
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E-mail: chenzhou.yu@flairmicro.com

DECLARATION OF CONFORMITY

I hereby declare that the product

Product:
Product Name: Bluetooth Module
Model: FLC-BTM901, FLC-BTM901IQ2A, FLC-BTM901IQ2B, FLC-BTM901IQ2C, FLC-BTM901IQ2D
Brand Name: Flairmicro
Hardware Version: V0.1
Software Version: V1.0

(Name of product, type or model, batch or serial number)

satisfies all the technical regulations applicable to the product within the scope of Council Directives 2014/53/EU, 2014/35/EU and 2014/30/EU:and declare that the same application has not been lodged with any other notified body.

EN 62368-1:2014+A11:2017
EN 62479:2010
Draft ETSI EN 301 489-17 V3.2.2 (2019-12)
ETSI EN 301 489-1 V2.2.3 (2019-11)
ETSI EN 300 328 V2.2.2 (2019-07)

(Title(s) of regulations, standards, etc.)

All essential radio test suites have been carried out.

NOTIFIED BODY: MiCOM Labs Inc
- **Address**:

575 Boulder Court,
Pleasanton, California94566
USA
Identification Number: 2280

MANUFACTURER or **AUTHORISED REPRESENTATIVE**:

- **Address**:

Flaircomm Microelectronics, Inc.
7F, Guomai Building, 116 East JiangBin Ave, Fuzhou, Fujian, China

This declaration is issued under the sole responsibility of the manufacturer and, if applicable, his authorised representative.

Point of contact:

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(Name, telephone and fax number)

2020-03-24
(Place, date of issue)

(Signature)

chenzhou yu, N/A
(Name and title in block letters)