Flairmicro

Flaircomm Microelectronics, Inc.

FLC-BTM702
Datasheet

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V1.0	March 13, 2018	Release
V1.1	April 13,2018	1. Increase the module's model:BTM702IQ2C and BTM702IQ2D 2. Increase the power description 3. Modify PIO's name

CONTENTS

TABLES AND FIGURES

1. Introduction

FLC-BTM702 is a small form factor, low power and highly economic Bluetooth radio module that allows OEM to add wireless capability to their products. The module supports multiple interfaces that make it simple to design into fully certified embedded Bluetooth solutions.

With FLC's AT+™ programming interfaces, designers can easily customize their applications to support different Bluetooth profiles, such as HS/HF, A2DP, AVRCP, SPP, and etc. The module supports Bluetooth® Enhanced Data Rate (EDR) ,BT5.0 and delivers up to 3 Mbps data rate for distances to 10M.

The module is an appropriate product for designers who want to add wireless capability to their products.

1.1 Naming Declaration

New Naming	Old Naming	Description
FLC-BTM702IQ2A	NA	Without shielding case
FLC-BTM702IQ2B	NA	With a shielding case
FLC-BTM702IQ2C	NA	Support aptX；Without a shielding case
FLC-BTM702IQ2D	NA	Support aptX；With a shielding case

Table 1: Naming Declaration

1.2 Block Diagram

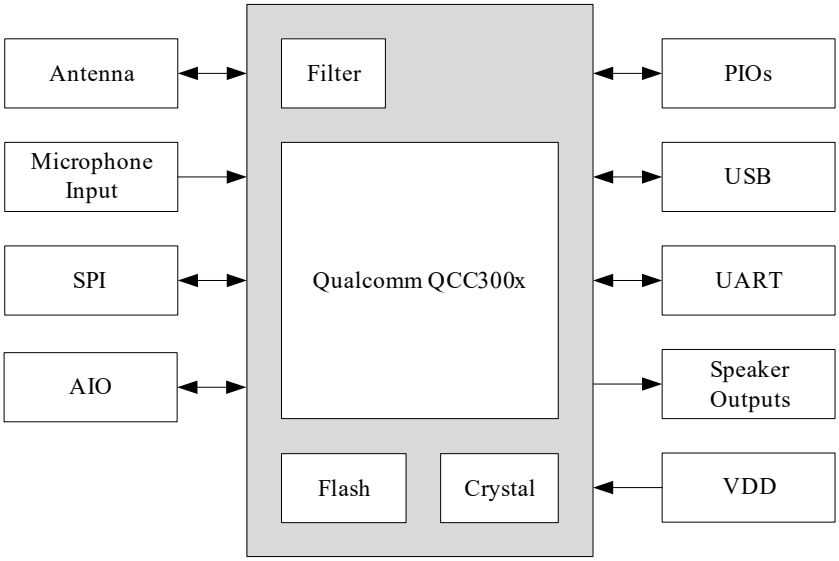


Figure 1: Block Diagram

1.3 Features

- Fully qualified single-chip dual mode Bluetooth v5.0
- Profiles including HS/HF, A2DP, AVRCP, SPP, and etc.
- UART and USB programming and data interfaces
- Small form factor
- SMT pads for easy and reliable PCB mounting
- Qualcomm TrueWireless™ Stereo (TWS), which allows two devices to be configured as a stereo pair
- SBC and AAC audio codecs.
- FLC-BTM702IQ2C/ FLC-BTM702IQ2D support aptX and aptX low latency

1.4 Applications

- Automobile hands-free applications
- Stereo headset applications
- Cable replacements
- Bar code and RFID scanners

- Measurement and monitoring systems
- Industrial sensors and controls
- Medical devices
- Industrial PCs and laptops

2. General Specification

Bluetooth Specification	
Standard	Fully qualified single-chip dual mode Bluetooth v5.0 , Class 1.5[a]
Profiles	HS/HF, A2DP, AVRCP, SPP, etc. detailed profiles depends on the firmware
Frequency Band	2.402GHz ~ 2.480GHz
Maximum Data Rate	3Mbps
RF Input Impedance	50 ohms
Baseband Crystal OSC	26MHz
Interface	UART, PIO, AIO, USB, SPI, Speaker, Microphone, etc.
Sensitivity	-85dBm@0.1%BER
RF TX Power	7dBm
Power	
Supply Voltage	2.7V ~ 3.6V DC
Working Current	Depends on profiles
Operating Environment	

Temperature	-40ºC to +85ºC
Humidity	10%~90% Non-Condensing
Dimension and Weight	
Dimension	23.2mm x 11.9mm x 2.0mm

Table 2: General Specification

a) The maximum RF TX Power is 9dBm.

3. Pin Definition

3.1 Pin Configuration

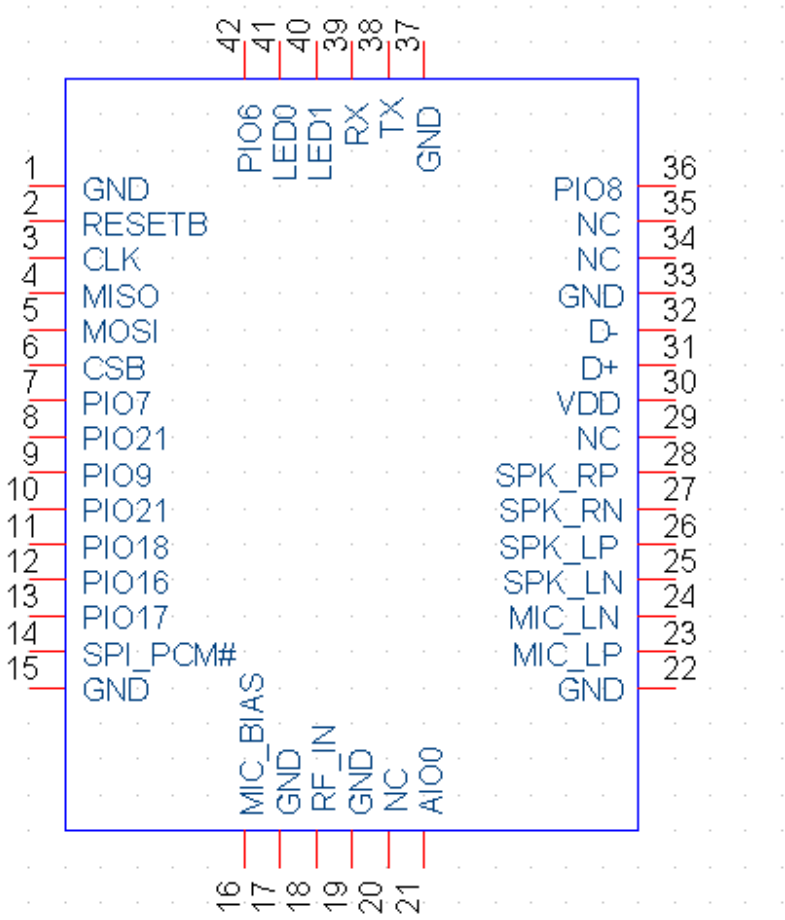


Figure 2: Pin Configuration

3.2 Pin Definition

Pin	Symbol	I/O Type	Description
1	GND	Ground	Ground
2	RESETB	Input with strong pull-up	Reset if low. Pull low for minimum 5ms to cause a reset.
3	SPI_CLK	Bidirectional with weak pull-down	SPI_CLK: Debug SPI clock Alternative function: • I2S_SCK:I²S synchronous data clock
4	SPI_MISO	Bidirectional with weak pull-down	SPI_MISO: Debug SPI data output Alternative function: • I2S_SD_OUT:I²S synchronous data output

5	SPI_MOSI	Bidirectional with weak pull-down	SPI_MISO: Debug SPI data input Alternative function: • I2S_SD_IN:I²S synchronous data input
6	SPI_CSB	Bidirectional with weak pull-down	SPI_CSB: chip select for Debug SPI, active low Alternative function: • I2S_WS:I²S word select
7	PIO7	Bidirectional with strong pull-down	Programmable input/output line Alternative function: • I2S2_WS:I²S2 word select
8	PIO21	Bidirectional with weak pull-down	Programmable input/output line
9	PIO9	Bidirectional with strong pull-down	Programmable input/output line Alternative function: • I2S2_SD_SCK:I²S2 synchronous data clock • UART_CTS:UART clear to send, active low
10	PIO21	Bidirectional with weak pull-down	Programmable input/output line
11	PIO18	Bidirectional with weak pull-down	Programmable input/output line
12	PIO16	Bidirectional with strong pull-up	Programmable input/output line Alternative function: • UART_RTS:UART request to send, active low
13	PIO17	Bidirectional with strong pull-down	Programmable input/output line Alternative function: • UART_CTS:UART clear to send, active low
14	SPI_PCM #	Input with weak pull-up	SPI/I²S select input: • 0=I²S/PIO interface • 1=SPI
15	GND	Ground	Ground
16	MIC_BIAS	Analogue	Microphone Bias
17	GND	RF Ground	RF ground
18	RF_IN	Analogue	Transceiver input/output line
19	GND	RF Ground	RF ground
20	NC	NC	NC
21	AIO0	Bidirectional	Analogue Programmable input/output line
22	GND	Ground	Ground
23	MIC_LP	Analogue	Microphone input positive

24	MIC_LN	Analogue	Microphone input negative
25	SPK_LN	Analogue	Speaker output negative (left side)
26	SPK_LP	Analogue	Speaker output positive (left side)
27	SPK_RN	Analogue	Speaker output negative (right side)
28	SPK_RP	Analogue	Speaker output positive (right side)
29	NC	NC	NC
30	VDD	3.3v power input	3.3v power input
31	USB_DP	Bidirectional	USB data plus with selectableinternal1.5kpull-upresistor
32	USB_DN	Bidirectional	USB data minus
33	GND	Ground	Ground
34	NC	NC	NC
35	NC	NC	NC
36	PIO8	Bidirectional with strong pull-up	Programmable input/output line Alternative function: • I2S2_SD_IN:I²S2 synchronous data input • UART_RTS:UART request to send, active low
37	GND	Ground	Ground
38	UART_TX	Bidirectional with strong pull-up	UART data output
39	UART_RX	Bidirectional with strong pull-up	UART data input
40	LED1	Bidirectional	Open-drain output
41	LED0	Bidirectional	Open-drain output
42	PIO6	Bidirectional with strong pull-down	Programmable input/output line Alternative function: • I2S2_SD_OUT:I²S2 synchronous data output

Table 3: Pin Definition

NOTE: Pin8 and pin10 are connected inside the module to accommodate the needs of old customers.

4. Physical Interfaces

4.1 RESETB

BTM702 is reset from several sources:

- RESETB pin
- Power-on reset
- Software configured watchdog timer
- UART break character

The RESETB pin is an active low reset. Assert the reset signal for a period > 5 ms to ensure a full reset.
At reset the digital I/O pins are set to inputs for bidirectional pins and outputs are set to tristate.

4.1.1 Digital Pin States on Reset

Table 4 shows the pin states of BTM702 on reset.

Pin Name / Group	I/O Type	Reset
USB_DP	Digital bidirectional	Tristate
USB_DN	Digital bidirectional	Tristate
PIO0	Digital bidirectional	Strong PU
PIO1	Digital bidirectional	Strong PD
PIO2	Digital bidirectional	Weak PD
PIO3	Digital bidirectional	Weak PD
PIO4	Digital bidirectional	Strong PU
PIO5	Digital bidirectional	Strong PD
PIO6	Digital bidirectional	Strong PD
PIO7	Digital bidirectional	Strong PD

Table 4: Pin Status on Reset

4.2 Automatic Reset Protection

BTM702 includes an automatic reset protection circuit that restarts the BTM702 when an unexpected reset occurs, for example, ESD strike or lowering of RST#. This reset protection circuit automatically restarts theBTM702 and enables the application to restore previous operation.
NOTE If RESETB is held low for > 2.4 s and VDD is not applied, BTM702 turns off. A rising edge on VDD is then required to power on BTM702.

4.3 Serial Interfaces

4.3.1 USB Interface

BTM702 has a full-speed (12 Mbps) USB interface for communicating with other compatible digital devices.
The USB interface on BTM702 acts as a USB peripheral, responding to requests from a master host
controller.
BTM702 contains internal USB termination resistors and requires no external resistors.
BTM702 supports the Universal Serial Bus Specification, Revision v2.0 (USB v2.0 Specification).

4.3.2 UART Interface

BTM702 has a UART serial interface that provides a simple mechanism for communicating with other serial devices using the RS232 protocol, including for test and debug.
When BTM702 is connected to another digital device, UART_RX and UART_TX transfer data between the 2 devices.
UART configuration parameters, such as baud rate and packet format, are set using the BTM702 firmware.
NOTE: To communicate with the UART at its maximum data rate using a standard PC, the PC requires an accelerated serial port adapter card.
The use of UART and USB are mutually exclusive.

Parameter		Possible Values
Baud rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4Mbaud (≤1%Error)
Flow control		None

Parity	None, Odd or Even
Number of stop bits	1 or 2
Bits per byte	8

Table 5: Possible UART Settings

Table 6 lists common baud rates and their associated error values for PSKEY_UART_BITRATE. To set the UART baud rate, load PSKEY_UART_BITRATE with the number of bits per second.

Baud rate	PS Key value(bits per second)	Error
1200	1200	1.73%
2400	2400	1.73%
4800	4800	1.73%
9600	9600	-0.82%
19200	19200	0.45%
38400	38400	-0.18%
57600	57600	0.03%
76800	76800	0.14%
115200	115200	0.03%
230400	230400	0.03%
460800	460800	-0.02%
921600	921600	0.00%
1382400	1382400	-0.01%
1843200	1843200	0.00%
2764800	2764800	0.00%
3686400	3686400	0.00%

Table 6: Standard Baud Rates

4.3.3 SPI

The synchronous serial port interface (SPI) can be used for system debugging. It can also be used for in-system programming for the flash memory within the module. SPI interface uses the SPI_MOSI, SPI_MISO, SPI_CSB and SPI_CLK pins.
The module operates as a slave and thus SPI_MISO is an output of the module. SPI_MISO is not in high-impedance state when SPI_CSB is pulled high. Instead, the module outputs 0 if the processor is running and 1 if it is stopped. Thus the module should NOT be connected in a multi-slave arrangement by simple parallel connection of slave SPI_MISO lines.

4.4 Audio Interface

4.4.1 Audio Codec Interface

The interface provides following features:

- Mono analogue input for voice band and audio band
- Stereo and mono analogue output for voice band and audio band

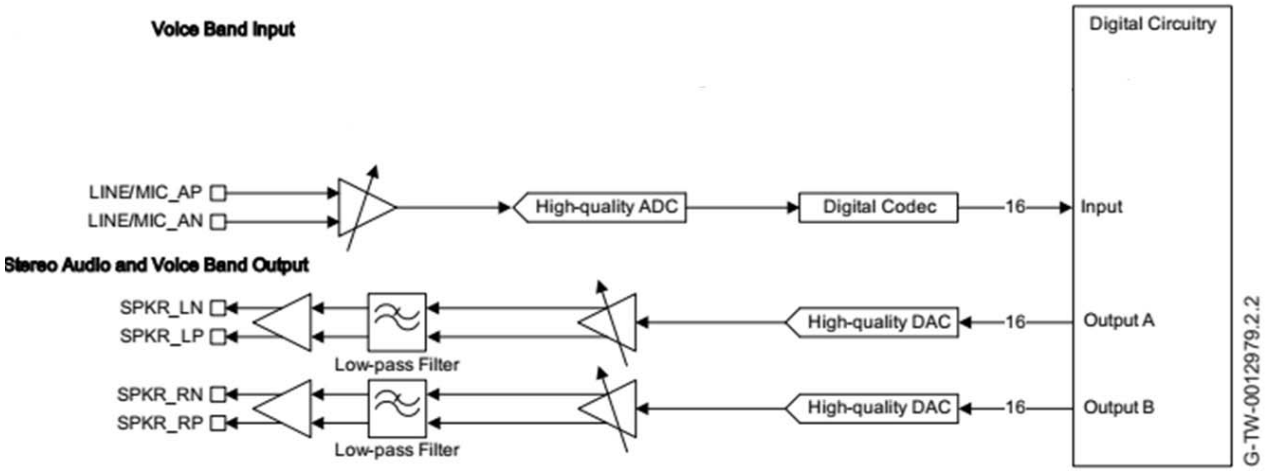


Figure 3: Audio Input and Output

The BTM702 audio codec uses a fully differential architecture in the analog signal path. This architecture results in low common-mode-noise sensitivity and good power supply rejection while effectively doubling the signal amplitude. The module features a differential stereo audio output interfaces.

4.4.1.1 ADC

The ADC has a second-order Sigma-Delta converter.
The ADC is a separate channel with identical functionality.
Each channel has an analog and a digital gain stage.

4.4.1.2 ADC Sample Rate Selection

ADC supports the following sample rates: 8kHz, 11.025kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz，48Khz.

4.4.1.3 ADC Audio Input Gain

The audio input gain consists of the following components:
An analog gain stage based on a pre-amplifier and an analog gain amplifier.
A digital gain stage.

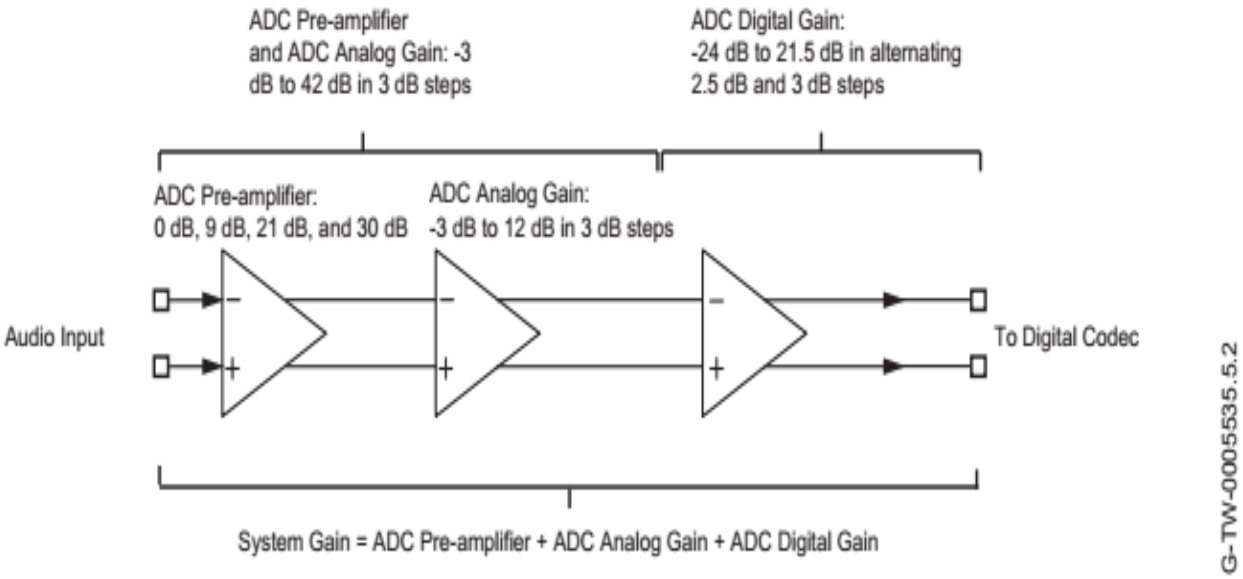


Figure 4: Audio Input Gain

4.4.1.4 ADC Pre-Amplifier And Analog/Digital Gain

The gain of the ADC inputs can be configured in the range of -27 dB to 63.5 dB steps, making it suitable for line and microphone input levels. 0 dB is 1600 mV pk-pk input.
The ADC input impedance is nominal 6 kΩ except when 0 dB pre-amplifier gain is selected when it becomes 12 kΩ.
If the input pre-amplifier is disabled, the input impedance varies between 6 kΩand 34 kΩ depending on gain selection. In normal operation, the input pre-amplifier is enabled.
Calls connected by the VM stream automatically select the distribution of gain within the ADC for best performance. Alternatively, the individual gain stages can be set.

4.4.1.5 ADC Digital Gain

Digital Gain Selection Value	ADC Digital Gain Setting(Db)	Digital Gain Selection Value	ADC Digital Gain Setting(Db)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5

6	18	14	-6
7	21.5	15	-2.5

Table 7: ADC Audio Input Gain Selection

4.4.1.6 ADC Digital IIR Filter

The ADC contains 2 integrated anti-aliasing filters:
A long IIR filter suitable for music (> 44.1 kHz).G.722 filter. This is a digital IIR filter that improves the stop-band attenuation required for G.722 compliance. This filter is the best selection for 8 kHz/16 kHz/voice.

4.4.1.7 DAC

The DAC consists of two high-quality DACs:
Each DAC has a fourth-order Sigma-Delta converter.
Each DAC is a separate channel with identical functionality.
Each channel has an analog and a digital gain stage.

4.4.1.8 DAC Sample Rate Selection

DAC supports the following sample rates: 8kHz, 11.025kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz，48Khz.

4.4.1.9 DAC Gain

The DAC outputs have two gain stages, a digital stage followed by an analog stage. The digital gain varies between -24 dB and 21.5 dB and the analog gain between 0 dB and -21 dB, giving a total range of -45 dB to 21.5 dB.
Calls connected by the VM stream automatically select the distribution of gain within the DAC for best performance. Alternatively, the individual gain stages can be set.

Digital Gain Selection Value	DAC Digital Gain Setting (Db)	Digital Gain Selection Value	DAC Digital Gain Setting (Db)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5

6	18	14	-6
7	21.5	15	-2.5

Table 8: DAC Digital Gain Selection

Analog gain selection value	DAC analog gain setting (dB)	Analog gain selection value	DAC analog gain setting (dB)
7	0	3	-12
6	-3	2	-15
5	-6	1	-18
4	-9	0	-21

Table 9: DAC Analog Gain Selection

4.4.1.10 DAC Digital FIR Filter

The DAC contains an integrated digital FIR filter with the following modes:

- A default long FIR filter for best performance at ≥ 44.1 kHz.
- A short FIR to reduce latency.
- A narrow FIR (a sharp roll-off at Nyquist) for G.722 compliance. Best for 8 kHz/16 kHz.

4.4.1.11 Microphone Bias Generator

BTM702 contains an independent low-noise microphone bias generator. The microphone bias generator is recommended for biasing electret condensor microphones.

Figure 5 shows a typical biasing circuit for electret condenser microphones..

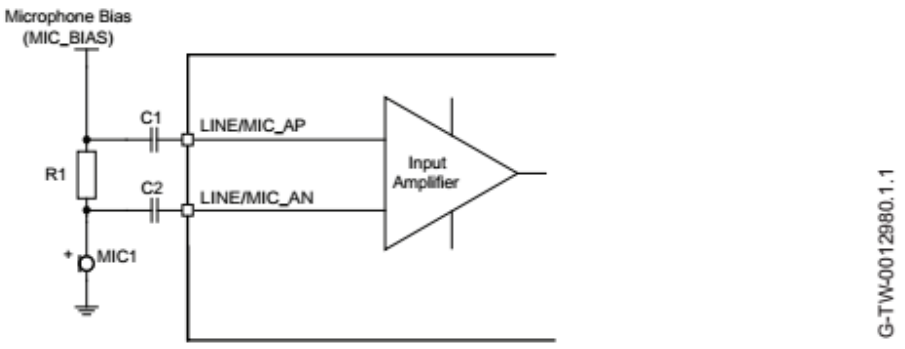


Figure 5: Micro phone Biasing

The microphone bias generator provides a selectable output voltage of 1.8 V or 2.6 V

nominal.

No output capacitor is required.

4.4.1.12 Output Stage

The output stage digital circuitry converts the signal from 16 bit per sample, linear PCM of variable sampling frequency to bit stream, which is fed into the analog output circuitry.

The analog output circuit comprises a DAC, a buffer with gain-setting, a low pass filter, and a class AB output stage amplifier.

Figure 6 shows that the output is available as a differential signal between SPKR_LN and SPKR_LP for the left channel, and between SPKR_RN and SPKR_RP for the right channel.

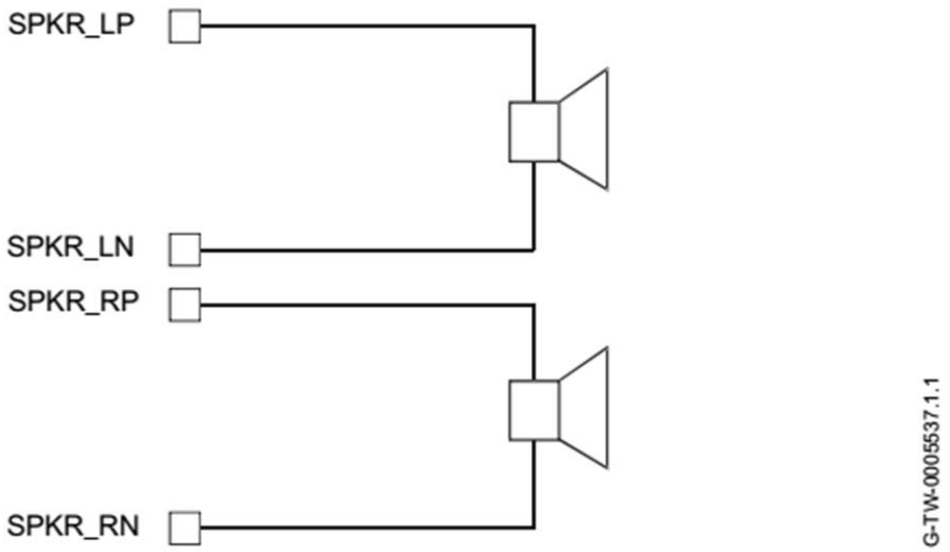


Figure 6: Speaker Output

4.4.1.13 Mono Operator

Mono operation is a single-channel operation of the stereo codec. The left channel represents the single mono channel for audio in and audio out. In mono operation, the right channel is the auxiliary mono channel for dual-mono channel operation.

In single channel mono operation, disable the other channel to reduce power consumption.

4.4.1.14 Sidetone

In some applications, it is necessary to implement sidetone. This sidetone function applies configurable gain to the microphone signal and feeds it into the DAC stream. The sidetone routing selects the version of the microphone signal from before or after the digital gain in the ADC interface and adds it to the output signal before or after the digital gain of the DAC interface

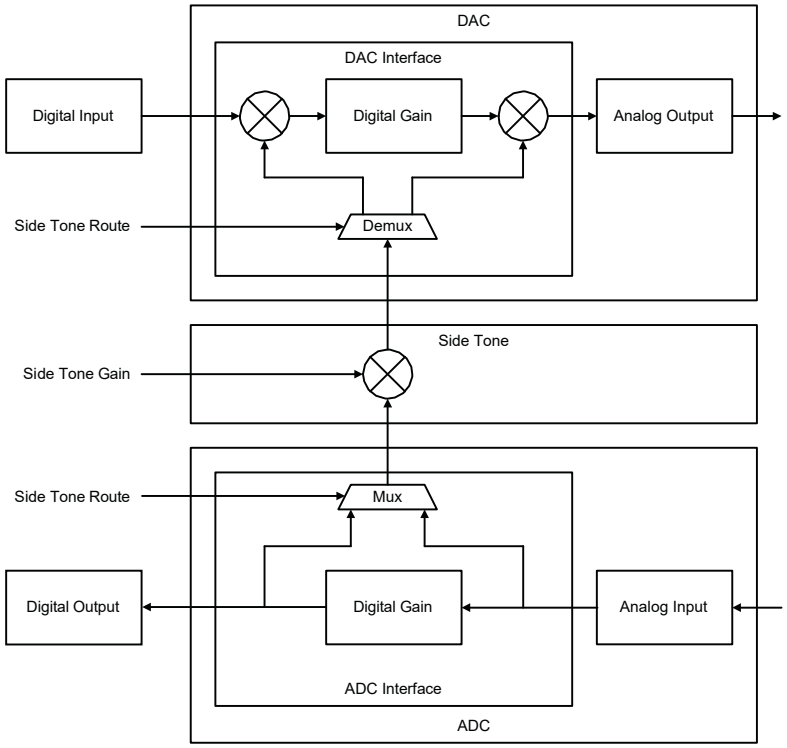


Figure 7: Sidetone

The ADC provides simple gain to the sidetone data. The gain values range from -32.6 dB to 12.0 dB in alternating steps of 2.5 dB and 3.5 dB

Value	Sidetone Gain	Value	Sidetone Gain
0	-32.6dB	8	-8.5dB
1	-30.1dB	9	-6.0dB
2	-26.6dB	10	-2.5dB
3	-24.1dB	11	0dB
4	-20.6dB	12	3.5dB
5	-18.1dB	13	6.0dB
6	-14.5dB	14	9.5dB
7	-12.0dB	15	12.0dB

Table 10: Sidetone Gain

4.4.1.15 Integrated Digital IIR Filter

BTM702 has a programmable digital filter integrated into the ADC channel of the codec.

The filter is a 2-stage, second-order IIR and is for functions such as custom wind noise reduction.

The filter also has optional DC blocking.

The filter has 10 configuration words in this order:

- 1 for gain value
- 8 for coefficient values (b_{01}, b_{02}, a_{01}, a_{02}, b_{11}, b_{12}, a_{11}, a_{12})
- 1 for enabling and disabling the DC blocking

The gain and coefficients are all 12-bit two's complement signed integer with the format NN.NNNNNNNNNN.

NOTE The position of the binary point is between bit[10] and bit[9], where bit[11] is the most significant bit.

4.4.2 I²S Interface

BTM702 supports I²S input and output via its industry-standard I²S digital audio interface. BTM702 also supports several alternative PCM data formats. When in PCM mode, the following pin name to function mappings apply.

I²S Pin	PCM Function
I2Sn_SD_IN	PCM_IN
I2Sn_SD_OUT	PCM_OUT
I2Sn_WS	PCM_SYNC
I2Sn_SCK	PCM_CLK

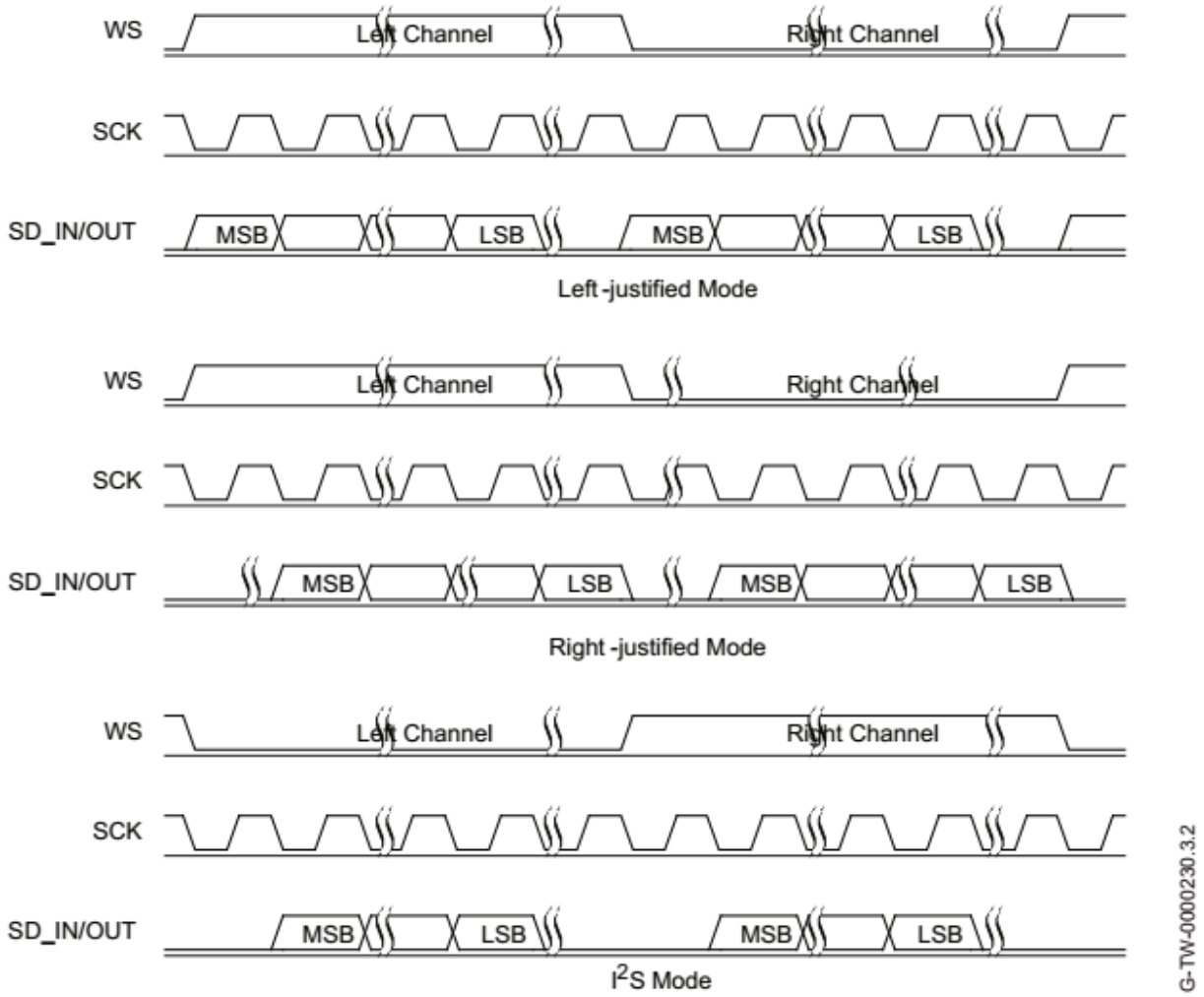


Figure 8: Digital Audio Interface Modes

The internal representation of audio samples within the BTM702 QFN is 16-bit and data on SD_OUT is limited to 16-bit per channel.

Symbol	Parameter	Min	Typ	Max	Unit
–	SCK Frequency	–	–	6.2	MHz
–	WS Frequency	–	–	96	kHz
T_{ch}	SCK high time	80	–	–	Ns
T_{cl}	SCK low time	80	–	–	Ns

Table 11: Digital Audio Interface Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{ssu}	WS valid to SCK high set-up time	20	–	–	Ns
t_{sh}	SCK high to WS invalid hold time	2.5	–	–	Ns
t_{opd}	SCK low to SD_OUT valid delay time	–	–	20	ns

t_{isu}	SD_IN valid to SCK high set-up time	20	–	–	ns
t_{ih}	SCK high to SD_IN invalid hold time	2.5	–	–	ns

Table 12: I²S Slave Mode Timing

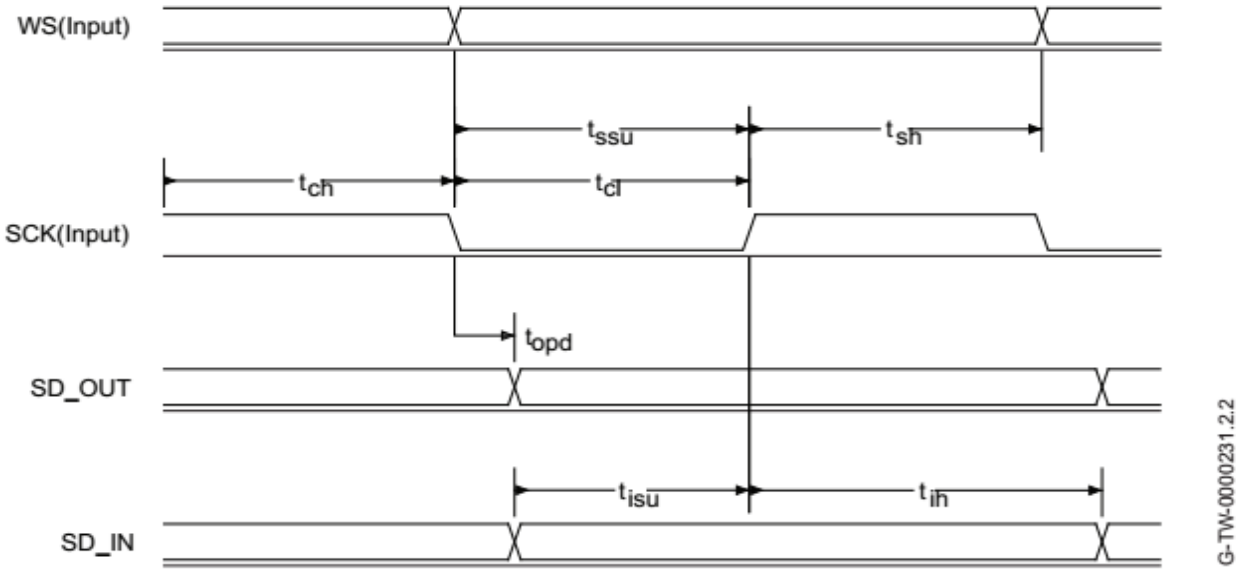


Figure 9: Digital Audio Interface Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
–	SCK Frequency	–	–	6.2	MHz
–	WS Frequency	–	–	96	kHz

Table 13: Digital Audio Interface Master Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{spd}	SCK low to WS valid delay time	–	–	39.27	ns
t_{opd}	SCK low to WS valid delay time	–	–	18.44	ns
t_{isu}	SD_IN valid to SCK high set-up time	18.44	–	–	ns
t_{ih}	SCK high to SD_IN invalid hold time	0	–	–	ns

Table 14: I²S Master Mode Timing Parameters, WS And SCK As Outputs

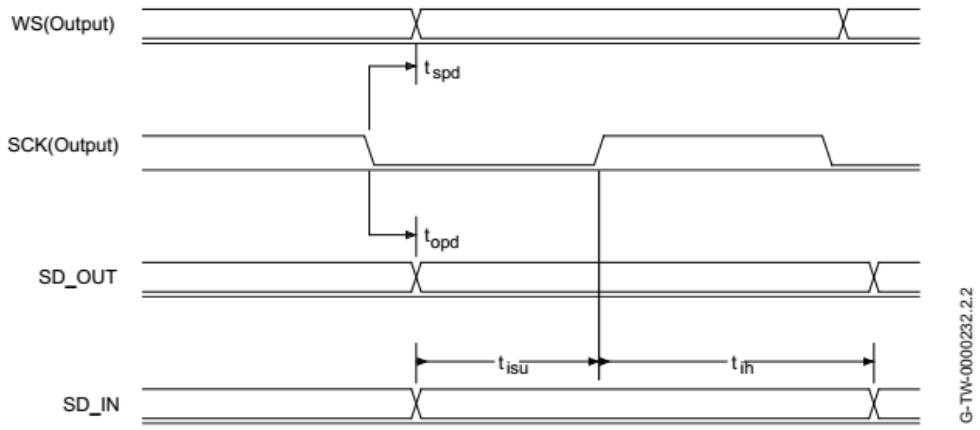


Figure 10: Digital Audio Interface Master Timing

4.4.3 aptx Codec

The aptX audio codec is available for high-quality stereo audio over Bluetooth. When incorporated in Bluetooth A2DP stereo products, aptX audio coding delivers full wired audio quality. The aptX audio codec source material is delivered transparently over the Bluetooth link, whether it is stored uncompressed or in an alternative compression (AAC, FLAC) format.

The aptX codec has the following target applications:

- Bluetooth stereo headphones/headsets
- Bluetooth automotive audio
- Bluetooth stereo speakers

The aptX codec has the following benefits:

- Outstanding Bluetooth Stereo audio quality
- Faithful reproduction of full audio bandwidth
- Minimization of lip-sync issues via low-delay audio decoding techniques
- Nondestructive transcoding from other standard coded audio formats
- Low code memory and data memory requirements
- A2DP-compliant negotiation back to the SBC codec when connecting with legacy audio sources

The aptX codec has the following key features:

- Multiple audio sample rate support, including Fs = 44.1 kHz and Fs = 48 kHz
- Conveyance of CD-quality audio (16-bit and Fs = 44.1 kHz) over Bluetooth at a data rate of 352 kbps
- Frequency response maintained from 10 Hz to 22 kHz for Fs = 48 kHz
- Algorithmic delay less than 1.89 ms for Fs = 48 kHz
- Dynamic range for 16-bit audio in excess of 92 dB

NOTE：FLC-BTM702IQ2C/D can support aptX only.

4.5 LED Drivers

BTM702 includes two 3-pad synchronised PWM LED drivers for driving RGB LEDs for producing a wide range of colours. All LEDs are controlled by firmware.

The terminals are open-drain outputs, so the LED must be connected from a positive supply rail to the pad in series with a current-limiting resistor.

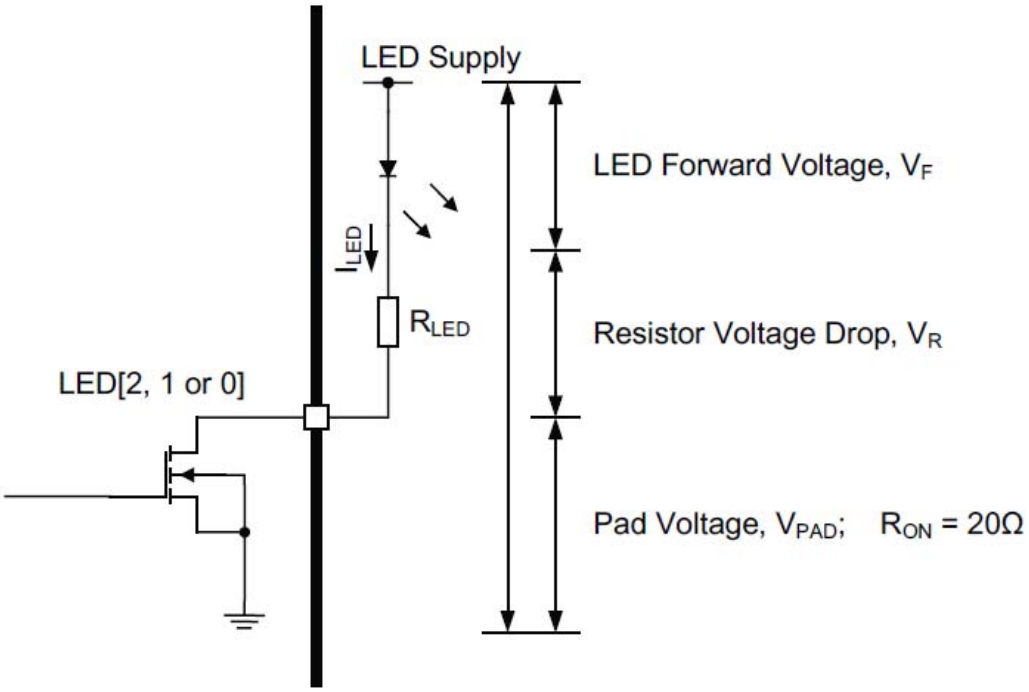


Figure 111: LED Equivalent Circuit

From Figure 3 it is possible to derive Equation 1 to calculate I_{LED}. If a known value of current is required through the LED to give a specific luminous intensity, then the value of R_{LED} is calculated.

$$I_{LED} = \frac{V_{SUPPLY} - V_F}{R_{LED} + R_{ON}}$$

Equation 1: LED Current

For the LED pads to act as resistance, the external series resistor, R_{LED}, needs to be such that the voltage drop across it, V_R, keeps V_{PAD} below 0.5V. Equation 2 also applies.

$$V_{SUPPLY} = V_F + V_R + V_{PAD}$$

Equation 2: LED PAD Voltage

Note:
The LED current adds to the overall current. Conservative LED selection extends battery life.

4.6 RF Interface

The module integrates a filter. The user can connect a 50ohms antenna directly to the RF port.

4.7 General Purpose Analogue IO

The general purpose analog IO can be configured as ADC inputs by software. Do not connect it if not use.

4.8 General Purpose Digital IO

There are eight general purpose digital IOs defined in the module. All these GPIOs can be configured by software to realize various functions, such as button controls, LED displays or interrupt signals to host controller, etc. Do not connect them if not use.

5. Electrical Characteristic

5.1 Absolute Maximum Rating

Rating	Min	Max	Unit
Storage Temperature	-40	+85	°C
PIO/AIO Voltage	-0.4	3.60	V
VDD	-0.4	3.60	V
USB_DP/USB_DN Voltage	-0.4	3.60	V
Other Terminal Voltages except RF	-0.4	3.60	V

Table 15: Absolute Maximum Rating

5.2 Recommended Operating Conditions

Operating Condition	Min	Typical	Max	Unit
Storage Temperature	-40	--	+85	°C
Operating Temperature Range	-40	--	+85	°C
VDD	+3.1	+3.3	+3.6	V
PIO	+1.7	+1.8	+3.6	V

Table 16: Recommended Operating Conditions

5.3 Input/output Terminal Characteristics

5.3.1 Digital Terminals

Supply Voltage Levels	Min	Typical	Max	Unit
Input Voltage Levels				
VIL input logic level low	-0.4	-	+0.4	V
VIH input logic level high	0.7VDDIO	-	VDDIO+0.4	V
Tr/Tf	-	-	25	ns
Output Voltage Levels				
VOL output logic level low, IOL = 4.0mA	-	-	0.4	V
VOH output logic level high, IOH = -4.0mA	VDDIO-0.2	-	-	V

Tr/Tf	-	-	5	ns
Input and Tri-state Current				
With strong pull-up	-150	-40	-10	μA
With strong pull-down	10	40	150	μA
With weak pull-up	-5	-1.0	-0.33	μA
With weak pull-down	0.33	+1.0	5.0	μA
I/O pad leakage current	-1	0	+1	μA
CI Input Capacitance	1.0	-	5.0	pF

Table 17: Digital Terminal

VDDIO is the supply domain for this i/o. Typical value is 1.8V.

5.3.2 USB

USB Terminals	Min	Typical	Max	Unit
Input Threshold				
VIL input logic level low	-	-	0.3VDD	V
VIH input logic level high	0.7VDD	-	-	V
Output Voltage Levels to Correctly Terminated USB Cable				
VOL output logic level low	0.0	-	0.2	V
VOH output logic level high	2.8	-	VDD	V

Table 18: USB Terminal

5.3.3 Stereo Codec: Analog-To-Digital Converter

Analog-To-Digital Converter						
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Resolution	–		–	–	16	Bits
Input sample rate, F_{sample}	–		8	–	48	kHz
Maximum ADC input signal amplitude	0dB =1600 mV_{pk-pk}		13	–	2260	mV_{pk-pk}
SNR	f_{in}=1 kHz B/W=20Hz→F_{sample}/2(20kHz max) A- Weighted THD+N<0.1% 1.6V_{pk-pk} input	**F_{sample}**				
		8 kHz	–	94.4	–	dB
		16 kHz	–	92.4	–	dB
		32 kHz	–	92.5	–	dB
		44.1 kHz	–	93.2	–	dB
		48 kHz	–	91.9	–	dB

THD+N	f_{in}= 1 kHz B/W=20Hz→Fsample/2 (20 kHz max) 1.6V_{pk-pk} input	**F_{sample}**				
		8 kHz	–	0.004	–	%
		48 kHz	–	0.016	–	%
Digital gain	Digital gain resolution = 1/32		-24	–	21.5	dB
Analog gain	Pre-amplifier setting =0 dB, 9dB, 21dB or 30 dB Analog setting =-3dB to12 dBin 3dB steps		-3	–	42	dB
Stereo separation (crosstalk)			–	-89.9	–	dB

5.3.4 Stereo Codec: Digital-To-Analog Converter

Digital-To-Analog Converter							
Parameter	**Conditions**			**Min**	**Typ**	**Max**	**Unit**
Resolution	–			–	–	16	Bits
Output sample rate, F_{sample}	–			8	–	48	kHz
SNR	f_{in}=1 kHz B/W= 20Hz →20 kHz A-Weighted THD+N<0.1% 0dBFSinput	**F_{sample}**	**Load**				
		48kHz	100k0	–	95.4	–	dB
		48kHz	320	–	96.5	–	dB
		48kHz	160	–	95.8	–	dB
THD+N	f_{in}=1 kHz B/W= 20Hz →20 kHz 0dBFSinput	**F_{sample}**	**Load**				
		8kHz	100k0	–	0.0021	–	%
		8kHz	320	–	0.0031	–	%
		8kHz	160	–	0.0034	–	%
		48kHz	100k0	–	0.0037	–	%
		48kHz	320	–	0.0029	–	%
		48kHz	160	–	0.0042	–	%
Digital gain	Digital gain resolution =1/32			-24	–	21.5	dB
Analog gain	Analog gain resolution =3 dB			-21	–	0	dB
Output voltage	Full-scale swing (differential)			–	–	778	mVrms
Stereo separation (crosstalk)				–	-90.5	–	dB

5.3.5 Microphone Bias Generator

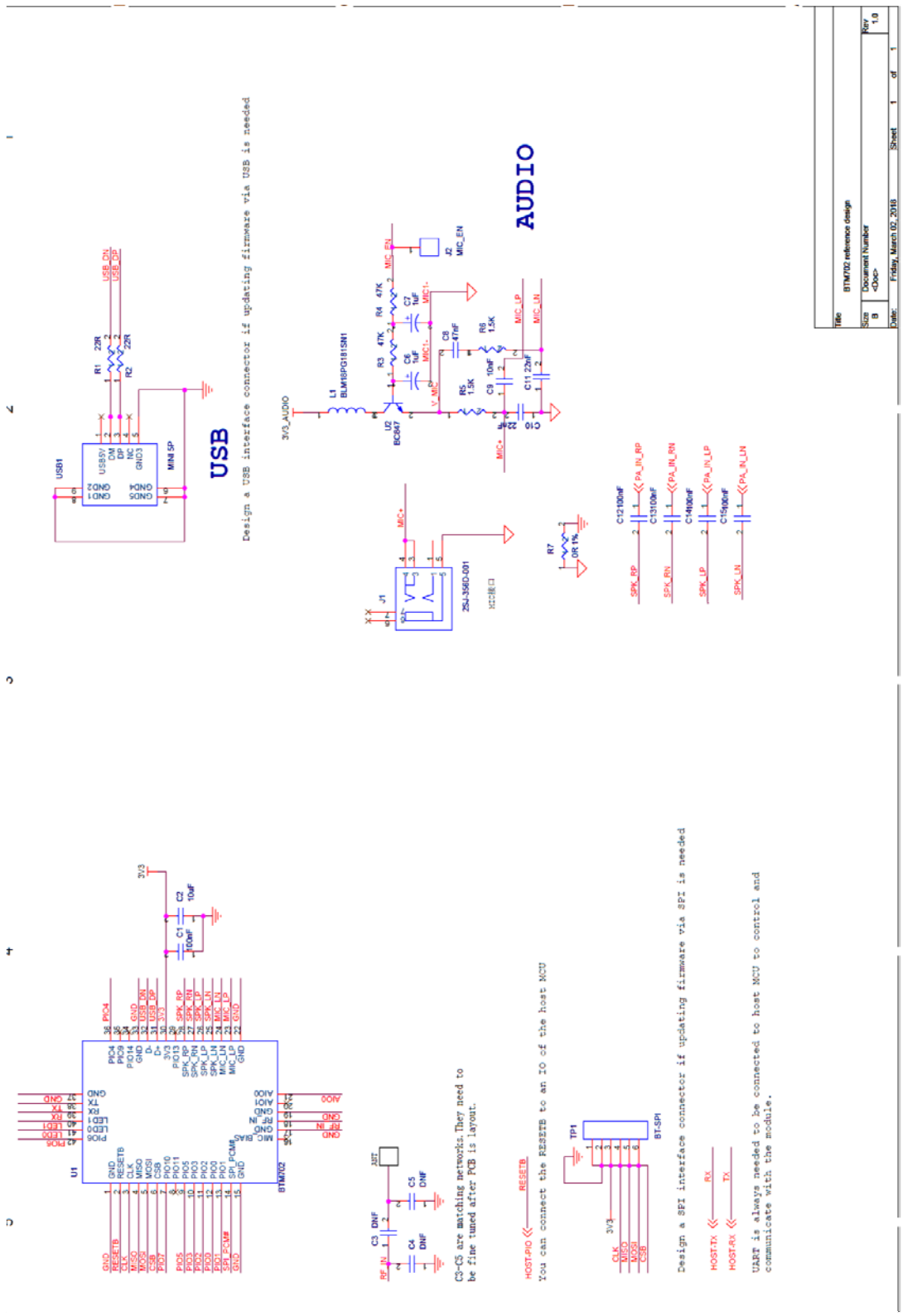
Microphone Bias Generator	Min	Typ	Max	Unit
Output voltage (1.8 V selected)	1.62	1.8	1.98	V
Output voltage (2.6 V selected)	2.34	2.6	2.86	V
Drop out from VBAT input	–	–	300	mV
Output current available	–	–	2.8	mA
Minimum load for stated performance	70	–	–	uA

5.3.6 Current[a]

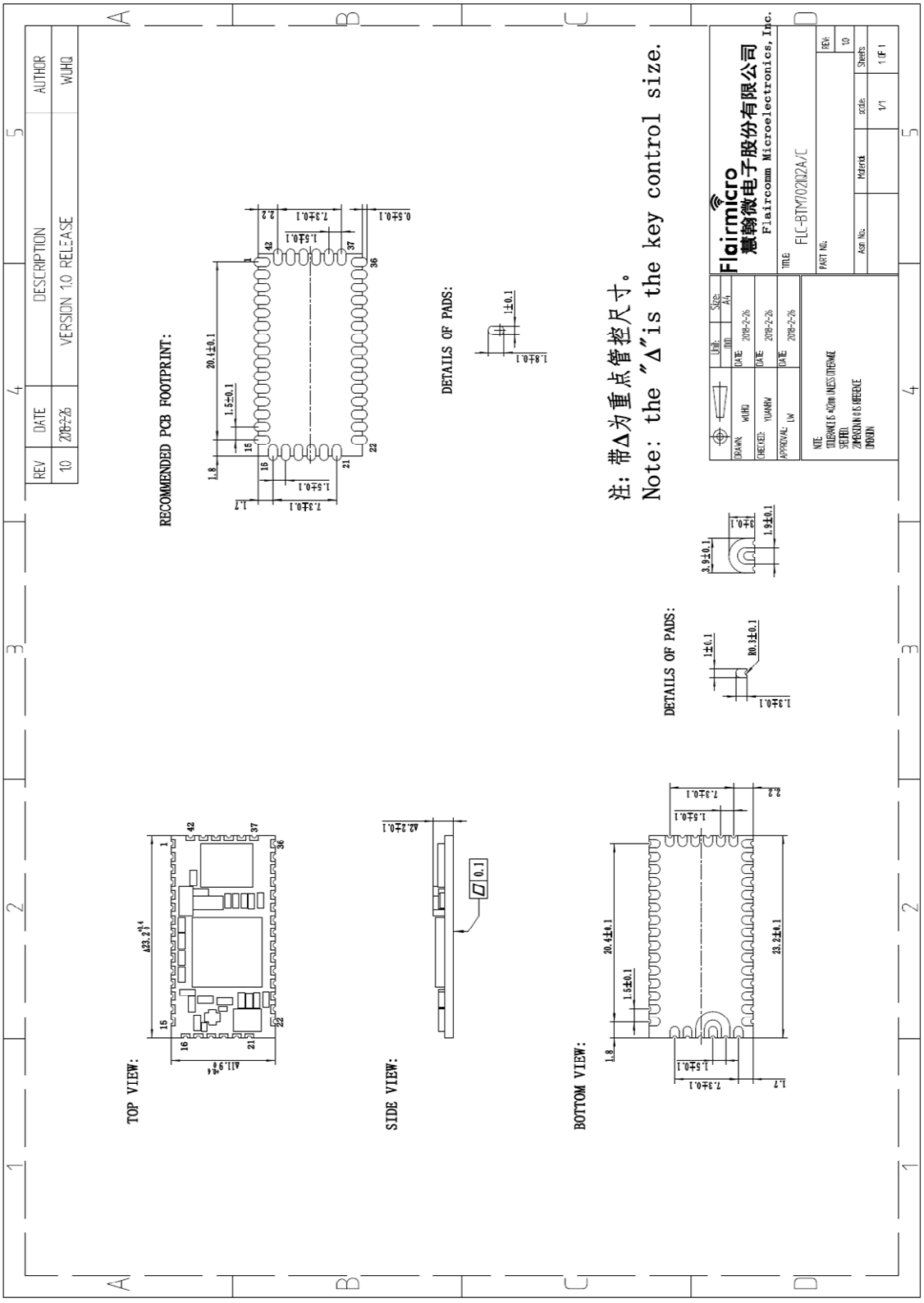
Mode	Current(Ma)		
	Min	Type	Max
Limbo(Sleep)		1	
Limbo(Idle)		4.8	
Connected		10.5	
Activecall		15.5	

a:The current is related to the firmware version.

6.Reference Design



7. Mechanical Characteristic


REV
DATE
DESCRIPTION
AUTHOR
1.0
2018-7-26
VERSION 1.0 RELEASE
WUHQ
RECOMMENDED PCB FOOTPRINT:
DETAILS OF PADS:
注：带Δ为重点管控尺寸。
Note: the "Δ"is the key control size.
DETAILS OF PADS:
TOP VIEW:
SIDE VIEW:
BOTTOM VIEW:
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wuhq
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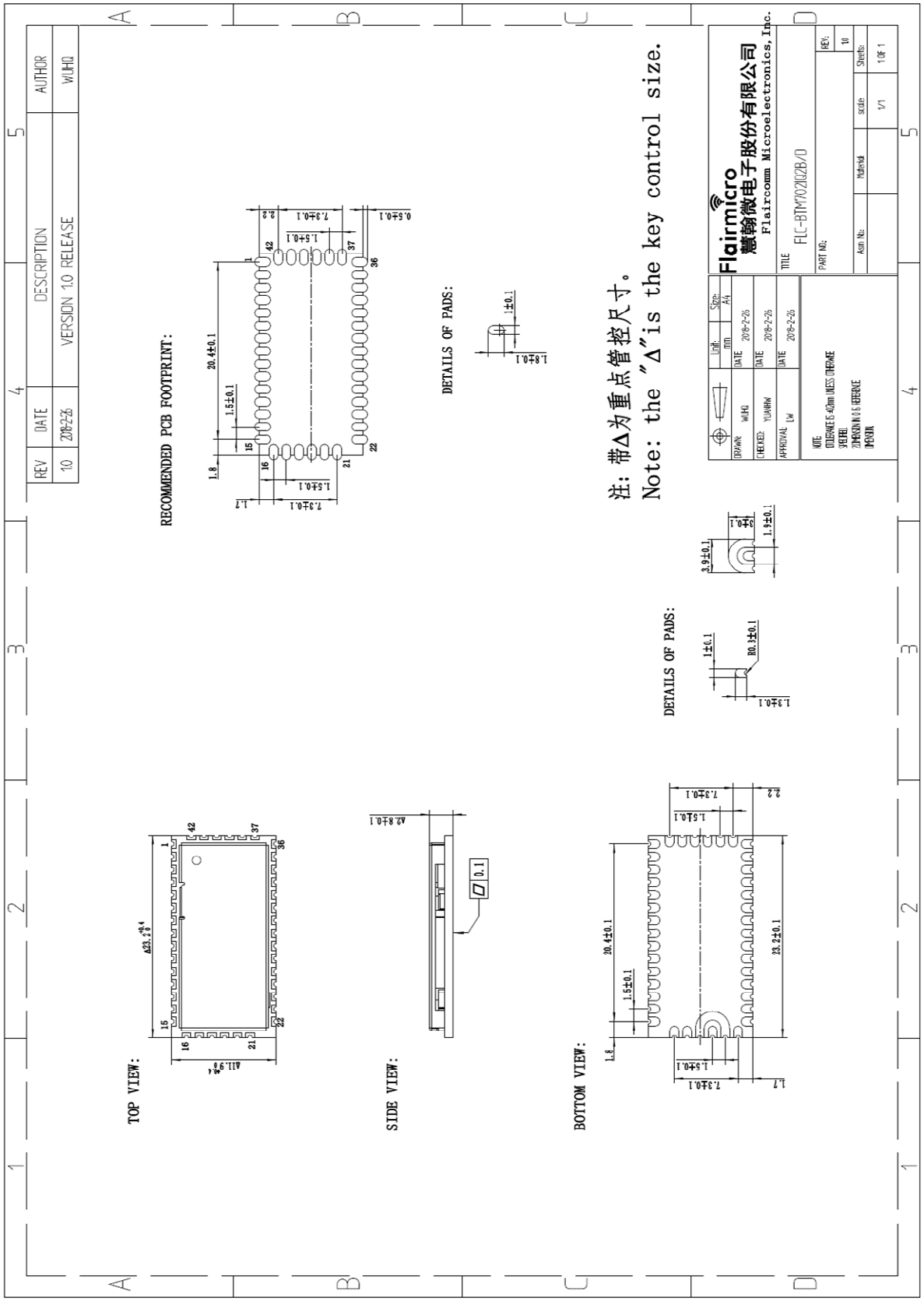
LW
2018-7-26
Unit: mm
Size: A4
Asm No.
Material
scale: 1/1
Sheets 1 OF 1
REV: 1.0


REV
DATE
DESCRIPTION
AUTHOR
1.0
2018-2-26
VERSION 1.0 RELEASE
WUHG
RECOMMENDED PCB FOOTPRINT:
DETAILS OF PADS:
注：带Δ为重点管控尺寸。
Note: the "Δ"is the key control size.
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DRAWN
CHECKED
APPROVAL
TOP VIEW:
SIDE VIEW:
BOTTOM VIEW:
DETAILS OF PADS:

8.Recommended PCB Layout and Mounting Pattern

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in figure 12 below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

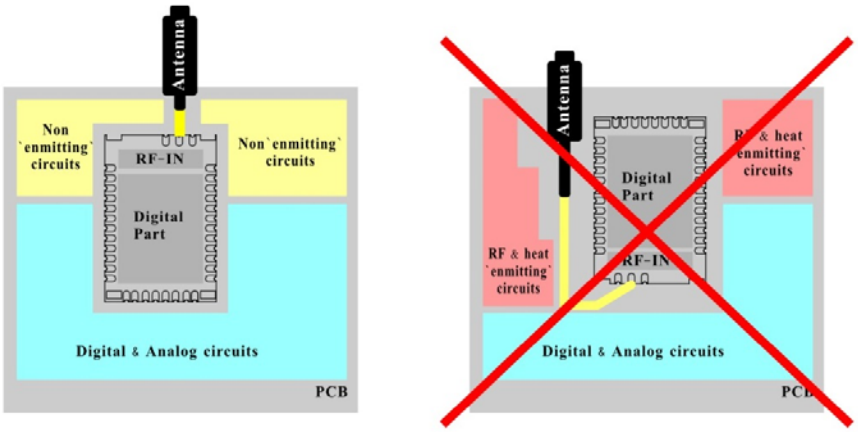

Figure 12: Placement the Module on a System Board

8.1 Input/output Terminal Characteristics

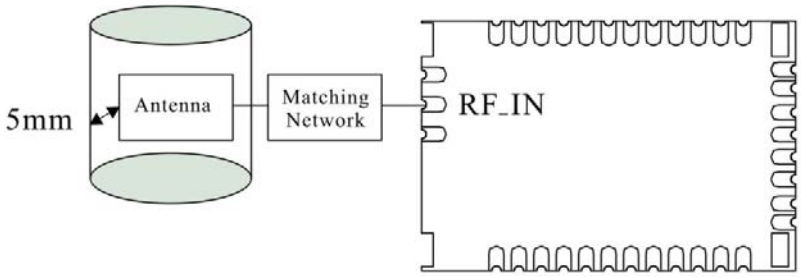

Figure 13: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.

- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

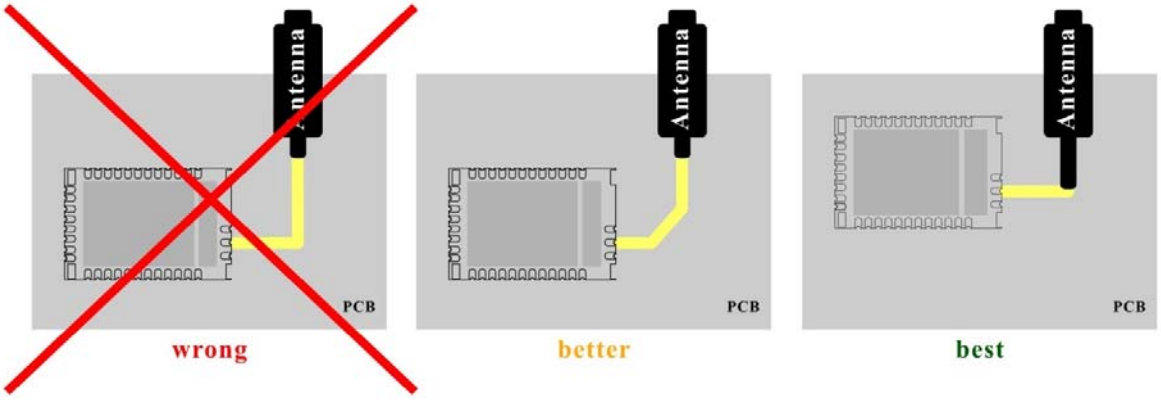

Figure 14: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

9.Recommended Reflow Profile

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

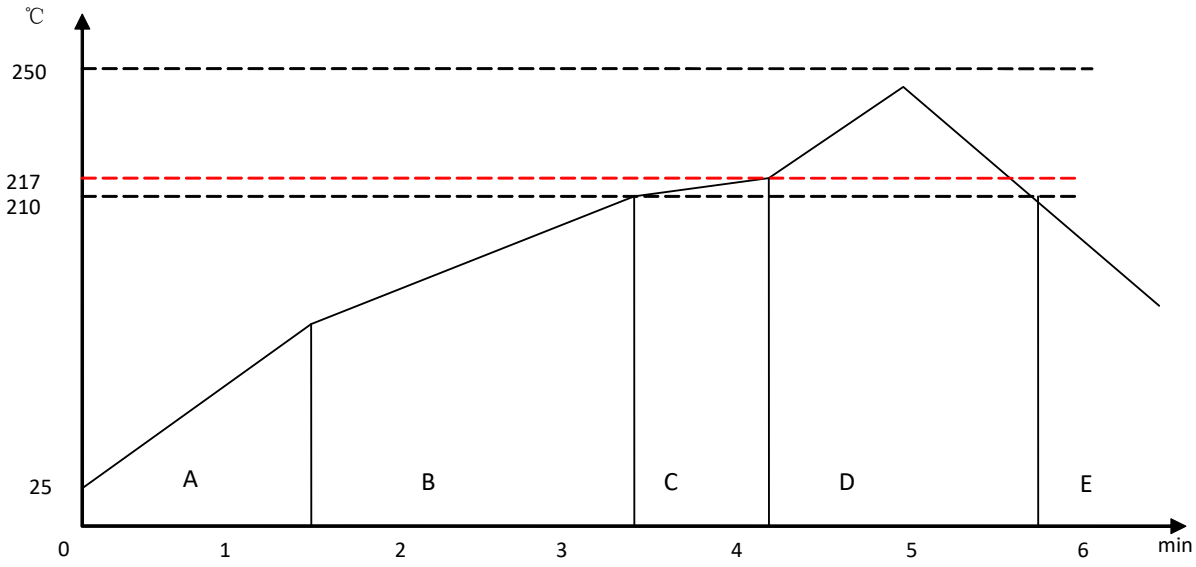

Figure 15: Recommended Reflow Profile

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone**.

Equilibrium Zone 2 (c) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longerlasting joint. **Typical cooling rate should be 4 °C**.

10.Ordering Information

10.1 Product Packaging Information

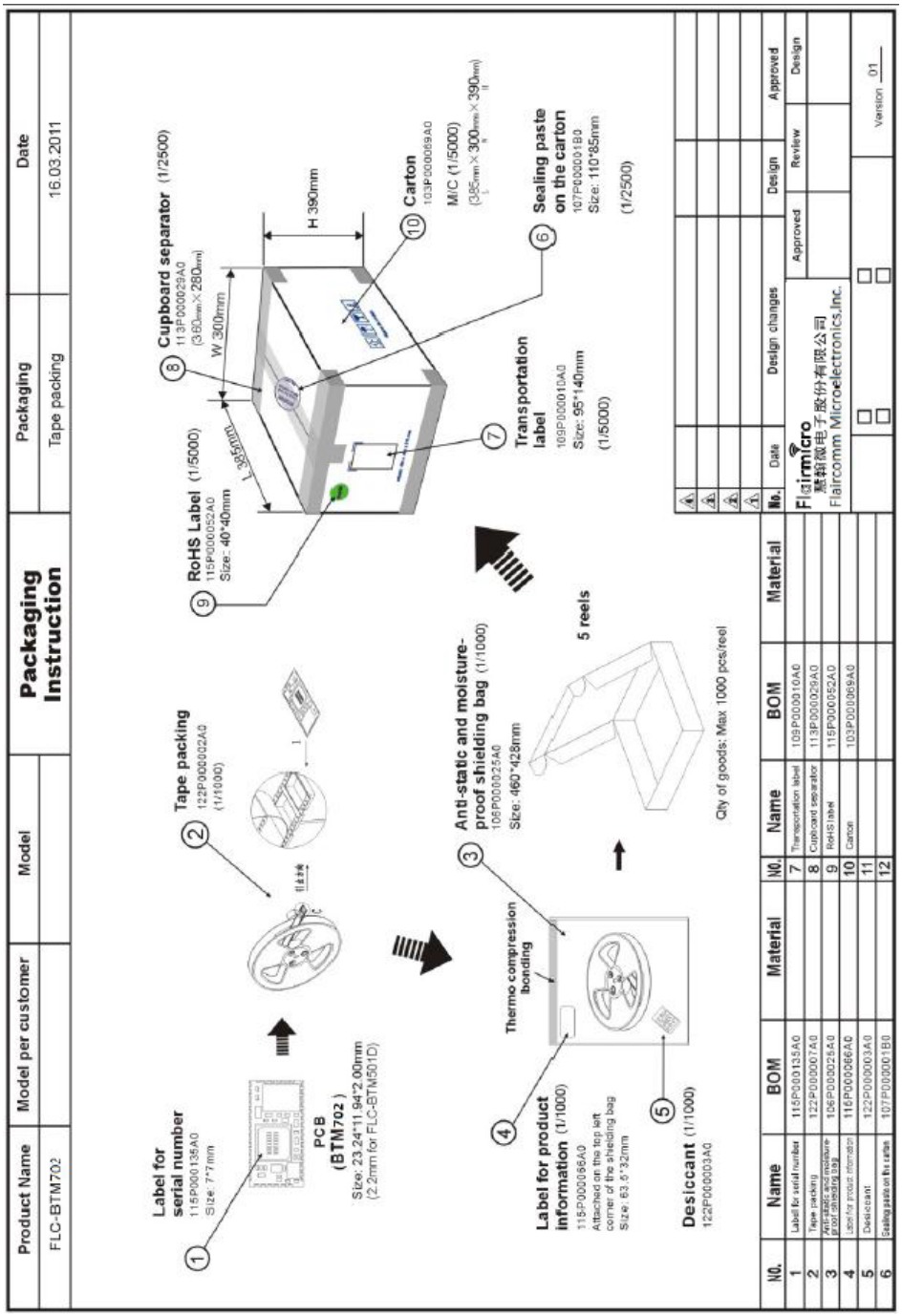

Figure 16: Product Packaging Information (Tape)

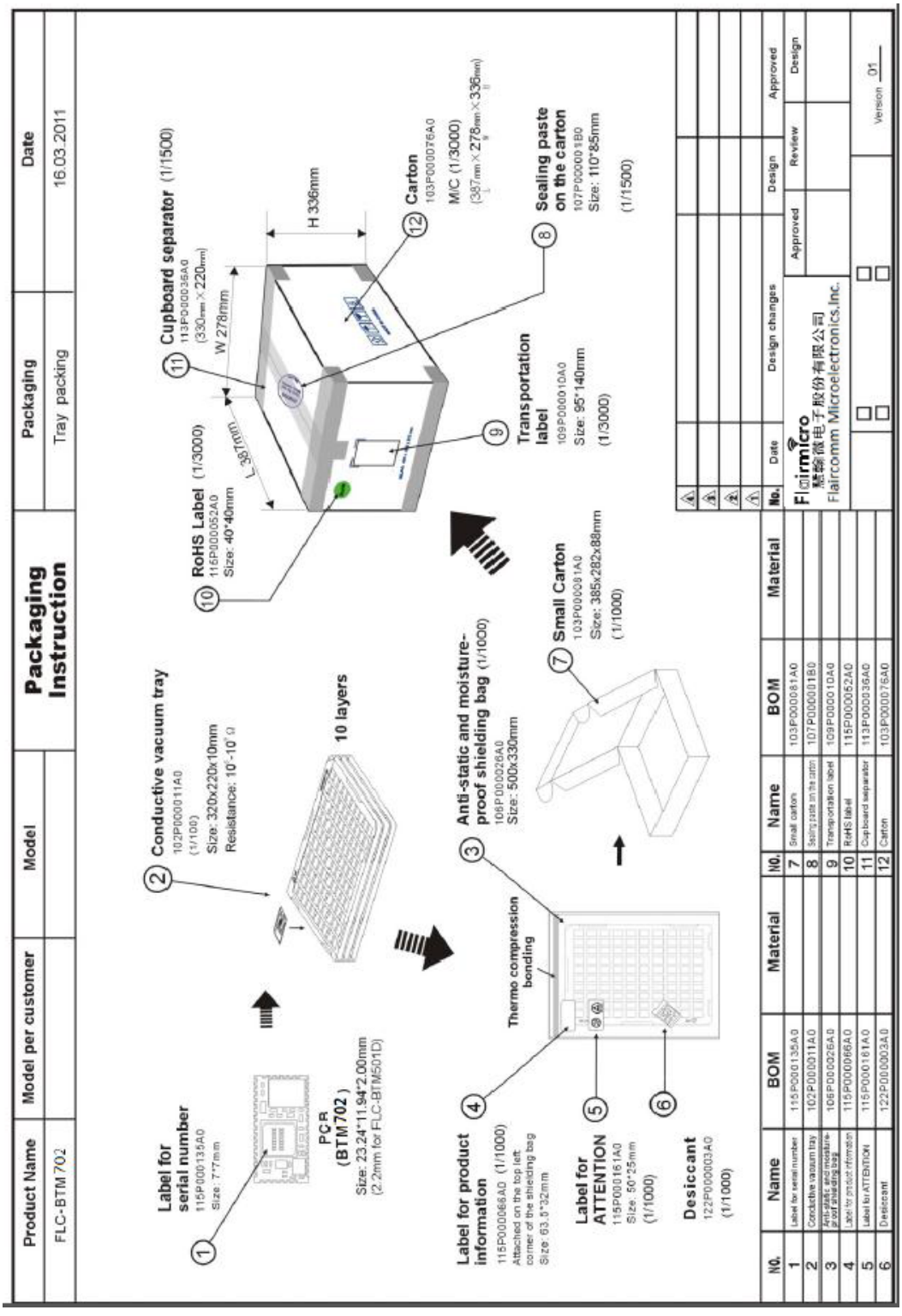

Figure 14: Product Packaging Information (Tray)

10.2 Ordering Information

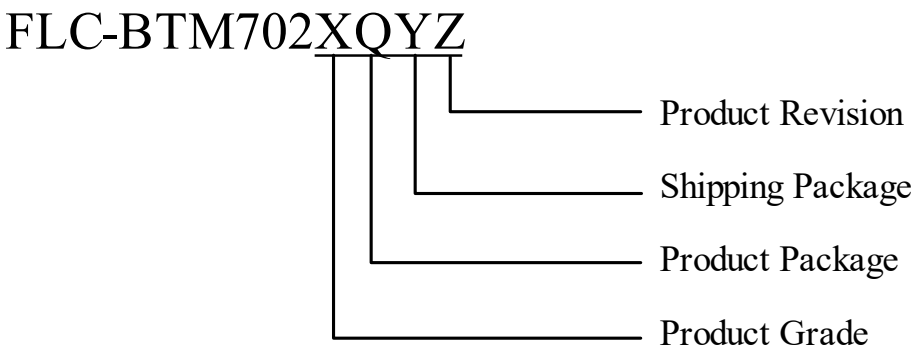

Figure 18: Ordering Information

10.2.1 Product Revision

Product Revision	Description	Availability
A	Without shielding case	Yes
B	With a shielding case	Yes
C	Support aptX, Without shielding case	Yes
D	Support aptX, With shielding case	Yes

Table 29: Product Revision

10.2.2 Shipping Package

Shipping Package	Description	Quantity	Availability
0	Form Tray	—	No
1	Plastic Tray	—	No
2	Tape	—	Yes

Table 20: Shipping Package

10.2.3 Product Package

Product Package	Description	Availability
Q	QFN	Yes
L	LGA	No
B	BGA	No
C	Connector	No

Table 21: Product Package

10.2.4 Product Grade

Product Grade	Description	Availability
C	Consumer	No
I	Industrial	Yes
V	Automobile After-Market	No
A	Automobile Before-Market	No

Table 22: Product Grade

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference.
(2) This device must accept any interference received, including interference that may cause undesired operation.

CAUTION: Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

RF Warning Statement

The device has been evaluated to meet general RF exposure requirement, The device can be used in portable exposure condition without restriction Federal Communication Commission (FCC) Radiation Exposure Statement Power is so low that no RF exposure calculation is needed.
This device is intended only for OEM integrators under the following conditions:
1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as two conditions above are met, further transmitter test will not be required.

However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed. To ensure compliance with all non-transmitter functions the host manufacturer is responsible for ensuring compliance with the module(s) installed and fully operational. For example, if a host was previously authorized as an unintentional radiator under the Declaration of Conformity procedure without a transmitter certified module and a module is added, the host manufacturer is responsible for ensuring that the after the module is installed and operational the host continues to be compliant with the Part 15B unintentional radiator requirements

The module is limited to OEM installation ONLY. The module is limited to installation in mobile or fixed application. We hereby acknowledge our responsibility to provide guidance to the host manufacturer in the event that they require assistance for ensuring compliance with the Part 15 Subpart B requirements.

IMPORTANT NOTE: In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for reevaluating the end product(including the transmitter) and obtaining a separate FCC authorization.

End Product Labeling

The final end product must be labeled in a visible area with the following: “Contains **FCC ID:P4I-BTM702D**”. The grantee's FCC ID can be used only when all FCC compliance requirements are met.

The following FCC part 15.19 statement has to also be available on the label:

This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions:
(1) this device may not cause harmful interference and
(2) this device must accept any interference received, including interference that may cause undesired operation.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module.

In the user manual of the end product, the end user has to be informed that the equipment complies with FCC radio-frequency exposure guidelines set forth for an uncontrolled environment.

The end user has to also be informed that any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

The end user manual shall include all required regulatory information/warning as show in this manual.

SIMPLIFIED EU DECLARATION OF CONFORMITY

The simplified EU declaration of conformity referred to in Article 10(9) shall be provided as follows: Hereby, Flaircomm Microelectronics,Inc. declares that the radio equipment type FLC-BTM702IQ2D is in compliance with Directive 2014/53/EU. The full text of the EU declaration of conformity is available at the following internet address: http://www.flairmicro.com/Certification