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Subject: Operational Description of Spotcell 141/142 and Spotcell 111/112(S),

The SpotCell 141/142 is a dual band adaptive repeater, which operates in the 800MHz Cellular band and in the 1900MHz PCS bands, for indoor signal enhancement. The indoor CU consists of two adaptive processors (AP) for each frequency band, an interface board, a fan and integrated antennas for each adaptive processor. The 800MHz Cellular adaptive processor is the same adaptive processor that is used in the SpotCell 100 CU and the 1900MHz PCS adaptive processor is the same adaptive processor that is used in the SpotCell 111/112 CU. The 1900MHz PCS processor is the Master processor while the subordinate processor could be either a Cellular processor, in the case of the SpotCell 141/142 or another PCS adaptive processor, as in the case of the SpotCell 111/112 (S).

When both adaptive processor are in the 1900MHz PCS band, the system is named Spotcell 111/112(S), indicating a split band. The interface board also contains two PSOCs which act a communications gateway to the two adaptive processors.

Each adaptive processor uses an IF frequency to perform gain control and filtering functions in both the downlink and uplink directions. The same LO signal is used to provide both down-conversion and up-conversion of the RF signal. In this configuration the output RF frequency is independent of the actual LO frequency, or any LO frequency error. The LO signal is generated by a frequency synthesizer that is phase locked to a TCXO reference source. However as noted above, because the same LO is used to convert to and from the IF frequency, this error is not transferred to the output frequency.

PCS Adaptive Processor (Master Adaptive Processor)- AP1

The PCS Adaptive processor or the Master AP,uses an IF frequency to perform gain control and filtering functions in both the downlink and uplink directions. The same LO signal is used to provide both down-conversion and up-conversion of the RF signal. In this configuration the output RF frequency is independent of the actual LO frequency, or any LO frequency error. The LO signal is generated by a frequency synthesizer that is phase locked to a TCXO reference source, which has a maximum frequency error of ± 2.5 ppm (see attached VC-TCXO-208C data sheet). However as noted above, because the same LO is used to convert to and from the IF frequency, this error is not transferred to the output frequency.

The only sources of spurious radiation within the PCS Adaptive processor are the Local Oscillators used in the uplink and downlink, and the clock frequency used by the on-board micro-controller. The LO frequencies have been

selected to prevent in-band spurious signals from being generated. Out of band spurious signals are filtered by SAW RF filters which are located between the uplink and downlink gain stages. The uplink and downlink oscillators and associated components are located in separate shielded compartments to control stray radiation. The microprocessor and associated digital circuits that use the 15MHz clock are housed in their own, separate shielded compartment to ensure that the clock and harmonics do not create spurious signals at the antennas. In addition, each RF stage in the uplink and downlink chain has its own decoupling components to prevent clock and LO signals from entering the signal path through the power supply. The PCB uses 3 separate ground planes to provide shielding and provide a low impedance ground for the RF stages and decoupling components.

The PCS Adaptive Processor uses an AGC circuit in both the uplink and downlink to control the RF power fed to the output stages. These stages are calibrated during manufacturing to ensure that output amplifiers are limited to operating at 10dB or more below the maximum output power of the device. This ensures linear operation, and prevents any distortion of the signal that may affect the occupied bandwidth of the signal (modulation). The AGC circuit uses logarithmic detectors to measure the AGC output power, together with an integrator and linear voltage controlled amplifier. This AGC configuration allows the system to operate linearly over a wide dynamic range. In addition, a supervisory system is used to monitor the input power level and to shut down the downlink or uplink if the input power exceeds the maximum specified.

Tune-Up Procedure and DC voltage of the last stage Amplifier.

The final amplifier stage in the uplink and downlink is a linear RF amplifier part number AH1(see attached PDF data sheet). This device is operated at a supply voltage of 5V, and current of 150mA.(V17 and V24 in the schematics indicate these voltage and current as supplied by the regulators). The input to the final stage amplifier is controlled by a software controlled variable gain amplifier (VGA) such that the DL output is only 0dBm per carrier at the RF port for a total composite power of 7dBm. The UL output is controlled in a similar way. The total composite power on the UL never exceeds +7.5dBm at the F connector of RF port following the diplexer.

Adaptive Processor 2 – Cellular Band

Adaptive Processor 2 (Cellular Band) uses an IF frequency to perform gain control and filtering functions in both the downlink and uplink directions. The same LO signal is used to provide both down-conversion and up-conversion of the RF signal. In this configuration the output RF frequency is independent of the actual LO frequency, or any LO frequency error. The LO signal is generated by a frequency synthesizer that is phase locked to a TCXO

reference source, which has a maximum frequency error of +/- 2.5 ppm (see attached vt204 data sheet). However as noted above, because the same LO is used to convert to and from the IF frequency, this error is not transferred to the output frequency.

The only sources of spurious radiation within Adaptive Processor 2 are the Local Oscillators used in the uplink and downlink, and the clock frequency used by the on-board micro-controller. The LO frequencies have been selected to prevent in-band spurious signals from being generated. Out of band spurious signals are filtered by SAW RF filters which are located between the uplink and downlink gain stages. The uplink and downlink oscillators and associated components are located in separate shielded compartments to control stray radiation. The microprocessor and associated digital circuits that use the 15MHz clock are housed in their own, separate shielded compartment to ensure that the clock and harmonics do not create spurious signals at the antennas. In addition, each RF stage in the uplink and downlink chain has its own decoupling components to prevent clock and LO signals from entering the signal path through the power supply. The AP2 PCB uses 3 separate ground planes to provide shielding and provide a low impedance ground for the RF stages and decoupling components.

Adaptive Processor 2 uses an AGC circuit in both the uplink and downlink to control the RF power fed to the output stages. These stages are calibrated during manufacture to ensure that output amplifiers are limited to operating at 10dB or more below the maximum output power of the device. This ensures linear operation, and prevents any distortion of the signal that may affect the occupied bandwidth of the signal (modulation). The AGC circuit use logarithmic detectors to measure the AGC output power, together with an integrator and linear voltage controlled amplifier. This AGC configuration allows the system to operate linearly over a wide dynamic range. In addition, a supervisory system is used to monitor the input power level and to shut down the downlink or uplink if the input power exceeds the maximum specified.

Tune-Up Procedure and DC voltage of the last stage Amplifier.

The final amplifier stage in the downlink is a linear RF amplifier part number Ah1(see attached PDF data sheet). This device is operated at a supply voltage of 5V, and current of 150 - 180mA. The input to the final stage amplifier is controlled by a software controlled variable gain amplifier (VGA) such that the DL output is only 0dBm per carrier at the RF port for a total composite power of 7dBm. The UL output is controlled in a similar way. The total composite power on the UL never exceeds -12dBm at the F connector of RF port following the diplexer.

Interface Board

The interface board assembly consists of two programmable PSOC chips which multiplex display data, control the fan, CU orientation during installation, status LED and DU signaling functions. The hardware also interfaces the two Adaptive repeaters to the DU, to the external AC adaptor and network management devices. The interface board also provides switches that can control the serial communication to either of the APs and the operational mode of each AP during installation. The interface board also provides an MCX RF connector for coverage extension antenna.

Integrated PCS and Cellular Antennas

The Spotcell 141/142 is provided with two integrated antennas, one for PCS AP and the second one for the Cellular AP. The RF signal on the downlink is radiated by the integrated antennas which are housed inside the plastic cover. Each antenna has a nominal gain of 0dBi and a maximum of 3dBi.

The Full Band PCS DU

The PCS DU is a 60MHz wide amplifier outdoor unit that receives the RF signal from the SpotCell 141/142 CU and transmits it to the Base Station and receives downlink RF signals from the base station to the CU for processing. The PCS DU is powered by a DC power that is transmitted with the same RF signal on the Coax cable from the CU. The PCS DU is also provided with a diplexer that separates the Cellular band RF signals from AP2 and transmits it the Cellular DU through a 1meter coax RF cable. The PCS DU is also provided with an integrated antenna with a peak gain of 11.5dBi. The PCS DU has a fixed gain on the downlink and on the uplink. It is also provided with an RSSI level indicator LED for installation. All the hardware is housed in a plastic housing for outdoor deployment. The PCS DU is also provided with a grounding stud for lightning protection.

The protection/regulatory circuitry is also capable of shutting down the final stage amplifier on the uplink when the system decides to do so due to high in-band signal, under/over input voltage, high downlink in-band signal, high out-band signals, minimum Downlink signal, an

isolation that can compromise the stability of the system and if the synthesizers get unlocked.

Tune-Up Procedure and DC voltage of the last stage Amplifier.

The final stage of the PCS DU on the downlink is a GaAs HBT linear amplifier, part N° **SXA-389**, from Sirenza Microdevices. (See attached datasheet for SXA-389). The device is operated at 5Vdc @120mA. The Uplink final stage of the PCS DU on the uplink is a GaAs HBT linear amplifier, part N° **SPA-2318**, from Sirenza Microdevices. (See attached datasheet for SPA-2318). The devices is operated at 5vdc @ 400mA.

There is no tune-up on the PCS DU. The PCS DU has a fixed gain of 23dB on the Downlink and an UL gain of 20dB. Please refer to the block diagram of the PCS Full band DU, Doc N° 761-00015-01.