Operational description

The final amplifier stage in the uplink is a linear RF amplifier part number AH1 (see attached PDF data sheet). This device is operated at a supply voltage of 5V, and current of 150 mA.The same holds true for the DL final stage RF amplifier.
The SpotCell 111/112 uses an IF frequency to perform gain control and filtering functions in both the downlink and uplink directions. The same LO signal is used to provide both down-conversion and up-conversion of the RF signal. In this configuration the output RF frequency is independent of the actual LO frequency, or any LO frequency error. The LO signal is generated by a frequency sythesizer that phase locked to a TCXO reference source, which has a maximum frequency error of +/- 2.5 ppm (see attached vt208C data sheet). However as noted above, because the same LO is used to convert to and from the IF frequency, this error is not transferred to the output frequency.

The only sources of spurious radiation within the SpotCell are the Local Oscialltors used in the uplink and downlink, and the clock frequency used by the on-board micro-controller. The LO frequencies have been selected to prevent in-band spurious signals from being generated. Out of band spurious signals are filtered by SAW RF filters which are located between the uplink and downlink gain stages. The uplink and downlink oscillators and associated components are located in separate shielded compartments to control stray radiation. The microprocessor and associated digital circuits that use the 20MHz clock are housed in their own, separate shielded compartment to ensure that the clock and harmonics do not create spurious signals at the antennas. In addition, each RF stage in the uplink and downlink chain has its own decoupling components to prevent clock and LO signals from entering the signal path through the power supply. The PCB uses 3 separate ground planes to provide shielding and provide a low impedance ground for the RF stages and decoupling components.

SpotCell 111/112 uses an AGC circuit in both the uplink and downlink to control the RF power fed to the output stages. These stages are calibrated during manufacture to ensure that output amplifiers are limited to operating at 10dB or more below the maximum output power of the device. This ensures linear operation, and prevents any distortion of the signal that may affect the occupied bandwidth of the signal (modulation). The AGC circuit use logarithmic detectors to measure the AGC output power, together with an integrator and linear voltage controlled amplifier. This AGC configuration allows the system to operate linearly over a wide dynamic range. In addition, a supervisory system is used to monitors the input power level and to shut down the downlink or uplink if the input power exceeds the maximum specified.