AME-4221SR(HU)

schematic modify history

DATE	Version	Change List	PCBA version	PCB version
2021/09/23	A00	First Draft	970DQB0AD00N128 A	490DQB00 A

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AME-4221SR(HU) 970DQB0AD00N128

01 History Rev A00

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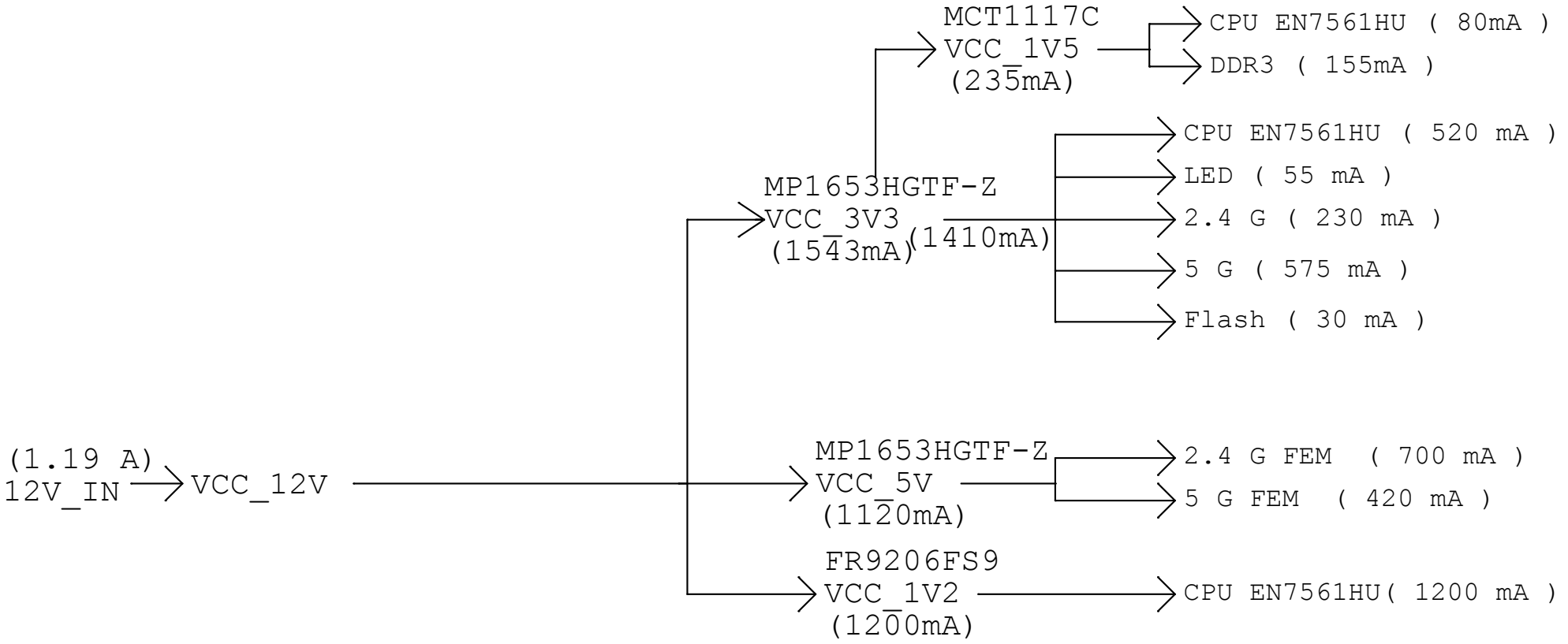

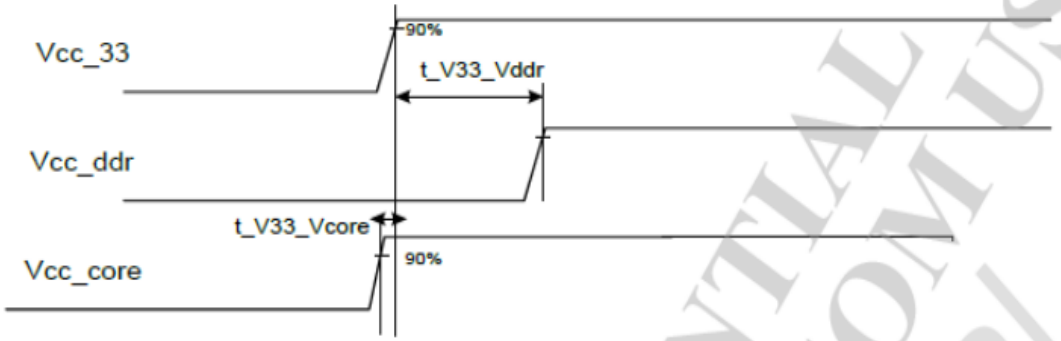

Figure 5-4 Power-on Sequence

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03_Power Tree

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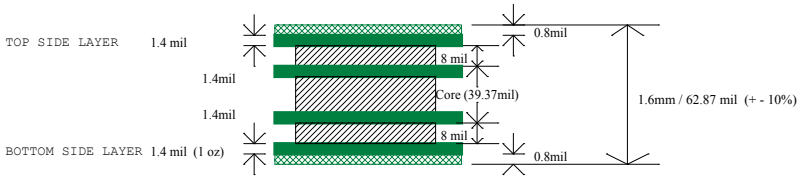
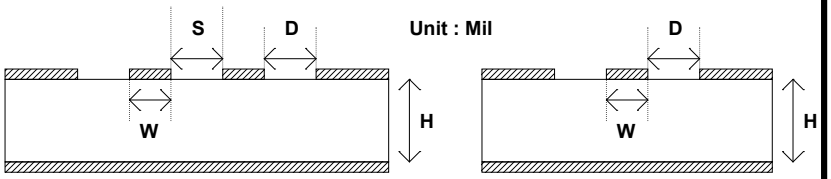
PCB Structure for 4 layers FR4 PCB



Layout trace guide



Differential Pair

Impedence	W	S	D	H	Line Mark
100 Ohm GPHY/PCIE	6mil	5.5mil	9.25mil		

Single End

50 Ohm RF	12mil		9mil		

GPHY - Layout Guidelines & Notes

1) Trace impedance: 100 Ohm differential impedance.
2) Match trace length of differential pairs, 20 mils max within a pair, and 500 mils max between pairs. Do NOT try to match trace lengths by adding extra length or serpentines. It is more important to maintain a pair as differential traces.
3) Max distance from SoC to Magnetics = 4.0 inches

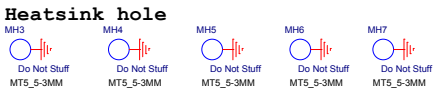
PCIe - Layout Guidelines & Notes

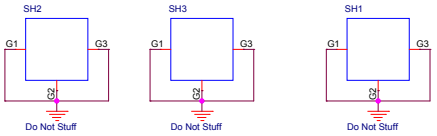
1) Trace impedance: 100 Ohm differential impedance.
2) No matching needed pair-to-pair.
3) Match trace length of differential pairs, 5 mils max within a pair. Symmetric routing for each pair (within a pair)
4) At least 2X pair to pair spacing than intra-pair spacing.

USB2.0 - Layout Guidelines & Notes

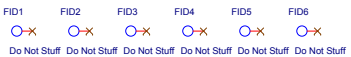
1. Route DM/DP pair with 90 ohms differential impedance.
2. The P and N traces are length matched, with max differential skew, within 20mils
4. Differential trace length must be less than 5 inches
5. No more than 2 vias per trace, prefer zero.

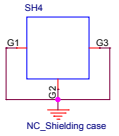
Heatsink hole





FID





2021/09/22:Add SH4 for CPU&DDR bot reserved

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04 Appendix

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EN7528 Hardware Trap

Pin Name	Description	Default
SPI_CLK,SPI_MISO,UART_TXD	SPINFC mode selection: 3'b000: SPI NAND dummy prepend controller ECC(SPI)(Boot from internal rom) 3'b001: SPI NAND dummy append controller ECC(SPI)(Boot from internal rom) 3'b100: SPI NAND dummy prepend Flash ECC(SPI)(Boot from Flash) 3'b101: SPI NAND dummy append Flash ECC(SPI)(Boot from Flash) 3'b010: SPI NOR 4B mode(SPI)(Boot from Flash) 3'b011: SPI NOR 3B mode(SPI)(Boot from Flash) 3'b110: NFD mode (boot from internal rom), FW defination trap bit 0 *3'b111: NFD mode (boot from internal rom), FW defination trap bit 1	1'b111
GPIO0	boot_from_flash : (boot_from_flash) *1'b0: disable (boot from internal ROM) *1'b1: enable (boot from SPI/SPINAND flash)	1'b1
TP,TN	Input clock mode selection: 2'b00: 25MHz-XTAL mode 2'b01: 40MHz-Single clock input mode(From XO) 2'b10: 25MHz-Differential clock input mode 2'b11: 40MHz-Differential clock input mode	
SPI_MOSI	CPU endian format *1'b0: little-endian , *1'b1: big-endian	1'b1

Jtag test pad reserved

I2C address
LED1 30H

EN7561HU

100 ohm

100 ohm

DDR3#1

Pin NO	Resistor	EN7561HU	EN7561DU
118	R297	V	NL
117	R299	V	NL
116	R298	NL	V
114	R300	V	NL
113	R301	NL	V
112	R556	NL	V
111	R302	V	NL
110	R1028	V	NL
109	R1029	V	NL
	R303	NL	V
108	R1008	V	NL
107	R1009	V	NL

DDR decoupling

DDR decoupling

EN7561HU:DDR part component mount
EN7561DU:DDR part component NL

2021/09/23:Reserve R1091~R1096 on bot

2021/09/24:Reserve R1097~R1099 on top

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05_CPU_EN7561HU

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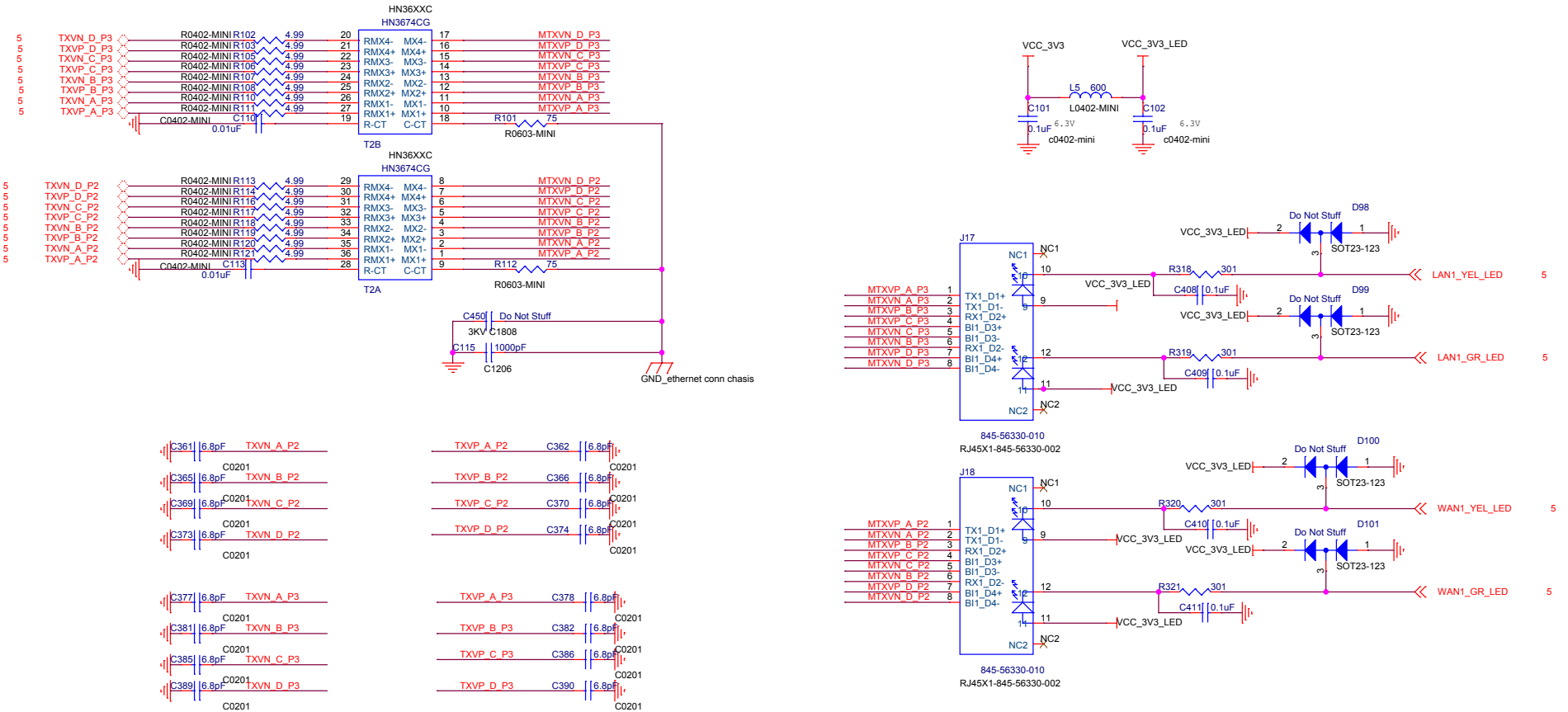

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970DQB0AD00N128

06 GE Port

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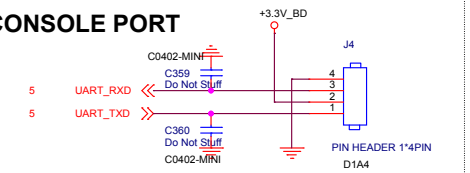
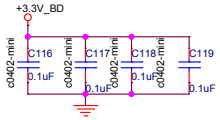
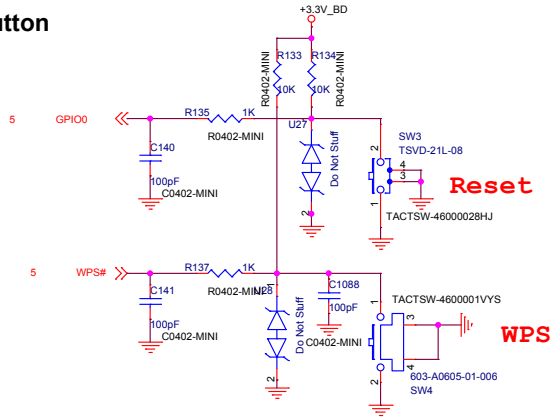
CONSOLE PORT





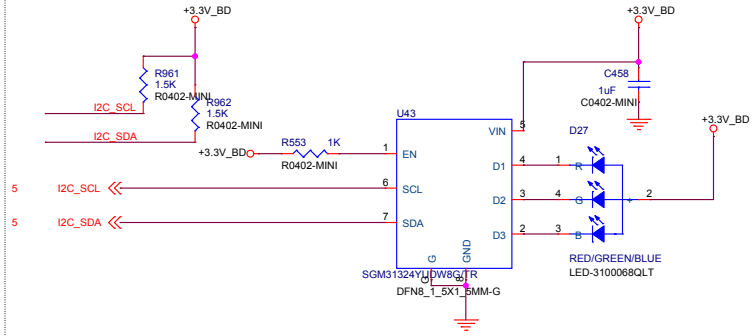
Button



2021/09/06:Change WPS button to 4600001VYS 3.3mm for layout
2021/09/15:Swap WPS pin1/2 for layout
2021/09/17:Add C1088 close SW4

LED1

ADDRESS 30H



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07_LED, Console, USB, Button

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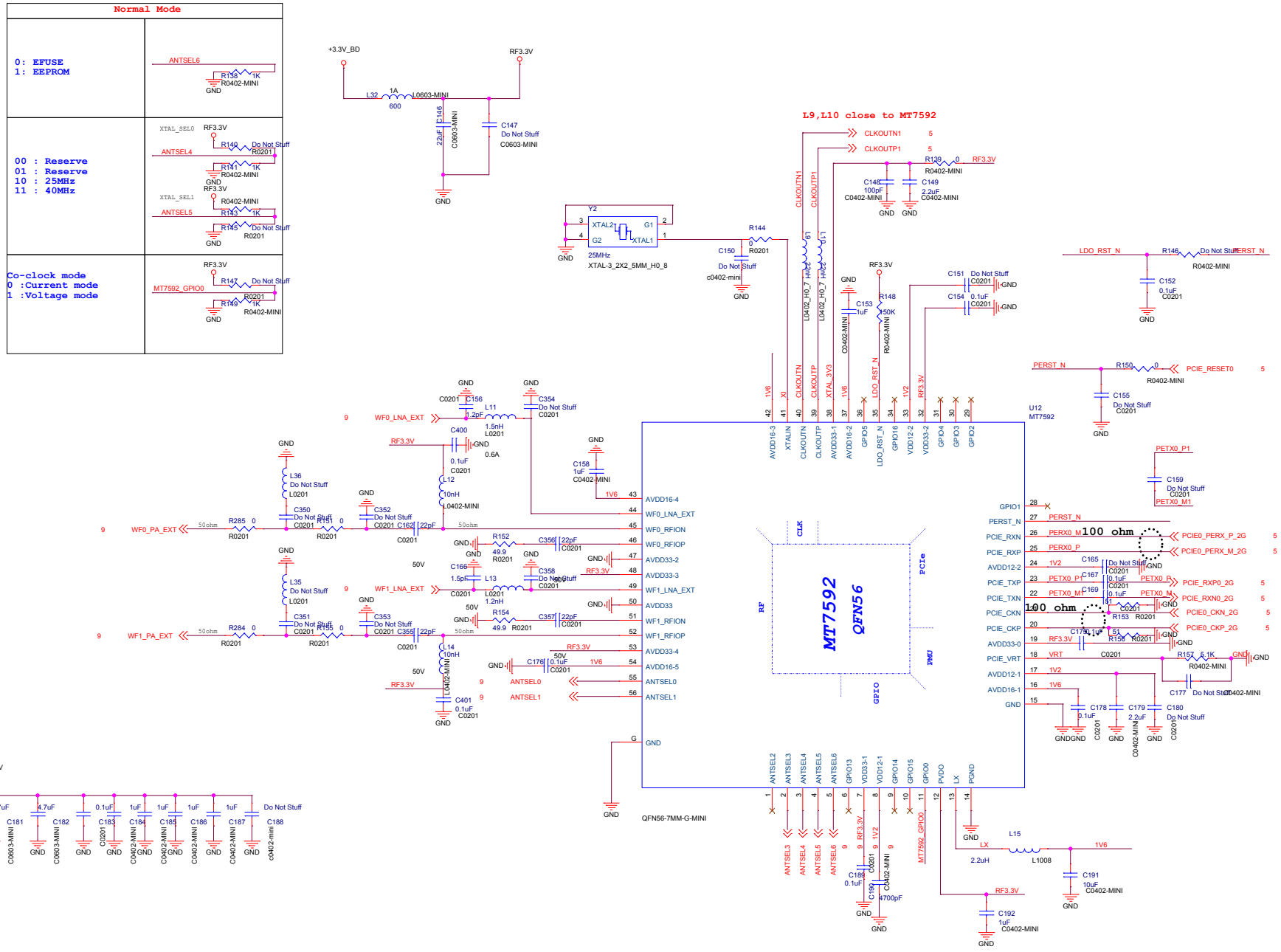

Note: Component with [...] is not installed

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08 2.4G_MT7592 Rev A00

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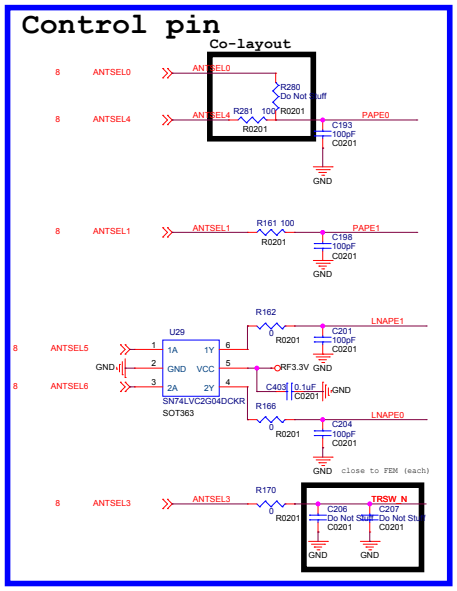
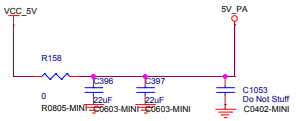
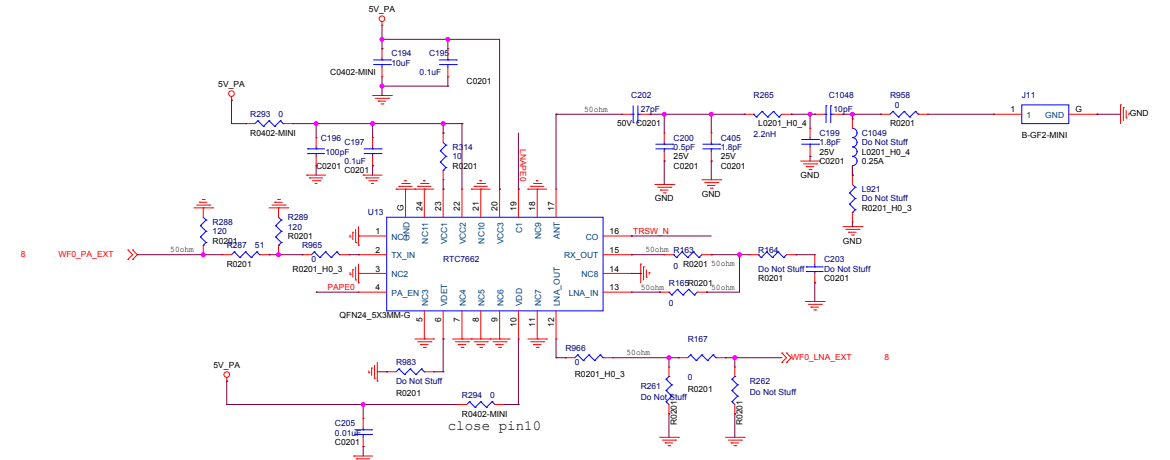
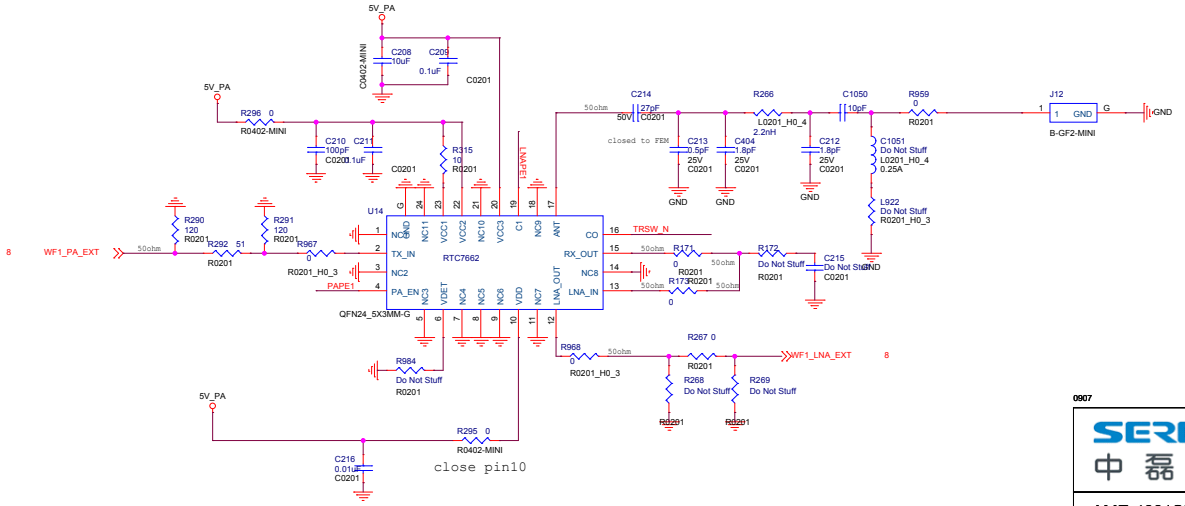




WF0





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AME-4221SR(HU)	970DQB0AD00N128
09_2.4 G FEM_RTC7662	Rev A00
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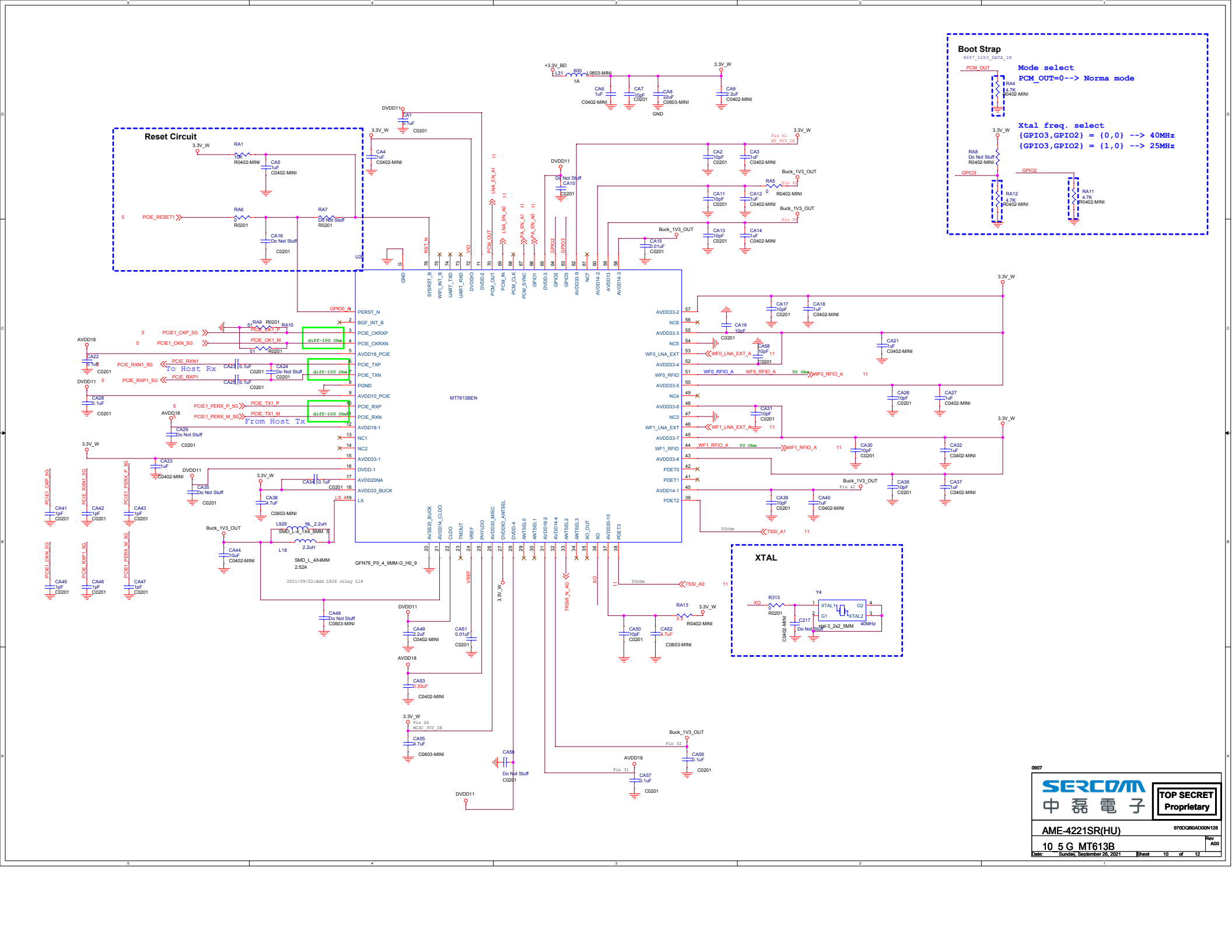
Boot Strap
Mode select
PCM_OUT=0--> Norma mode
Xtal freq. select
{GPIO3,GPIO2} = {0,0} --> 40MHz
{GPIO3,GPIO2} = {1,0} --> 25MHz
Reset Circuit
MT7613BEN
XTAL
To Host Rx
From Host Tx
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10_5 G_MT613B
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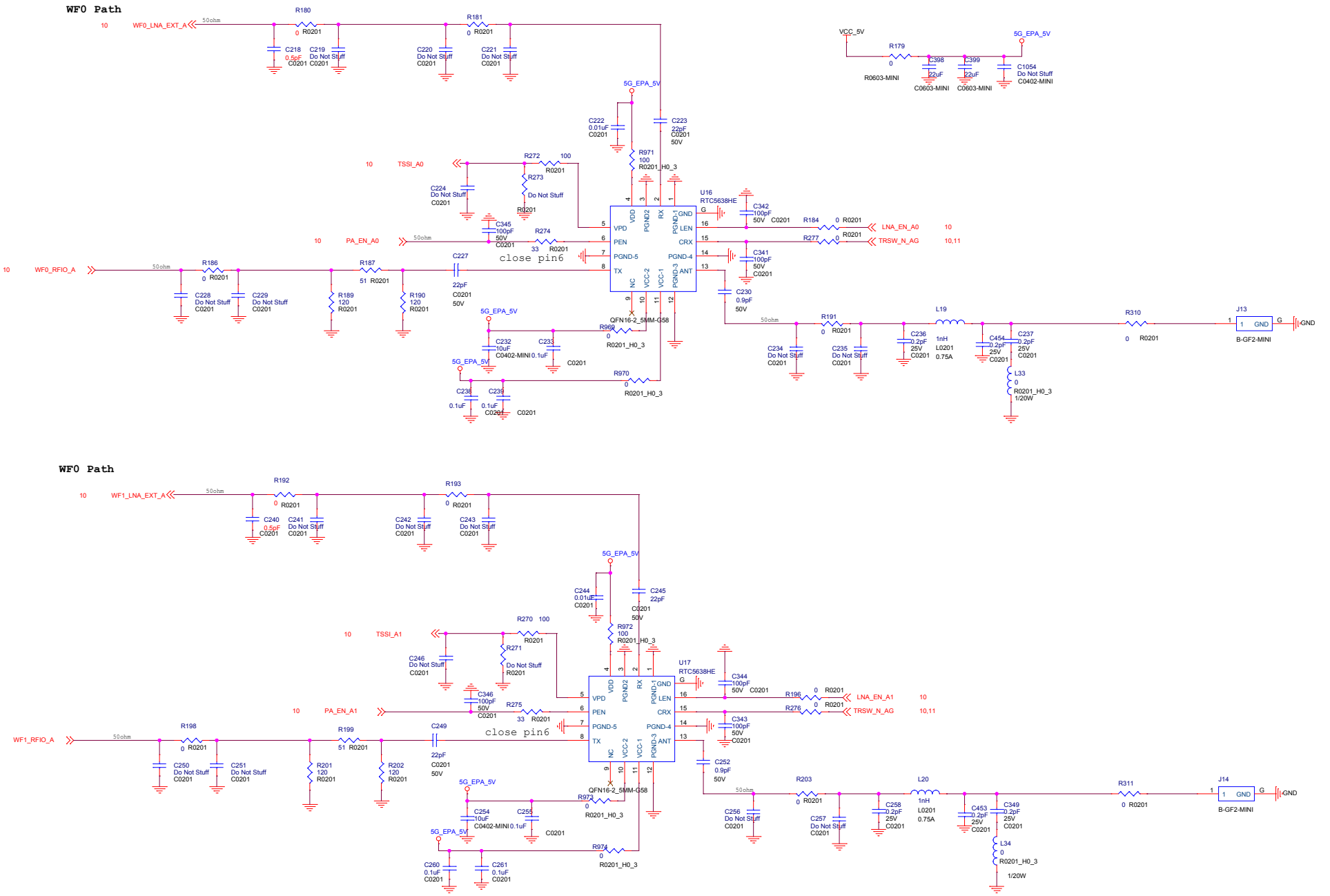

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11 5G FEM RTC5638HE

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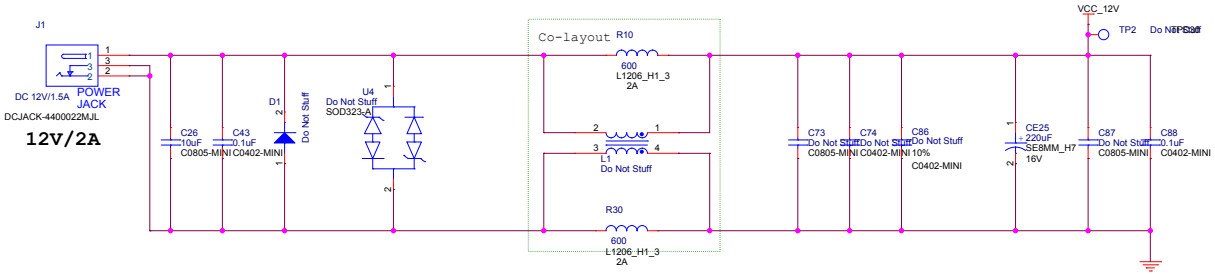
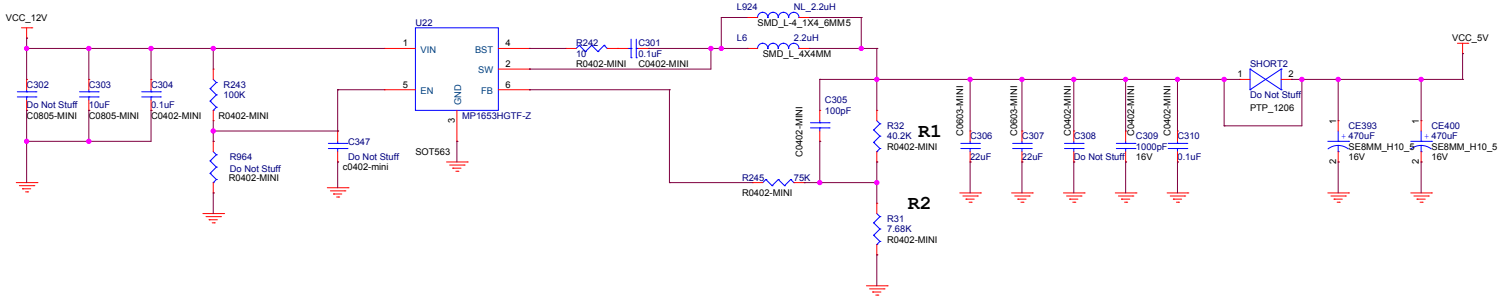
System DC Power



5V/3A FEM

Vout=0.805*(1+R1/R2)=0.805*(1+40.2/7.68)=5.02
L=2.2uH

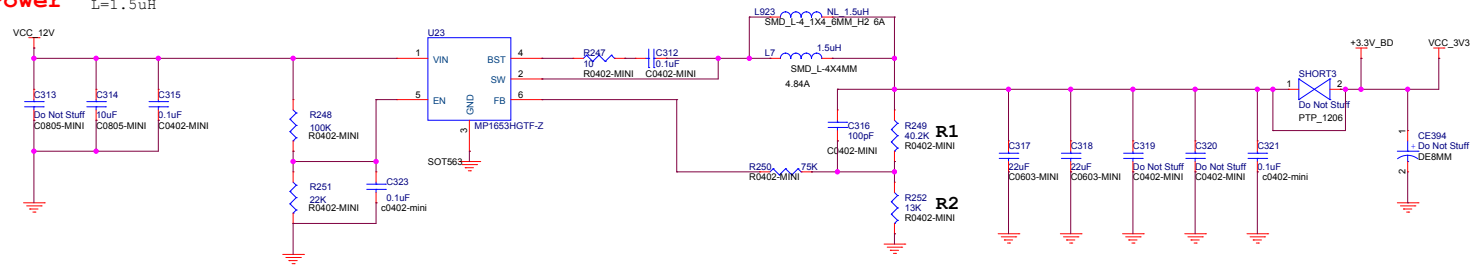
2021/09/18:Add L924 colay L6



3V3/3A Power

Vout=0.805*(1+R1/R2)=0.805*(1+40.2/13)=3.294
L=1.5uH

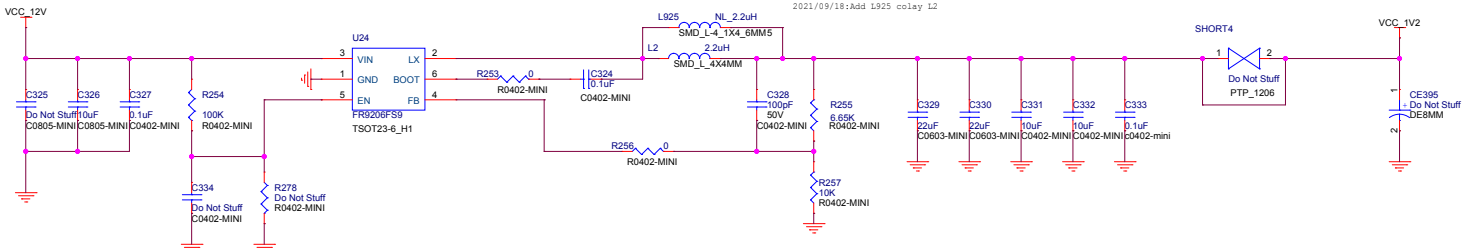
2021/09/18:Add L923 colay L7



CPU Power 1.2V/2A

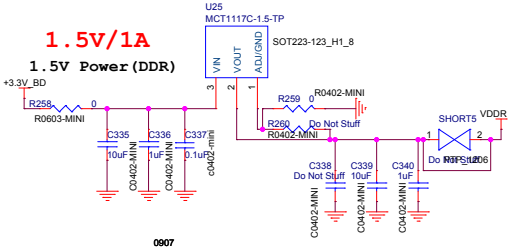
Vout=0.768*(1+R1/R2)=0.768*(1+6.65/10)=1.279
L=2.2uH

2021/09/18:Add L925 colay L2



1.5V/1A

1.5V Power(DDR)



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12 Power Circuit

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