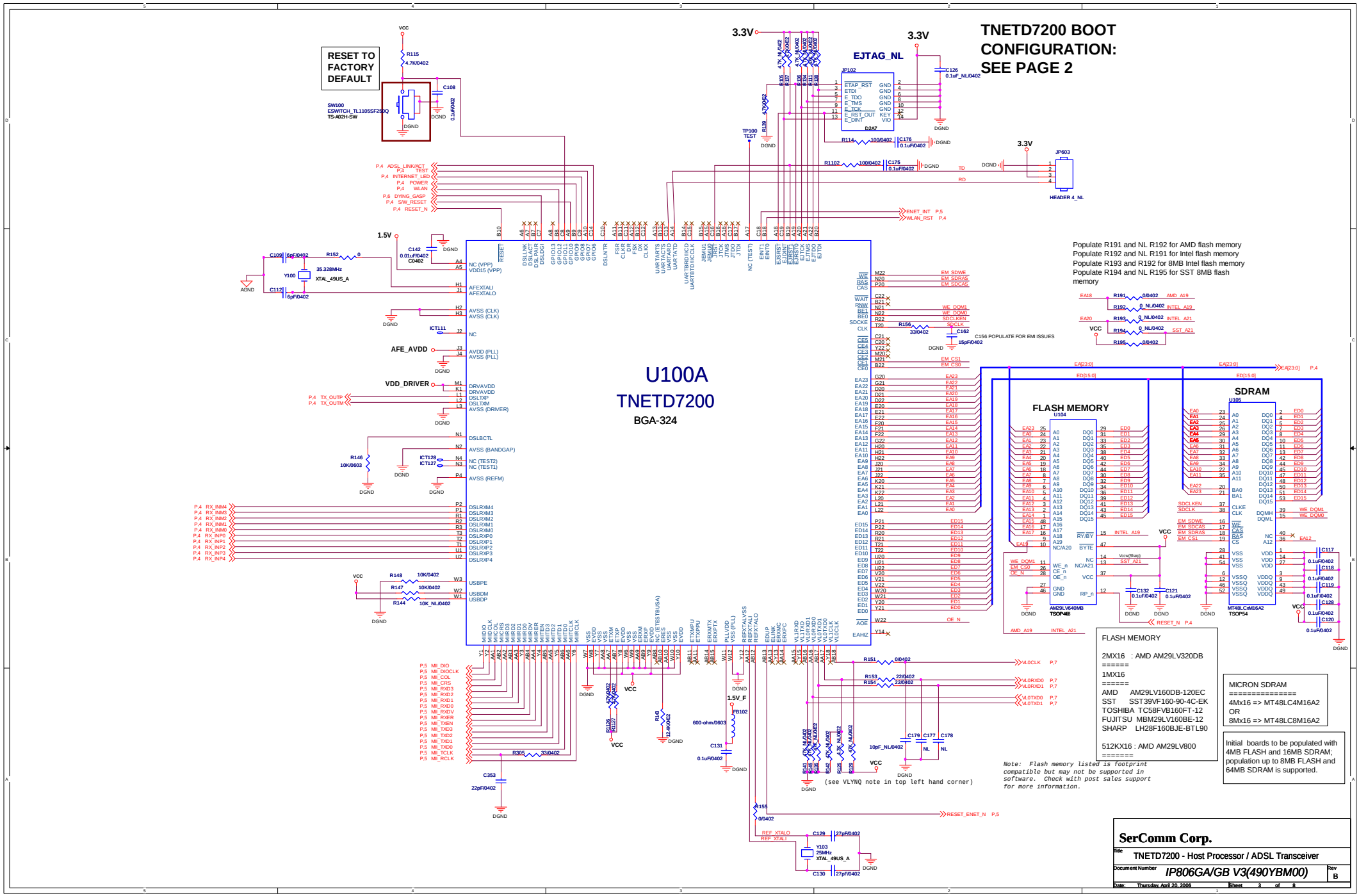
TNETD7200 BOOT CONFIGURATION: SEE PAGE 2
RESET TO FACTORY DEFAULT
SW100 ESWITCH_TL1105SF250Q TS-A02H-SW
EJTAG_NL
JP102
JP603
HEADER 4_NL
U100A
TNETD7200
BGA-324
Populate R191 and NL R192 for AMD flash memory
Populate R192 and NL R191 for Intel flash memory
Populate R193 and R192 for 8MB Intel flash memory
Populate R194 and NL R195 for SST 8MB flash memory
FLASH MEMORY
U104
AM29LV640MB
TSOP48
SDRAM
U105
MT48LC4M16A2
TSOP54
C156 POPULATE FOR EMI ISSUES
FLASH MEMORY
2MX16 : AMD AM29LV320DB
======
1MX16
======
AMD AM29LV160DB-120EC
SST SST39VF160-90-4C-EK
TOSHIBA TC58FVB160FT-12
FUJITSU MBM29LV160BE-12
SHARP LH28F160BJE-BTL90
512KX16 : AMD AM29LV800
========
Note: Flash memory listed is footprint compatible but may not be supported in software. Check with post sales support for more information.
MICRON SDRAM
==========
4Mx16 => MT48LC4M16A2
OR
8Mx16 => MT48LC8M16A2
Initial boards to be populated with 4MB FLASH and 16MB SDRAM; population up to 8MB FLASH and 64MB SDRAM is supported.
SerComm Corp.
TNETD7200 - Host Processor / ADSL Transceiver
IP806GA/GB V3(490YBM00)
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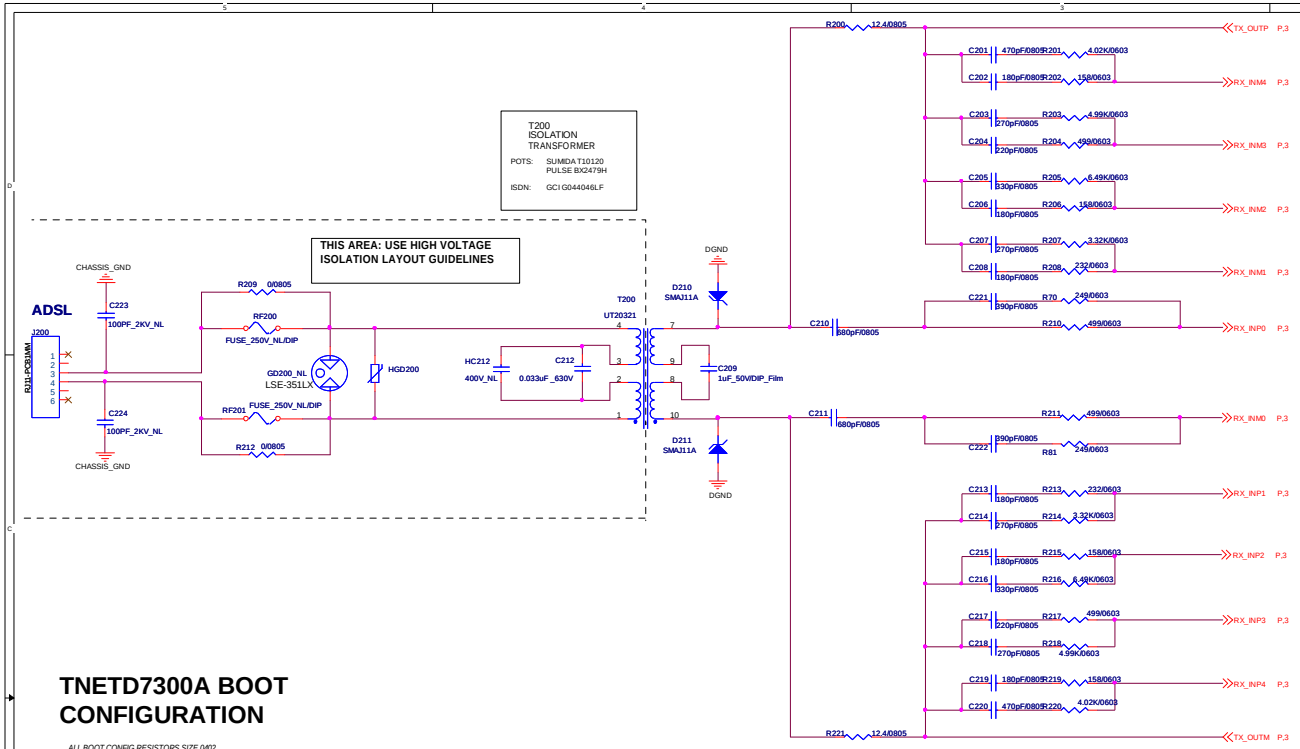


For ISDN, populate values as follows:

R208, R213 = 2.32k ohms ; C208, C213 = 100pF
R207 ,R214 = 187 ohms ; C207, C214 = 100pF

R206, R215 = 5.90k ohms ; C206 ,C215 = 150pF
R205 ,R216 =137 ohms ; C205, C216 = 120pF

R204, R217 = 1.47k ohms; C204, C217 = 100pF
R203 ,R218 = 158 ohms; C203, C218 = 82pF

R202, R219 = 1.5k ohms; C202, C219 = 100pF
R201 ,R220 = 113 ohms; C201, C220 = 82pF

R210, R211 = 499 ohms ; C209=0.033uF
R70, R81 = 249 ohms ; C212 = 0.022uF
C210, C211 = 330pF
C221, C222 = 1.2nF

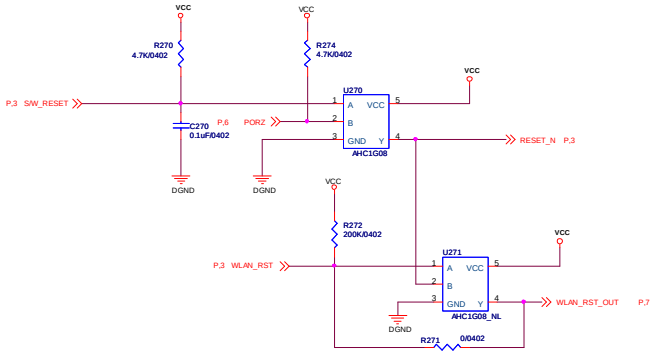
AR7_VWi REVISION HISTORY

Rev 1.0: 12-14-2003	INITIAL SCHEMATIC CAPTURE.
Rev 1.1: 12-15-2003	INITIAL SCHEMATIC CAPTURE.
Rev 1.17: 01-14-2004	ADDED WIRELESS AND VOICE
Rev 1.20: 01-26-2004	Added Package Type property for netlist extraction.
Rev 1.27: 01-29-2004 Release 1	FIXED SANGAM E-NET POLARITY
Rev 2.08 04-30-2004	Connected stitch caps to 1.5V_F instead of 1.5V
Rev 3.25: 05-11-2004 Release 3	REV 3 RELEASE
Rev 3.27: 06-28-2004	Corrected schematic error on Sheet 9 on the over-voltage circuitry. Also updated to reflect final BOM loading.

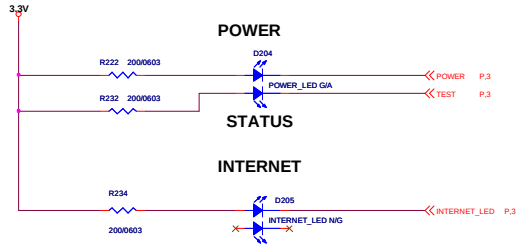
TNETD7300A BOOT CONFIGURATION

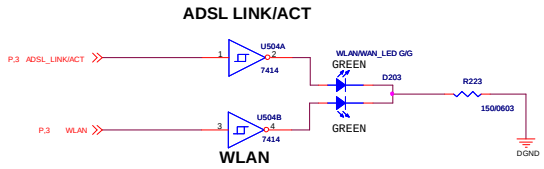
ALL BOOT CONFIG RESISTORS SIZE 0402

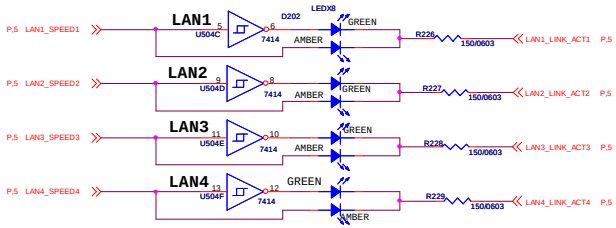
RESET CIRCUITRY



LEDs







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Title	Line Interface and Hybrid; Boot Config; Reset; LEDs
Document Number	IP806GA/GB V3(490YBM00)
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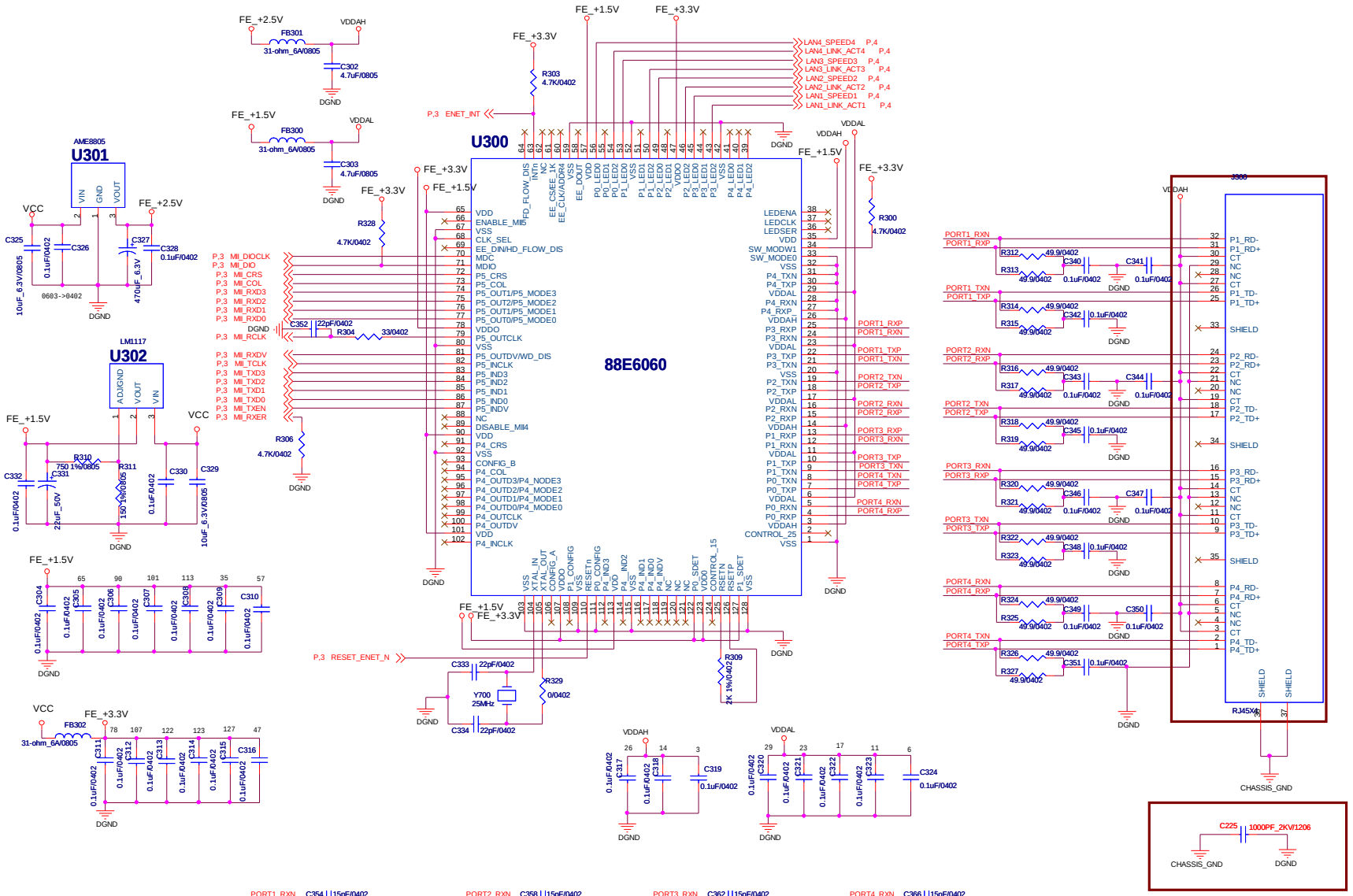

SerComm Corp.

Title	External Ethernet PHY - (optional)
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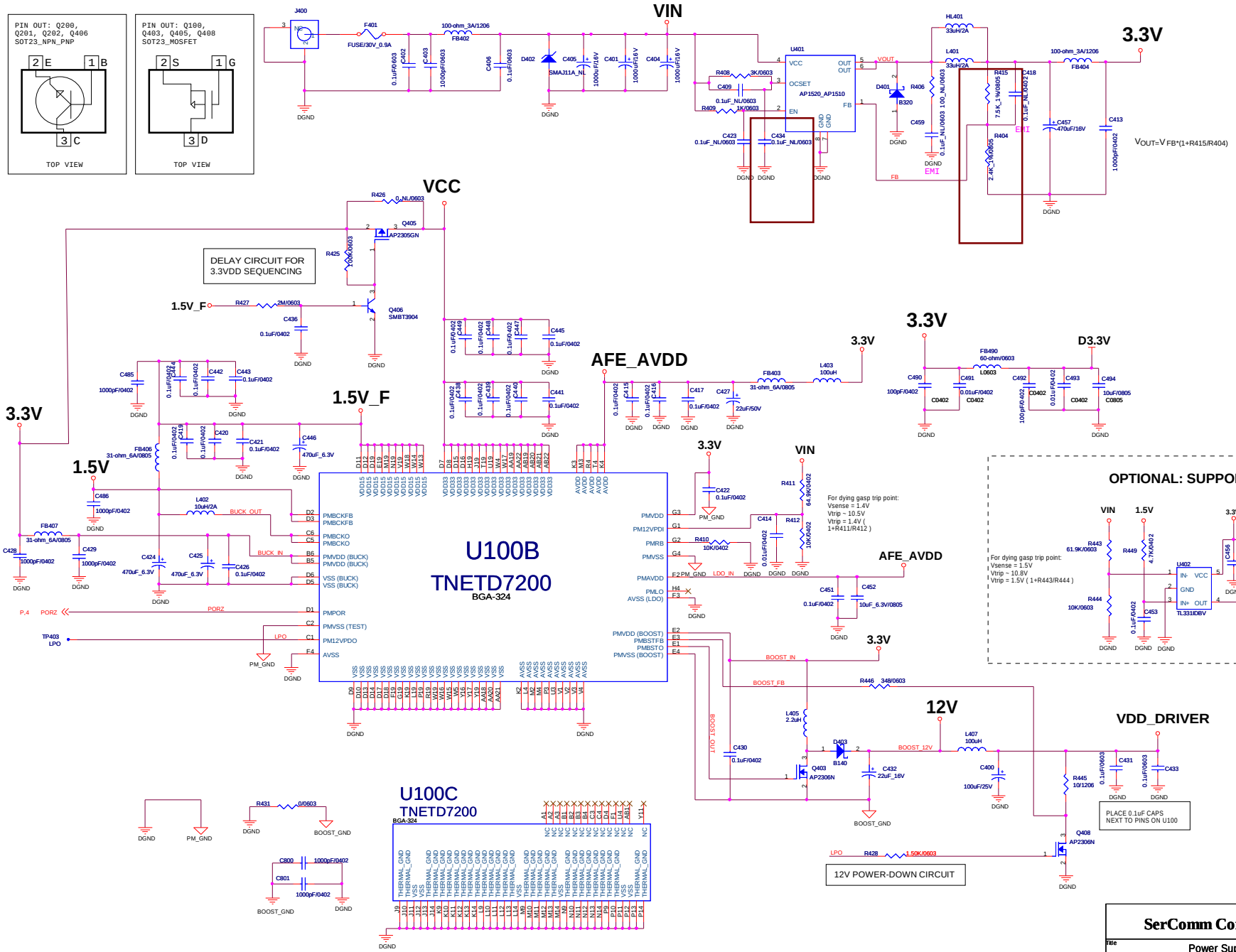
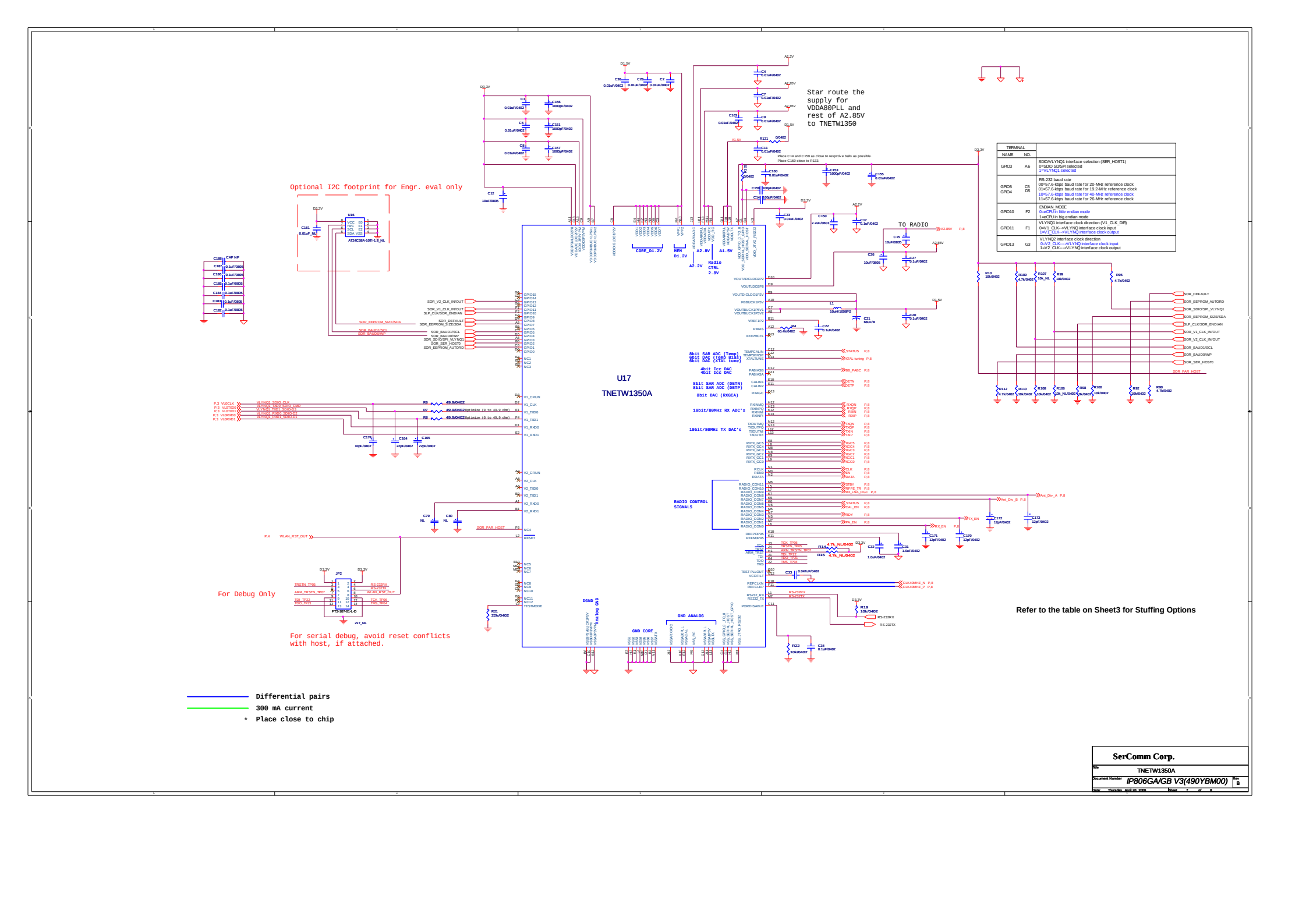
WALL BRICK INPUT
12VDC @ 1A





TERMINAL NAME	NO.	
GPIO3	A6	SDIO/VLYNQ1 interface selection (SER_HOST1) 0=SDIO SDISR selected 1=VLYNQ1 selected
GPIO5 GPIO4	C5 D5	RS-232 baud rate 00=57.6-kbps baud rate for 20-MHz reference clock 01=57.6-kbps baud rate for 19.2-MHz reference clock 10=57.6-kbps baud rate for 40-MHz reference clock 11=57.6-kbps baud rate for 26-MHz reference clock
GPIO10	F2	ENDIAN_MODE 0=CPU in little endian mode 1=CPU in big endian mode
GPIO11	F1	VLYNQ1 interface clock direction (V1_CLK_DIR) 0=V1_CLK-->VLYNQ interface clock input 1=V1_CLK-->VLYNQ interface clock output
GPIO13	G3	VLYNQ2 interface clock direction 0=V2_CLK<--VLYNQ interface clock input 1=V2_CLK-->VLYNQ interface clock output

SerComm Corp.

Title	TNETW1350A
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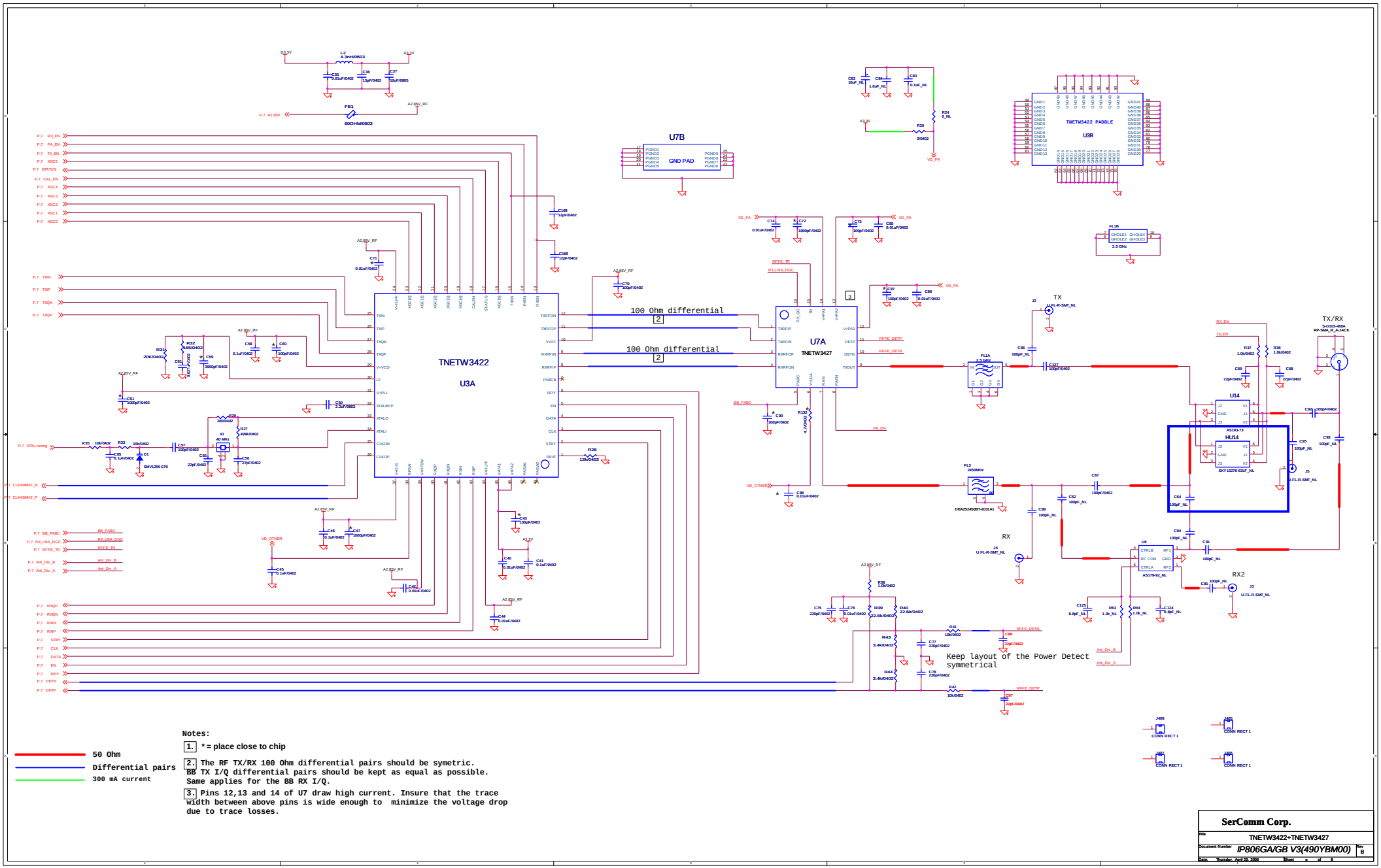

Notes:

1. * = place close to chip
2. The RF TX/RX 100 Ohm differential pairs should be symetric. BB TX I/Q differential pairs should be kept as equal as possible. Same applies for the BB RX I/Q.
3. Pins 12,13 and 14 of U7 draw high current. Insure that the trace width between above pins is wide enough to minimize the voltage drop due to trace losses.

Title	TNETW3422+TNETW3427
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