Chapter 6 Internal Photographs

Overview

This section includes internal photographs of the FWAN PCS B1.8 Base Station.

Contents

6.1 Internal Photographs of FWAN PCS B1.8 Base Station Digital Cards

Figure 6.1 and Figure 6.13 show the overall view of the Base Station showing hardware, cabling, and loads during radiated emissions testing.

The Base Station comprises six sections (top to bottom):

1. Circuit breakers
2. AC/DC power rectifier
3. Telephony DSX panel
4. Eight RF transceiver modules
5. Digital shelf
6. Air-moving device

6.1.1 Digital Shelf

Figure 6.1 Overview of the FWAN PCS B1.8 Base Station Digital Cabinet

Figure 6.2 shows the air-moving device (AMD), which is located beneath the digital shelf. Also shown is the typical space between the AMD and the bottom of the EMI cabinet where excess cables are bundled.

Figure 6.2 View of the Lowermost Shelf and Under-Space of the FWAN PCS B1.8 Base Station Digital Cabinet

6.1.2 Network Interface Circuit Pack PCA

The Network Interface Circuit (NIC) Pack is responsible for interfacing the Base to the 5ESS for voice and to the DSN for HSD via T1/DS1, 1.544 Mbps interfaces. These T1 signals are in Extended Super Frame, ESF, format and carry either GR303 DS0 voice or Point-to-Point Protocol, PPP, over HDLC frames for High Speed Data, HSD. Any mix of voice or HSD interfaces are supported by the NIC for a total of sixteen T1 signals.

Figure 6.3 Network Interface Circuit Pack PCA

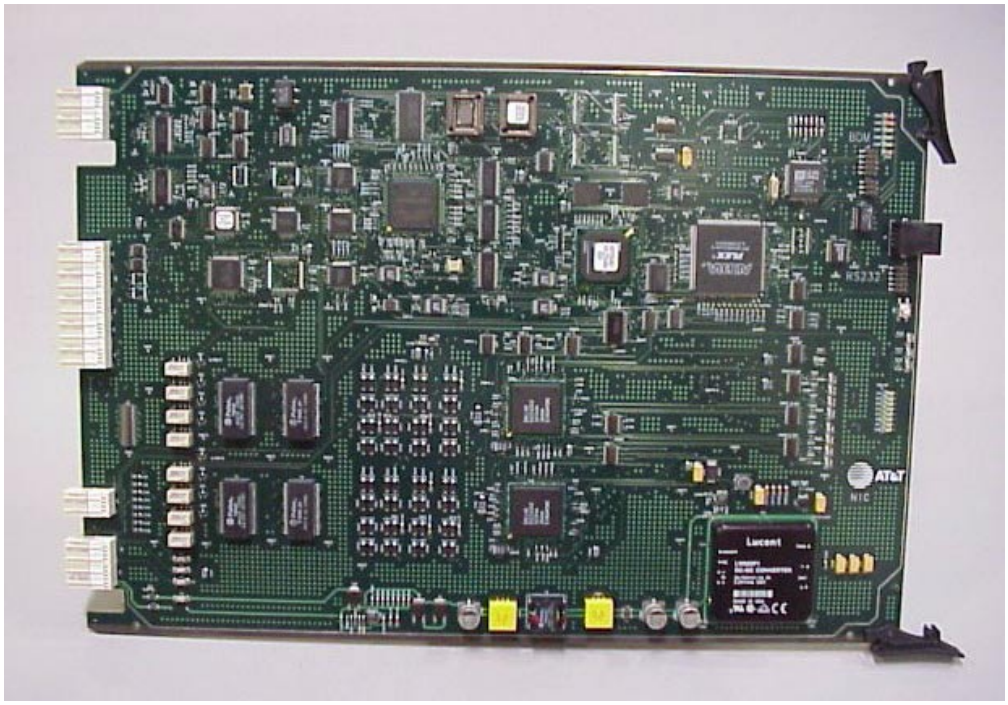
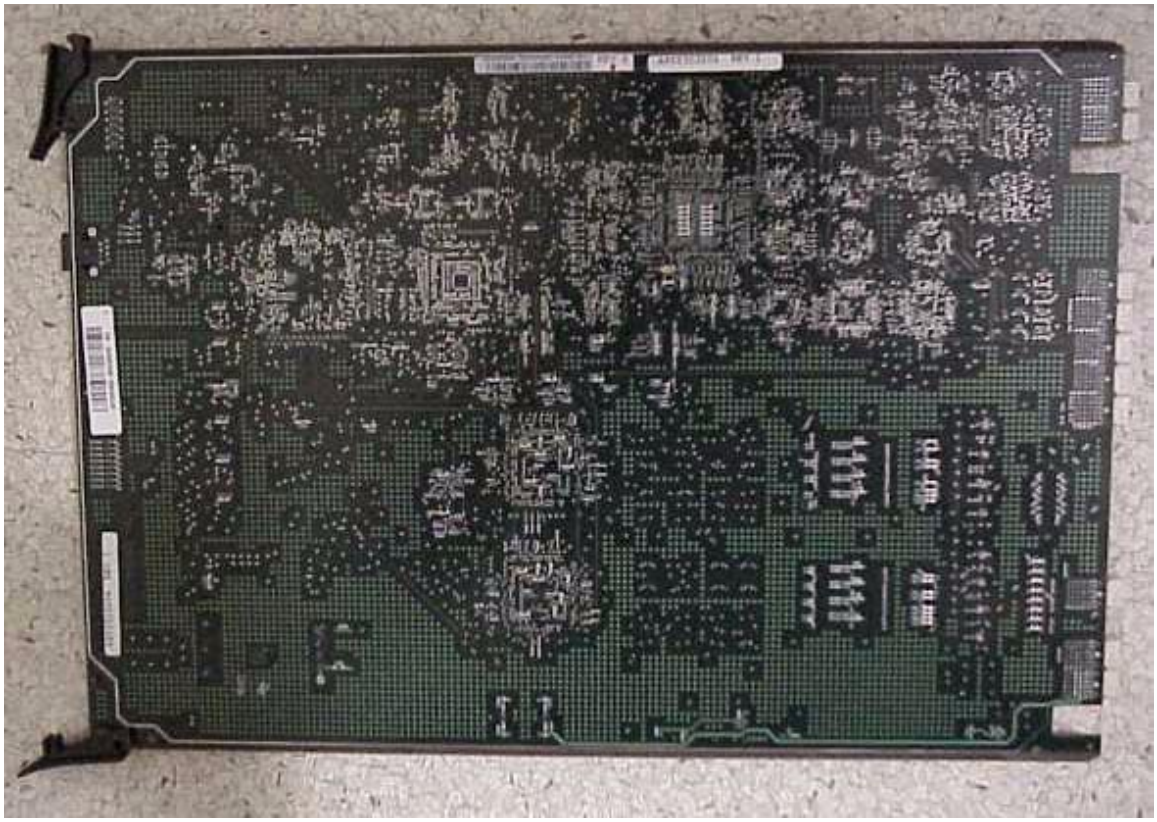


Figure 6.4 Bottom of the Network Interface Circuit Pack PCA



6.1.3 WP PCA

The WP card provides waveform coding function, fax modem demod/remod, and echo cancellation functions for multiple simultaneous voice channels.

Figure 6.5 WP PCA

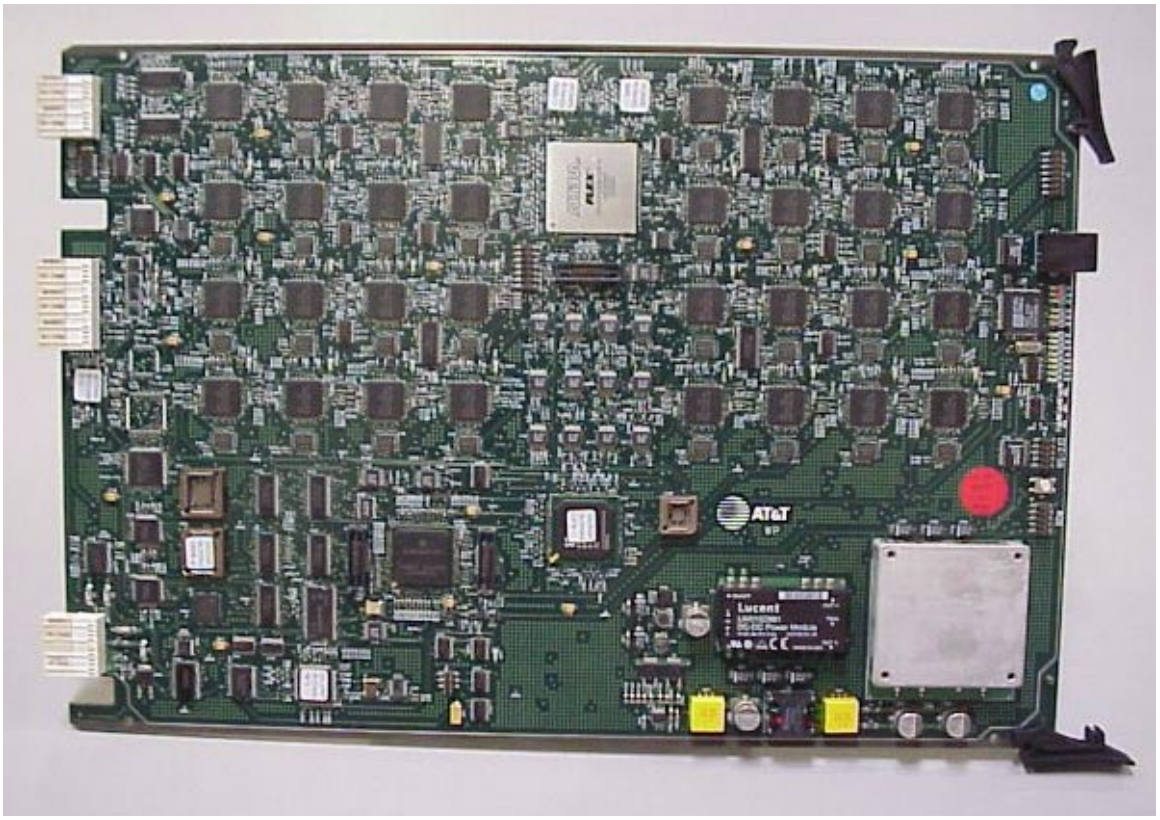
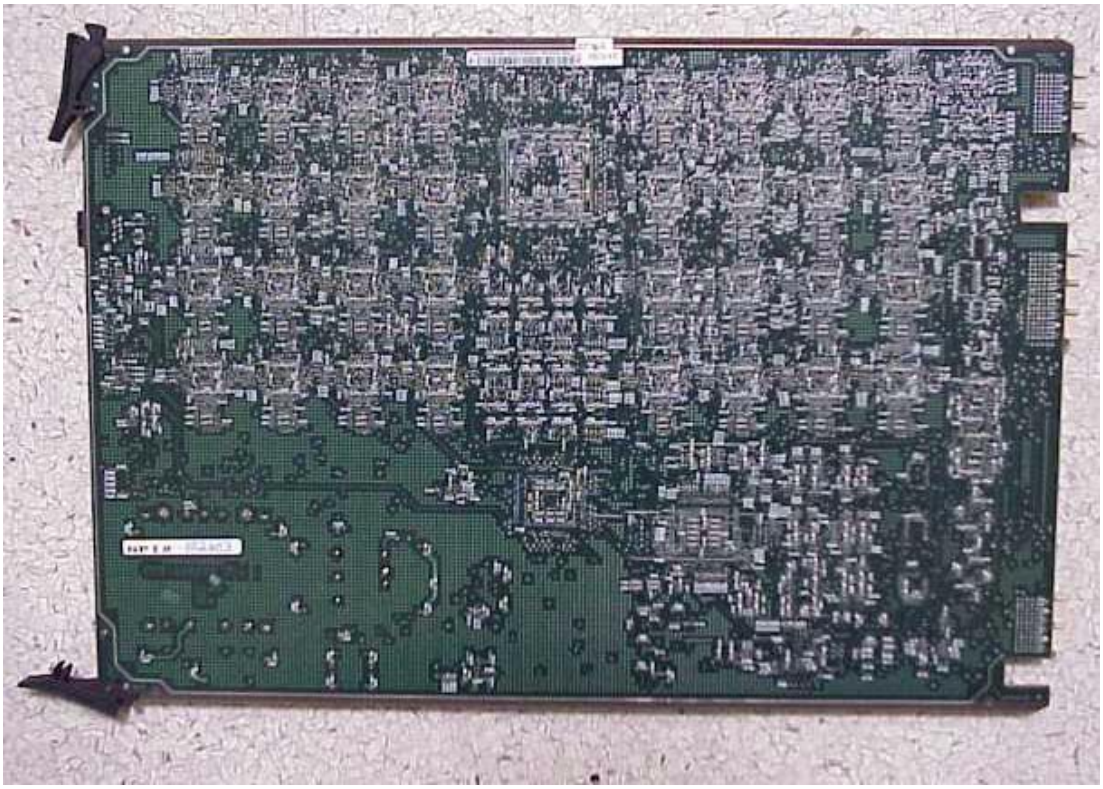


Figure 6.6 Bottom of WP PCA



6.1.4 BCP PCA

The Base Control Processor Circuit Pack, BCP is responsible for interfacing the NIC, WP, and SBC circuit packs via serial 8 Mbps TDM bit streams. The BCP performs the Base interworking function with the 5ESS, i.e. TMC channel termination and generation, as well as, the IP routing function, and digital switching.

Figure 6.7 BCP PCA

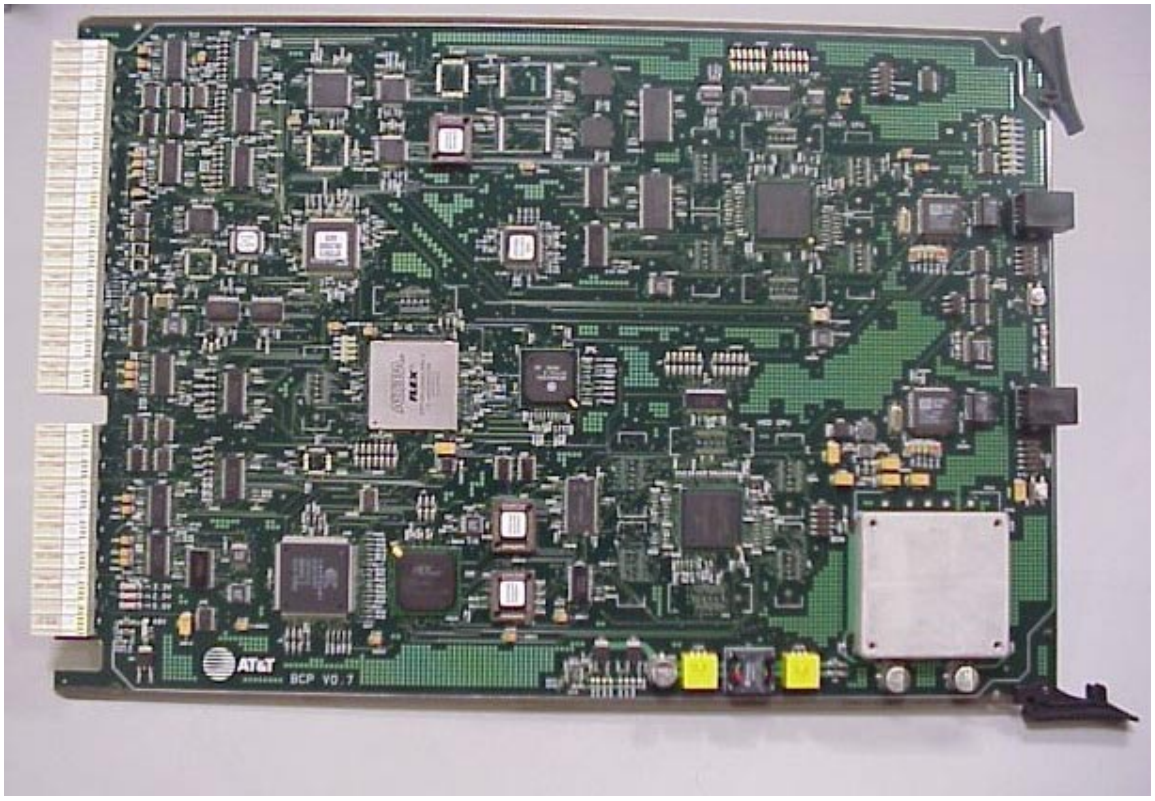
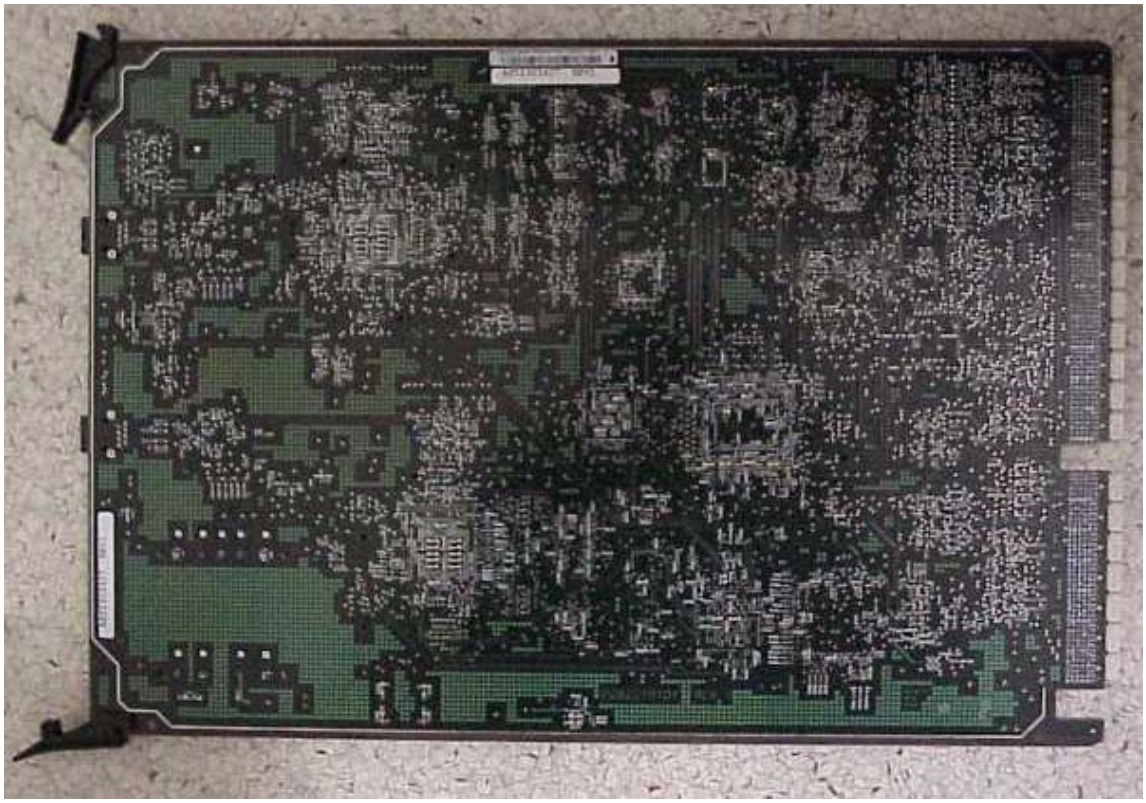


Figure 6.8 Bottom of BCP PCA



6.1.5 SBC PCA

The SBC circuit pack performs the airlink functionality required to implement the Voice channels, Network Access channels, the high speed data (HSD) channels, and a number of subband functions including - delay compensation, Remote Unit (RU) synchronization pilot generation, and dynamic channel allocation.

Figure 6.9 SBC PCA

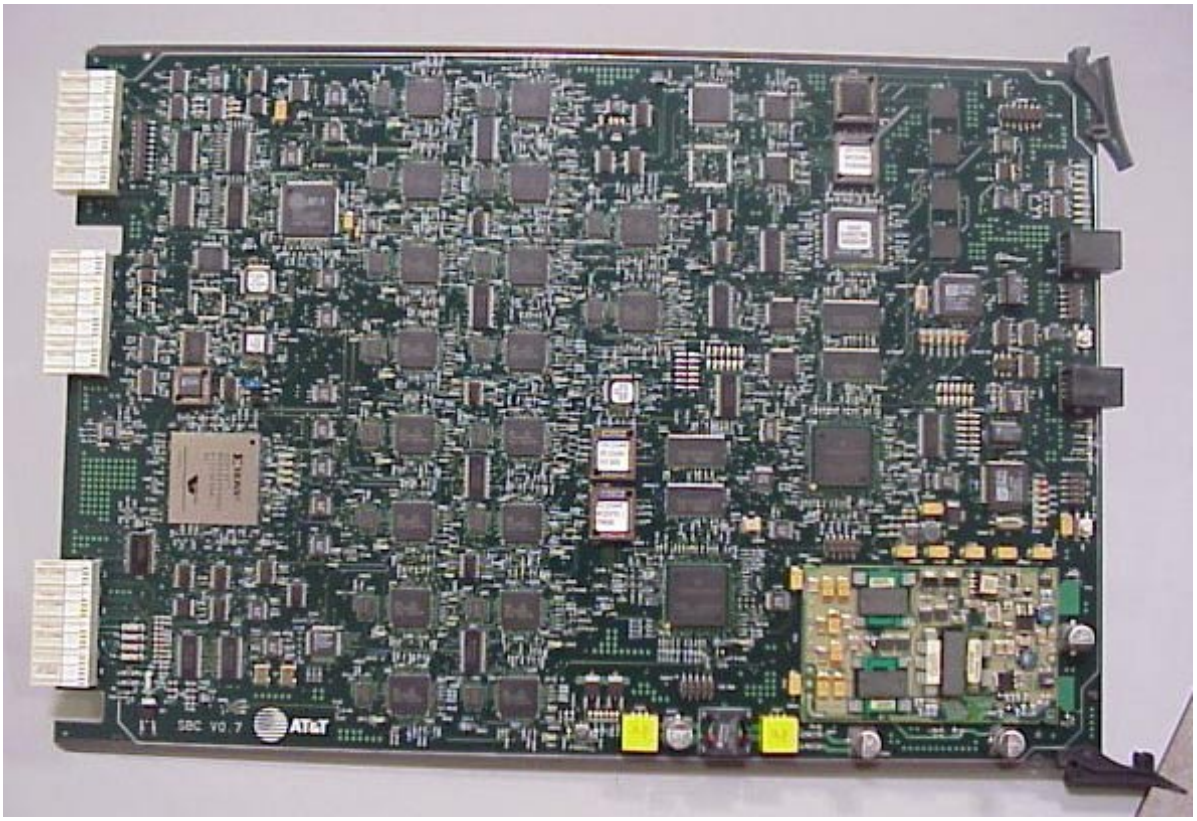
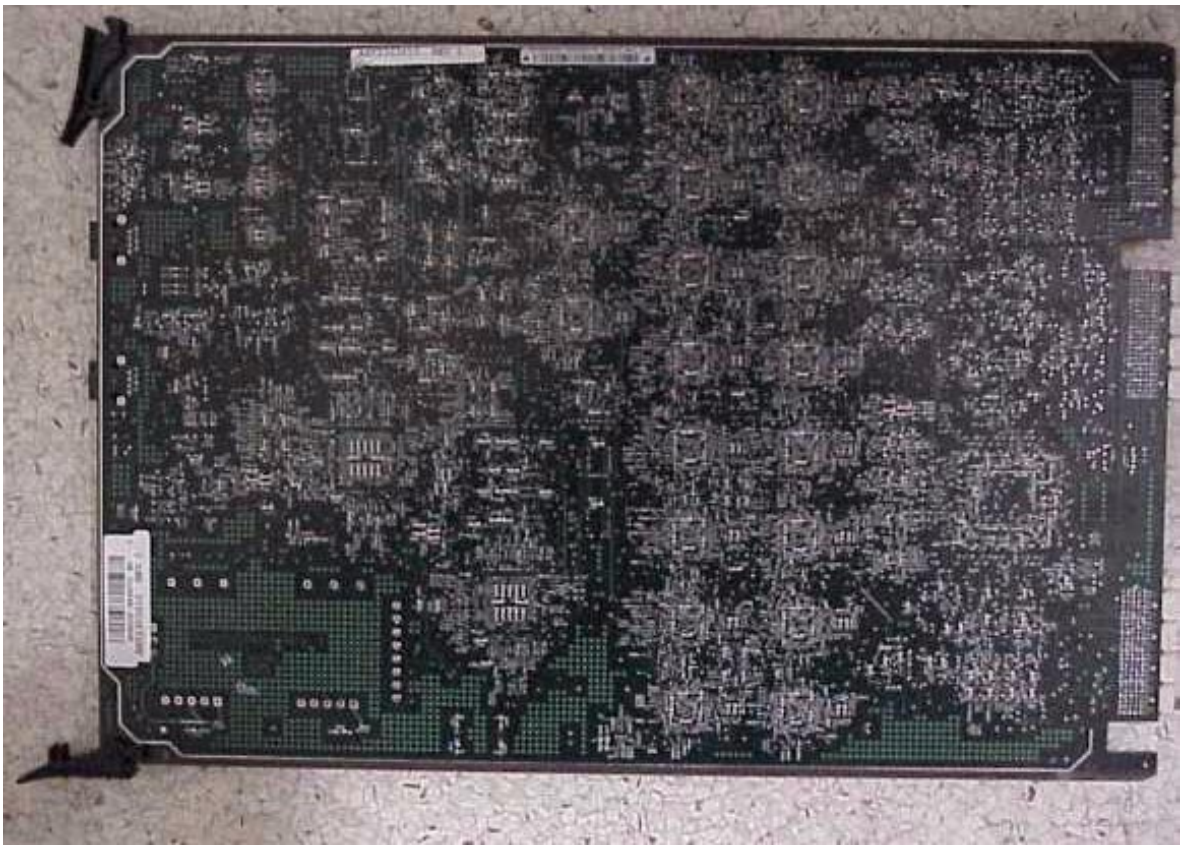


Figure 6.10 Bottom of SBC PCA



6.1.6 SMP PCA

The SMP provides for Base system/circuit pack management.

Figure 6.11 SMP PCA

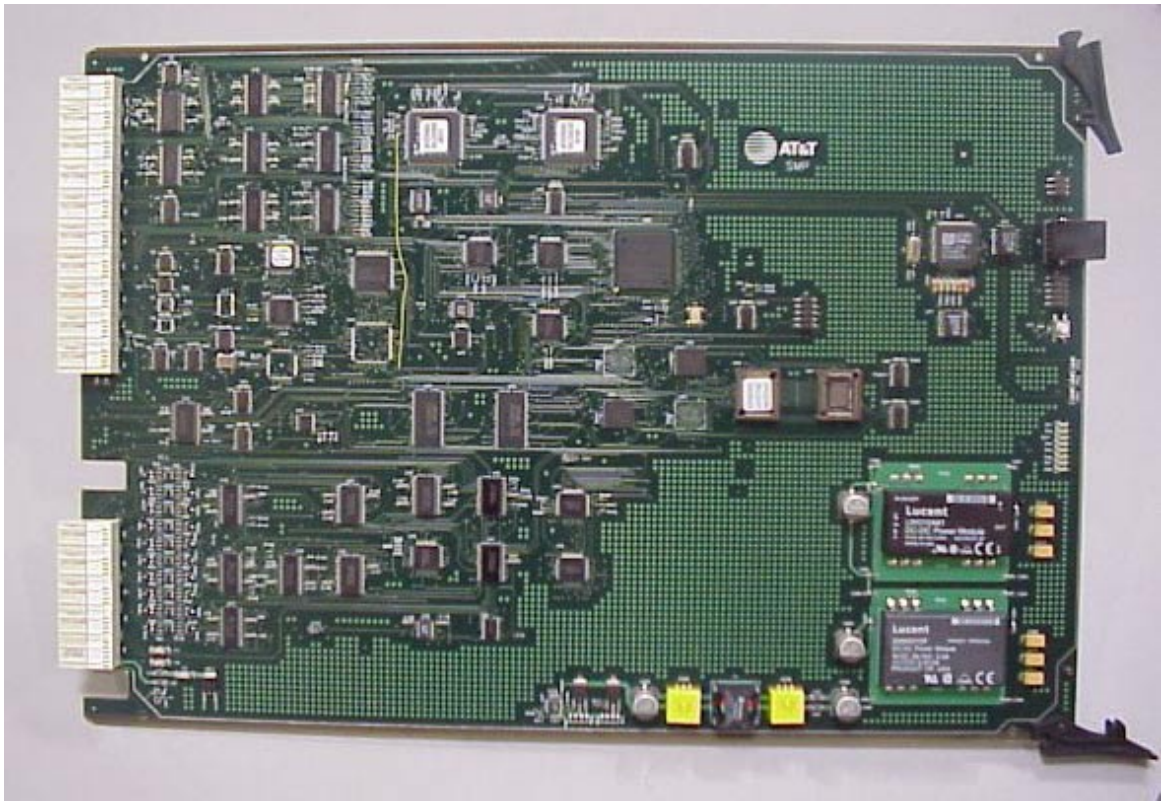
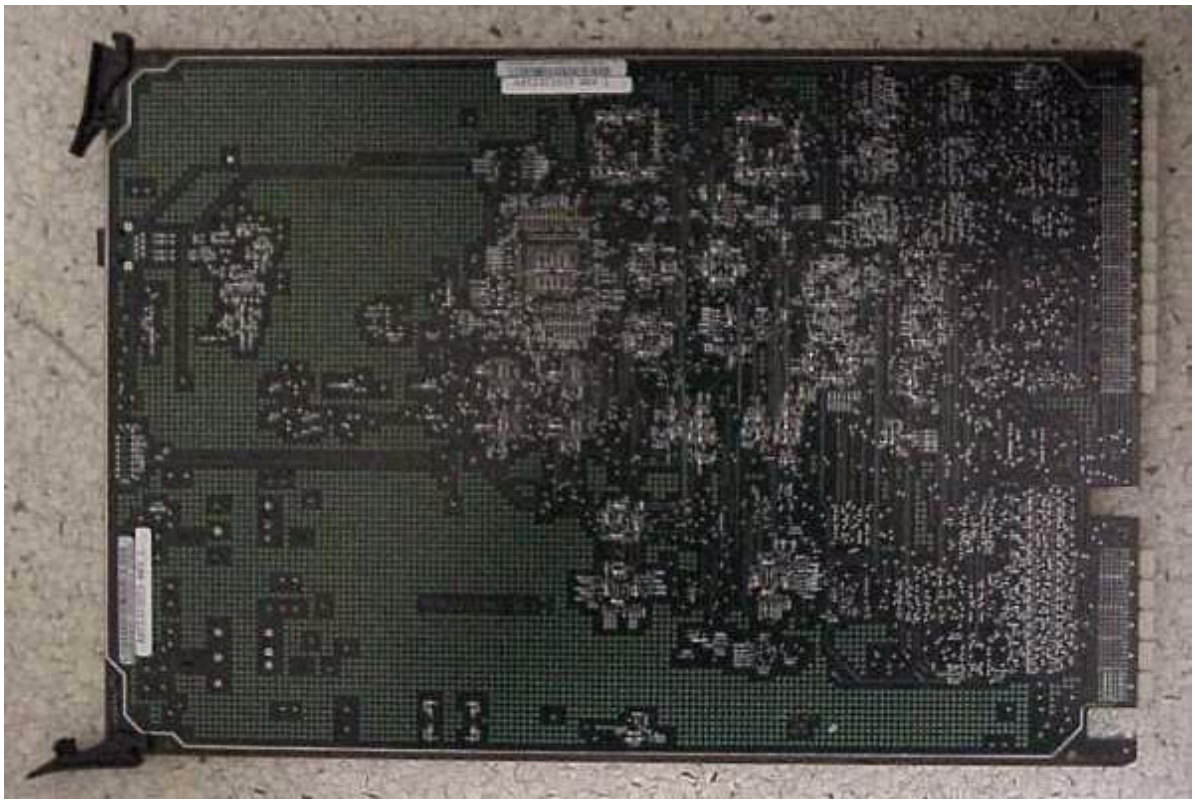


Figure 6.12 Bottom of SMP PCA



6.2 Internal Photographs of the FWAN PCS B1.8 Base Station RF Modules

Figure 6.13 shows the overall view of the Base Station showing hardware, cabling, and loads during radiated emissions testing. Refer to Section 6.1 for details.

Figure 6.13 Overview of the FWAN PCS B1.8 Base Station

Figure 6.14 identifies the air-moving device (AMD) which is located beneath the digital shelf. Also shown is the typical space between the AMD and the bottom of the EMI cabinet where excess coaxial cables are bundled.

Figure 6.14 View of the Lower Portion of the FWAN PCS B1.8 Base Station Cabinet

6.2.1 Photographs of the Transceiver Module Unit

Figure 6.15 shows the right side view of the transceiver module unit. The transceiver module provides amplification of TX and RX signals, redundancy switching, gain control, diplexing, DC/DC conversation, front panel test points (RF), LED alarm indicators, ESN capability, and control and monitoring of status and alarm conditions.

Figure 6.15 Transceiver Module — Right Side View

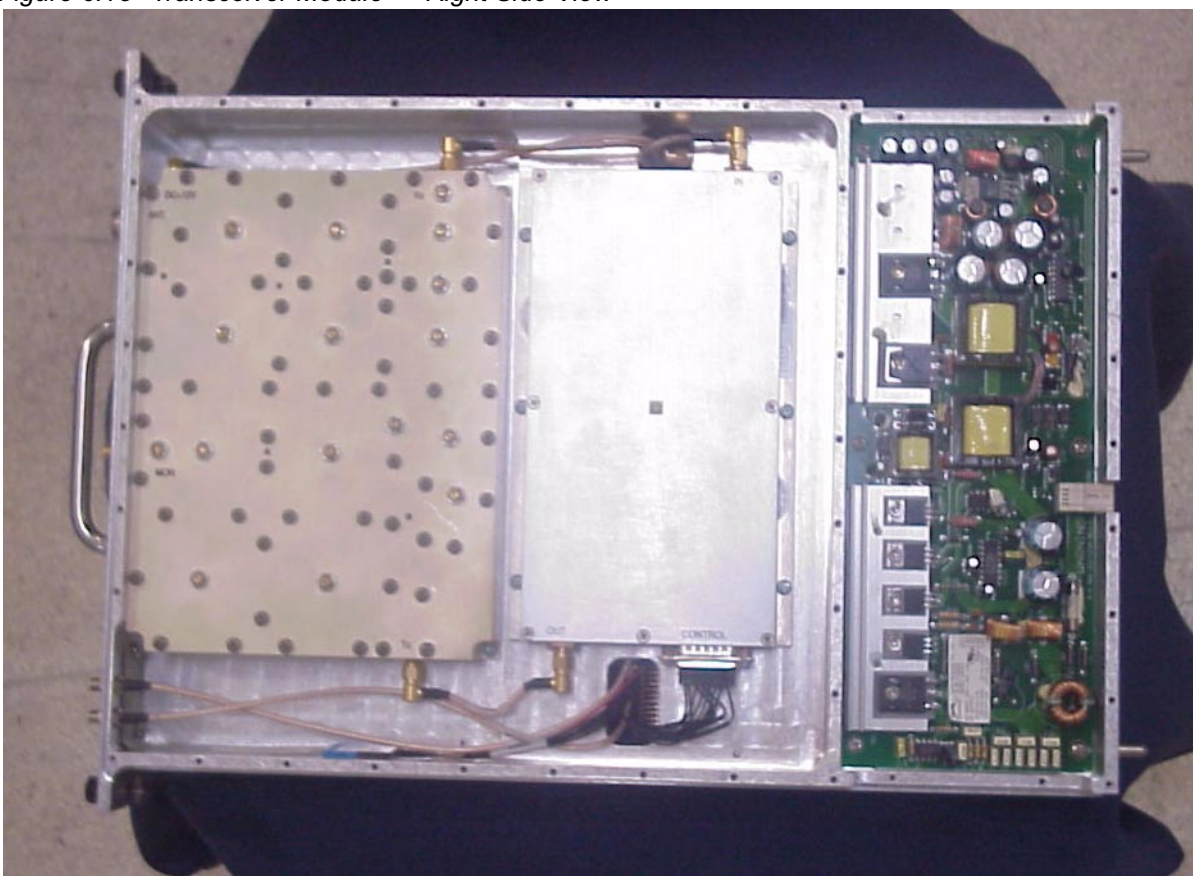


Figure 6.16 shows the left side view of the transceiver module. The transceiver module provides amplification of TX and RX signals, redundancy switching, gain control, diplexing, DC/DC conversation, front panel test points (RF), LED alarm indicators, ESN capability, and control and monitoring of status and alarm conditions.

Figure 6.16 Transceiver Module - Left Side View

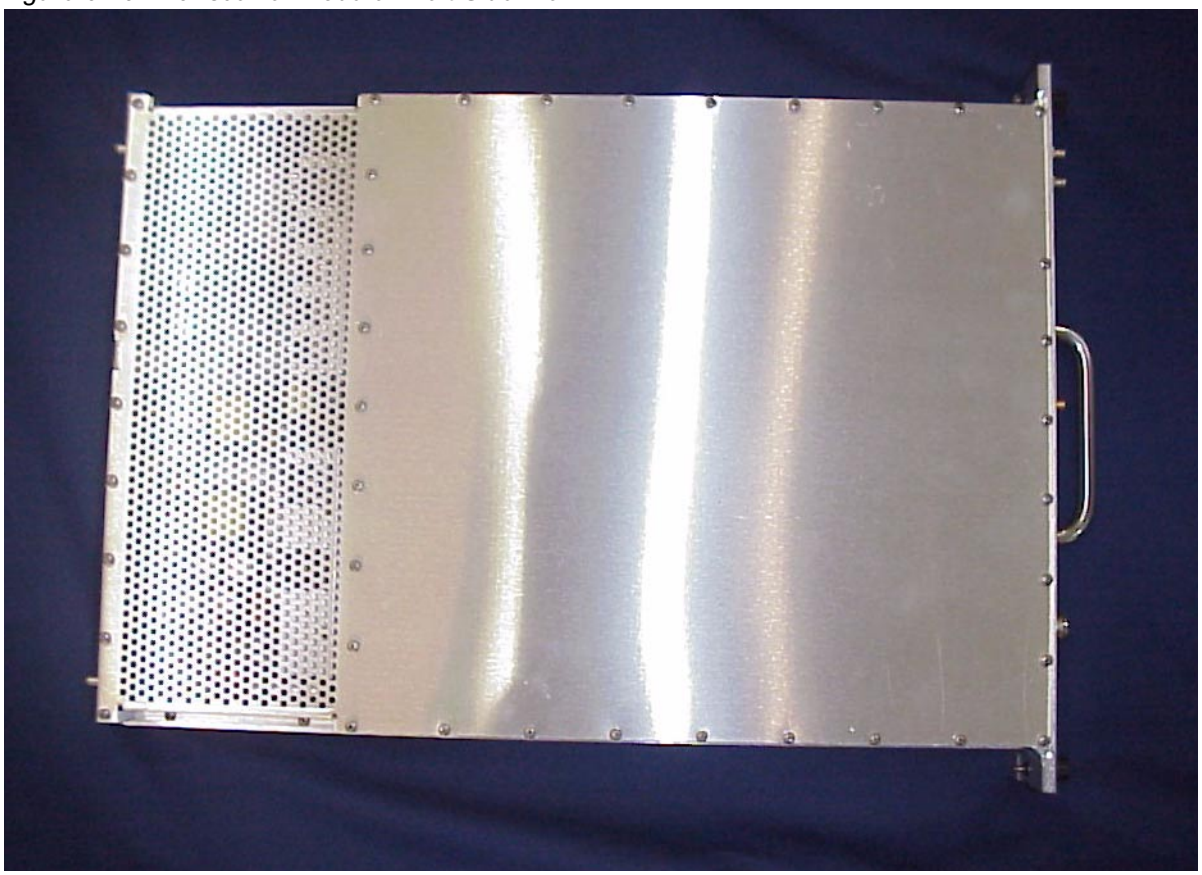


Figure 6.17 shows the transceiver unit.

Figure 6.17 Transceiver

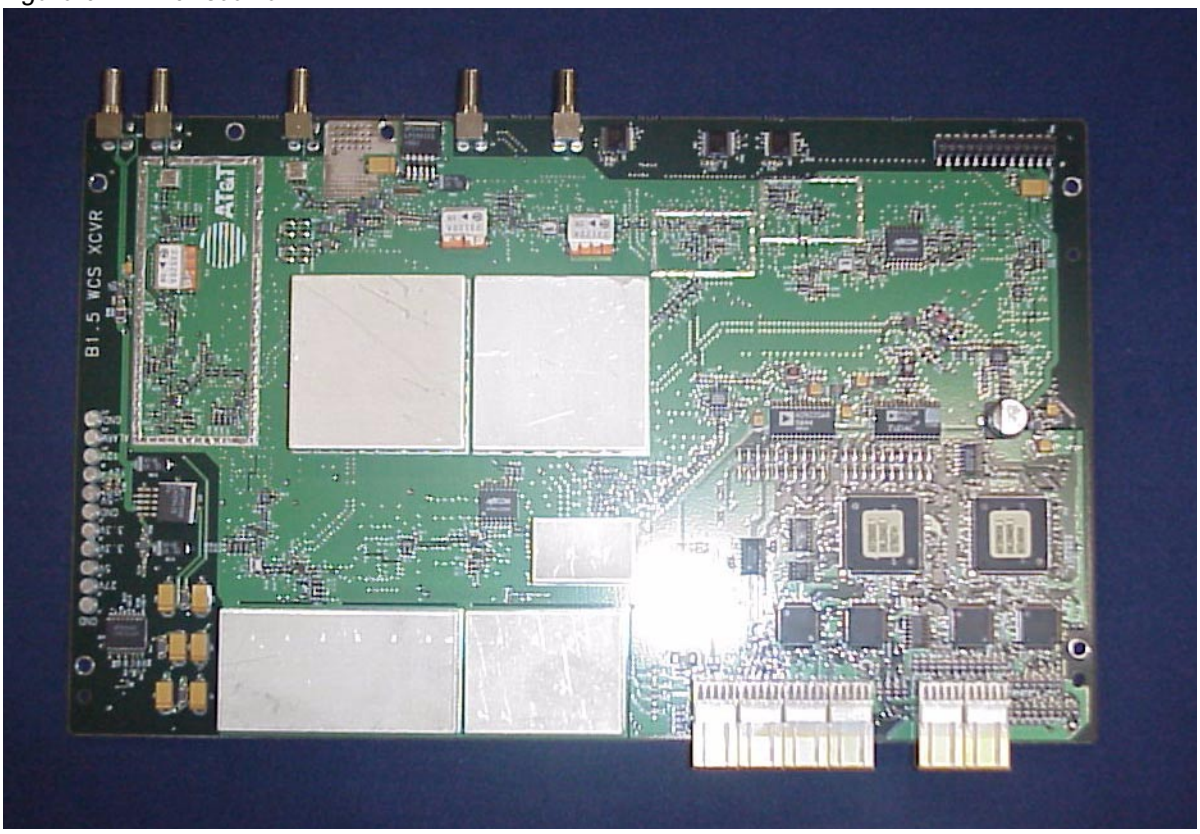
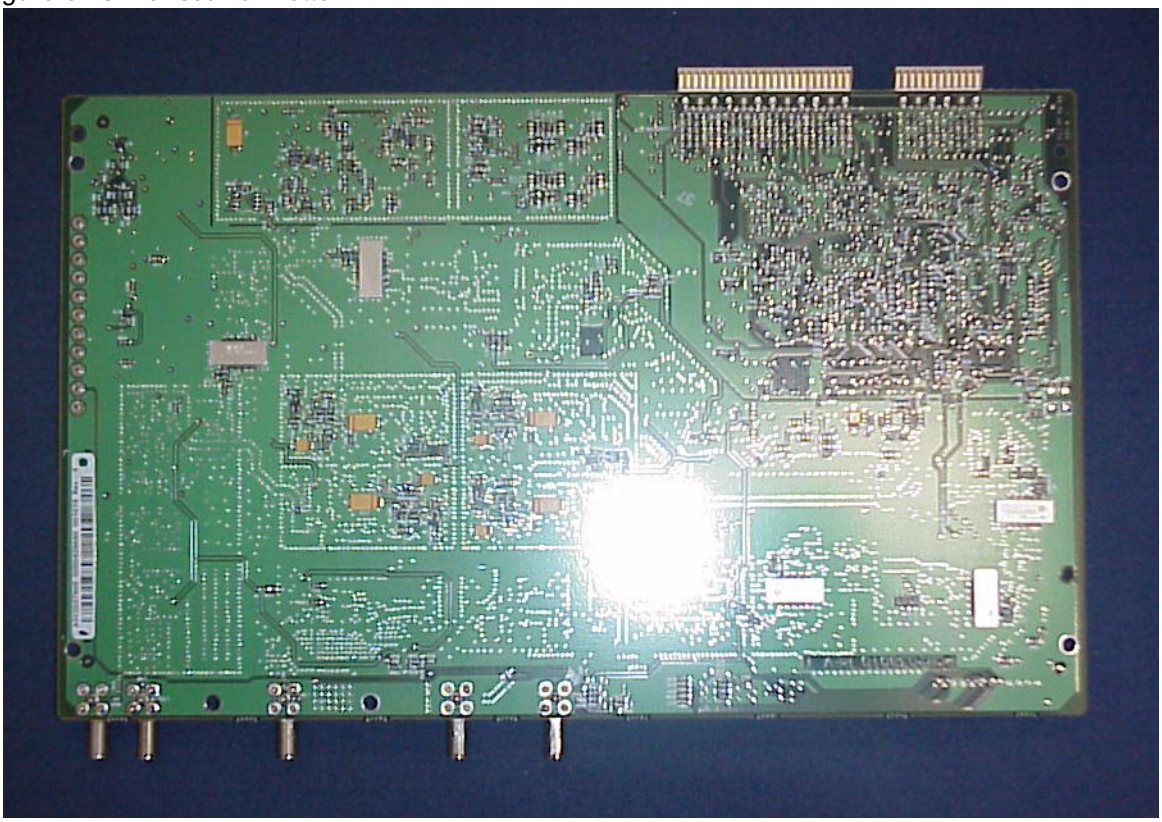


Figure 6.18 Transceiver Bottom



6.2.2 Photographs of the Power Supply

Figure 6.19 identifies the transceiver DC-DC Converter unit. The functions that the DC-DC Converter performs are:

- Conversion of the primary voltage, -48 volts DC, to the required secondary voltages.
- Signalling the failure condition of any secondary voltages.

Figure 6.19 Power Supply

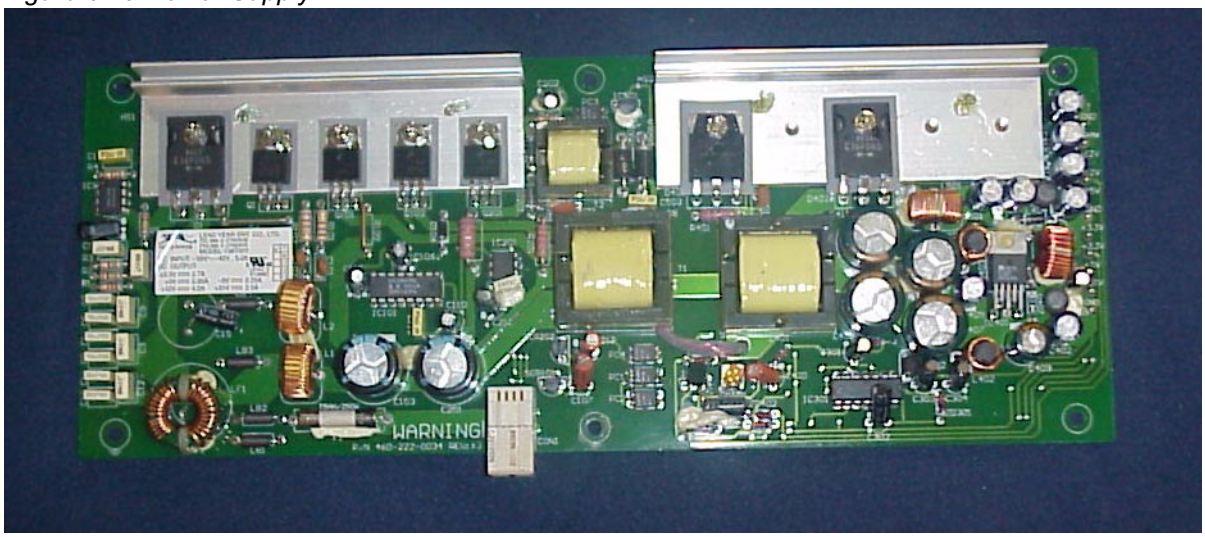
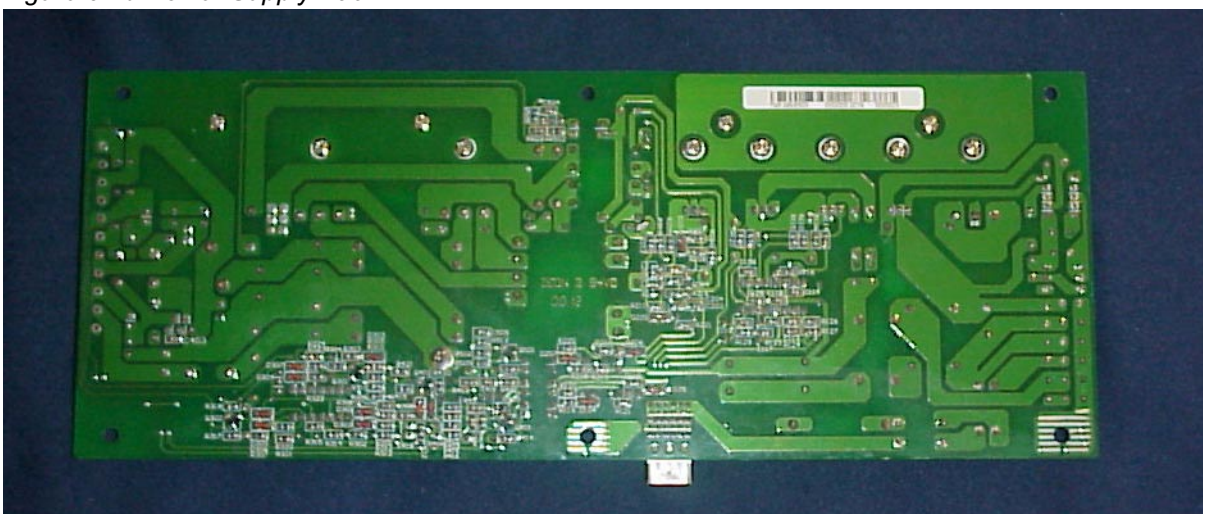


Figure 6.20 Power Supply Back



6.2.3 Photographs of the Duplexer

Figure 6.21 identifies the transceiver duplexer. The duplexer combines the TX and the RX of the transceiver to interface with a single cable to the tower-top amplifier. This duplexer has an IL of approximately 1.0 dB in both the TX and RX paths. The duplexer carries the +12 volts DC required for the tower-top amplifier by means of Bias-T integrated in the duplexer assembly and also provides a test port for TX forward power monitoring port at 20 dB down.

Figure 6.21 Duplexer Top View

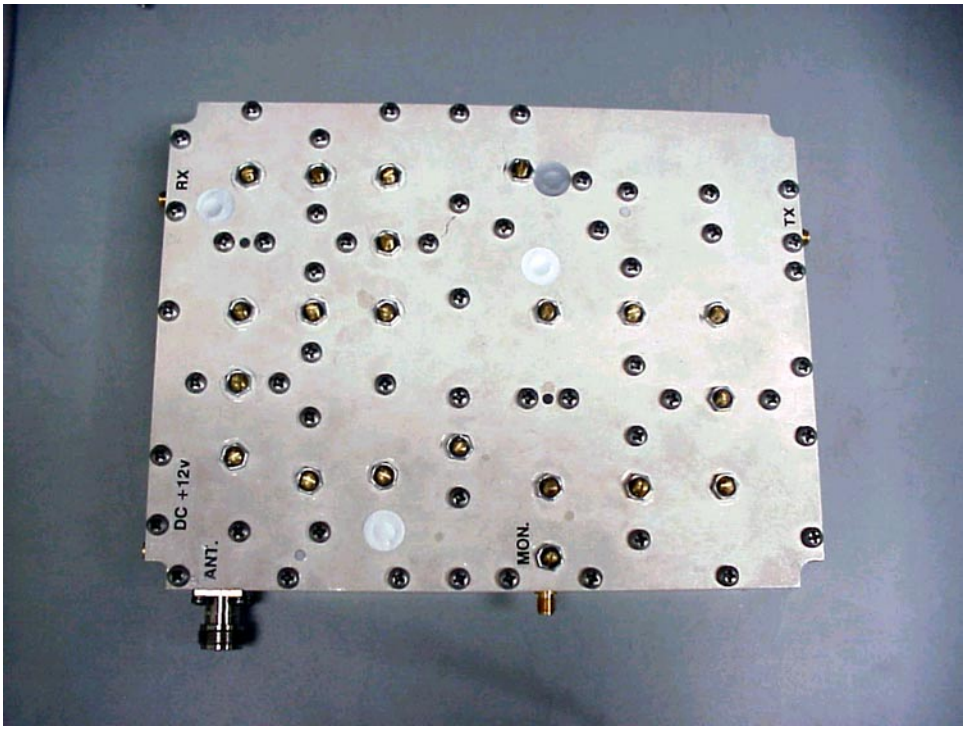


Figure 6.22 Duplexer Side View

Chapter 7 Operational Description

Overview

The AT&T Fixed Wireless Services (FWS) Personal Communications System (PCS) Wireless Access Network has been designed to provide robust, high-quality telephony and data services to residential homes using sophisticated radio technology operating in the 1850-1990 MHz band. This chapter describes the architecture of the FWAN PCS and overview of both the telephony and data portions of the airlink.

Contents

7.1 System Overview

7.1.1 FWAN PCS General Description

The AT&T Fixed Wireless Services FWAN PCS is a Remote Digital Terminal (RDT) system that has been designed to operate over a wireless interconnect. Traditional RDT systems have always been based upon a wireline interface between the Local Digital Switch (LDS) and the subscriber RDT. The FWAN PCS utilizes a wireless radio interface (the FWAN PCS airlink) between the network and line-side interfaces of a Bellcore TR-303 compliant RDT. For that reason, the FWAN PCS RDT is named the Wireless Remote Digital Terminal (WRDT). Although it incorporates wireless elements, the FWAN PCS is intended solely for local loop replacement and will not support typical wireless mobility features such as intercell handoff or roaming. The FWAN PCS airlink utilizes a proprietary radio technology capable of providing a secure wireless interface to the WRDT.

As in a traditional RDT system, the FWAN PCS includes telephony network elements and management network elements. The FWAN PCS telephony network elements (NEs) are the Base Station and Remote Unit (RU). The management NEs are the Wireless Network Management System (WNMS), Wireless Element Management System (WEMS), and the Base Station. For an illustration of how these network elements interact, refer to Figure 7.1.

7.1.2 FWAN PCS Network Elements Overview

The Base Station terminates the TR-303 interface to the Local Digital Switch (LDS) and the Management Operations Channel (MOC) to WEMS. The Base Station also supports multiple airlink connections to the RU population it serves.

The RU terminates the subscriber analog line interfaces and performs the line interface functions of a traditional RDT. The RU also supports its connection to the Base Station via the airlink.

In order to support management functions within the FWAN, the WEMS serves as an element manager for Operations, Administration, Maintenance, and Provisioning (OAM&P) functions that supplement traditional TR-303 RDT OAM&P. The WNMS provides network provisioning and monitoring. The WNMS also provides the FWAN PCS interface to the Wireless Service Management System (WSMS), which coordinates service management. The Switch Element Management System (SEMS) manages the LDS. Each network management system (WNMS, WEMS, WSMS and SEMS) is deployed in a Fixed Wireless Service Network Operation Center (FWS NOC).

Figure 7.1 outlines the major interfaces within the FWAN PCS architecture.

Figure 7.1 FWAN PCS Telephony Architecture

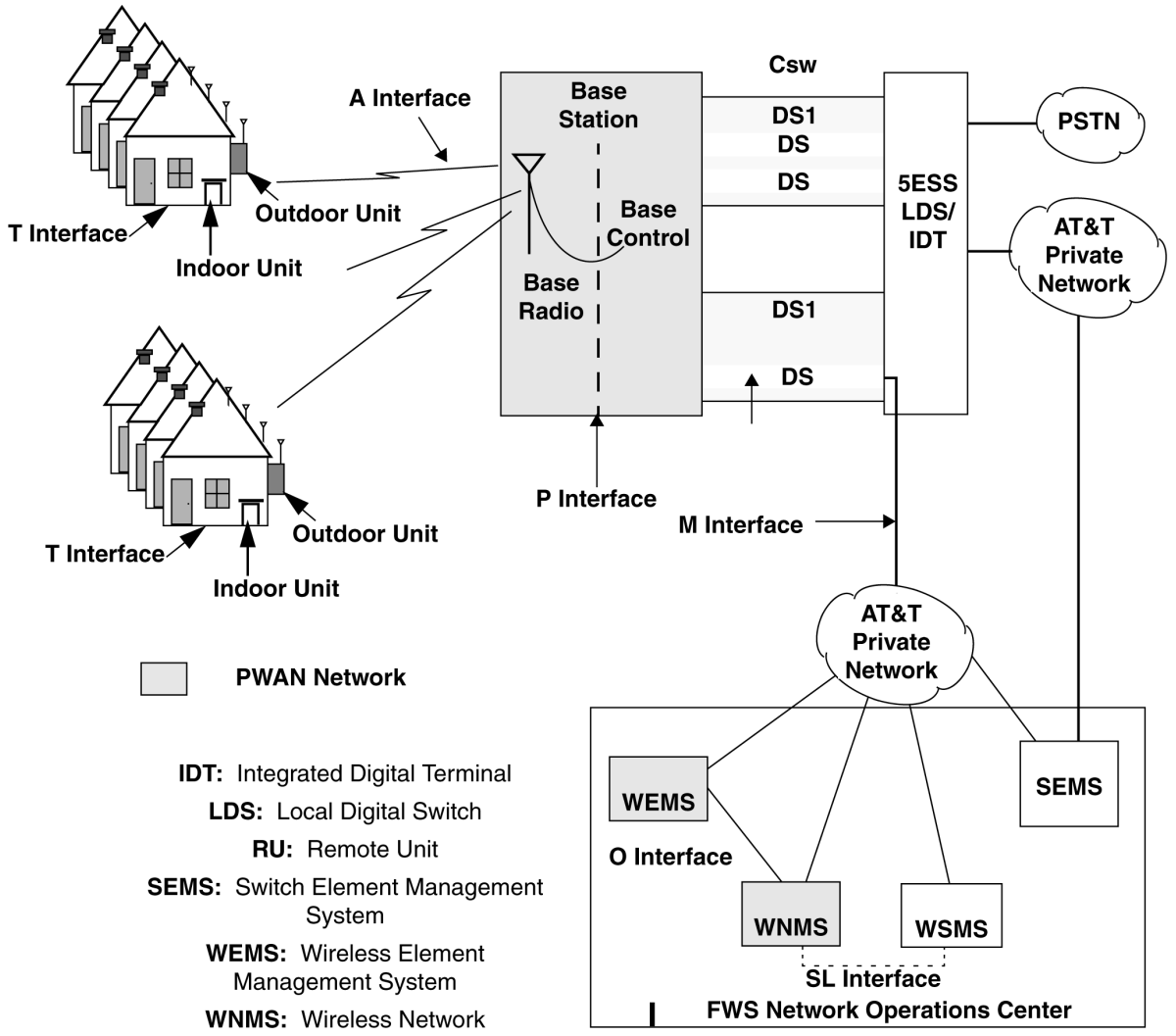


Table 7.1 FWAN PCS Reference Architecture - Interface Definitions

Interface ID	Description
T Interface	Terminal interface to RUs
A Interface	Air interface between RUs and Base Station radio equipment
P Interface	Interface between Base Station radio equipment and Base Station control
Csw Interface	Interface that provides public switched telephone network (PSTN) connectivity for call processing
M Interface	Mgmt. interface between WEMS and Base Station agent

Table 7.1 FWAN PCS Reference Architecture - Interface Definitions

Interface ID	Description
O Interface	Operations interface between WEMS and WNMS
SL Interface	Operations interface between WNMS and WSMS

7.1.3 Wireless Network Elements Deployment

The FWAN PCS service area is comprised of a number of small service regions or cells. Each cell consists of one Base Station and a number of RUs. FWAN PCS cells are typically smaller than those of a mobility network. In a typical FWAN PCS system, the link budget dictates a cell radius of between 100 m and 1.6 km, corresponding to a path loss range of 70 to 140 dB.

To provide sufficient traffic resources for the RU population surrounding a Base Station, each cell may be split into two, three, or four sectors. A typical FWAN PCS cell site will employ a four-sector Base Station and associated antennas designed to provide coverage over a 90-degree horizontal beamwidth within each sector. The number and type of Base Station antennas will vary depending upon site requirements, and either spatial or polarization diversity antenna configurations may be employed. Each sector of the Base Station requires access to 1 MHz of downlink and 1 MHz of uplink bandwidth.

Within FWAN PCS systems that support four-sector cells, the frequency reuse between adjacent cells will be one. This reuse factor is possible by virtue of the unique nature of the interference environment and the control that the Base Station maintains through the RU channel allocation process.

Unlike cellular communication systems designed for a mobility environment, the FWAN PCS has an advantage of supplying service to fixed users in known locations. In order to take advantage of this unique relationship between the Base Station and multiple fixed users, each RU employs a directional antenna and RF power control to minimize the adverse effects of multipath propagation and reduce its contribution to the overall interference environment.

RUs are situated at the subscriber's location and serve as full-duplex RDTs. Communication between the Base Station and the RU population surrounding it may take place either as circuit-switched point-to-point connections for telephony traffic or packet-switched point-to-multipoint connections for high-speed-data traffic. Each RU is capable of supporting two simultaneous circuit-switched connections and a concurrent packet-switched data link.

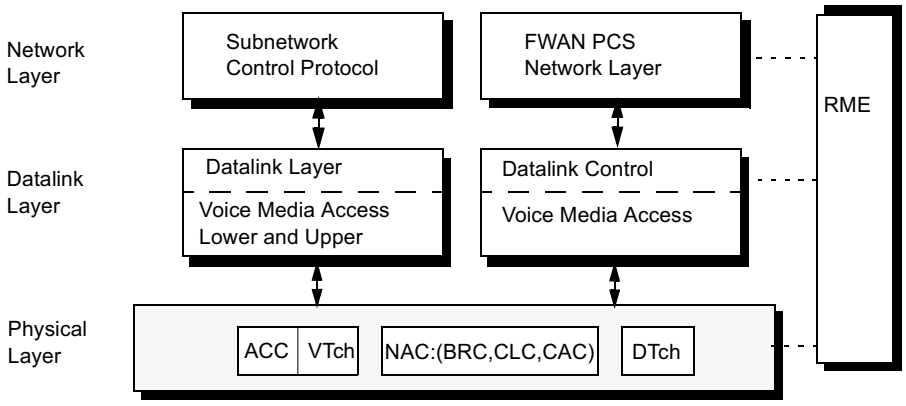
Each RU is powered by an uninterruptible power supply (UPS) located within the RU. The telephony interface between the RU and the customer's equipment is compliant with the specifications set forth in Bellcore TR-57.

During the installation of an RU at the customer premises, the installer utilizes a special Field Installation Tool (FIT) to obtain signal quality information for each trial mounting location on the structure. Through the use of this tool, the installer can often select a mounting location agreeable to the customer and optimize the propagation path between the RU and its serving Base Station.

7.1.4 FWAN PCS Airlink Profile

The FWAN PCS system is based upon the Open Systems Interconnect (OSI) model depicted in Figure 7.2. Subsequent sections in this chapter provide an overview of this model as it applies to the FWAN PCS airlink. Subsequent chapters provide more detailed information concerning the unique design aspects of the physical layer.

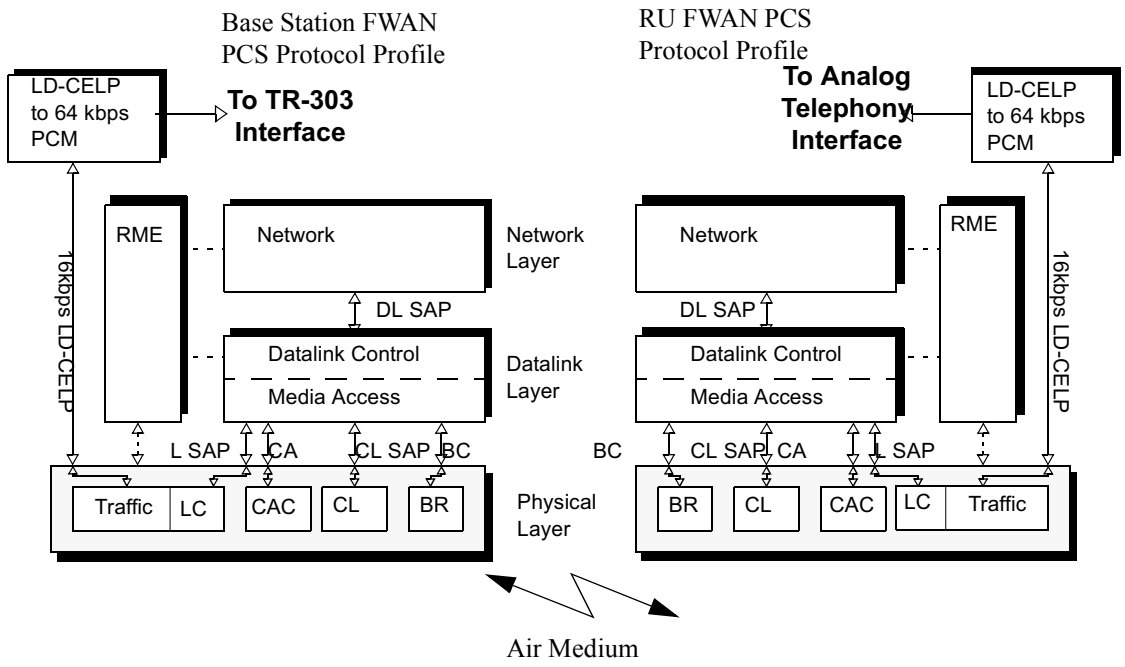
Figure 7.2 FWAN PCS OSI Model



7.1.5 FWAN PCS Telephony Functions

The airlink functions for telephony traffic are carried out utilizing the protocol profile depicted in Figure 7.3. Control information, such as call establishment requests from an RU to the serving Base Station or call termination requests from the Base Station to an RU are carried out through the airlink protocol stack. Voice traffic is passed from the associated telephony interface directly to the physical layer. Consequently, the physical layer is subdivided into entities allocated to supporting specific functions, such as control channel management, traffic channel management, and broadcast data management. Each entity communicates with the Media Access layer through its Service Access Point (SAP). The Media Access layer serves as an airlink management interface between the multiple entities within the physical layer and the Datalink layer.

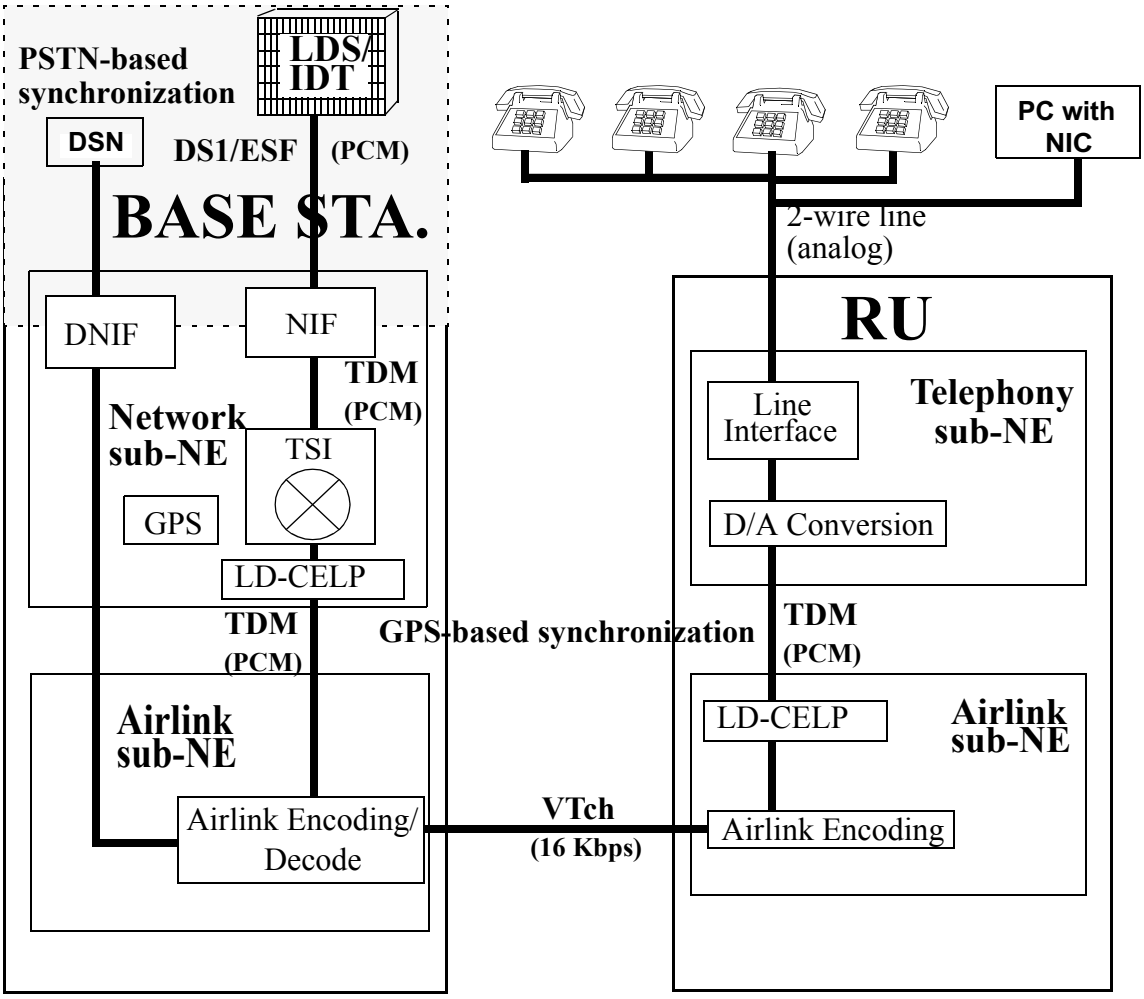
Figure 7.3 FWAN PCS Airlink Protocol Profile



The support of VF telephony signals in the FWAN PCS differs from a traditional RDT (refer to Figure 7.4). In a traditional RDT, analog VF signals are converted to 64 kbps Pulse Coded Modulation (PCM) for transmission across the network. However, to conserve airlink resources the WRDT supports Low Delay-Codebook Excited Linear Prediction (LD-CELP) voice compression. This implementation provides PCM voice quality at one fourth the bandwidth (16 kbps).

As is the case in a traditional RDT, the RU line interface converts incoming analog VF signals to 64 kbps PCM. Unlike a traditional RDT, however, the resulting PCM signals are compressed by LD-CELP for transmission over the airlink at 16 kbps. The received LD-CELP voice data is decompressed at the Base Station and restored to 64 kbps PCM for compatibility with the LDS. Conversely, the Base Station utilizes LD-CELP to compress the incoming 64 kbps PCM to 16 kbps for transmission over the airlink to the RU, where it is decompressed and restored to 64 kbps PCM. The PCM signal is then converted to an analog VF signal in the RU line interface.

Figure 7.4 FWAN PCS Telephony Processing



Guide to Abbreviations

PCM Pulse Code Modulation
DS1 Digital Signal Level 1 transmission facility (1.544 Mbps)
ESF Extended Superframe signal format
PSTN Public Switched Telephone Network
LDS/IDT Local Digital Switch / TR303 Integrated Digital Terminal
NIF Network Interface Function
TDM Internal Time Division Multiplex signal
TSI Time-Slot Interchange
VTch Airlink Voice Traffic Channel (16 Kbps)
D/A Digital to Analog / Analog to Digital
GPS Global Positioning System
LD-CELP Low Delay-Codebook Excited Linear Prediction
NIC Network Interface Card
DNIF Digital Network Interface Function

7.1.6 FWAN PCS FAX/Modem VF Traffic Functions

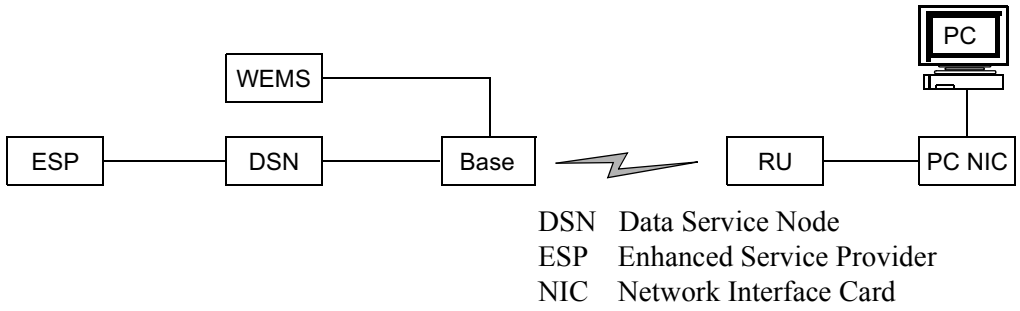
The bandwidth efficiencies of LD-CELP compression place limitations on the type of VF traffic that can transverse the airlink. For example, FAX and voice-band modem signals will not pass through LD-CELP without distortion. To eliminate this problem, both the RU and Base Station are capable of detecting the presence of these signals in the VF data. When FAX or voice-band modem data is detected, both the Base Station and RU route the VF signals to special FAX/modem demodulation-remodulation circuitry. In so doing, the Base Station accepts FAX/modem VF data from the incoming 64 kbps PCM stream and remodulate it for inclusion in the 16 kbps traffic-channel bitstream, bypassing LD-CELP compression. Consequently, the RU will demodulate this data stream and encode it as 64 kbps PCM for conversion to analog in the RU line interface, where the signals appear as voice-band FAX/modem tones. FAX/modem data sent from the RU to the Base Station follows this same process in reverse.

7.1.7 FWAN PCS High-Speed-Data Functions

In addition to telephony services, the FWAN PCS also provides customers with a connectionless packet data service to an Enhanced Service Provider (ESP). In this application, the RU serves as an IP gateway.

The High-Speed-Data (HSD) airlink provides a reliable connectionless packet-switched connection between an RU and its serving Base Station. This virtual connection supports data transfer between the customer and an ESP as well as the transfer of traffic management information between the Base Station and RU. The airlink forms one segment of the connection over which packet data travels between the customer's PC and the ESP, as depicted in Figure 7.5.

Figure 7.5 FWAN PCS HSD Architecture



HSD network elements are managed in the same fashion and utilize the same systems as the telephony NEs.

7.1.8 HSD Medium Access

A number of physical channels have been set aside for HSD services within each sector of all FWAN PCS Base Stations. The number of channels allocated for HSD services may be provisioned per Base

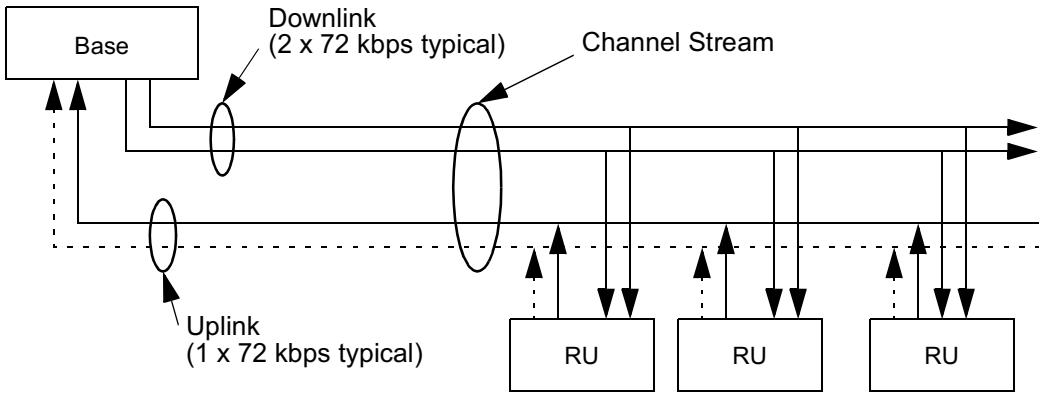
Station to accommodate the data traffic requirements within each sector or cell. This pool of physical channels is divided into groups, resulting in subsets of logical channels (or data streams) over which data transfer between the Base Station and RU may take place. The logical channels corresponding to the Base Station-to-RU airlink constitute the “downlink” and the logical channels corresponding to the RU-to-Base Station airlink constitute the “uplink.” Depending upon the data requirements in either of these two directions, the channel capacities of the two airlinks may differ.

The downlink can be considered a connectionless broadcast channel handling traffic from the Base Station to RU only (refer to Figure 7.6). Data destined for a specific RU is broadcast to the entire RU population within the Base Station sector, where it is simultaneously received and decoded by all RUs within that sector. Although all RUs receive the same data from the downlink, only the destination RU (determined by its IP address) will pass the received data up the protocol stack to the customer’s computer equipment. All other RUs will discard any received data not intended for them.

The uplink is shared among all RUs associated with a given sector on a Base Station. Access to the uplink from any RU is managed through an arbitration process administered by the Base Station. In so doing, the Base Station assists RUs in gaining access to the uplink, as well as in notifying them when contention has occurred by means of channel status indicators on the downlink.

The HSD airlink is considered a reliable transport medium for messages exchanged between an RU and its associated Base Station. This is achieved through the use of error-detection and retransmission mechanisms supported by the physical layer.

Figure 7.6 HSD Logical Channel Relationships



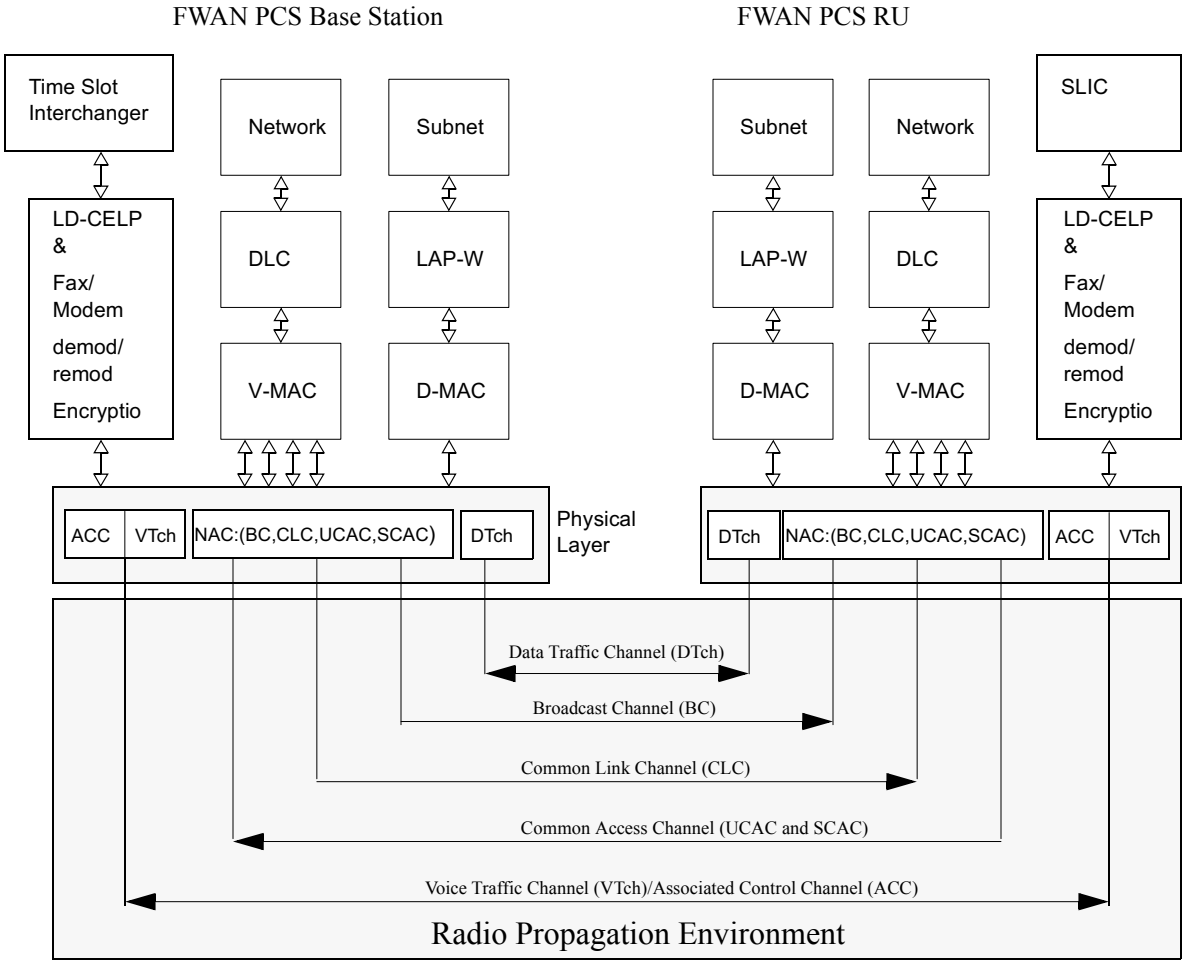
7.2 Airlink Overview

The AT&T Fixed Wireless Services FWAN PCS utilizes a proprietary airlink technology to maximize the efficient use of spectrum while providing a secure wireless interface to the WRDT. This section provides an overview of the airlink design as well as functional descriptions of the control and traffic channels.

7.2.1 FWAN PCS Physical Layer Overview

The FWAN PCS physical layer is based on an Open Systems Interconnect (OSI) layer model. Figure 7.7 depicts the application of the OSI model to the FWAN PCS airlink protocol stack.

Figure 7.7 FWAN PCS OSI Model



The physical layer is divided into six separate entities as follows:

- Voice Traffic channel entity (VTch)

- Associated Control Channel entity (ACC)
- Data Traffic channel entity (DTch)
- Common Access Channel entity (CAC)
- Common Link Channel entity (CLC)
- Broadcast Channel entity (BC)

The Voice Traffic, ACC and Data Traffic entities are the only entities that communicate on both the uplink and downlink. The remaining entities communicate on the link direction appropriate to their function.

Interactions between the physical layer and Medium Access Channel (MAC) layer entities are handled through the definition of abstract primitives that define the services provided by each layer. The primitives are passed between the physical and MAC layer entities at Service Access Points (SAPs).

7.2.1.1 Services Provided by the Physical Layer

The physical layer provides the following services to the Voice Medium Access Layer (V-MAC), Digital Medium Access Layer (D-MAC), as well as the VTch interface:

- Transmission and reception of voice and data traffic
- Transmission and reception of control information over the airlink channel between the RU and the Base Station
- Forward Error Control (FEC) and detection of messages corrupted during the transmission or reception process
- RU frame and bit-level synchronization to global time references transmitted by the serving Base Station

7.2.1.2 Associated Control Channel Functional Description

The Associated Control Channel (ACC) is a small (10%) partition within the VTch data frame which serves as the primary airlink signalling channel for voice traffic call processing. This channel exists only after a voice traffic channel has been established between the Base Station and the RU. In addition to airlink signalling, the ACC can also be used to support channel management functions such as power control and active delay compensation. Other undefined services are possible over the ACC as well.

7.2.1.3 FWAN PCS Voice Traffic Channel (VTch) Functional Description

The Voice Traffic channel (VTch) provides a circuit-switched airlink connection between the Base Station and an RU for the duration of the call. Each RU is capable of supporting up to two simultaneous VTch connections.

Each Base Station is capable of supporting between 60 and 92 VTch connections per sector. The exact number of VTch resources available that can be provisioned by a Base Station is dependent upon the size of the high-speed-data service partition. At a minimum, all Base Stations will be provisioned for

high-speed-data services as shown in Figure 7.14, where 32 FTRs are dedicated to the data service, leaving 92 resources available for voice traffic. Heavy data traffic loading in some cells may call for the Base Station to support additional data resources. In such cases, the Base Station may be provisioned to support two high-speed data service partitions (64 FTRs), leaving 60 resources available for voice traffic.

VF traffic, which appears as 64 kbps PCM to both the Base Station and RU, is compressed to a 16 kbps data stream using Low Delay-Codebook Excited Linear Prediction (LD-CELP). The LD-CELP bit stream is mapped into data symbols for transmission over the airlink using either 16-QAM or QPSK modulation.

The Radio Management Entity (RME) maintains and accounts for FTR utilization. The Base Station RME may allocate FTRs that are independent in time to maintain the RU Effective Isotropic Radiated Power (EIRP) budget. Regardless of the type of modulation in use, it is not necessary for the downlink and the uplink FTRs to be paired.

7.2.1.4 FWAN PCS Network Access Channel (NAC) Functional Description

The FWAN PCS Network Access Channel (NAC) provides a means by which calls can be set up between a Base Station and its population of RUs. Several physical layer entities utilize the NAC for the exchange of peer-peer information between the Base Station and RU over the airlink. As a result, the NAC is subdivided into logical channels, as shown in Table 7.2.

Table 7.2 NAC Logical Channel Summary

Logical Channel	Link Direction	Description
Broadcast Channel (BC)	Downlink	Base Station identification; initial RU provisioning
Common Link Channel (CLC)	Downlink	Call establishment, Base Station-to-RU
Unsolicited Common Access Channel (UCAC)	Uplink	Call establishment, RU-to-Base Station
Solicited Common Access Channel (SCAC)	Uplink	Call establishment, RU-to-Base Station in response to request from Base Station

These logical channels are defined in the following four subsections.

7.2.1.5 BC Definition

The Broadcast Channel (BC) is a point to multipoint channel between the serving Base Station and its population of RUs. The BC's main functions are to broadcast cell-wide provisional parameters, provide Base Station identification (ID), and to provision new RUs during the RU installation procedure. During normal operation, a fully provisioned RU rarely requires BC updates of any kind. The downlink BC time slots are paired with the uplink UCAC time slots. The BC is time shared with

the CLC (refer to Figure 7.8), with one BC time slot allotted for every four CLC time slots. In addition, the BC is deployed across Base Stations in a time-reuse pattern of 32 to guarantee negligible co-channel interference.

7.2.1.6 CLC Definition

The Common Link Channel (CLC) provides a downlink transmission channel used by the Base Station during call setup and access procedures. The downlink CLC time slots are paired with the uplink SCAC time slots. The CLC is time shared with the BC (refer to Figure 7.8), with four CLC time slots set aside for every one BC time slot. Because the CLC is controlled by the Base Station, it is not subject to intra-cell contention, but RUs must accept inter-cell interference.

7.2.1.7 UCAC Definition

The Unsolicited Common Access Channel (UCAC) provides an uplink access channel from any RU to its serving Base Station. Being unsolicited, the UCAC is a slotted ALOHA access channel. It is subject not only to collisions between RUs in the same cell but also to interference from RUs in co-channel cells. The uplink UCAC time slots are paired with the downlink BC time slots. The UCAC is time-shared with the SCAC, with one UCAC time slot for every four SCAC time slots (refer to Figure 7.8).

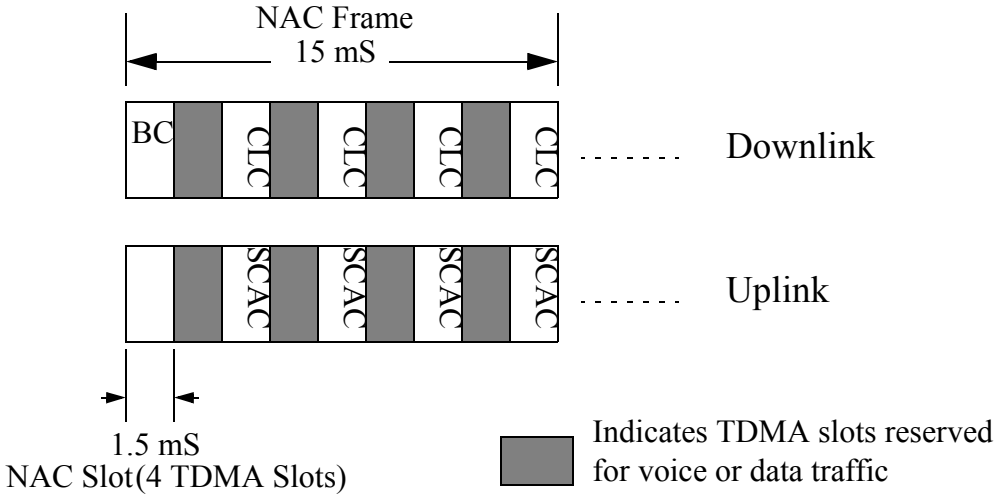
7.2.1.8 SCAC Definition

The Solicited Common Access Channel (SCAC) provides an uplink transmission channel used by an RU during call setup and channel access procedures. The uplink SCAC time slots are paired with the downlink CLC time slots. The SCAC is time-shared with the UCAC, with four SCAC time slots for every one UCAC time slot (refer to Figure 7.8).

All four NAC logical channels employ QPSK modulation.

The CLC, SCAC and UCAC logical channels are all deployed with a reuse factor of one.

Figure 7.8 NAC Logical Channel Timing Relationships



7.2.1.9 FWAN PCS Data Traffic Channel (DTch) Definition

The Data Traffic channel (DTch) referenced earlier in the FWAN PCS OSI Model (Figure 7.7) is defined as 1 of *N* downlink LDCs and 1 of *M* uplink LDCs. In other words, the number of LDC resources allocated to the DTch is dynamic according to bandwidth requirements, and the number of LDCs utilized for each direction of the link may be allocated independently.

Each Base Station is provisioned with one primary LDC allocation. Primary LDCs are distributed among cell sites in a reuse pattern of eight to minimize co-channel interference. The downlink primary LDC provides data service control functions and delivers user data at 72 kbps. The uplink primary LDC provides a multiple access, contention-based resource shared by the active RU population served by the Base Station. Currently, the maximum data rate on the uplink primary LDC is 72 kbps. Future releases of the product may support higher uplink data rates.

Higher downlink data rates are possible by dynamically recovering resources. To support this, the Base Station utilizes the resources of LDCs other than the primary to increase the downlink or uplink speed in 72 kbps increments. Since the use of LDCs other than the primary implies the potential creation of co-channel interference (due to the lower reuse factor), it would be advantageous if the Base Station had some knowledge of the interference environment at each of the RUs. Future releases of the FWAN PCS will enable RUs to provide the Base Station with information regarding their interference environment. With this knowledge, the Base Station may select additional downlink or uplink LDCs to maximize bandwidth usage while minimizing the generation of co-channel interference.

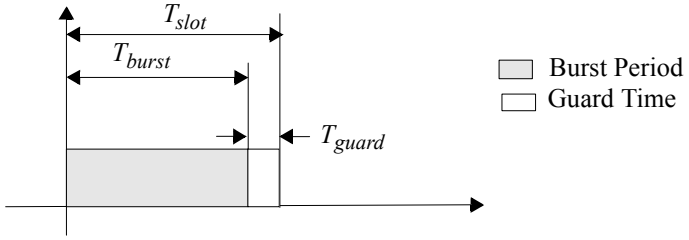
7.2.2 FWAN PCS Datalink Layer Overview

The FWAN PCS datalink is based upon an Orthogonal Frequency Division Multiplex (OFDM) transmission system. OFDM was specifically designed to counteract the adverse effects of multipath delay spread in the radio-frequency environment and to support high data rates. To accomplish this,

OFDM converts a single high-speed serial data stream into several low-speed parallel data streams for transmission across the airlink medium. At the receiving end of the airlink, the parallel data streams are recombined into a single high-speed serial data stream. By converting from high-speed serial to low-speed parallel transmission, the amount of RF energy per bit is greatly increased due to the lengthened data symbol period. In order to support parallel transmission at a high effective data rate, an OFDM signal is made up of a large group of sinusoidal carriers or "tones," each of which is phase- and amplitude-modulated to carry unique data symbol information.

OFDM compensates for the time delay spread of a multipath propagation channel by transmitting each data symbol as an RF burst, with a brief "guard interval" separating the end of each burst from the beginning of the next (refer to Figure 7.9).

Figure 7.9 Illustration of OFDM Burst Parameters

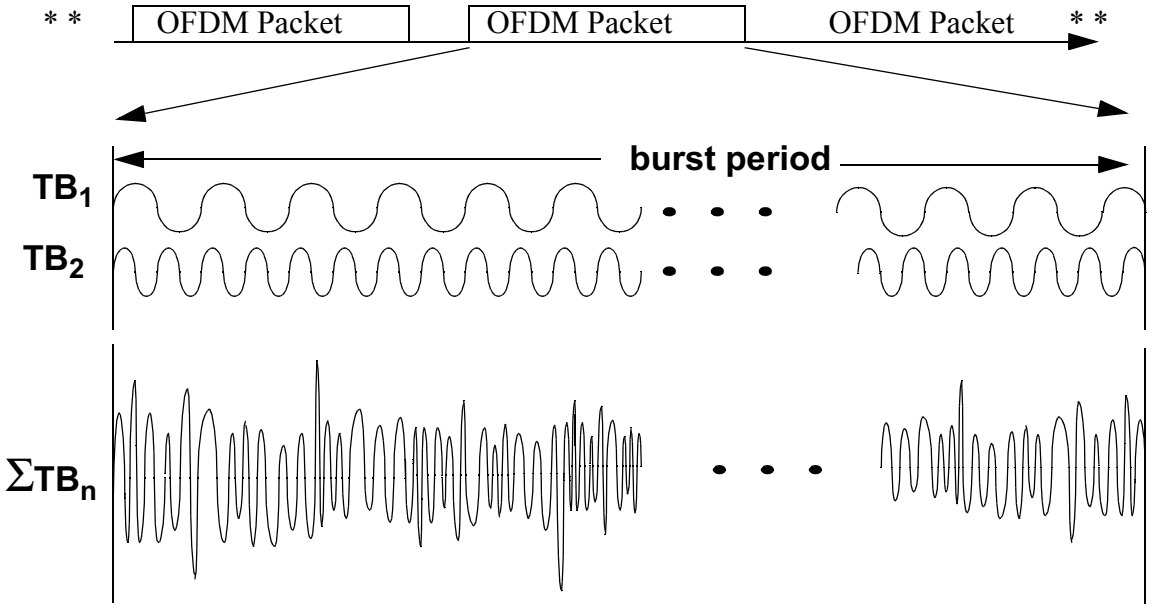


The amount of time allocated to the guard interval is sufficient to allow the channel's time-delayed multipath components to dissipate prior to the transmission of the following burst. The guard interval essentially eliminates the inter-symbol interference (ISI) common to multipath communications channels.

Although OFDM requires a large number of tones to carry data across the channel, its frequency spectrum requirements are minimized through the use of very narrow individual tone spacing. Normally, such narrow spacing would be problematic due to the nature of pulsed RF transmissions, which exhibit spectrum spreading. This spreading takes the form of a sine function, the characteristics of which are dependent upon the burst risetime and burst duration. The inter-tone (sin x/x) interference that would normally occur with narrow tone spacing is minimized in an OFDM system. This is accomplished by taking advantage of the orthogonality that exists between tones when their frequency spacing is equal to the reciprocal of the burst period. Such tone spacing greatly minimizes the effects of inter-tone (sin x/x) interference if the receiver window is properly synchronized with the transmitted OFDM bursts.

Once all the active frequency-domain tones have been generated for a burst, these tones are transferred to the time domain using an Inverse Fast Fourier Transform (IFFT). The resulting OFDM time-domain waveform is simply a summation of the phase and amplitude components associated with each active tone during the burst period (refer to Figure 7.10). Following the execution of an IFFT, a cyclic prefix is added to the time domain signal samples, and the samples are filtered. The filtered digital samples are converted to analog signals, which are then converted to the operating frequency for transmission over the airlink.

Figure 7.10 OFDM Time-Domain Waveform Generation

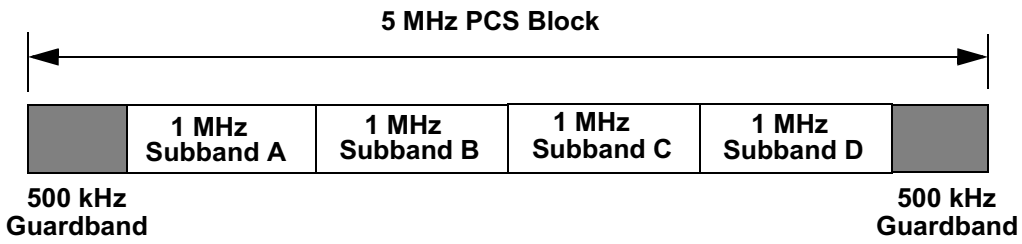


At the receiver, the incoming analog signal is converted to digital samples, which are then transferred from the time-domain to the frequency-domain using a Fast Fourier Transform (FFT). The resulting OFDM tones are demodulated and their data passed on to the appropriate physical layer entities.

7.2.2.1 FWAN PCS Implementation of OFDM

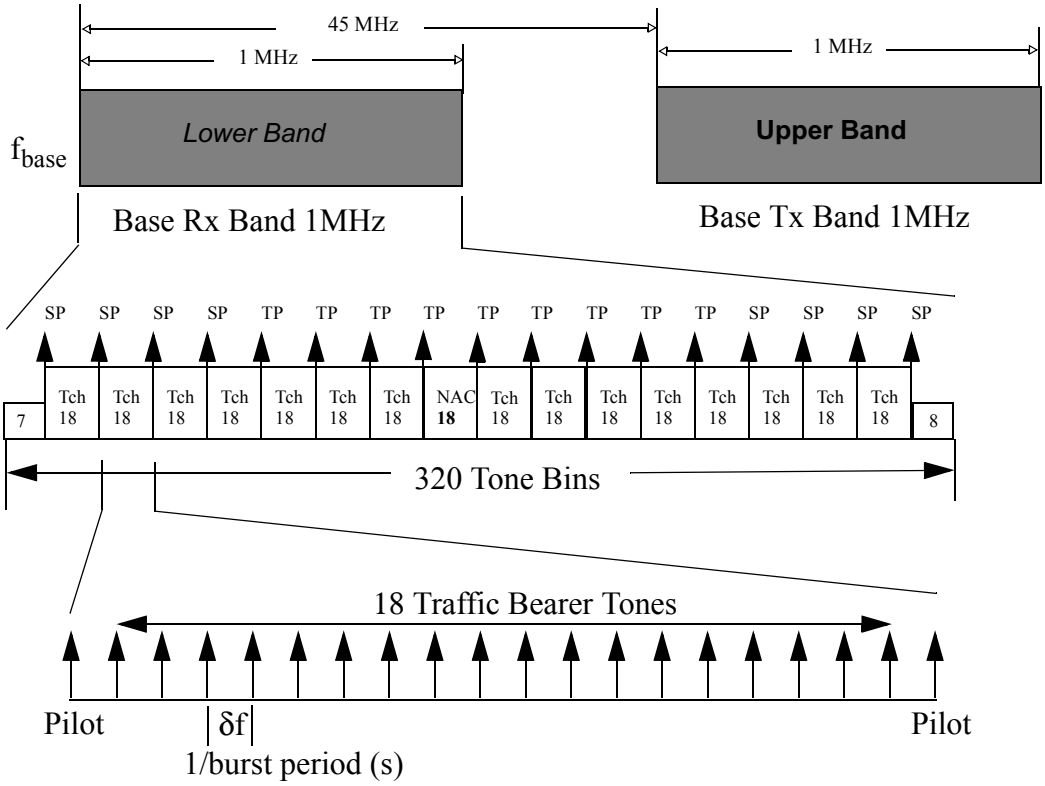
The communications link between the Base Station and its RU population takes place in a Frequency-Division Duplex (FDD) RF environment, with 80 MHz of spacing between the Base Station downlink and the RU uplink transmissions. The FWAN PCS system is designed to operate in the United States wideband PCS spectrum defined in Part 24 of the Federal Communications Commission (FCC) regulations. Cells in the FWAN PCS are divided into four sectors, with each sector utilizing 1 MHz of downlink and 1 MHz of uplink spectrum. The individual 1 MHz segments associated with each sector are known as subbands. The allocation of these subbands within a 5 MHz PCS frequency block is depicted in Figure 7.11.

Figure 7.11 FWAN PCS Subband Allocation



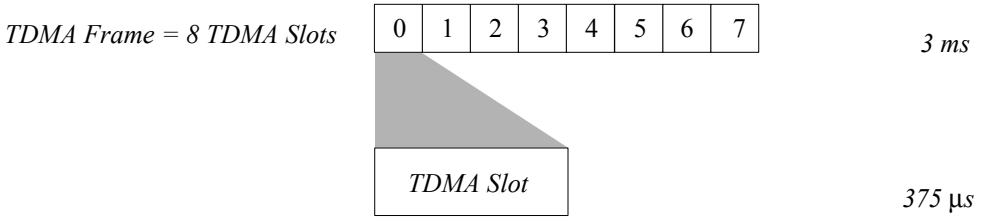
The FWAN PCS utilizes a total of 320 OFDM tones per 1 MHz subband on both the downlink and uplink. Of the 320 available tones, 16 clusters of 18 tones each are allocated in the frequency domain as airlink Frequency Division Multiple Access (FDMA) slots (refer to Figure 7.12). Each FDMA slot is delineated by the presence of a synchronization pilot tone on each side of the slot, bringing the total number of energized tones to 305. The remaining 15 OFDM tones in the 320-tone suite are not energized; they represent the first seven tones at the low frequency end of the subband and eight tones at the high end. The allocation of tones is identical between the uplink and downlink.

Figure 7.12 FWAN PCS FDMA Structure



Dividing the 1 MHz subband into 16 FDMA slots is an effective means of providing multiple access in the frequency domain. However, the capacity of the FWAN PCS would be insufficient if this were the only multiple access method utilized. Consequently, Time Division Multiple Access (TDMA) is utilized as well, where each of the 16 FDMA slots are divided into eight TDMA slots (refer to Figure 7.13).

Figure 7.13 FWAN PCS TDMA Framing Structure



The datalink resources derived from this process are most easily visualized in terms of a matrix, with 16 FDMA slots along the x-axis and eight TDMA slots along the y-axis, resulting in a total of 128 Frequency-Time Resources (FTRs) for allocation in each datalink subband.

In an OFDM system, the modulation format for any given tone is entirely independent of that used by its neighbor(s). The FWAN PCS datalink takes advantage of this and will utilize either Quadrature Phase Shift Keying (QPSK) or 16 Quadrature Amplitude Modulation (16-QAM) within individual FTRs on an as-needed basis.

The basic FWAN PCS parameter values are summarized in Table 7.3.

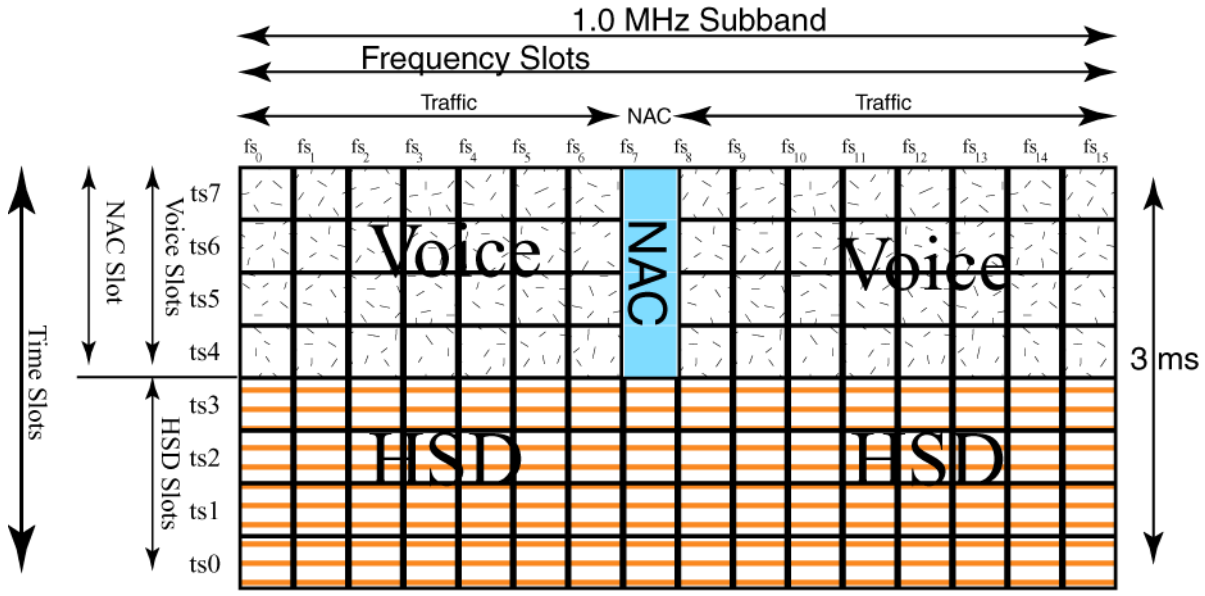
Table 7.3 Basic FWAN PCS OFDM Parameters

FWAN PCS OFDM Parameter	Value
Burst Period	340-µs
Guard Time	35-µs
TDMA Time Slot Period	375-µs
TDMA Frame Period	3-ms (Eight 375-µs TDMA time slots)
Subband Size	1 MHz
Total Number of OFDM Tones	320 per subband
Number of Energized OFDM Tones	305 per subband
Tone Spacing	3.125 KHz
Frequency Slot (FDMA slot) Size	56.25 KHz (18 adjacent tones)
Total Number of Frequency-Time Resources (FTRs)	128 per subband
Tone Modulation Formats Supported	QPSK, 16-QAM

7.2.2.2 FWAN PCS Datalink Layer Resource Allocation

The 16 x 8 FTR matrix described in the previous section provides a total of 128 potential resources for the datalink. However, datalink control overhead and the specialized needs of packet-switched data services consume a fixed portion of these resources. Figure 7.14 depicts the allocation of subband resources in the FTR matrix by function.

Figure 7.14 FWAN PCS Datalink Layer Resource Matrix



7.2.2.3 FWAN PCS High-Speed-Data Services

High-speed-data services are supported over a group of 32 dedicated FTRs in each subband known as a Basic Data Service Allocation (BDSA). All Base Stations are provisioned for at least one BDSA. Table 7.4 shows the default location of the BDSA in the resource matrix. If required, a Base Station can be provisioned for a second BDSA, which by convention will utilize TDMA slots two and three across all 16 FDMA slots.

Each BDSA is subdivided into eight clusters of four FTRs which form a Logical Data Channel (LDC) or "data quad." Each LDC supports an airlink data rate of 72 kbps (refer to Table 7.4)

Table 7.4 Basic Data Service Allocation

	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
T3	1a	1c	2a	2c	3a	3c	4a	4c	5a	5c	6a	6c	7a	7c	8a	8c
T2	1b	1d	2b	2d	3b	3d	4b	4d	5b	5d	6b	6d	7b	7d	8b	8d
T1	1a	1c	2a	2c	3a	3c	4a	4c	5a	5c	6a	6c	7a	7c	8a	8c
T0	1b	1d	2b	2d	3b	3d	4b	4d	5b	5d	6b	6d	7b	7d	8b	8d

72 kbps Logical Data Channel (LDC)

7.2.2.4 FWAN PCS Data Traffic Channel (DTch) Definition

The Data Traffic channel (DTch) referenced earlier in the FWAN PCS OSI Model (Figure 7.7) is defined as 1 of *N* downlink LDCs and 1 of *M* uplink LDCs. In other words, the number of LDC resources allocated to the DTch is dynamic according to bandwidth requirements, and the number of LDCs utilized for each direction of the link may be allocated independently.

Each Base is provisioned with one primary LDC allocation. Primary LDCs are distributed among cell sites in a reuse pattern of eight to minimize co-channel interference. The downlink primary LDC provides data service control functions and delivers user data at 72 kbps. The uplink primary LDC provides a multiple access, contention-based resource shared by the active RU population served by the Base. Currently, the maximum data rate on the uplink primary LDC is 72 kbps. Future releases of the product may support higher uplink data rates.

Higher downlink data rates are possible by dynamically recovering resources. To support this, the Base will utilize the resources of LDCs other than the primary to increase the downlink or uplink speed in 72 kbps increments. Since the use of LDCs other than the primary implies the potential creation of co-channel interference (due to the lower reuse factor), it would be advantageous if the base had some knowledge of the interference environment at each of the RUs. Future releases of the FWAN PCS will enable RUs to provide the Base with information regarding their interference environment. With this knowledge, the Base may select additional downlink or uplink LDCs to maximize bandwidth usage while minimizing the generation of co-channel interference.

7.2.2.5 High-Speed Data Medium Access Control

Although the Digital Medium Access Control (D-MAC) is not part of the FWAN PCS physical layer, it is briefly described here in order to differentiate the access method used for packet-switched data services from that employed for circuit-switched voice traffic.

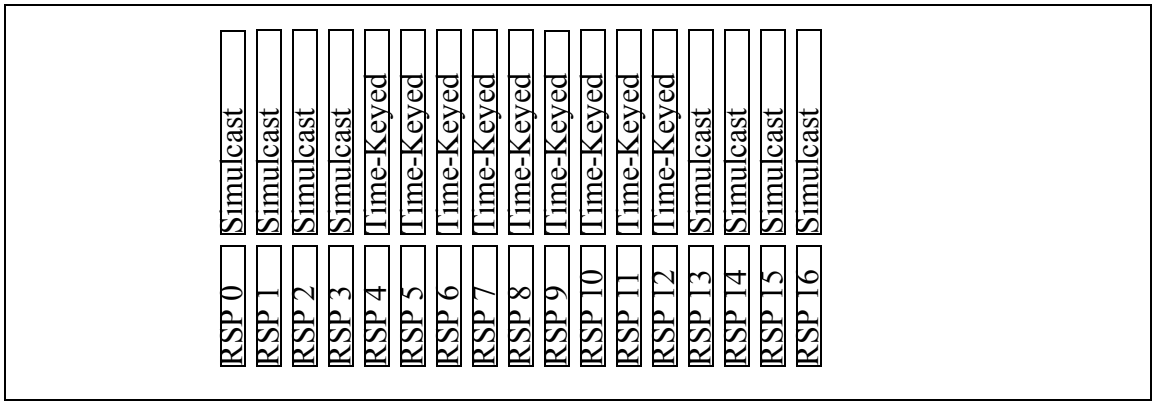
The D-MAC method used for the uplink is a variant of the Digital Sense Multiple Access with Collision Detection (DSMA/CD) scheme. DSMA/CD provides contention control through the use of two flags that signal the status of the uplink. These status flags are broadcast on the downlink at specified intervals. One status flag indicates whether the reverse channel is idle or busy, and the other indicates packet decoding success or failure. This scheme allows the RU population to not only recognize when the reverse channel is idle or busy, but it also allows the RUs to determine whether or not a transmission was successfully decoded. For example, a channel status flag of busy followed by a decode failure status flag indicates that channel contention took place, and the RUs that transmitted should back off a random amount of time before a retransmission is attempted.

7.3 Network Synchronization

Time and frequency synchronization is extremely important to the proper operation of an OFDM system. Consequently, the airlink supports a means by which RUs can maintain constant frequency synchronism with the Base Station.

The Base Station RF signal contains 17 Remote Synchronization Pilots (RSPs), which are used to provide frequency transfer across the airlink (refer to Figure 7.15). Of the 17 RSPs, the outside eight are transmitted continuously by all Base Stations (simulcast) and nine are transmitted in a time-keyed manner. The inner nine RSPs are time-keyed to be energized only during the CLC frames that correspond to the Base Station Offset Code (BSOC). For example, if the BSOC is 02, the time-keyed RSPs will be energized during the NAC frame containing

Figure 7.15 RSP Definitions



BC time slot 02 and its four subsequent CLC slots. The time-keyed RSPs will remain inactive during the remaining 31 NAC frames. The presence of the time-keyed RSPs is used to direct the receiving RU to the correct broadcast frame boundary for the serving Base Station. Regardless of whether an RSP is simulcast or time-keyed, each pilot is assigned a fixed amplitude and phase component, the parameters of which are identical between all Base Stations and are selected to minimize the overall peak-average ratio of the transmitted bursts.

All Base Stations obtain their frequency references from an internal clock which is disciplined by a Global Positioning System (GPS) receiver. The use of GPS assures a minimal frequency offset between Base Stations, which is essential for minimizing co-channel beat-note interference.

The RU is also capable of generating a variant of the Base Stations' RSP tones known as Delay Compensation Pilots (DCPs). DCPs occupy the same relative positions in the baseband signal as RSPs, however, they are only transmitted upon request by the Base Station. The Base Station can direct a specific RU to energize its DCPs for the purpose of verifying proper time delay (time-of-flight) compensation.

Chapter 8 Parts List/Tune Up Information

Overview

This section includes the FWAN PCS Base Station parts list and tune up information.

Contents

8.1 Parts List

Table 8.1 List of FWAN PCS Base Station Active Components

Assembly	Part #	Description	Ref Des	Schematic
ASY2147001		PCS, B1.5, PCS, V0.9		XCVR
ASY2147001	IXC1135717	IC, RF, Freq, Synth, 550MHz, TSSOP16	U36, U40	XCVR
ASY2147001	ICX1040611	IC, Logic, Inv, 74AC04, SOIC14	U9	XCVR
ASY2147001	ICS1053009	IC, Analog, Vreg,50MA, SOT23-5	U39, U43	XCVR
ASY2147001	XTR1132714	XTR, NPN, Bipolar, SOT23	Q1	XCVR
ASY2147001	ICX1135818	IC, RF, Freq, Synth, 3.0 GHz, TSSOP16	U45, U46	XCVR
ASY2147001	MAG1076014	XFMR,3-5MHz,5MA,4:1, AT244	T1	XCVR
ASY2147001	MAG1135919	XFMR,Balun,3.5-7.0MHz, B4F	T2	XCVR
ASY2147001	ICX1140006	IC, RF, MMIC, GAAS, MW-6	U42	XCVR
ASY2147001	OSC1140915	RFM, RF OSC, VCO, 1640 MHz, 3.3V	Y4	XCVR
ASY2147001	OSC1140814	RFM, RF OSC, VCO, 1720MHz, 3.3V	Y5	XCVR
ASY2147001	XTR114815	XTR, PNP, Driver, SOT23	Q2, Q3, Q4, Q5	XCVR
ASY2147001	ICX1183114	IC, Analog, OP-AMP, Single, 800MHz, SOIC8	U41	XCVR
ASY2147001	ICX1187118	IC, Logic, DRVR, 74ACT244, SSOP20	U58	XCVR
ASY2147001	ICX1188220	IC, Analog, DAC, 12Bit SOIC28	U38	XCVR
ASY2147001	ICX1188321	IC, Analog, OP-AMP, Single, SOIC8	(U11), U6, U18	XCVR
ASY2147001	ICX1200104	IC, Analog, CMOS, OP_AMP, SOT23-5	U7, U8	XCVR
ASY2147001	OSC1195723	RFM, RF OSC, VCO, 233.15MHz, 3.0V	Y2, Y3	XCVR
ASY2147001	ICX1198928	IC, Analog, Sngl, OP-AMP, SOIC8	U1	XCVR
ASY2147001	ICX1215312	IC, Analog, SMT, 32MHz, VCXO	Y1	XCVR

Table 8.1 List of FWAN PCS Base Station Active Components

Assembly	Part #	Description	Ref Des	Schematic
ASY2147001	ICX1255316	Analog, Low Dropout Adj., VREG, 5V-20V, 1A, TO-263	U33	XCVR
ASY2147001	ICX1512702	Logic, DRVR, 3ST, 74LVC244, SOICW20	U59, U60	XCVR
ASY2147001	ICX1523304	Logic, Gate, AND, Quad 2-IN 74ACT08, -40/+85C, SO14	U30	XCVR
ASY2147001	RFM1667907	AMplifier, MMIC, 3GHz, BW, 8dBM, P1DB, SOT-363	U24,U25,U28,U54, U56, U57	XCVR
ASY2147001	RFM1659103	RFM, AMP, .1-6MHz, 3V, 17dBM, SOT-363	U35,U47,U48,U49, U50, U52, U55	XCVR
ASY2147001	RFM1670108	RFM, Isolator, 2.5W, 1850-1910MHz, SMT	AT5	XCVR
ASY2147001	RFM1670204	RFM, Isolator, 2.5W, 1930-1990MHz, SMT	AT6	XCVR
ASY2147001	RFM1670001	RFM, Ceramic, Band Pass Filter, 4 Pole, 1960MHz	FL4, FL5	XCVR
ASY2147001	RFM1670407	RFM,MMIC,DBMixer,IF AMP, 5GHz, SOIC8	U29, U44, U53	XCVR
ASY2147001	RFM1670300	Attentuator, 31dB, 5 Bit, 1dB Step w/Driver, SOIC16	AT2, AT3	XCVR
ASY2147001	RFM1671907	RFM,Attenuator,.007TCA, 6dB, Negative Shifting	AT7	XCVR
ASY2147001	RFM1710204	Amplifier, MMIC, 2GHz BW,+18.5dBGain,SOP-16	U51	XCVR
ASY2147001	RFM19097105	RFM, Filter, IF SAW, 240MHz 15.9MM, Metal, SMT	FL3, FL6	XCVR
ASY2147001	RFM1907308	RFM, Filter, IF SAW, 242MHz 15.99MM, Metal, SMT	FL1, FL2	XCVR
ASY1995010		ASY, EPLD PLL, 042000, B1.5 XCVR V 0.7	U3	XCVR
ASY1995010	ICX169740	EPLD, 3.3V, ISP, PQFP44	EMP7032AETC44-10 Altera	XCVR
ASY2030705		ASY, EPLD, SPI 052400, B1.5 XCVR, V 0.7	U32	XCVR
ASY2030705	ICX172070	EPLD, 3.3V, 12NS, PQFP144	EMP7512AETC114-12 Altera	XCVR

Table 8.1 List of FWAN PCS Base Station Active Components

Assembly	Part #	Description	Ref Des	Schematic
ASY2084500		ASY,EPLDDATA,081000, B1.5 XCVR	U31	XCVR
ASY2084500	ICX172070	EPLD, 3.3V, 12NS, PQFP144	EMP7512AETC114-12 Altera	XCVR
ASY2084500	PCB2057704	PCB, B1.5 XCVR, PCS, V0.8	PCB1	XCVR
ASY2084500	ICX1029719	IC, Logic, FET, 2:01 74CBT3257, SOIC16	U16	XCVR
ASY2084500	ICX1246518	IC, Logic, D-Type, Flip-Flop, 74ACT74, SOIC14	(U13)	XCVR
ASY2084500	ICX1081212	IC, Logoc, Gate, NAND 74ACT00, SOIC14	U12	XCVR
ASY2084500	ICX1246417	IC,Logic,SyncBinaryCntr, 74ACT163, SOIC16	(U14), (U2)	XCVR
ASY2084500	ICX1629009	EEPROM, 8KX8Bit, w/Blk Lck, 2.5-5.5V, -40/+85C, SOI4	U34	XCVR
ASY2084500	ICX1514709	Logic, Multivibrtr, w/Reset, -55/+125C, SOI6	U4, U26	XCVR
ASY2084500	ICX1527702	Logic, XCVR, 18Bit, 3.3V, -40/+85C, TQFP64	U20, U21, U22, U23	XCVR
ASY2084500	ICX1711500	Analog, Dual OP-AMP, Dual Comp, ADJ Ref, SOP16	U10	XCVR
ASY2084500	ICX1697508	Analog, A/D Converter, 12Bit, 10MSPS, SOIC28	U37	XCVR
ASY2084500	ICX1700300	UP Supervisory Circuit, +3V Volt Monitoring, SO8	U27	XCVR
ASY2084500	ICX1744908	Logic, Quad Buffer, 3.3V, Tri State, High OE, SOIC14	U19	XCVR
ASY2084500	ICX1843509	Analog,Comp,Single,7NS, Ultra Fast, SOIC-8	U5, U17	XCVR
ASY2084500	ICX1805605	Analog, LDO Reg, 3.3V, 150MA, SOT23	U15	XCVR
ASY2303610		PCA,SBC,V0.71		SBC
ASY2303610	ICX1257116	IC, PLD, PRGBL CPLD 36 MACRO., 5NS, VQ 1		SBC
ASY2152907		ASY,HPI MUX PLD,SBC V0.6 ,102600		SBC

Table 8.1 List of FWAN PCS Base Station Active Components

Assembly	Part #	Description	Ref Des	Schematic
ASY2152907	ICX1707105	CPLD,3.3V,7.5NS,72 MACRO ,HIGH SPEED,V 1		SBC
ASY2152907	ICX1698506	FLASH,2.7V,512KX8,4MB IT, NON-VOLATILE, 1		SBC
ASY2152907	ICX1698506	FLASH,2.7V,512KX8,4MB IT, NON-VOLATILE, 1		SBC
ASY2152907	ICX1698506	FLASH,2.7V,512KX8,4MB IT, NON-VOLATILE, 1		SBC
ASY2152907	ASY2250307	ASY,BUS CONTROL EPLD, 03/16/01,SBC		SBC
ASY2152907	ICX1837801	CPLD,PRGRMBL,3.3V,7.5 NS, 0/+70C,TQFP14 1		SBC
ASY2250510		ASY,SMP,LATCH PLD, 03/ 16/01,SBC		SBC
ASY2250510	ICX1707105	CPLD,3.3V,7.5NS,72 MACRO ,HIGH SPEED,V 1		SBC
ASY2250510	CRY1533802	CRYSTAL,20MHZ,-40/ +85C, SMT,SERIES RES 2		SBC
ASY2250510	ICX1014511	IC, LOGIC, INV, 74F04, SOIC14	(U17), U8	SBC
ASY2250510	ICX1051815	IC,LOGIC,GATE,OR,74LC X32 SOIC14	U41	SBC
ASY2250510	ICX1075922	IC,LOGIC,CLK/ DRVR,1:10 74FCT3807,QSOP2 8		SBC
ASY2250510	ICX1117010	IC,ANALOG,HEX INVERTER 74AC14SC,SOIC14 2		SBC
ASY2250510	ICX1155113	IC.LOGIC,XCVR,DIFF BUS LO-SWING,SO8	(U3), (U4), U1, U2	SBC
ASY2250510	ICX1196118	IC,LOGIC,BACKPLANE XCVR/ARBTR,1394,TQF 1		SBC
ASY2250510	ICX1216212	IC,LOGIC,INV,3V,74LCX0 4 SOIC14	U58, U65, U66, U68, U69, U70	SBC
ASY2250510	ICX1221107	IC,ANALOG,3.3V ECONO RESET,SOT-223		SBC
ASY2250510	ICX1255114	LOGIC,XCVR/REG,18 BIT 3.3V,74LVTH18646 4		SBC

Table 8.1 List of FWAN PCS Base Station Active Components

Assembly	Part #	Description	Ref Des	Schematic
ASY2250510	ICX1256216	LOGIC,BFR/ DRVR,3ST,3.3V 74LVTH244A,SSO 4		SBC
ASY2250510	ICX1512702	LOGIC,DRVR,3ST,74LVC244, SOICW20	U57	SBC
ASY2250510	ICX1581900	UP,MICROMONITOR,3.3V, -40/+85C,SO8		SBC
ASY2250510	ICX1627707	DSP,2.5/3.3V,16BIT,64K, -40/+85C,100MH 18		SBC
ASY2250510	ICX1629009	EEPROM,8KX8BIT,W/ BLK LCK 2.5-5.5V,-40/ 1		SBC
ASY2250510	ICX1667500	ANALOG,LDO REG,1.8V, 150MA,SOT23		SBC
ASY2250510	ICX1688902	SRAM,64KX16,10NS,3.3V, 48PIN,UBGA	U27, U29, U31, U33, U41, U43, U45, U47, U59, U61, U63, U65, U76, U78, U80, U82, U115, U117, U119, U121, U125, U127, U129, U131, U136, U138, U140, U142, U144, U146, U148, U150	SBC
ASY2250510	ICX1697209	HEX BUFFERS/DRIVERS WITH OPEN-DRAIN OU 5		SBC
ASY2250510	ICX1697305	TRANSVR,EIA232,3.0-5.5V, LOW POWER,SO1 1		SBC
ASY2250510	ICX1700300	UP SUPERVISORY CIRCUIT, +3V VOLT MONIT 2		SBC
ASY2250510	ICX1700407	LOGIC,HEX INVERTER,3.3V, WITH OPEN DRA 3		SBC
ASY2250510	ICX1700503	LOGIC,XCVR,10-BIT ADDRS SCAN PORT,3.3V 1		SBC
ASY2250510	ICX1700610	LOGIC,QUAD BUFFER,3.3V, W/3-STATE OUTP 3		SBC
ASY2250510	ICX1711009	LOGIC,XCVR,10BASE-T,3.3V ,0/+70,ETHERN 2		SBC

Table 8.1 List of FWAN PCS Base Station Active Components

Assembly	Part #	Description	Ref Des	Schematic
ASY2250510	ICX1712509	FLASH,64MEG,4MX16BI T,3V, 90NS,-40/+85, 4		SBC
ASY2250510	ICX1713304	LOGIC,BFR/CLK DRVR,3.3V, DUAL 1:5,0/ +7 12		SBC
ASY2250510	ICX1736702	IC,ANALOG,PWR SUPPLY, HOT SWAP,MANAGER 1		SBC
ASY2250510	ICX1736905	IC,ANALOG,DC-DC CONV, 600KHZ,POWER BOO 1		SBC
ASY2250510	ICX1739803	IC,LOGIC,RCVR,3.3,LVD S, QUAD,SOIC16		SBC
ASY2250510	ICX1744908	LOGIC,QUAD BUFFER,3.3V, TRI STATE,HIGH 6		SBC
ASY2250510	ICX1752900	SIGNAL PROCESSING MODULE ,CUSTOM ASIC		SBC
ASY2250510	ICX1769704	FPGA,2.5V,VIRTEX,150K GATES,0/+85C, BG 1		SBC
ASY2250510	ICX1770304	PROM,OTP,SERIAL,3.3V, HIGH DENSITY,PLC 0		SBC
ASY2250510	ICX1805605	ANALOG,LDO REG,3.3V, 150MA,SOT23	U30	SBC
ASY2250510	ICX1897603	LOGIC,XCVR,18BIT,3.3V, -40/+85C,TSSOP6 14		SBC
ASY2250510	ICX2035005	IC,ZERO DLY CLK BUFFER 5 OUT,3.3V		SBC
ASY2250510	ICX2084408	LOGIC,BUS LINK-LAYER, 3.3V,IEEE1394,SQ 1		SBC
ASY2250510	ICX2290606	POWERQUICC,MPU,50 MHZ, -40/+85C,PBGA35 2		SBC
ASY2250510	ICX2297208	SDRAM,4M X 16BIT X 4 BANK,0/+70C,7.5NS 4		SBC
ASY2250510	OSC1817401	OSC,HCMOS,32.000MHZ, 3.3V ,50PPM,SMT		SBC
ASY2250510	OSC1893401	OSC,HCMOS,16.384MHZ, 3.3V,100PPM,SMT	Y1	SBC
ASY2250510	OSC1897105	OSC,HCMOS,10.000MHZ, 3.3V,-40/+85,SMT	Y3	SBC

Table 8.1 List of FWAN PCS Base Station Active Components

Assembly	Part #	Description	Ref Des	Schematic
ASY2250510	PWR1215413	PWR,DC-DC CONV,48V NOM 20W,F61		SBC
ASY2250510	PWR1737403	PWR,DC-DC CONV,50W, 2.5V OUT,3.3 V OUT 1		SBC
ASY2250510	PWR1806402	PWR,DC-DC CONV,25W, 2.5V OUT		SBC
ASY2250510	XTR1998107	XTR,HEXFET,100 V,16 A TO252AA	Q2, Q3	SBC
ASY2250510	PCB2037407	PCB,SBC,V0.7		SBC
ASY2250510	ICX1257116	IC, PLD, PRGBL CPLD 36 MACRO., 5NS, VQ 1		SBC
ASY2250510	ICX1698506	FLASH,2.7V,512KX8,4MB IT, NON-VOLATILE, 1		SBC
ASY2303407		PCA,BCP,V0.71		BCP
ASY2303407	ICX1257116	IC, PLD, PRGBL CPLD 36 MACRO., 5NS, VQ 1		BCP
ASY2303407	ICX2009203	CPLD,PRGRMBL,3.3V,10 NS, 0/+70C,TQFP100 1		BCP
ASY2214805		ASY,BCPM,BT,R1.58 R158BPMB1040101		BCP
ASY2214805	ICX1698506	FLASH,2.7V,512KX8,4MB IT, NON-VOLATILE, 1		BCP
ASY2215408		ASY,BCPS,BT,R1.58,UPPE R R158BPSB104010 1		BCP
ASY2215408	ICX1698506	FLASH,2.7V,512KX8,4MB IT, NON-VOLATILE, 1		BCP
ASY2216000		ASY,BCPS,BT,R1.58,LOW ER R158BPSB104010 1		BCP
ASY2216000	ICX1698506	FLASH,2.7V,512KX8,4MB IT, NON-VOLATILE, 1		BCP
ASY2256210		ASY,BCP SMP LATCH PLD, 033001,BCP V0.7 1		BCP
ASY2256210	ICX1714601	CPLD,3.3V,10NS,288 MACRO ,0/+70,TQFP14 1		BCP
ASY2256210	CRY1533802	CRYSTAL,20MHZ,-40/ +85C, SMT,SERIES RES 2		BCP
ASY2256210	ICX1014511	IC, LOGIC, INV, 74F04, SOIC14	(U17), U8	BCP
ASY2256210	ICX1051815	IC,LOGIC,GATE,OR,74LC X32 SOIC14		BCP

Table 8.1 List of FWAN PCS Base Station Active Components

Assembly	Part #	Description	Ref Des	Schematic
ASY2256210	ICX1075922	IC,LOGIC,CLK/ DRVR,1:10 74FCT3807,QSOP2 7		BCP
ASY2256210	ICX1117010	IC,ANALOG,HEX INVERTER 74AC14SC,SOIC14 6		BCP
ASY2256210	ICX1155113	IC.LOGIC,XCVR,DIFF BUS LO-SWING,SO8	(U3), (U4), U1, U2	BCP
ASY2256210	ICX1196118	IC,LOGIC,BACKPLANE XCVR/ARBTR,1394,TQF 1		BCP
ASY2256210	ICX1212208	IC,ANALOG,REG,LDO-VAR SOIC8	U71	BCP
ASY2256210	ICX1216212	IC,LOGIC,INV,3V,74LCX0 4 SOIC14	U58, U65, U66, U68, U69, U70	BCP
ASY2256210	ICX1216313	IC,LOGIC,GATE,AND,3V 74LCX08,SOIC14	U60	BCP
ASY2256210	ICX1255114	LOGIC,XCVR/REG,18 BIT 3.3V,74LVTH18646 2		BCP
ASY2256210	ICX1512702	LOGIC,DRVR,3ST,74LVC2 44, SOICW20	U57	BCP
ASY2256210	ICX1629009	EEPROM,8KX8BIT,W/ BLK LCK 2.5-5.5V,-40/ 1		BCP
ASY2256210	ICX1680704	LOGIC,PCI BUS MSTR,32BIT ,33MHZ,I/O AC 1		BCP
ASY2256210	ICX1697209	HEX BUFFERS/DRIVERS WITH OPEN-DRAIN OU 1		BCP
ASY2256210	ICX1697305	TRANSVR,EIA232,3.0-5.5V, LOW POWER,SO1 1		BCP
ASY2256210	ICX1700407	LOGIC,HEX INVERTER,3.3V, WITH OPEN DRA 3		BCP
ASY2256210	ICX1700503	LOGIC,XCVR,10-BIT ADDRS SCAN PORT,3.3V 1		BCP
ASY2256210	ICX1700610	LOGIC,QUAD BUFFER,3.3V, W/3-STATE OUTP 6		BCP
ASY2256210	ICX1710705	IC,UP,HDLC CONTROLLER, 0/70,128 CHANNE 1		BCP

Table 8.1 List of FWAN PCS Base Station Active Components

Assembly	Part #	Description	Ref Des	Schematic
ASY2256210	ICX1711009	LOGIC,XCVR,10BASE-T,3.3V ,0/+70,ETHERN 2		BCP
ASY2256210	ICX1712509	FLASH,64MEG,4MX16BIT,3V, 90NS,-40/+85, 2		BCP
ASY2256210	ICX1736702	IC,ANALOG,PWR SUPPLY, HOT SWAP,MANAGER 1		BCP
ASY2256210	ICX1736905	IC,ANALOG,DC-DC CONV, 600KHZ,POWER BOO 1		BCP
ASY2256210	ICX1744908	LOGIC,QUAD BUFFER,3.3V, TRI STATE,HIGH 2		BCP
ASY2256210	ICX1805605	ANALOG,LDO REG,3.3V, 150MA,SOT23	U30	BCP
ASY2256210	ICX1876105	LOGIC,LRG DGTL SWTCH,3V, PBGA120		BCP
ASY2256210	ICX1876607	LOGIC,FET,16BIT,2:1,MUX/ DEMUX,74CBT16 1		BCP
ASY2256210	ICX1895607	FLASH,64MBIT,3V,120NS, TSOP56	(U48), (U49)	BCP
ASY2256210	ICX1897603	LOGIC,XCVR,18BIT,3.3V, -40/+85C,TSSOP6 14		BCP
ASY2256210	ICX1898206	EPROM,CONFIG DEVICE FOR APEX FPGA,3.3- 0		BCP
ASY2256210	ICX1909207	IC,UP SUPERVISORY CIRCT, DUAL VOLT MNT 1		BCP
ASY2256210	ICX1909303	IC,UP SUPERVISORY CIRCT, TRIPLE VOLT M 1		BCP
ASY2256210	ICX1952205	FPGA,2.5V,10K130,130K GATES,BGA356		BCP
ASY2256210	ICX2084408	LOGIC,BUS LINK-LAYER, 3.3V,IEEE1394,SQ 1		BCP
ASY2256210	ICX2102307	SDRAM,512KX32BITX4,6 NS, 0/+70,TSOP86	U28	BCP
ASY2256210	ICX2290606	POWERQUICC,MPU,50 MHZ, -40/+85C,PBGA35 2		BCP
ASY2256210	ICX2297208	SDRAM,4M X 16BIT X 4 BANK,0/+70C,7.5NS 2		BCP

Table 8.1 List of FWAN PCS Base Station Active Components

Assembly	Part #	Description	Ref Des	Schematic
ASY2256210	OSC1893401	OSC,HCMOS,16.384MHZ, 3.3V,100PPM,SMT	Y1	BCP
ASY2256210	OSC1897105	OSC,HCMOS,10.000MHZ, 3.3V,-40/+85,SMT	Y3	BCP
ASY2256210	PWR1926202	PWR,DC-DC CONV,75W,3.3V, HALF-BRICK,TH 0		BCP
ASY2256210	XTR1998107	XTR,HEXFET,100 V,16 A TO252AA	Q2, Q3	BCP
ASY2303503		PCA,SMP,V0.71		SMP
ASY2303503	ICX1257116	IC, PLD, PRGBL CPLD 36 MACRO., 5NS, VQ 1		SMP
ASY2303503	ICX1698506	FLASH,2.7V,512KX8,4MB IT, NON-VOLATILE, 1		SMP
ASY2250200		ASY,EPLD,SPI/TDM, 031501,SMP		SMP
ASY2250200	ICX2187204	CPLD,3.3V,7 NS 288 MACRO,0/+70,TQFP144 1		SMP
ASY2256402		ASY,BUS CONTROL EPLD, 040201,SMP		SMP
ASY2256402	ICX2187204	CPLD,3.3V,7 NS 288 MACRO,0/+70,TQFP144 1		SMP
ASY2256402	CRY1533802	CRYSTAL,20MHZ,-40/ +85C, SMT,SERIES RES 1		SMP
ASY2256402	ICX1014511	IC, LOGIC, INV, 74F04, SOIC14	(U17), U8	SMP
ASY2256402	ICX1040712	IC,LOGIC,GATE,NAND 74AC00,SOIC14		SMP
ASY2256402	ICX1051815	IC,LOGIC,GATE,OR,74LC X32 SOIC14	U41	SMP
ASY2256402	ICX1072515	IC,LOGIC,F/F,16BIT 74LVTH162374,SSOP48 1		SMP
ASY2256402	ICX1075922	IC,LOGIC,CLK/ DRVR,1:10 74FCT3807,QSOP2 1		SMP
ASY2256402	ICX1102509	IC,LOGIC,XCVR,16BIT 74LVT16245ADL,SSOI 2		SMP
ASY2256402	ICX1102610	IC,ANALOG,REG,3.3V 74LVT16244,SSOIC48		SMP

Table 8.1 List of FWAN PCS Base Station Active Components

Assembly	Part #	Description	Ref Des	Schematic
ASY2256402	ICX1155113	IC.LOGIC,XCVR,DIFF BUS LO-SWING,SO8	(U3), (U4), U1, U2	SMP
ASY2256402	ICX1180818	IC,LOGIC EMBEDDED TEST-BUS,SOP24		SMP
ASY2256402	ICX1196118	IC,LOGIC,BACKPLANE XCVR/ARBTR,1394,TQF 1		SMP
ASY2256402	ICX1216212	IC,LOGIC,INV,3V,74LCX0 4 SOIC14	U58, U65, U66, U68, U69, U70	SMP
ASY2256402	ICX1216313	IC,LOGIC,GATE,AND,3V 74LCX08,SOIC14	U60	SMP
ASY2256402	ICX1255114	LOGIC,XCVR/REG,18 BIT 3.3V,74LVTH18646 5		SMP
ASY2256402	ICX1256216	LOGIC,BFR/ DRVR,3ST,3.3V 74LVTH244A,SSO 3		SMP
ASY2256402	ICX1527702	LOGIC,XCVR,18BIT,3.3V, -40/+85C,TQFP64 1		SMP
ASY2256402	ICX1629009	EEPROM,8KX8BIT,W/ BLK LCK 2.5-5.5V,-40/ 1		SMP
ASY2256402	ICX1697305	TRANSVR,EIA232,3.0-5.5V, LOW POWER,SO1 1		SMP
ASY2256402	ICX1699002	LOGIC,OCTAL BUS XCVR, 3.3V,TSSOP	U113	SMP
ASY2256402	ICX1700407	LOGIC,HEX INVERTER,3.3V, WITH OPEN DRA 1		SMP
ASY2256402	ICX1700503	LOGIC,XCVR,10-BIT ADDRS SCAN PORT,3.3V 1		SMP
ASY2256402	ICX1700610	LOGIC,QUAD BUFFER,3.3V, W/3-STATE OUTP 1		SMP
ASY2256402	ICX1711009	LOGIC,XCVR,10BASE-T,3.3V ,0/+70,ETHERN 1		SMP
ASY2256402	ICX1712509	FLASH,64MEG,4MX16BI T,3V, 90NS,-40/+85, 2		SMP
ASY2256402	ICX1713304	LOGIC,BFR/CLK DRVR,3.3V, DUAL 1:5,0/ +7 2		SMP

Table 8.1 List of FWAN PCS Base Station Active Components

Assembly	Part #	Description	Ref Des	Schematic
ASY2256402	ICX1736702	IC,ANALOG,PWR SUPPLY, HOT SWAP,MANAGER 1		SMP
ASY2256402	ICX1744908	LOGIC,QUAD BUFFER,3.3V, TRI STATE,HIGH 4		SMP
ASY2256402	ICX1805605	ANALOG,LDO REG,3.3V, 150MA,SOT23	U30	SMP
ASY2256402	ICX1897603	LOGIC,XCVR,18BIT,3.3V, -40/+85C,TSSOP6 11		SMP
ASY2256402	ICX1909207	IC,UP SUPERVISORY CIRCT, DUAL VOLT MNT 2		SMP
ASY2256402	ICX1911606	IC,ANALOG,TEMP SENSOR, 10BIT,SOT23		SMP
ASY2256402	ICX2084408	LOGIC,BUS LINK-LAYER, 3.3V,IEEE1394,SQ 1		SMP
ASY2256402	ICX2290606	POWERQUICC,MPU,50 MHZ, -40/+85C,PBGA35 1		SMP
ASY2256402	ICX2297208	SDRAM,4M X 16BIT X 4 BANK,0/+70C,7.5NS 2		SMP
ASY2256402	OSC1893401	OSC,HCMOS,16.384MHZ, 3.3V,100PPM,SMT	Y1	SMP
ASY2256402	OSC1897105	OSC,HCMOS,10.000MHZ, 3.3V,-40/+85,SMT	Y3	SMP
ASY2256402	PWR1182113	PWR,DC-DC CONV,15W,48VIN 3.3VOUT		SMP
ASY2256402	PWR1215514	PWR,DC-DC CONV,10W,48VIN 5VOUT,A61		SMP
ASY2256402	PWR1727906	PWR,DC-DC,CONV,10W, 48V IN,3.3V OUT,SM 1		SMP
ASY2256402	PWR1789501	PWR,DC-DC CONV,15W, 48V IN,5V OUT,SMT		SMP
ASY2256402	XTR1998107	XTR,HEXFET,100 V,16 A TO252AA	Q2, Q3	SMP
ASY2256402	ICX1698506	FLASH,2.7V,512KX8,4MB IT, NON-VOLATILE, 0		SMP
ASY2303204		PCA,NIC,V0.71		NIC

Table 8.1 List of FWAN PCS Base Station Active Components

Assembly	Part #	Description	Ref Des	Schematic
ASY2303204	ICX1257116	IC, PLD, PRGBL CPLD 36 MACRO., 5NS, VQ 1		NIC
ASY2303204	ICX1698506	FLASH,2.7V,512KX8,4MB IT, NON-VOLATILE, 1		NIC
ASY2273203		ASY,BUS CONTROL EPLD, 041901,NIC	U50	NIC
ASY2273203	ICX1879708	CPLD,3.3V,7NS,288 MACRO, 0/+70C,BGA256 1		NIC
ASY2273203	CRY1533802	CRYSTAL,20MHZ,-40/ +85C, SMT,SERIES RES 1		NIC
ASY2273203	ICX1014511	IC, LOGIC, INV, 74F04, SOIC14	(U17), U8	NIC
ASY2273203	ICX1051815	IC,LOGIC,GATE,OR,74LC X32 SOIC14	U41	NIC
ASY2273203	ICX1075922	IC,LOGIC,CLK/ DRVR,1:10 74FCT3807,QSOP2 4		NIC
ASY2273203	ICX1095116	IC,EPROM,1MEGABIT,PL CC20	(U61)	NIC
ASY2273203	ICX1117010	IC,ANALOG,HEX INVERTER 74AC14SC,SOIC14 1		NIC
ASY2273203	ICX1155113	IC.LOGIC,XCVR,DIFF BUS LO-SWING,SO8	(U3), (U4), U1, U2	NIC
ASY2273203	ICX1196118	IC,LOGIC,BACKPLANE XCVR/ARBTR,1394,TQF 1		NIC
ASY2273203	ICX1212208	IC,ANALOG,REG,LDO-VAR SOIC8	U71	NIC
ASY2273203	ICX1216212	IC,LOGIC,INV,3V,74LCX0 4 SOIC14	U58, U65, U66, U68, U69, U70	NIC
ASY2273203	ICX1216313	IC,LOGIC,GATE,AND,3V 74LCX08,SOIC14	U60	NIC
ASY2273203	ICX1255114	LOGIC,XCVR/REG,18 BIT 3.3V,74LVTH18646 3		NIC
ASY2273203	ICX1512702	LOGIC,DRVR,3ST,74LVC2 44, SOICW20	U57	NIC
ASY2273203	ICX1629009	EEPROM,8KX8BIT,W/ BLK LCK 2.5-5.5V,-40/ 1		NIC

Table 8.1 List of FWAN PCS Base Station Active Components

Assembly	Part #	Description	Ref Des	Schematic
ASY2273203	ICX1697209	HEX BUFFERS/DRIVERS WITH OPEN-DRAIN OU 1		NIC
ASY2273203	ICX1697305	TRANSVR,EIA232,3.0-5.5V, LOW POWER,SO1 1		NIC
ASY2273203	ICX1698100	FPGA,10K50E,3.3V,10NS, PQFP240	U62	NIC
ASY2273203	ICX1700407	LOGIC,HEX INVERTER,3.3V, WITH OPEN DRA 1		NIC
ASY2273203	ICX1700503	LOGIC,XCVR,10-BIT ADDRS SCAN PORT,3.3V 1		NIC
ASY2273203	ICX1700610	LOGIC,QUAD BUFFER,3.3V, W/3-STATE OUTP 5		NIC
ASY2273203	ICX1710609	LOGIC,QUAD,T1 SCT,0/+70, LIU/FRAMER,LN 2		NIC
ASY2273203	ICX1711009	LOGIC,XCVR,10BASE-T,3.3V ,0/+70,ETHERN 1		NIC
ASY2273203	ICX1712509	FLASH,64MEG,4MX16BIT,3V, 90NS,-40/+85, 2		NIC
ASY2273203	ICX1713304	LOGIC,BFR/CLK DRVR,3.3V, DUAL 1:5,0/+7 2		NIC
ASY2273203	ICX1736702	IC,ANALOG,PWR SUPPLY, HOT SWAP,MANAGER 1		NIC
ASY2273203	ICX1736905	IC,ANALOG,DC-DC CONV, 600KHZ,POWER BOO 1		NIC
ASY2273203	ICX1744908	LOGIC,QUAD BUFFER,3.3V, TRI STATE,HIGH 4		NIC
ASY2273203	ICX1805605	ANALOG,LDO REG,3.3V, 150MA,SOT23	U30	NIC
ASY2273203	ICX1878507	LOGIC,QUAD BUFFER,3.3V, SOIC14	U15, U16	NIC
ASY2273203	ICX1895607	FLASH,64MBIT,3V,120NS, TSOP56	(U48), (U49)	NIC
ASY2273203	ICX1897603	LOGIC,XCVR,18BIT,3.3V, -40/+85C,TSSOP6 6		NIC

Table 8.1 List of FWAN PCS Base Station Active Components

Assembly	Part #	Description	Ref Des	Schematic
ASY2273203	ICX1909207	IC,UP SUPERVISORY CIRCT, DUAL VOLT MNT 1		NIC
ASY2273203	ICX1909303	IC,UP SUPERVISORY CIRCT, TRIPLE VOLT M 1		NIC
ASY2273203	ICX2084408	LOGIC,BUS LINK-LAYER, 3.3V,IEEE1394,SQ 1		NIC
ASY2273203	ICX2102307	SDRAM,512KX32BITX4,6 NS, 0/+70,TSOP86	U28	NIC
ASY2273203	ICX2290606	POWERQUICC,MPU,50 MHZ, -40/+85C,PBGA35 1		NIC
ASY2273203	OSC1023208	OSC,CMOS,1.544MHZ	Y2	NIC
ASY2273203	OSC1893401	OSC,HCMOS,16.384MHZ, 3.3V,100PPM,SMT	Y1	NIC
ASY2273203	OSC1897105	OSC,HCMOS,10.000MHZ, 3.3V,-40/+85,SMT	Y3	NIC
ASY2273203	PWR1070614	PWR,DC-DC CONV,48V NOM 20W	PS1	NIC
ASY2273203	XTR1068318	XTR,N-CHAN,MOSFET,SO8	Q1	NIC
ASY2273203	XTR1998107	XTR,HEXFET,100 V,16 A TO252AA	Q2, Q3	NIC
ASY2273203	ICX1698506	FLASH,2.7V,512KX8,4MB IT, NON-VOLATILE, 0		NIC
ASY2303300		PCA,WP,V0.71		WP
ASY2303300	ICX1257116	IC, PLD, PRGBL CPLD 36 MACRO., 5NS, VQ 1		WP
ASY2303300	ICX1707105	CPLD,3.3V,7.5NS,72 MACRO ,HIGH SPEED,V 1		WP
ASY2303300	ICX1698506	FLASH,2.7V,512KX8,4MB IT, NON-VOLATILE, 1		WP
ASY2303300	ICX1879708	CPLD,3.3V,7NS,288 MACRO, 0/+70C,BGA256 1		WP
ASY2303300	ICX1737508	CPLD,3.3V,7.5NS,144MAC RO HIGH PERF,0/+ 1		WP
ASY2303300	CRY1533802	CRYSTAL,20MHZ,-40/ +85C, SMT,SERIES RES 1		WP

Table 8.1 List of FWAN PCS Base Station Active Components

Assembly	Part #	Description	Ref Des	Schematic
ASY2303300	ICX1014511	IC, LOGIC, INV, 74F04, SOIC14	(U17), U8	WP
ASY2303300	ICX1021307	IC,LOGIC,CLK/ DRVR,1:10 49FCT805,SOIC20 1		WP
ASY2303300	ICX1051815	IC,LOGIC,GATE,OR,74LC X32 SOIC14	U41	WP
ASY2303300	ICX1075922	IC,LOGIC,CLK/ DRVR,1:10 74FCT3807,QSOP2 17		WP
ASY2303300	ICX1117010	IC,ANALOG,HEX INVERTER 74AC14SC,SOIC14 2		WP
ASY2303300	ICX1155113	IC.LOGIC,XCVR,DIFF BUS LO-SWING,SO8	(U3), (U4), U1, U2	WP
ASY2303300	ICX1196118	IC,LOGIC,BACKPLANE XCVR/ARBTR,1394,TQF 1		WP
ASY2303300	ICX1216212	IC,LOGIC,INV,3V,74LCX0 4 SOIC14	U58, U65, U66, U68, U69, U70	WP
ASY2303300	ICX1255114	LOGIC,XCVR/REG,18 BIT 3.3V,74LVTH18646 2		WP
ASY2303300	ICX1256216	LOGIC,BFR/ DRVR,3ST,3.3V 74LVTH244A,SSO 2		WP
ASY2303300	ICX1512702	LOGIC,DRVR,3ST,74LVC2 44, SOICW20	U57	WP
ASY2303300	ICX1627707	DSP,2.5/3.3V,16BIT,64K, -40/+85C,100MH 32		WP
ASY2303300	ICX1629009	EEPROM,8KX8BIT,W/ BLK LCK 2.5-5.5V,-40/ 1		WP
ASY2303300	ICX1688902	SRAM,64KX16,10NS,3.3V, 48PIN,UBGA	U27, U29, U31, U33, U41, U43, U45, U47, U59, U61, U63, U65, U76, U78, U80, U82, U115, U117, U119, U121, U125, U127, U129, U131, U136, U138, U140, U142, U144, U146, U148, U150	WP
ASY2303300	ICX1697209	HEX BUFFERS/DRIVERS WITH OPEN-DRAIN OU 7		WP

Table 8.1 List of FWAN PCS Base Station Active Components

Assembly	Part #	Description	Ref Des	Schematic
ASY2303300	ICX1697305	TRANSVR,EIA232,3.0-5.5V, LOW POWER,SO1 1		WP
ASY2303300	ICX1699002	LOGIC,OCTAL BUS XCVR, 3.3V,TSSOP	U113	WP
ASY2303300	ICX1700407	LOGIC,HEX INVERTER,3.3V, WITH OPEN DRA 3		WP
ASY2303300	ICX1700503	LOGIC,XCVR,10-BIT ADDRS SCAN PORT,3.3V 1		WP
ASY2303300	ICX1700610	LOGIC,QUAD BUFFER,3.3V, W/3-STATE OUTP 2		WP
ASY2303300	ICX1711009	LOGIC,XCVR,10BASE-T,3.3V ,0/+70,ETHERN 1		WP
ASY2303300	ICX1712509	FLASH,64MEG,4MX16BIT,3V, 90NS,-40/+85, 1		WP
ASY2303300	ICX1713304	LOGIC,BFR/CLK DRVR,3.3V, DUAL 1:5,0/+7 2		WP
ASY2303300	ICX1736702	IC,ANALOG,PWR SUPPLY, HOT SWAP,MANAGER 1		WP
ASY2303300	ICX1736905	IC,ANALOG,DC-DC CONV, 600KHZ,POWER BOO 1		WP
ASY2303300	ICX1737700	IC,LOGIC,GATE,AND,5V, 74HC21,SOIC14	U108	WP
ASY2303300	ICX1744908	LOGIC,QUAD BUFFER,3.3V, TRI STATE,HIGH 4		WP
ASY2303300	ICX1805605	ANALOG,LDO REG,3.3V, 150MA,SOT23	U30	WP
ASY2303300	ICX1897603	LOGIC,XCVR,18BIT,3.3V, -40/+85C,TSSOP6 11		WP
ASY2303300	ICX1898003	FPGA,2.5V,10K100,100K GATES,BGA356	U94	WP
ASY2303300	ICX1898206	EPROM,CONFIG DEVICE FOR APEX FPGA,3.3- 0		WP

Table 8.1 List of FWAN PCS Base Station Active Components

Assembly	Part #	Description	Ref Des	Schematic
ASY2303300	ICX1909207	IC,UP SUPERVISORY CIRCT, DUAL VOLT MNT 1		WP
ASY2303300	ICX1909303	IC,UP SUPERVISORY CIRCT, TRIPLE VOLT M 1		WP
ASY2303300	ICX2084408	LOGIC,BUS LINK-LAYER, 3.3V,IEEE1394,SQ 1		WP
ASY2303300	ICX2102307	SDRAM,512KX32BITX4,6 NS, 0/+70,TSOP86	U28	WP
ASY2303300	ICX2290606	POWERQUICC,MPU,50 MHZ, -40/+85C,PBGA35 1		WP
ASY2303300	OSC1893401	OSC,HCMOS,16.384MHZ, 3.3V,100PPM,SMT	Y1	WP
ASY2303300	OSC1897105	OSC,HCMOS,10.000MHZ, 3.3V,-40/+85,SMT	Y3	WP
ASY2303300	PWR1735706	PWR,DC-DC CONV,6W, 48V IN,2.0V OUT,TH	PS1A	WP
ASY2303300	PWR1926202	PWR,DC-DC CONV,75W,3.3V, HALF-BRICK,TH 0		WP
ASY2303300	PWR1926309	PWR,DC-DC CONV,75W,3.3V, HALF-BRICK,SM 1		WP
ASY2303300	PWR1996110	PWR,DC-DC CONV,48V IN, 2.5V OUT,6W,SMT 0		WP
ASY2303300	ICX1698506	FLASH,2.7V,512KX8,4MB IT, NON-VOLATILE, 0		WP
ASY2303300	PWR2059905	RECTIFIER,-48V,25A, VORTEX PCU		WP
ASY2303300	PWR2009301	TVSS,MOV,PROTECTION		WP

8.2 Tuning Procedures

The Base Station does not require any tuning beyond the adjustments performed during manufacture.

As part of the Base Station installation process, a technician will configure three variable attenuators in the transmit chain. These attenuators allow the technician to compensate for the variable transmission line loss and antenna gain associated with each FWAN PCS cell site installation.

8.3 Limiting Base Station RF Power Output

8.3.1 Applicable FCC Rules

- FCC Subpart 24.232(b) states: In no case may the peak output power of a Base Station transmitter exceed 100 watts. FCC Subpart 24.232(c) states: Peak transmitter power may be measured over any interval of continuous transmission using instrumentation calibrated in terms of RMS equivalent voltage. The measurement results shall be properly adjusted for any instrument limitations, such as detector response times, limited resolution bandwidth capability when compared to the emission bandwidth, sensitivity, etc., so as to obtain a true peak measurement for the emission in question over the full bandwidth of the channel.

8.3.2 Overview of the FWAN Linear Power Amplifier (LPA)

The LPA was designed to provide linear operation within a 12-dB peak-average ratio, based on a nominal average output power of +34 dBm (2.5 Watts). In order to support the 12-dB peak/average ratio required for OFDM service, the FWAN LPA must be capable of providing a peak output power of at least +46 dBm (40 Watts).

By design, the peak output power of the PWAN LPA is limited to +50dBm (100W).

Chapter 9 RF Exposure Information

Overview

This chapter contains information on how the product was determined to be compliant with FCC Rules, Part 24, subsection 24.51.

Contents

9.1 RF Human Exposure

9.1.1 Applicable FCC Rules

- FCC Subpart 24.51 - Applicants for Type Approval of transmitters operating within the PCS region must determine that the equipment complies with IEEE C95.1-1991, *IEEE Standards for Safety Levels with Respect to Human Exposure to Radio Frequency Electromagnetic Fields, 3 kHz to 300 GHz* as measured using methods specified in IEEE C95.3 - 1991, *Recommended Practice for the Measurement of Potentially Hazardous Electromagnetic Fields - RF and Microwave*.

9.1.2 FWAN PCS Test Configuration

Maximum Permissible Exposure (MPE) configuration will be completed per FCC MPE Site Requirements.

MPE testing will be performed on each FWAN PCS Base Station installed. MPE data, analysis, and required paperwork will be stored and filed per FCC regulatory requirements.