Technical Description :

The brief circuit description is listed as follows :
- U1 and associated circuit act as Encoder
- U2 and associated circuit act as Voltage regulator
- X1 and associated circuit act as 27.145MHz Oscillator
-L2,T1 and associated circuit act as antenna matching circuit.

Antenna Used:

Integral,External

DATA SHEET

GPRC205A

FIVE FUNCTIONS REMOTE CONTROL ENCODER/DECODER PAIRS

JUL. 19, 2007

Version 1.2

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FIVE FUNCTIONS REMOTE CONTROL ENCODER / DECODER PAIRS

1. GENERAL DESCRIPTION

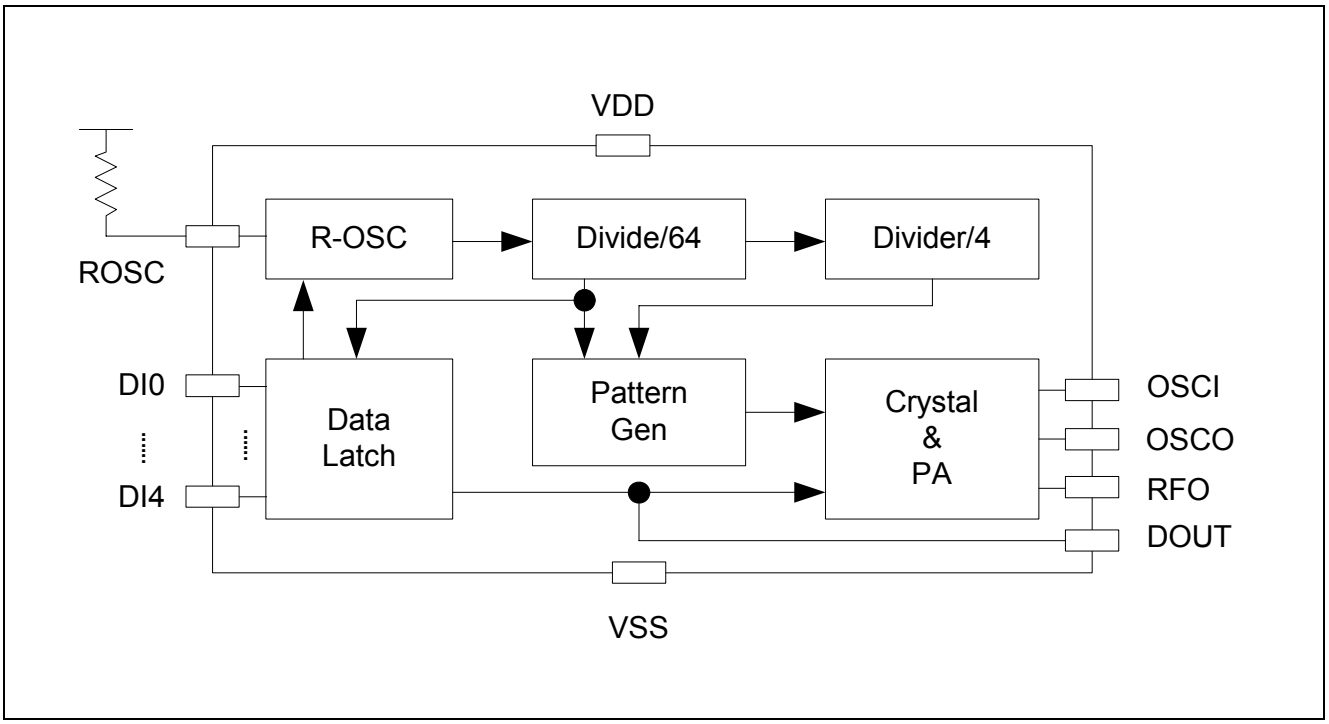
The GPRC205A, a RC encoder, is able to encode five lines of binary information into a serial bit-stream data. When any of the 5-line information is activated, built-in crystal oscillator and power amplifier will be enabled to deliver the encoded bit-stream data. After the 5-line information becomes inactive, the GPRC205A will transmit additional fifteen data frames to increase transmission reliability.

With GENERALPLUS state-of-the-art technology and strong support, GPRC205A is the simplest and most suitable product for your RC product.

2. FEATURES

- Operating voltage
  - 2.2V - 5.5V operation
- Built-in R-oscillator (a 5% resistor required)
- Low standby and operating current
  - I_{STBY} < 1.0μA, R-oscillator stops
  - $I_{OPERATE}$ < 15mA, R-oscillator free run, crystal & PA on
- Built-in power on reset
- Built-in Crystal & PA
- 5-function I/O pins
- 2^5 = 32 encoding
- Variable frame rates controlled by external resistor

3. BLOCK DIAGRAM



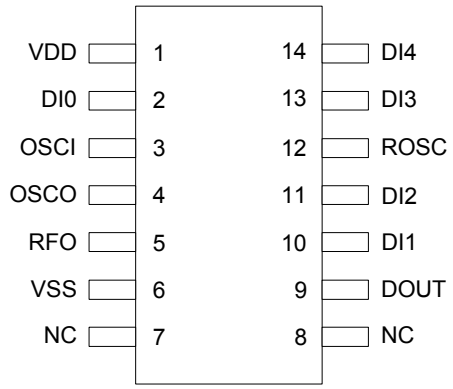
4. SIGNAL DESCRIPTIONS

4.1. PIN Description

Mnemonic	Type	PIN No.	Description
DI0 DI1 DI2 DI3 DI4	I	2 8 9 11 12	5-function parallel data input.
DOUT	O	7	Serial bit-stream data output; connected a capacitor of 10nF to VSS to reduce RF spurious.
OSCI	I	3	Crystal oscillator input pin.
OSCO	O	4	Crystal oscillator output pin.
RFO	O	5	Power Amplifier output pin. The waveform do not exceed 9Vpp.
ROSC	I	10	R-oscillator input, connected to VDD through a resistor.
VDD	P	1	Power voltage input.
VSS	P	6	Power ground input.

4.2. PIN Configuration

PDIP 14



5. FUNCTIONAL DESCRIPTIONS

5.1. Frame Format

Preamble						PO	E	D0	D1	D2	D3	D4
P	P	P	P	P	P	A/I	A/I	A/I	A/I	A/I	A/I	A/I

Preamble field: 6 preamble fields.

PO field: Even parity check field.

E field: Frame polarity indication field; frames are transmitted in positive/negative sequence.

Data field: 5 data fields.

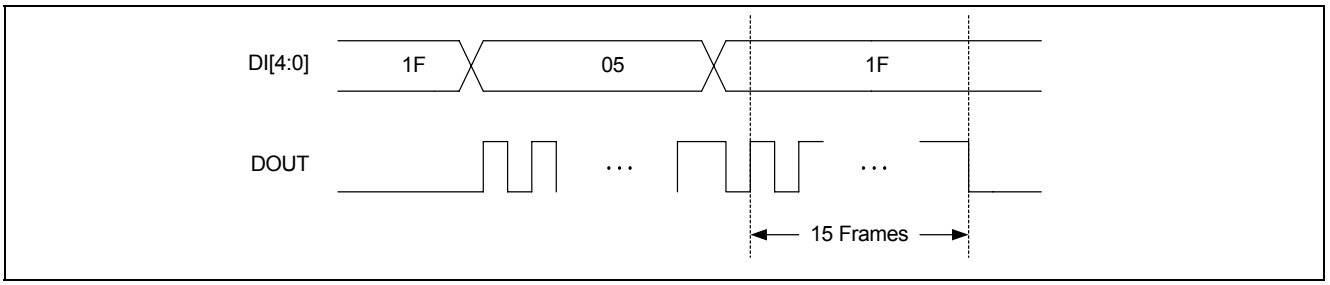
P pattern: encoded as 10.

A pattern: encoded as 100.

I pattern: encoded as 110.

5.2. Operation

The GPRC205A encodes 5-function information into 2^5 series of bit-stream data and transmits the encoded data stream via RFO when any of the 5-function I/Os is activated. The cycle will repeat until all 5-function I/Os become inactive. After these 5-function I/Os become inactive, GPRC205A will transmit another 15 all-zero frames to inform GPRC206A returning to disabled state. The transmitting timing is shown as follows:



5.3. R-oscillator

GPRC205A has built in R-oscillator. Users need only one resistor (or a capacitor if needed) to implement the clock input and to change the frame rate by replacing different resistor.

Frame rate = F_{OSC} / 64 / 33

The only limitation is using a 5% accuracy resistor is required in GPRC205A.

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	-20℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

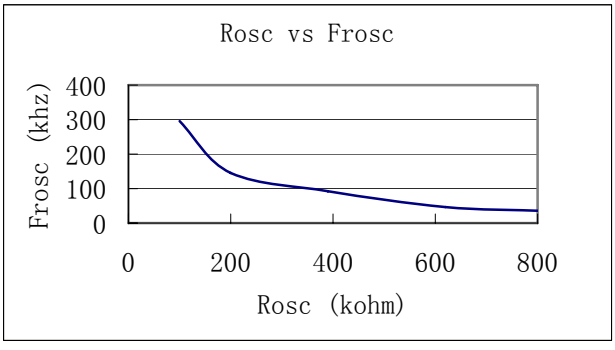
Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. DC Characteristics (VDD = 3.0V, T_A = 25℃)

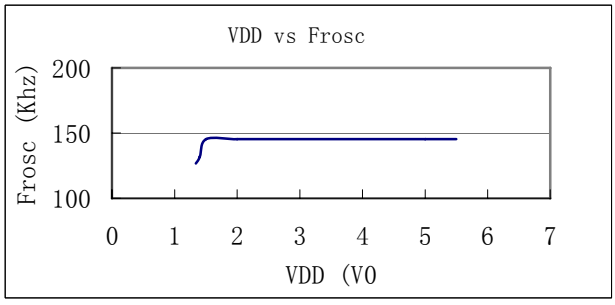
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.2	-	5.5	V	R-OSC resistor = 200KΩ
RFO Maximum Waveform	VRFO	-	-	9	Vpp	VDD = 4.5V, Inductor load.
Operating Current	I_{OP}	-	-	15	mA	R-OSC resistor = 200KΩ Crystal & PA on (6.0dBm)
Standby Current	I_{STBY}	-	-	1.0	μA	R-OSC disable
Input High level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High Current	I_{OH}	-	-6.0	-	mA	VDD = 3.0V, V_{OH} = 2.4V
Output Sink Current	I_{OL}	-	6.0	-	mA	VDD = 3.0V, V_{OL} = 0.4V
DI[4:0] Pull High Resistor	R_{DI}	-	200	-	KΩ	VDD = 3.0V
OSC Frequency	F_{OSC}	-	128	-	KHz	R_{OSC} = 200KΩ @ VDD from 2.0V - 5.5V

6.3. AC Characteristics

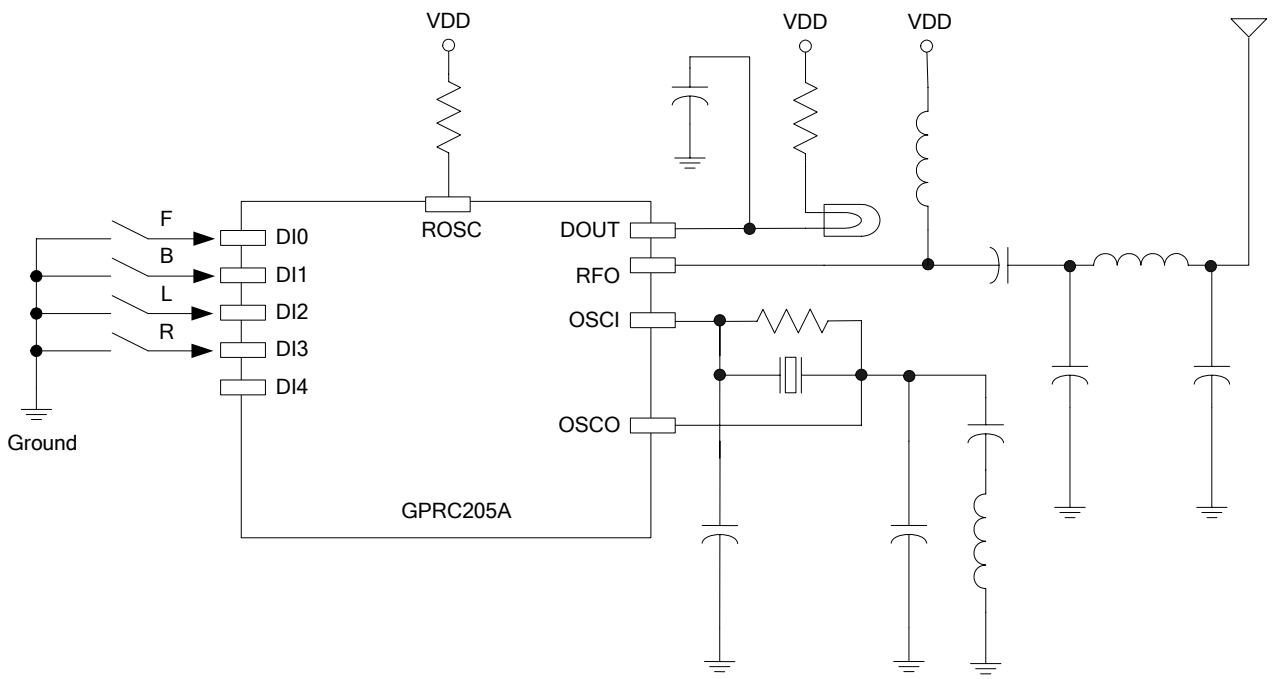
6.3.1. The Relationships of the R_{OSC} and the F_{ROSC} VDD = 3.0V, T_A = 25℃



6.3.2. The Relationships of the VDD and the F_{ROSC}



7. APPLICATION CIRCUITS



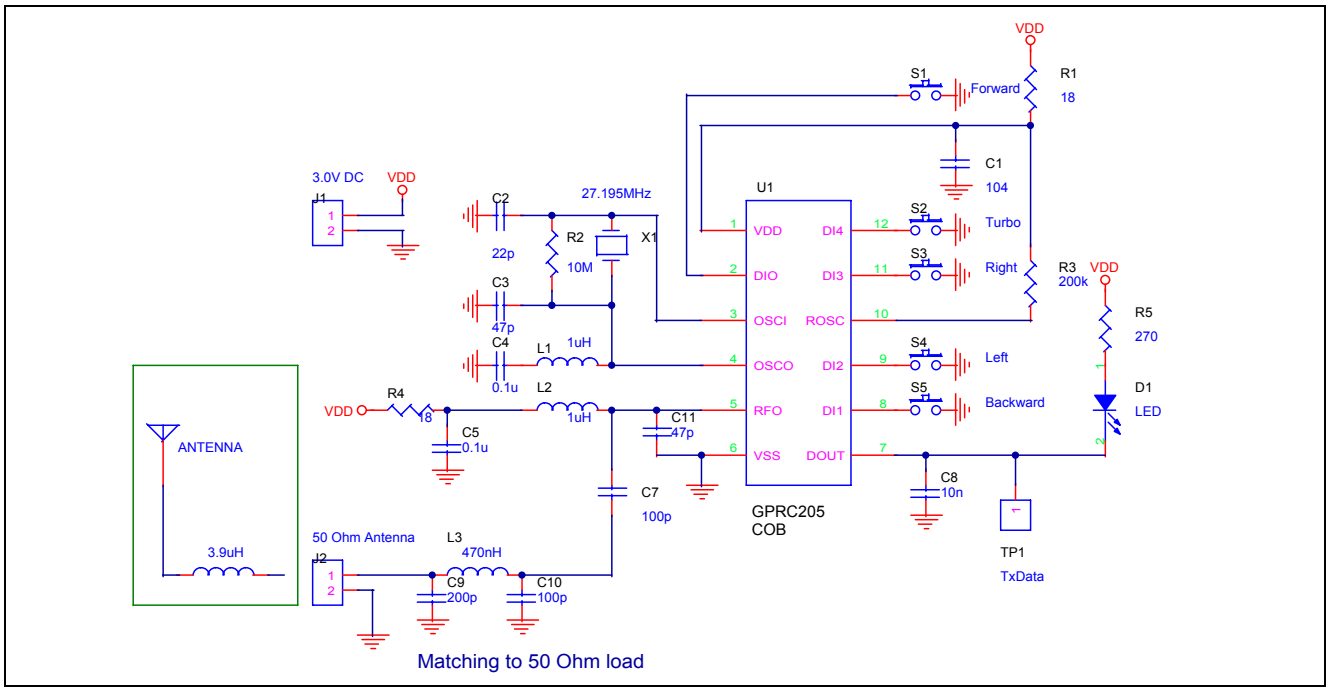
GPRC205A Encoder application circuit

7.1. Reference Design

For general application, “DI0” is defined as “Forward”. “DI1” is “Backward”, “DI2” as ‘Left’, “DI3” as “Right”, and “DI4” for “Turbo” or other functions.

7.2. 27MHz Transmitter

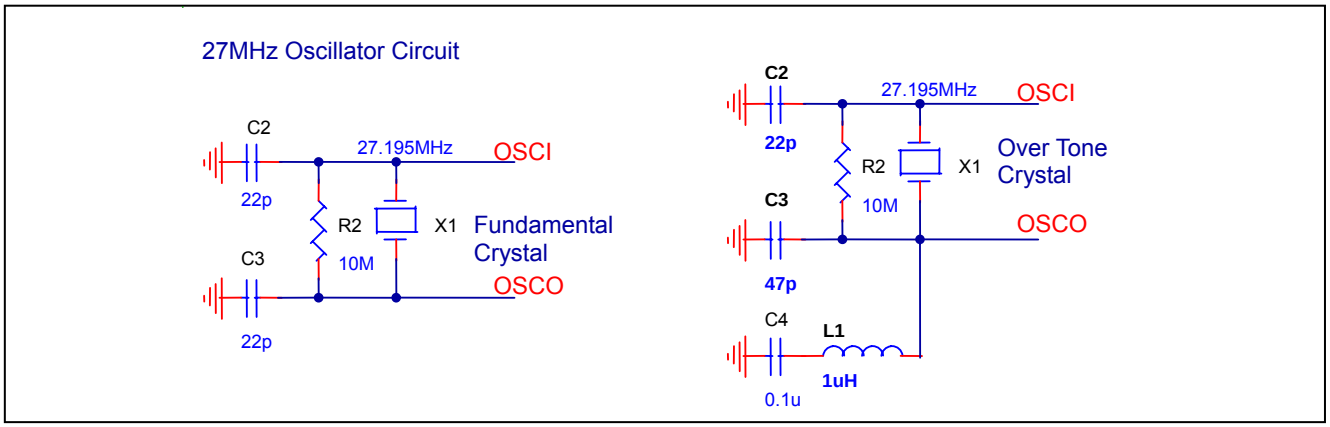
The standby current is estimated less than 1.0μA if no button pressed. When a button is pressed, the GPRC205A wakes up and transmit the encoded RF signal.

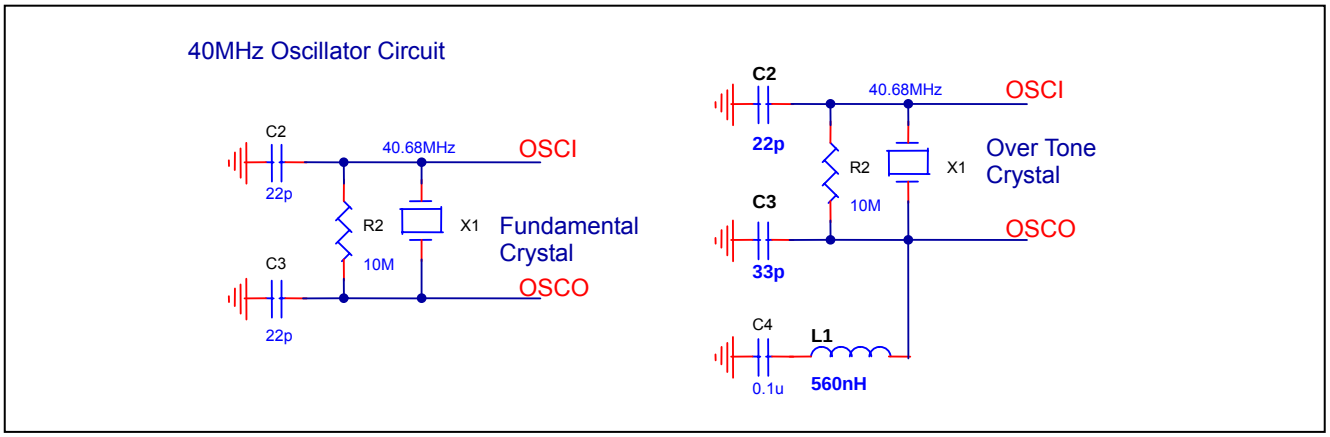


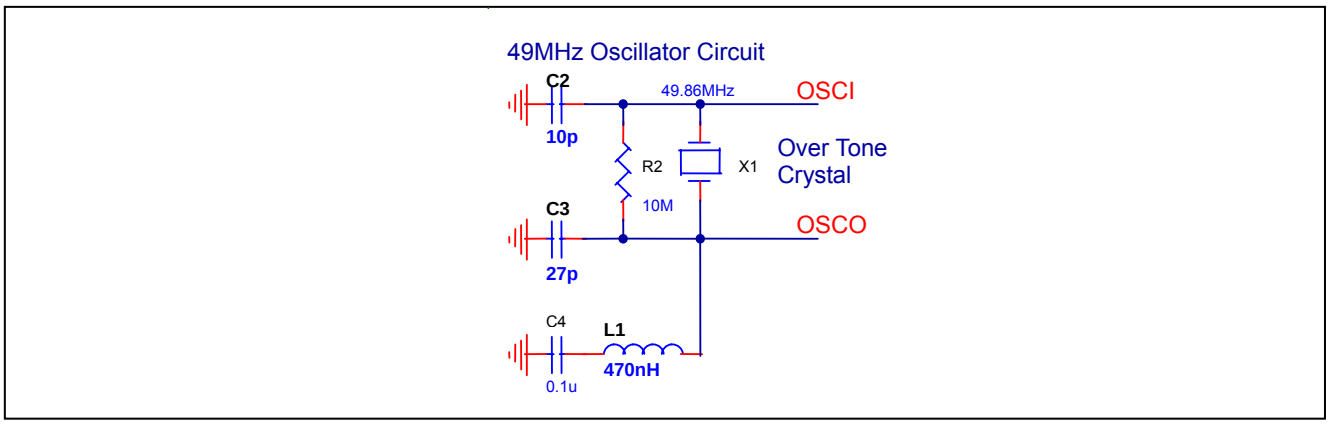
7.3. Crystal Oscillator Example

For over tone type crystal, a LC tank circuit is necessary to prevent base tone oscillating.

$$Fx > \frac{1}{2\pi\sqrt{LC}}, Fx = \text{crystal frequency}, L = L1, C = C3$$

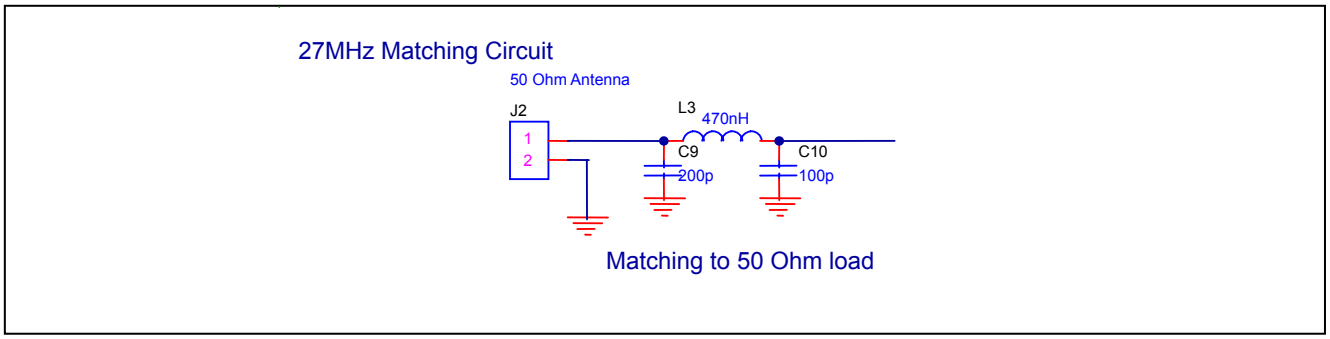


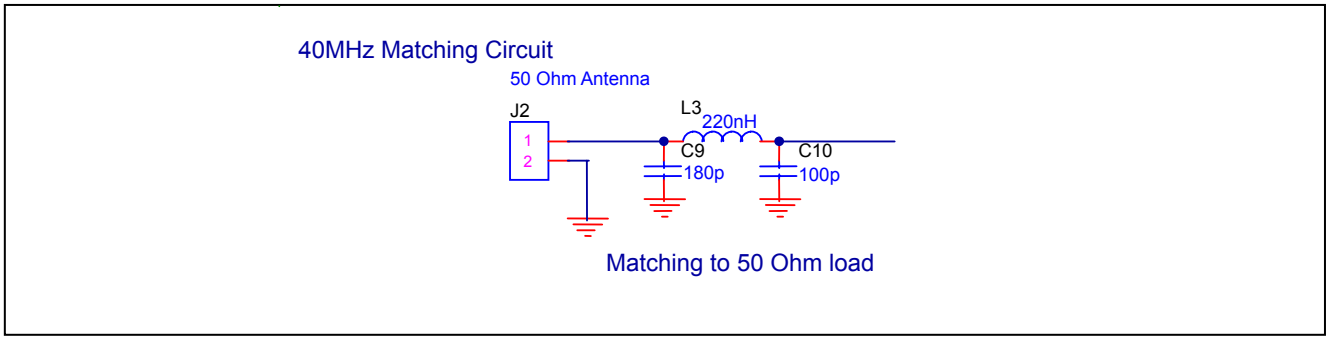


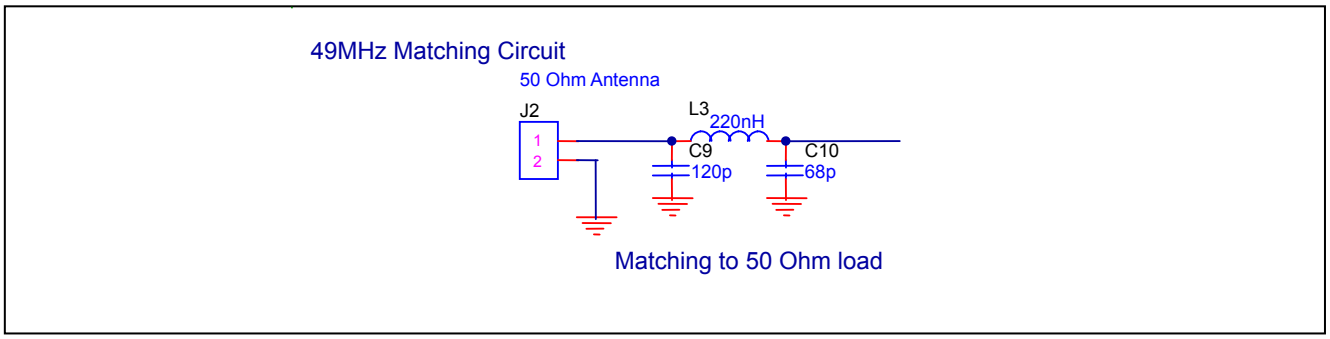


Note: There are different values of C2, C3 and L1 for 27MHz, 40MHz and 49MHz. User must use these values correctly, otherwise it possibly causes oscillator circuit malfunction.

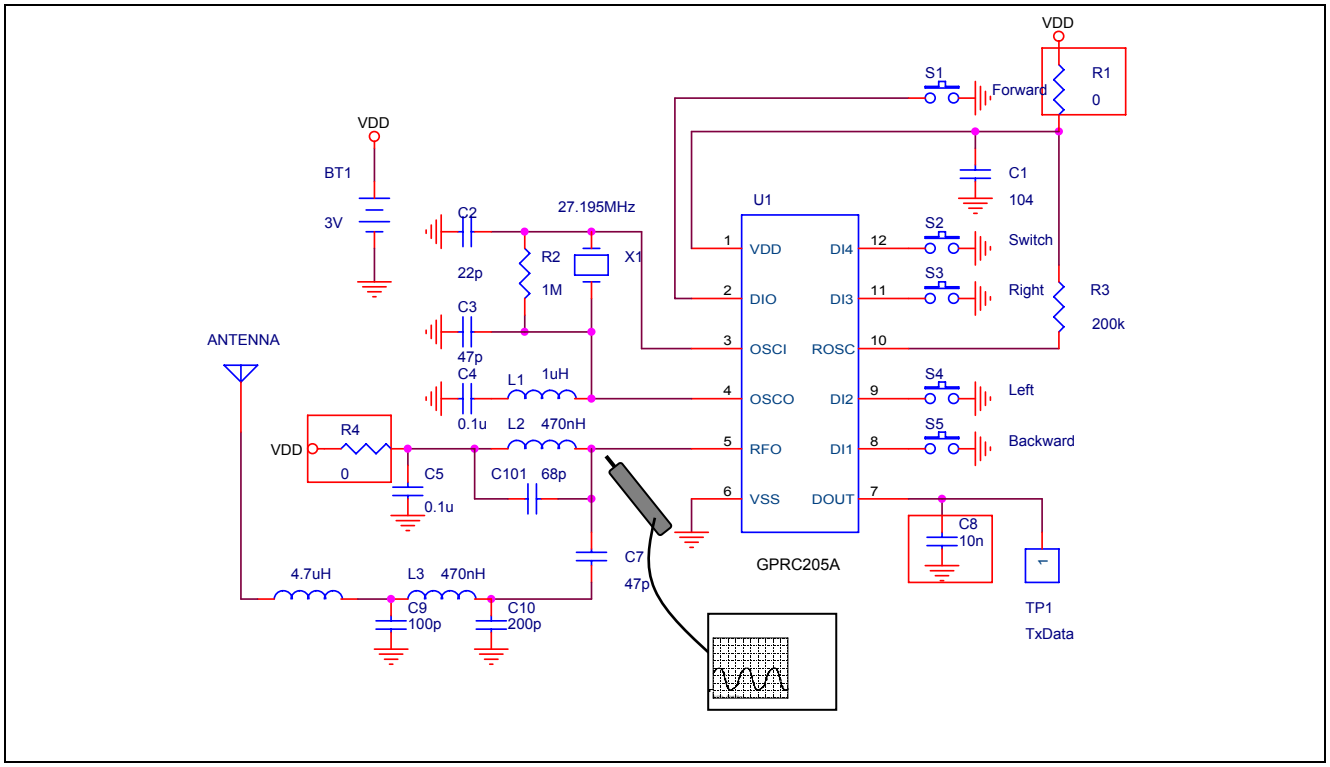
RF Output Matching Example







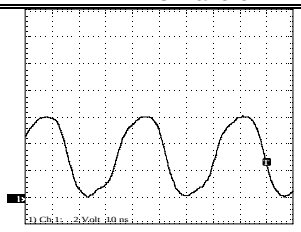
7.4. RF Harmonic and Bandwidth

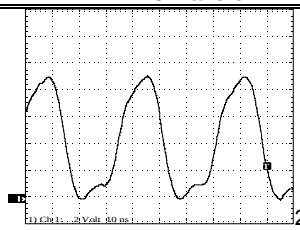
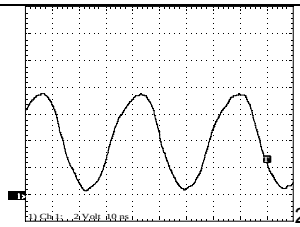
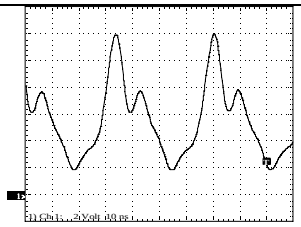
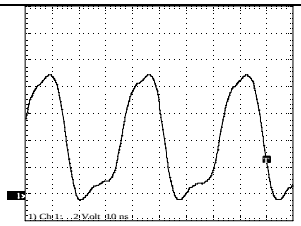


The RF fundamental power is related to supply voltage, and the harmonic power is, too. R4 and R1 can reduce harmonic if it works at higher voltage (ex 5.5V). C8 is used to reduce the RF bandwidth (for 27MHz, 40MHz, 49MHz to meet band edge limitation).

The following table shows RFO (pin5 of GPRC205A) waveform by various conditions

Note: the antenna loading is 50 Ohm

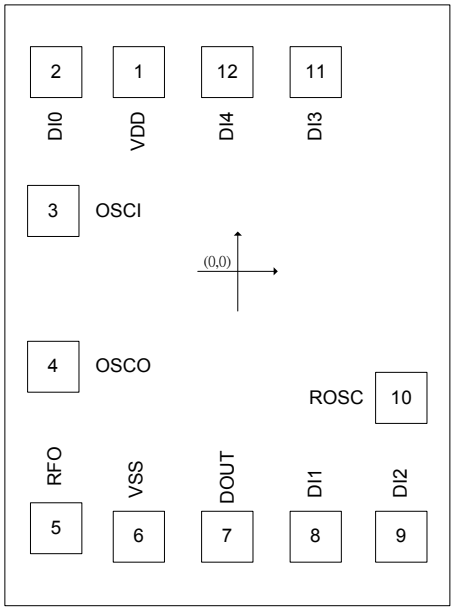
Test condition	RFO waveform
VDD=3.0V, R4=0, R1=0 Perfect wavefrom.	 2v/, 10ns/

Test condition	RFO waveform
VDD=4.0V, R4=0, R1=0 Higher the supply voltage, higher the fundamental and harmonic power	 2v/, 10ns/
VDD=4.0V, R4=0, R1=330 Ohm Add R1 to lower supply voltage to reduce harmonic	 2v/, 10ns/
VDD=5.5V, R4=0, R1=0 Ohm If the peak voltage of RFO exceeds 9V, RFO breaks down. It gets lower fundamental and higher harmonic.	 2v/, 10ns/
VDD=5.5V, R4=100 Ohm, R1=330 Ohm Use R4 to limit the RFO waveform.	 2v/, 10ns/

8. PACKAGE/PAD LOCATIONS

8.1. PAD Assignment

8.1.1. GPRC205A



This IC substrate should be connected to VSS

Note1: To ensure that the IC functions properly, please bond all of VDD and VSS pins.
Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

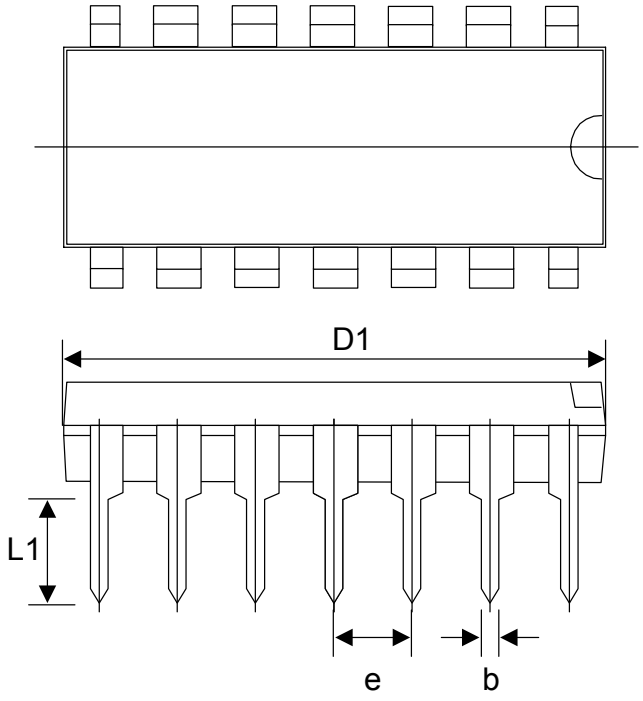
8.2. Ordering Information

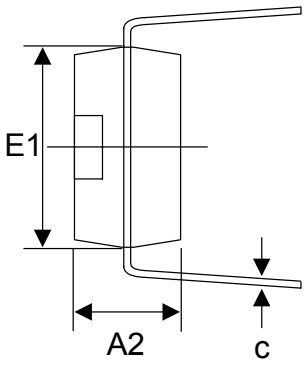
Product Number	Package Type
GPRC205A - C	Chip form
GPRC205A - HD02x	Green Package - PDIP 14

Note: Package form number (x = 0 - 9, serial number).

8.3. Package Information

8.3.1. GPRC205A - PDIP 14





Body Size			Lead Size			
D1	E1	A2	L1	b	c	e
750±10	250±4	130±5	130±5	18±2	10Typ	100Typ

All units are in mil. 1mil = 25.4μm

D1	Body Length
E1	Body Width
A2	Body Thickness
L1	Lead Length
b	Lead Width
c	Lead Thickness
e	Lead Pitch

PDIP-14-300

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10. REVISION HISTORY

Date	Revision #	Description	Page
JUL. 19, 2007	1.2	Separating the GPRC205A/GPRC206A data sheet into two independent documents.	15
FEB. 18, 2005	1.1	P pattern: encoded as 10. Original is 101 Frame rate = F_{OSC} / 64 / 33. Original is F_{OSC} / 64 / 54 Adjust the value of C2 from 12p to 10p in 49 MHz oscillator circuit	5 6 11
JUN. 14, 2004	1.0	Original Note: The GPRC205A/ GPRC206A data sheet v1.0 is a continued version of SPRC205A/ SPRC206A data sheet v0.2.	18