Technical Description:

The brief circuit description is listed as follows:

U1 and Associated circuit act as Encoder and MCU.
U2 acts as Voltage Regulator
U3 acts as 2.4GHz RF transceiver module
Q1 acts as Buzzer driver
Y1 acts as Buzzer
VR1, VR2, S1, S2, SW3 & SW4 act as control keys

Antenna Used:

An internal, integral antenna has been used.
Antenna Gain: 0dBi
Nominal rated field strength: 91.5dBµV/m at 3m
Maximum allowed field strength of production tolerance: +/- 3dB

1. General Description

A7106 is a high performance and low cost 2.4GHz ISM band wireless transceiver. This device integrates both high sensitivity receiver (- 95dBm @ 500Kbps) and high efficiency power amplifier (up to 1dBm). In low data rate application, A7106 has special strength for long LOS (line-of-sight) distance because of its ultra high sensitivity (-107 dBm @ 2Kbps, - 104 dBm @ 25Kbps) with no requirement of external LNA or PA. Based on Data Rate Register (0x0E), user can configure on-air data rates from 2Kbps to 500Kbps.

A7106 supports fast settling time (130 us) for frequency hopping system. For packet handling, A7106 has built-in separated 64-bytes TX/RX FIFO (could be extended to 256 bytes) for data buffering and burst transmission, CRC for error detection, FEC for 1-bit data correction per code word, RSSI for clear channel assessment, data whitening for data encryption / decryption. Those functions are very easy to use while developing a wireless system. All features are integrated in a small QFN 4X4 20 pins package.

A7106's control registers can be easily accessed via 3-wire or 4-wire SPI bus. For power saving, A7106 supports sleep mode, idle mode, standby mode. For easy-to-use, A7106 has an unique SPI command set called **Strobe command** that are used to control internal state machine. Based on Strobe commands via SPI bus, MCU can control everything from power saving, TX delivery, RX receiving, channel monitoring, frequency hopping to auto calibrations. In addition, A7106 supports two general purpose I/O pins, GIO1 and GIO2, to inform MCU its status so that MCU could use either polling or interrupt scheme to do radio control. Hence, it is very easy to monitor radio transmission between MCU and A7106 because of its digital interface.

2. Typical Applications

- Wireless keyboard and mice
- Remote control
- Helicopter and airplane radio controller

- 2400 ~ 2483.5 MHz ISM system
- Wireless metering and building automation
- Wireless toys and game controllers

3. Feature

- Small size (QFN4 X4, 20 pins).
- Frequency band: 2400 ~ 2483.5MHz.
- FSK or GFSK modulation
- Low current consumption: RX 16mA, TX 20mA (at 0dBm output power).
- Low sleep current (1.5 uA).
- On chip regulator, support input voltage 2.0 ~ 3.6 V.
- Programmable data rate from 2Kbps to 500Kbps.
- Programmable TX power level from – 20 dBm to 1 dBm.
- Ultra High sensitivity:
  - -95dBm at 500Kbps on-air data rate.
  - -97dBm at 250Kbps on-air data rate
  - -104dBm at 25Kbps on-air data rate
  - -107dBm at 2Kbps on-air data rate
- Fast settling time (130 us) synthesizer for frequency hopping system.
- Built-in Battery Detector.
- Support low cost crystal (6 / 8 /12 / 16 / 20 / 24MHz).
- Support crystal sharing, (1 / 2 / 4 / 8MHz) to MCU.
- Auto Frequency Compensation
- Easy to use.
  - Support 3-wire or 4-wire SPI.
  - Unique Strobe command via SPI.
  - ONE register setting for new channel frequency.
  - 8-bits Digital RSSI for clear channel indication.
  - Fast exchange mode during TRX role switching.

◆ Auto RSSI measurement.
◆ Auto Calibrations.
◆ Auto IF function.
◆ Auto CRC Check.
◆ Auto FEC by (7, 4) Hamming code (1 bit error correction / code word).
◆ Data Whitening for encryption and decryption.
◆ Separated 64 bytes RX and TX FIFO.
◆ Easy FIFO / Segment FIFO / FIFO Extension (up to 256 bytes).
◆ Support direct mode with recovery clock output to MCU.
◆ Support direct mode with frame sync signal to MCU.

4. Pin Configurations

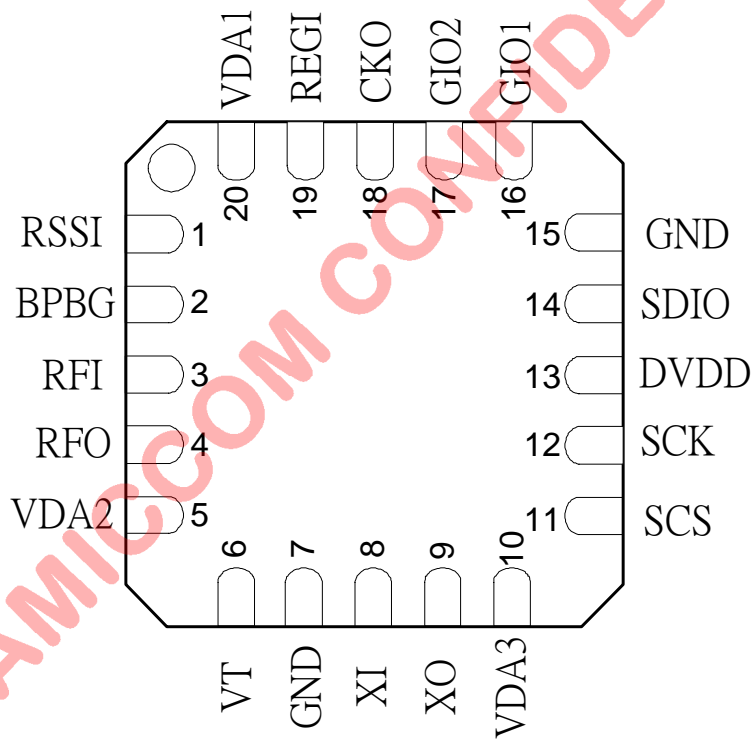Fig 4-1. A7106 QFN 4x4 Package Top View

5. Pin Description (I: input; O: output, I/O: input or output)

Pin No.	Symbol	I/O	Function Description
1	RSSI	O	Connected to a bypass capacitor for RSSI reading.
2	BPBG	O	Connected to a bypass capacitor for internal Regulator bias point
3	RFI	I	Low noise amplifier input.
4	RFO	O	Power amplifier output.
5	VDA2	I/O	Voltage supply **(from VDA1, pin 20)** for RX & TX analog part.
6	VT	I	VCO frequency control input, internal connected to PLL charge pump.
7	GND	G	Ground
8	XI	I	Crystal oscillator input node
9	XO	O	Crystal oscillator output node
10	VDA3	I	Voltage supply **(from VDA1, pin 20)** for PLL part
11	SCS	I	3 wire SPI chip select.
12	SCK	I	3 wire SPI clock input pin.
13	DVDD	I	Connected to a bypass capacitor to supply voltage for digital part.
14	SDIO	I/O	3 wire SPI read/write data pin.
15	GND	G	Ground
16	GIO1	I/O	Multi-function GIO1 / 4-wire SPI data output.
17	GIO2	I/O	Multi-function GIO2 / 4-wire SPI data output.
18	CKO	O	Multi-function clock output.
19	REGI	I	Internal Regulator input **(External Power Input)**
20	VDA1	I/O	Internal Regulator output to supply **VDA2 (pin 5), VDA2 (pin 10) and RFO (pin 4).**
	Back side plate	G	Ground. Back side plate shall be well-solder to ground; otherwise, it will impact RF performance.