FCC ID: OYK-FCC82333

Technical Description:

The brief circuit description is listed as follows:
U1 and associated circuit act as charging part.
U2 and associated circuit act as voltage regulator.
U3 and associated circuit act as 2.4GHz RF modular (WT24C02).
U4 and associated circuit act as decoder (XXX8P418K-54).
U5, SW4 and associated circuit act as control key.
Q1-Q8 and associated circuit act as motor driver.

Antenna Used:

An internal, integral antenna has been used.

Frequency Table (Channel 00-23)							
Channel	Fequency(MHz)	Channel	Fequency(MHz)	Channel	Fequency(MHz)	Channel	Fequency(MHz)
00	2402	**04**	2410	**11**	2421	**17**	2430
01	2404	**05**	2412	**12**	2422	**18**	2432
02	2406	**06**	2414	**13**	2424	**19**	2433
03	2408	**07**	2415	**14**	2425	**20**	2434
		08	2416	**15**	2427	**21**	2436
		09	2417	**16**	2428	**22**	2437
		10	2418			**23**	2439
Frequency Table (Channel 24-50)							
Channel	Fequency(MHz)	Channel	Fequency(MHz)	Channel	Fequency(MHz)	Channel	Fequency(MHz)
24	2440	**31**	2451	**36**	2460	**44**	2470
25	2442	**32**	2452	**37**	2461	**45**	2471
26	2443	**33**	2454	**38**	2463	**46**	2472
27	2444	**34**	2455	**39**	2464	**47**	2473
28	2445	**35**	2457	**40**	2465	**48**	2475
29	2446			**41**	2466	**49**	2476
30	2448			**42**	2467	**50**	2478
				43	2469		

1 General Description

The XXX8P418K is an 8-bit microprocessor designed and developed with low-power, high-speed CMOS technology. This device has an on-chip 4K×13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM). It provides Protection bits to prevent intrusion of user's code in the OTP memory as well as from unwanted external accesses. Three Code Option bits are also available to meet user's application requirements.

With its enhanced OTP-ROM features, the XXX8P418K provides a convenient way of developing and verifying user's programs. Moreover, this OTP device offers the advantages of easy and effective program updates, using development and programming tools. User can avail of the Writer to easily program his development code.

2 Feature

- CPU configuration
  - 4K×13 bits on-chip ROM
  - 144×8 bits on-chip registers (SRAM)
  - 8 level stacks for subroutine nesting
  - Less than 2.2 mA at 5V/4MHz
  - Typically 15 μA, at 3V/32kHz
  - Typically 1 μA, during sleep mode
- I/O port configuration
  - 3 bi-directional I/O ports
  - Wake-up port : P6
  - 8 Programmable pull-down I/O pins
  - 8 programmable pull-high I/O pins
  - 8 programmable open-drain I/O pins
  - External interrupt : P50
- Operating voltage range:
  - 2.3V~5.5V at 0°C~70°C(commercial)
  - 2.5V~5.5V at -40°C~85°C(industrial)
- Operating frequency range(base on 2 clocks):
  - Crystal mode: DC ~ 20 MHz, 5V; DC ~ 8MHz, 3V
  - ERC mode: DC ~ 16MHz, 5V; DC ~ 4MHz, 3V
  - IRC mode: 4MHz at 2.3V~5.5V

Internal RC Frequency	Drift Rate			
	Temperature (-40°C+85°C)	Voltage (2.3V~5.5V)	Process	Total
4MHz	±10%	±5%	±4%	±19%
8MHz	±10%	±6%	±4%	±20%
1MHz	±10%	±5%	±4%	±19%
455kHz	±10%	±5%	±4%	±19%

- All these four main frequencies can be trimmed by programming with four calibrated bits in the ICE418N Simulator. OTP is auto trimmed by Writer.
- Fast set-up time requires only 2ms in high Crystal and 32 CLKS in IRC mode from wake up to operating mode
- Peripheral configuration
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - 8-bit multi-channel Analog-to-Digital Converter with 12-bit resolution in Vref mode
  - Three Pulse Width Modulation (PWM) with 10-bit resolution
  - One pair of comparator (Can be set as an OP)
  - Power-down (Sleep) mode
- Six available interrupts
  - TCC overflow interrupt
  - Input-port status changed interrupt (wake up from sleep mode)
  - External interrupt
  - ADC completion interrupt
  - PWM period match completion
  - Comparator high/low interrupt
- Programmable free running watchdog timer
- Power-on voltage detector provided (2.0V+0.1V)
-
  -
  -
  -
  -
  -
  -
  -

Note: Green products do not contain hazardous substances

DATA SHEET

WT24C02V02

2.4 GHz ISM Band RF Transceiver Module

Production Specification

Wailly Technology Ltd.
Unit 503-505,Fook Hong Industrial Building,
19 Sheung Yuet Road,Kowloon Bay,Kowloon,Hong Kong.
TEL: (852) 2756 4500
FAX: (852) 2624 8510
http://www.wailly.net

CONTENTS

2.4 GHZ ISM BAND RF TRANSCEIVER MODULE

1. Description

The WT24C02V02 is a 2.4GHz ISM band RF transceiver module consists of EM198810 transceiver. In normal applications,WT24C02V02 module is connected to a low cost microcontroller .

The on-chip framer processes and stores the RF data in the background, unloading this critical timing function from the MCU. This lowers MCU speed requirements, expedites product development time, and frees the MCU for implementing additional product features.

This module has high transmission data rate; low current consumption and simple control interface is easy to apply to the wireless products.

2. Key Features:

- Combines 2.4 GHz GFSK RF transceiver with 8-bit data framer function
- Simple microcontroller interface – 4 wires for SPI, plus 3 wires for RST/buffer control
- Each transmit, receive buffer is 64 bytes deep
- Long packets are possible if buffers are read/written before overflow/underflow occurs
- Always 1Mbps over-the-air symbol rate, regardless of MCU speed or architecture
- Preamble can be 1 to 8 bytes
- Supports 1, 2, 3, or 4 word address (up to 64 bits)
- Various Payload data formats to eliminate DC offset, enhance receive clock recovery and BER
- Supports Forward Error Correction (FEC): none, 1/3
- Supports 16-bit CRC
- Power management for minimizing current consumption
- **FCC certified for unlicensed operation**

3. Applications

- Wireless devices that need quick time-to-market
- Wireless mouse, keyboard, joystick
- Wireless data communication
- Wireless security and access control
- Home and factory automation
- Toys
- Telemetry
- Industrial sensors
- Battery powered wireless devices

4.Electrical Characteristics

4.1 Absolute maximum rating

Parameter	Symbol	Rating			Unit
		Min.	Typ.	Max.	
Operating Temp.	TOP	-20		+70	℃
Storage Temp.	TSTORAGE	-30		+80	℃
VDD_IO Supply Voltage	VDDIO_MAX			+3.7	VDC
VDD Supply Voltage	VDD_MAX			+2.5	VDC
Applied Voltages to Other Pins	VOTHER	-0.3		+3.7	VDC

- Table 1 -

4.2 Characteristics

The following specifications are guaranteed for T_A=25℃, unless otherwise noted:

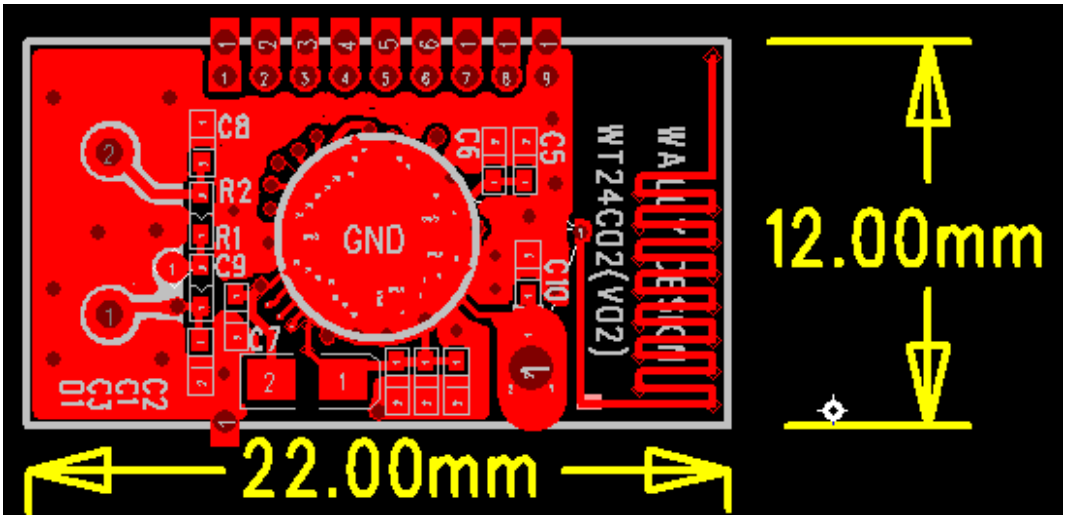
Parameter	Symbol	Specification			Unit	Test Condition and Notes
		Min.	Typ.	Max.		
Current Consumption						
Current Consumption - TX	IDD_TX		29		mA	
Current Consumption - RX	IDD_RX		27		mA	
Current Consumption – DEEP IDLE	IDD_D_IDLE		1.9		mA	RF Synthesizer and VCO: OFF
Current Consumption – SLEEP	IDD_SLP		15		uA	
Digital Inputs						
Logic input high	VIH	0.8VDD_io		VDD_io	V	
Logic input low	VIL	0		0.8	V	
Digital Outputs						
Logic output high	VOH	0.8VDD_io		VDD_io	V	
Logic output low	VOL			0.4	V	
Overall Transceiver						
Operating Frequency Range	F_OP	2400		2482	MHz	
Receive Section: @ BER≦0.1%						
Receiver sensitivity			-83		dBm	Conductive measurement.
Maximum useable signal		-20			dBm	
Transmit Section: Reg. 9, bits 15-8 set to 00000000						
RF Output Power	P_{AV}		+0		dBm	Conductive measurement.

- Table 2 -

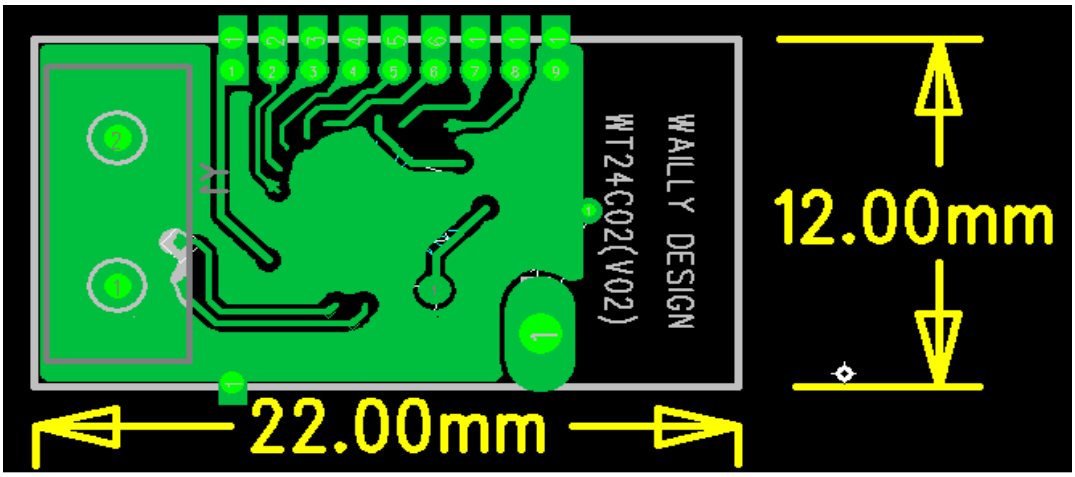
5. Module Drawing and I/O Pin Assignment

5.1 PCB drawing

* PCB size: 22 x 12 x 1.0 mm



(top)



(bottom)

5.2 I/O Pin function

Pin	Name	Description
1	VDD	Power supply voltage +3.3V.
2	SPI_MISO	Data output for the SPI bus.
3	RESET_n	When RESET_n is low,most of the chip shuts down to conserve power. When raised high, RESET_n is used to turn on the chip, restoring all registers to their default value.
4	SPI_CLK	Clock line for the SPI bus.
5	SPI_MOSI	Data input for the SPI bus.
6	SPI_SS	Enable line for the SPI bus. Active low.
7	NC	
8	PKT_FLAG	Transmit/Receive packet process flag.
9	GND	Ground connection.

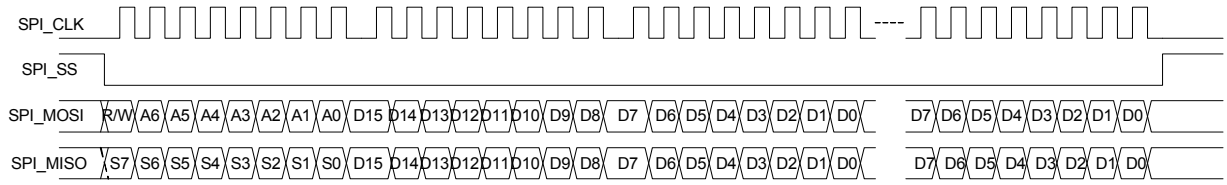
- Table 3 -

6. Digital base band interface and control

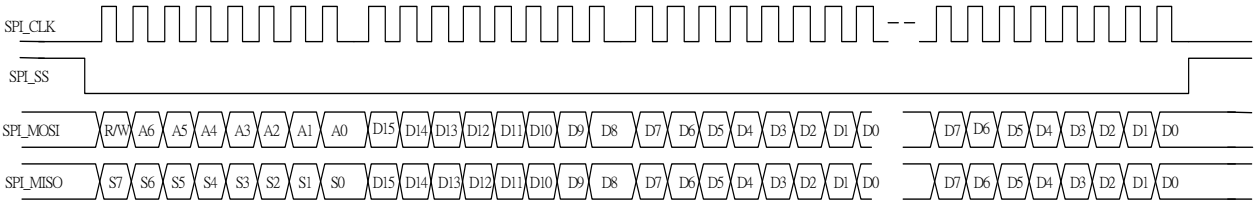
6.1 SPI Command Format

The SPI interface is used to program the module via the 4 pins SPI_CLK, SPI_SS, SPI_MOSI and SPI_MISO. The SPI_MOSI and SPI_CLK pins are used to load data into an internal shift register. The SPI_MOSI and SPI_CLK pins are use to send data to microcontroller.

Format 1
CKPHA = 0:



Format 2
CKPHA = 1:

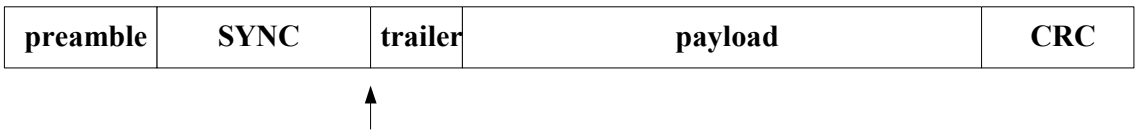


- Fig. 3 –

Note: Default setting is format 1.

6.2 Register Information

6.2.1 Package type define and FIFO point set



Automatically set FIFO write_point=0,when RX received SYNC.

Automatically set FIFO read_point=0,when RX received SYNC or after transmit SYNC when TX.

* Preamble: 1 ~ 8 bytes programmable
* SYNC: 32/48/64 bits programmable as device syncword
* Trailer: 4~16 bits programmable
* Payload: TX/RX data, there are 4 data types: raw data, 8_10 bits, Manchester, interleave with FEC option
* CRC: 16 bit CRC is option

Note: For transmit, it is needed to clear FIFO write point before application write in data via access reg82[15].

6.2.2 Digital interface

RF module interface with uC consisting of SPI interface plus two handshake signals (Table 2).

The WT24C02V02 SPI can only support slave mode,SPI clock =< 12MHz.

Pin	Description
SPI_CLK	**SPI clock input**
SPI_SS	**SPI slave select input**
SPI_MOSI	**SPI data in**
SPI_MISO	**SPI data out**
PKT_FLAG	**Packet TX/RX flag**
RESET_n	**Reset input, active low**

- Table 2 –

6.2.3 Typical register values

The following register values are recommended.

RF initiation

Reg address	Read/Write	Default value (Hexadecimal)	Recommend value (12MHz crystal frequency) (Hexadecimal)
0x09	R/W	3003	2182
0x00	R/W	CD51	345D
0x02	R/W	137B	1E01
0x04	R/W	3CD0	BCF0
0x05	R/W	0081	00A1
0x07	R/W	0030	124C
0x08	R/W	0404	8000
0x0A	R/W	0004	0004
0x0B	R/W	4041	4041
0x0C	R/W	0000	8000
0x0D	R/W	0000	0000
0x0E	R/W	6697	169B
0x0F	R/W	017B	0DED
0x10	R/W	F000	B000
0x12	R/W	E000	E000
0x13	R/W	2114	A114
0x14	R/W	819C	8195
0x15	R/W	6962	6962
0x16	R/W	0402	0002
0x17	R/W	0802	0002
0x18	R/W	B040	B140
0x19	R/W	7819	A80F
0x1A	R/W	6704	3F07
0x1C	R/W	1800	5800

- Table 5 -

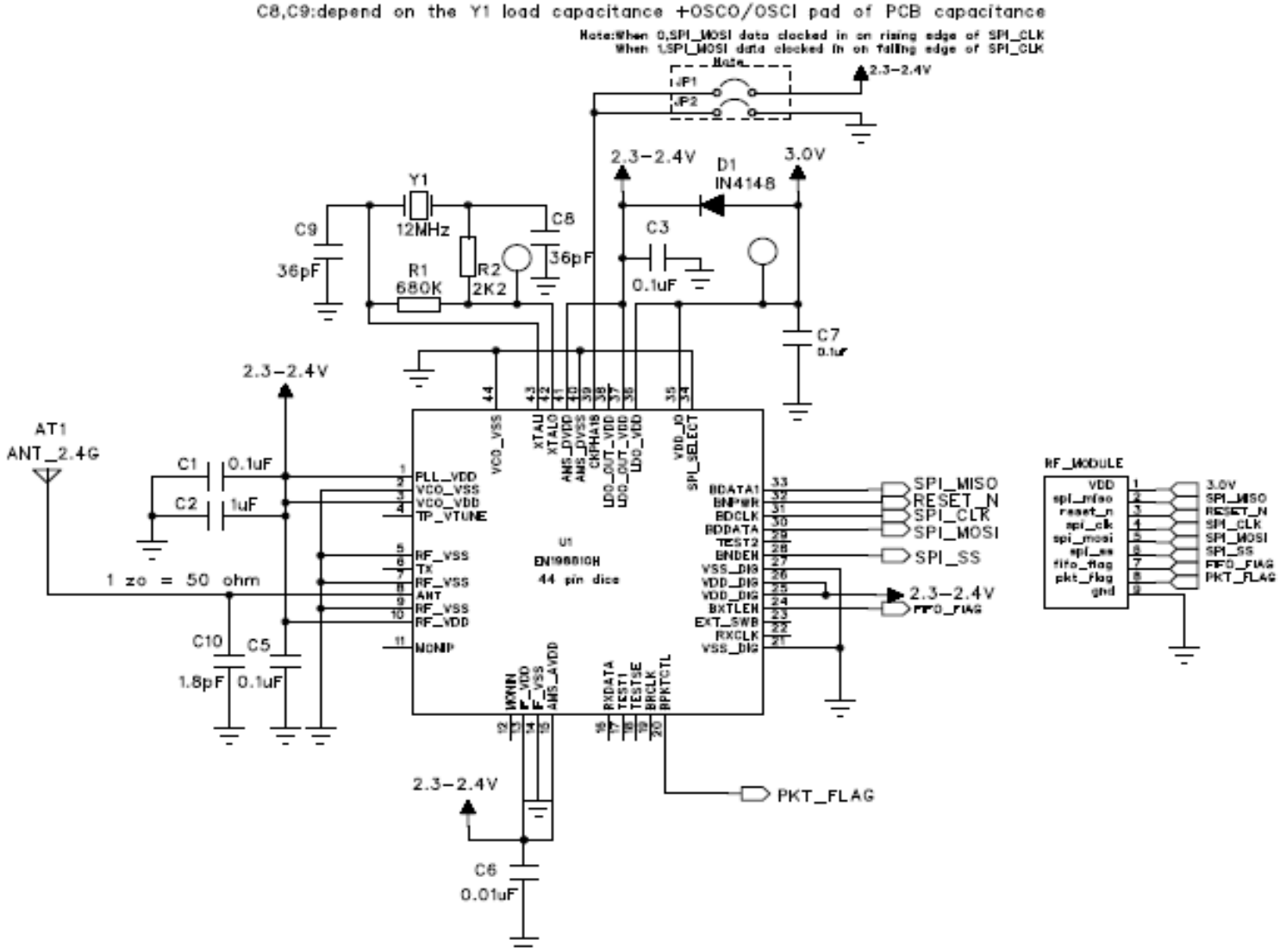
Framer initiation

Reg address	Read/Write	Default value (Hexadecimal)	Recommend value (12MHz crystal frequency) (Hexadecimal)
0x30	R/W	5800	9800
0x31	R/W	C00F	FF8F
0x32	R/W	9628	8018
0x33	R/W	8300	8056
0x34	R/W	0000	4EF6
0x35	R/W	0000	F6F5
0x36	R/W	0000	185C

0x37	R/W	0000	D651
0x38	R/W	4407	4444
0x39	R/W	B000	E000

- Table 6 –

7. Application Circuit



BOM list

Comment	Description	Tolerance	Designator	Quantity	Remark
1.8P/10V	1005 NPO Ceramic Capacitor	±0.25P	C10	1	Darfon/Murata or equal
36P/10V	1005 NPO Ceramic Capacitor	±5%	C8	1	Darfon/Murata or equal
36P/10V	1005 NPO Ceramic Capacitor	±5%	C9	1	Darfon/Murata or equal
10n/10V	1005 X7R Ceramic Capacitor	±10%	C6	1	Darfon/Murata or equal
100n/10V	1005 X7R Ceramic Capacitor	±10%	C1, C3, C5, C7.	4	Darfon/Murata or equal
1u/6.3V	1005 Y5V Ceramic Capacitor	±20%	C2	1	Darfon/Murata or equal
2K2	1005 Carbon Film Resistor	± 5%	R2	1	Yageo or equal
680K	1005 Carbon Film Resistor	±5%	R1	1	Yageo or equal
EM198810H	RF IC		U1	1	Elan
12MHz Crystal	HC-49US/CL20P	± 20ppm	Y1	1	LZ or equal
ANT	Diameter 1.2mm ,Length 31mm copper wire		ANT	1	
1N4148	Silicon Epitaxial Planar Diode(SMD)			1	
PCB	22 x 12 x 1.0 mm FR-4 PCB			1	

- Table 7 –

WAILLY TECHNOLOGY LTD.

Hong Kong:

Wailly Technology Ltd.
Unit 503-505,Fook Hong Industrial Building,
19 Sheung Yuet Road,Kowloon Bay,Kowloon,Hong Kong.
TEL: (852) 2756 4500
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DATA SHEET

EM198810

2.4 GHz ISM Band Transceiver/Framer IC

Production Data Sheet

ELAN MICROELECTRONICS CORP.
No.12, Innovation 1st RD., Science-based Industrial Park
Hsin Chu, Taiwan, R.O.C.
TEL: (03) 5639977
FAX: (03) 5782037(SL) 5630118 (SA2)

CONTENTS

2.4 GHz ISM BAND TRANSCEIVER/FRAMER IC

1. FEATURES

The EM198810 is a CMOS integrated circuit that performs all functions from the antenna to the microcontroller for transmission and reception of a 2.4GHz digital data. This transceiver IC integrates most of the functions required for data transmission into a single integrated circuit. Additionally, the programmability implemented reduces significantly external components count, board space requirements and external adjustments.

Key Features:

- Combines 2.4 GHz GFSK RF transceiver with 8-bit data framer function
- Eliminates need for external software or hardware FIFO; offloads MCU for other tasks
- Simple microprocessor interface – 4 wires for SPI, plus 3 wires for RST/buffer control
- Each transmit, receive buffer is 64 bytes deep
- Long packets are possible if buffers are read/written before overflow/underflow occurs
- Always 1Mbps over-the-air symbol rate, regardless of MCU speed or architecture
- Preamble can be 1 to 8 bytes
- Supports 1, 2, 3, or 4 word address (up to 64 bits)
- Various Payload data formats to eliminate DC offset, enhance receive clock recovery and BER
- Programmable data whitening
- Supports Forward Error Correction (FEC): none, 1/3, or 2/3
- Supports 16-bit CRC
- Baseband output clock available
- Power management for minimizing current consumption
- 5x5mm QFN package with minimum RF parasitic
- Lead-free packaging and dice is available on request

Applications

- Wireless devices that need quick time-to-market
- Simple and fast wireless data networks
- Cordless headsets and Cellular Phones
- Wireless streaming audio
- Wireless voice and VOIP
- Wireless Skype earphone
- Home and factory automation
- Wireless security and access control
- Battery Powered wireless devices

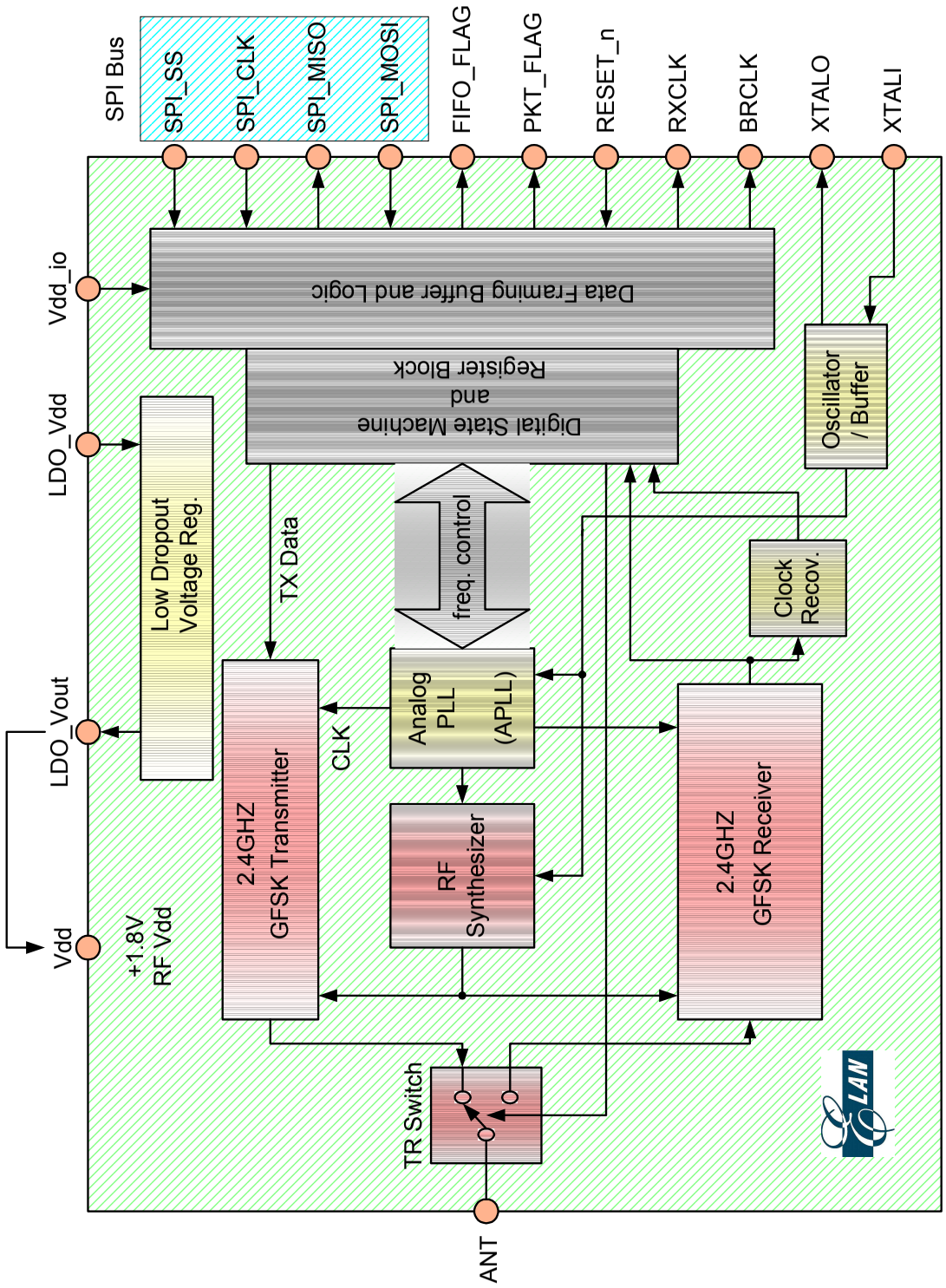
1.1 Description

The Elan EM198810 IC is a low-cost, fully integrated CMOS radio frequency (RF) transceiver block, combined with a 64-byte buffered framer block. The RF transceiver block is a self-contained, fast-hopping GFSK data modem, optimised for use in the widely available 2.4 GHz ISM band. It contains transmit, receive, VCO and PLL functions, including an on-chip channel filter and resonator, thus minimizing the need for external components. The receiver utilizes extensive digital processing for excellent overall performance, even in the presence of interference and transmitter impairments. Transmit power is digitally controlled. The low-IF receiver architecture results in sensitivity to -80dBm or better, with impressive selectivity.
In normal applications, the EM198810 is connected to a low cost microcontroller(ex:EM78P451S).

In normal application The on-chip framer processes and stores the RF data in the background, unloading this critical timing function from the MCU. This lowers MCU speed requirements, expedites product development time, and frees the MCU for implementing additional product features.

The framer register settings determine the over-the-air formatting characteristics. Many configurations are possible, depending on the user's specific needs. Raw transmit data is easily sent over-the-air as a complete frame of data, with preamble, address, payload, and CRC. Receiving data is just the opposite, using the preamble to train the receiver clock recovery, then the address is checked, then the data is reverse formatted for receive, followed by CRC. All of this is done in hardware to ease the programming and overhead requirements of the baseband MCU.
For longer battery life, power consumption is minimized by automatic enabling of the various transmit, receive, PLL, and PA sections, depending on the instantaneous state of the chip. A sleep mode is also provided for ultra low current consumption.
This product is available in 32-lead 5x5 mm JEDEC standard QFN package, featuring an exposed pad on the bottom for best RF characteristics. Lead-free RoHS compliant packaging is available on request.

2. Block diagram



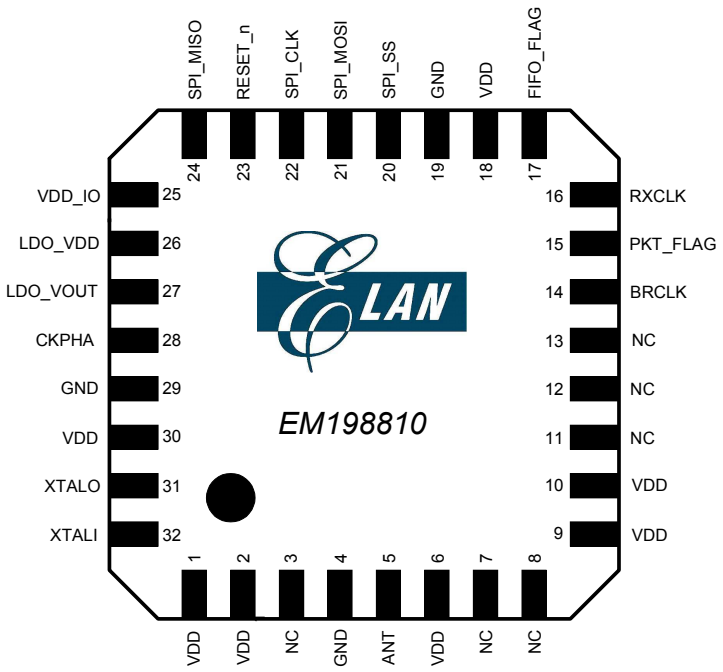
- Fig. 1 –

3. Pins names and pins location

3.1 Pins names

SYMBOL	Type	PIN	DESCRIPTION
VDD	PWR	1	Power supply voltage.
VDD	PWR	2	
NC	--	3	DO NOT CONNECT. Reserved for factory test.
GND	GND	4	Ground connection.
ANT	50ΩRF	5	RF input/output.
VDD	PWR	6	Power supply voltage.
NC	--	7	DO NOT CONNECT. Reserved for factory test.
NC	--	8	
VDD	PWR	9	Power supply voltage.
VDD	PWR	10	
NC	--	11	DO NOT CONNECT. Reserved for factory test.
NC	--	12	
NC	--	13	
BRCLK	O	14	Outputs 1MHz TX symbol clock, 12MHz APLL, or crystal clock. See register definitions for details.
PKT_FLAG	O	15	Transmit/Receive packet process flag.
RXCLK	O	16	Receiver symbol timing clock recovery output. Fixed at 1MHz fundamental rate.
FIFO_FLAG	O	17	FIFO full/empty flag.
VDD	PWR	18	Power supply voltage.
GND	GND	19	Ground connection.
SPI_SS	I	20	Enable line for the SPI bus. Active low.
SPI_MOSI	I	21	Data input for the SPI bus.
SPI_CLK	I	22	Clock line for the SPI bus.
RESET_n	I	23	When RESET_n is low, most of the chip shuts down to conserve power. When raised high, RESET_n is used to turn on the chip,restoring all registers to their default value.
SPI_MISO	O	24	Data output for the SPI bus.
VDD_IO	PWR	25	Vdd for the digital i/o pins. Nominally +3.3 VDC.
LDO_VDD	PWR	26	Unregulated input to the on-chip LDO volt. regulator.
LDO_OUT	PWR	27	+1.8V output of the on-chip LDO voltage regulator.
CKPHA	DI	28	SPI clock phase. When 0, SPI_MOSI data clocked in on rising edge of SPI_CLK. When 1, SPI_MOSI data clocked in on falling edge of SPI_CLK.
GND	GND	29	Ground connection.
VDD	PWR	30	Power supply voltage.
XTALO	AO	31	Output of the crystal oscillator gain block.
XTALI	AI	32	Input to the crystal oscillator gain block.
GND	GND	Exposed pad	Ground connection.

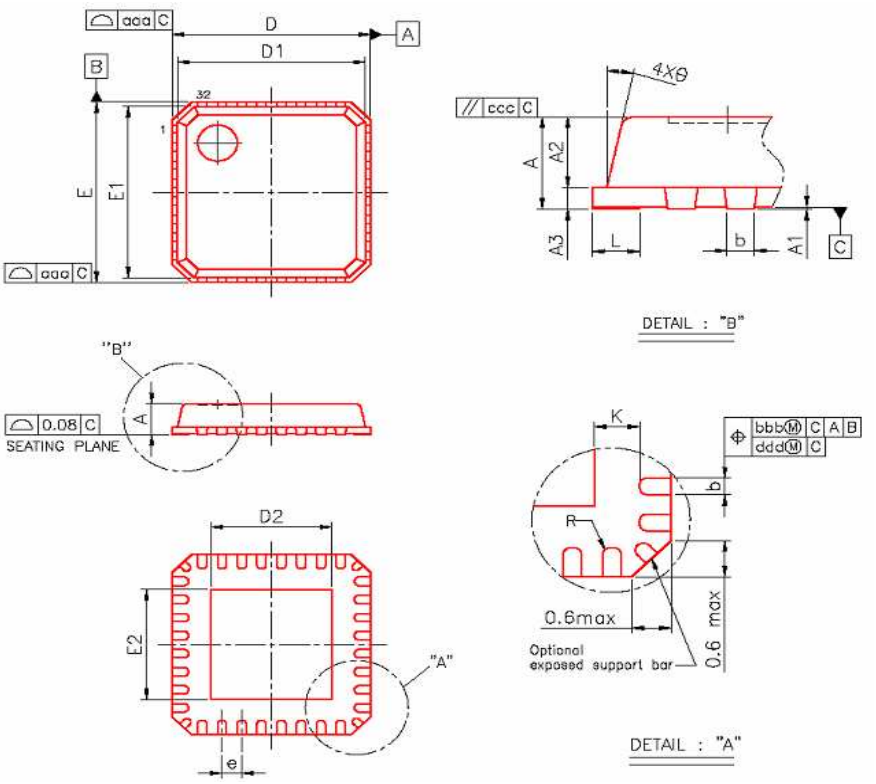
- Table 1 –



- Figure 2 –

3.2 Package Outline

QFN32 Lead Exposed Pad Package, 5x5 mm Pkg. 0.5mm Pitch (JEDEC) MO-220-A



Dim.	Min.	Nom.	Max.	Dim.	Min.	Nom.	Max.
A	0.80	0.85	1.00	L	0.30	0.40	0.50
A1	0.00	0.02	0.05	θ	0°	–	12°
A2	0.60	0.65	0.80	R	0.09	–	–
A3		0.20 REF		K	0.20	–	–
b	0.18	0.25	0.30	aaa	–	–	0.15
D/E		5.00 BSC		bbb	–	–	0.10
D1/E1		4.75 BSC		ccc	–	–	0.10
D2/E2	3.15	3.30	3.45	ddd	–	–	0.05
e		0.50 BSC					

3.3 Pads name and location

SYMBOL	PAD no	Center pad position	
		X um	Y um
PLL_VDD(A)	1	41.71	1629.675
VCO-VSS(A)	2	41.71	1505.481
VCO_VDD(A)	3	41.71	1385.661
TP_VTUNE(A)	4	41.71	1264.66
RF_VSS(A)	5	41.71	1025.481
TX(A)	6	41.71	904.661
RF_VSS(A)	7	41.71	785.482
ANT(A)	8	41.71	664.661
RF_VSS(A)	9	41.71	545.482
RF_VDD(A)	10	41.71	425.662
MONIp(A)	11	41.71	184.8
MONIn(A)	12	228.8	41.71
IF_VDD(A)	13	347.799	41.71
IF_VSS(A)	14	467.979	41.71
AMS_AVDD(A)(IF_VDD(A))	15	587.62	41.71
RXDATA(A)	16	1465.94	40.71
TEST1	17	1585.94	40.71
Testse(A)	18	1705.94	40.71
BRCLK(D)	19	1825.94	40.71
BPKTCTL(D)	20	1945.94	40.71
VSS_DIG(D)	21	2087.058	227.595
RXCLK(D)	22	2087.058	346.595
ext_swb(D)	23	2087.058	466.595
BXTLEN(D)	24	2087.058	586.595
VDD_DIG(D)	25	2087.058	706.595
VDD_DIG(D)	26	2087.058	826.595
VSS_DIG(D)	27	2087.058	947.595
BnDEN(D)	28	2087.058	1066.595
TEST2(D)	29	2087.058	1186.595
BDDATA(D)	30	2087.058	1306.595
BDCLK(D)	31	2087.058	1427.501
BnPWR(D)	32	2087.058	1546.594
BDATA1(D)	33	2087.058	1671.661
spi_select(D)	34	1891.458	1811.551
VDD_IO(D)	35	1768.299	1811.551
LDO_VDD(A)	36	1571.298	1811.551
LDO_OUT_VDD(A)	37	1444.377	1810.551
LDO_OUT_VDD(A)	38	1324.379	1810.551
ckpha18(A)	39	1205.286	1811.551
AMS_DVSS(A)	40	1081.401	1810.551
AMS_DVDD(A)	41	961.221	1810.551
XTALO(A)	42	839.399	1810.65
XTALI(A)	43	677.411	1810.65
VCO_VSS(A)	44	266.913	1810.553

- Table 2 -

3.4 Order information

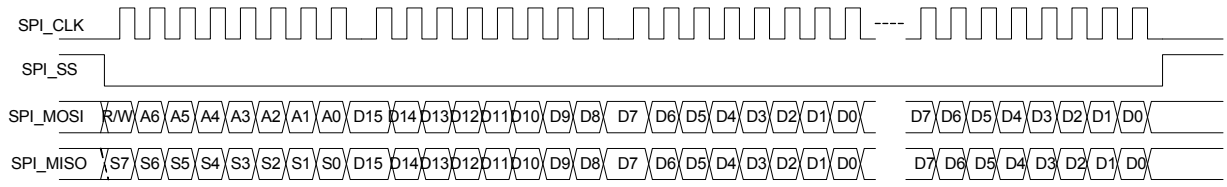
Type number	Package	
	Name	Description
EM198810W	QFN32	Plastic, quad flat package; no leads; 32 terminals; body 5 x 5 x 0.8 mm
EM198810H	Bare die	available

4 Digital Base Band Interface

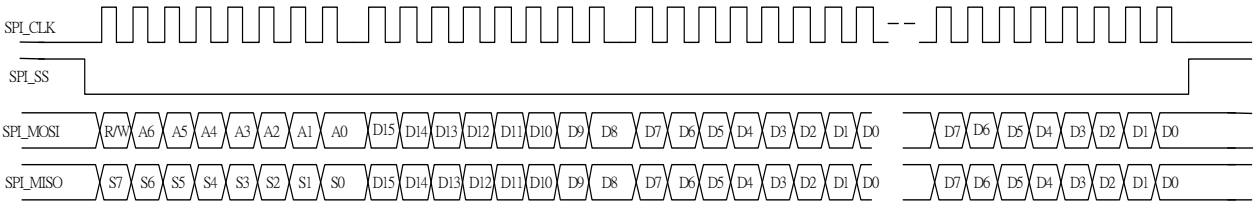
4.1 SPI Command Format

The SPI interface is used to program the IC via the 4 pins SPI_CLK, SPI_SS, SPI_MOSI and SPI_MISO. The SPI_MOSI and SPI_CLK pins are used to load data into an internal shift register. The SPI_MOSI and SPI_CLK pins are use to send data to microcontroller. The data are loaded into the shift register and sent to microcontroller on the falling edge of the clock SPI_CLK and latched on the rising edge of the SPI_SS signal. When the SPI_SS pin is high, the data stored in the shift register is retained even if a SPI_CLK is applied. When the SPI_SS pin is low the data can be rewritten and resent. Inputs timing of the SPI_CLK, SPI_SS, SPI_MOSI and SPI_MISOD are shown in the Fig.3.

Format 1
CKPHA = 0:



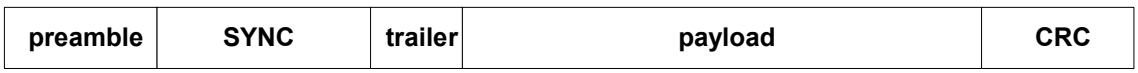
Format 2
CKPHA = 1:



- Fig. 3 –

4.2 Register Information

4.2.1 Package type define and FIFO point set



Automatically set FIFO write_point=0
when RX received SYNC

Automatically set FIFO read_point=0
when RX received SYNC or after transmit SYNC when TX

- Figure 4 –

* Preamble: 1 ~ 8 bytes programmable
* SYNC: 32/48/64 bits programmable as device syncword
* Trailer: 4~16 bits programmable
* Payload: TX/RX data, there are 4 data types: raw data, 8_10 bits, Manchester, interleave , with FEC option
* CRC: 16 bit CRC is option

Note: For transmit, it is needed to clear FIFO write point before application write in data via access reg82[15].

4.2.2 Digital Interface

It is very simple interface with application, consisting of SPI interface plus two handshake signals (Table 2).
The EM198810 SPI can only support slave mode.

Pin	Description
SPI_CLK	SPI clock input
SPI_SS	SPI slave select input
SPI_MOSI	SPI data in
SPI_MISO	SPI data out
PKT_FLAG	Packet TX/RX flag
FIFO_FLAG	FIFO full/empty
RESET_n	Reset input, active low

- Table 3 -

4.2.3 Typical Register Values

The following register values (Table 3) are recommended for the Elan Microelectronics details define refer to registers definitions

Reg. address	Read/Write	Default value (Hexadecimal)	Recommend value (12MHz crystal frequency) (Hexadecimal)
0	R/W	0000	CD51
2	R/W	00C1	0061
4	R/W	0688	3CD0
5	R/W	0041	00A1
9	R/W	0003	3003
14	R/W	6617	6697
16	R/W	0000	F000
18	R/W	FC00	E000
19	R/W	0014	2114
20	R/W	8103	819C
21	R/W	0962	6962
22	R/W	2602	0402
23	R/W	2602	0802
24	R/W	30C0	B080
25	R/W	3814	7819
26	R/W	5304	6704
48	R/W	1800	5800
51	R/W	4000	A000
56	R/W	4407	4407
57	R/W	B000	E000*

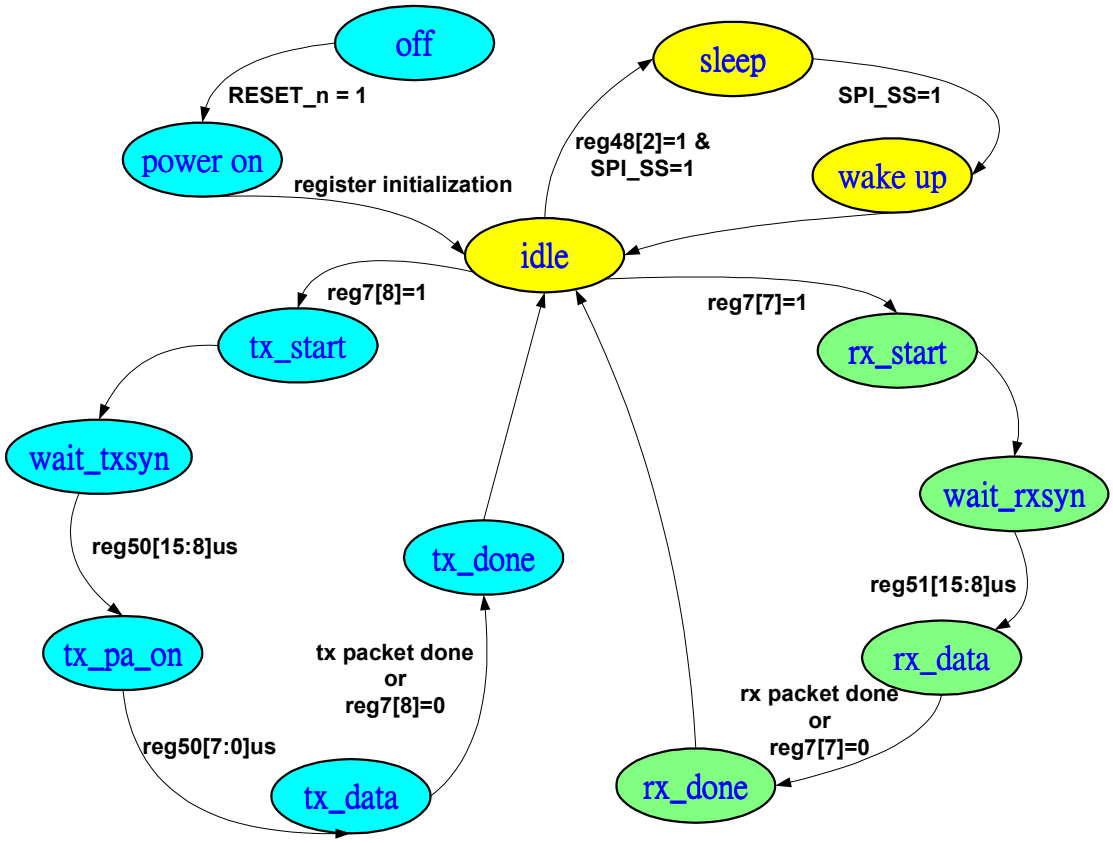
- Table 4 -

- Reg57, if MCU handle packet length and framer detect FIFO fully empty, Reg57=0xC080
- Reg57, if MCU handle packet length and terminates TX done, Reg57=0xC000

For more detail description about digital base band interface, please refer to application note AN198810-1.

For the latest register value recommendations, please contact Elan Microelectronics technical group.

4.2.4 State Diagram



- Figure 5 -

5.Electrical Characteristics

5.1 Absolute Maximum Rating

Parameter	Symbol	Rating			Unit
		Min.	Typ.	Max.	
Operating Temp.	T_{OP}	-40		+85	℃
Storage Temp.	$T_{STORAGE}$	-55		+125	℃
V_{DD_IO} Supply Voltage	V_{DDIO_MAX}			+3.7	VDC
V_{DD} Supply Voltage	V_{DD_MAX}			+2.5	VDC
Applied Voltages to Other Pins	V_{OTHER}	-0.3		+3.7	VDC
Input RF Level	P_{IN}			+10	dBm
Output Load mismatch (Z_0=50 ohm)	$VSWR_{OUT}$			10:1	VSWR

- Table 5 -

Note: 1.Absoute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics section below.

2.These devices are electro-static sensitive. Devices should be transported and stored in anti-static containers. Equipment and personnel contacting the devices need to be properly grounded. Cover workbenches with grounded conductive mats.

5.2 Characteristics

The following specifications are guaranteed for T_A=25℃, V_{DD}=1.80±0.18VDC, unless otherwise noted:

Parameter	Symbol	Specification			Unit	Test Condition and Notes
		Min.	Typ.	Max.		
Current Consumption						
Current Consumption - TX	I_{DD_TX}		26		mA	P_{OUT} = nominal output power
Current Consumption - RX	I_{DD_RX}		25		mA	
Current Consumption – DEEP IDLE	$I_{DD\_D\_IDLE}$		1.9		mA	RF Synthesizer and VCO: OFF (see Reg. 21)
Current Consumption – SLEEP	I_{DD_SLP}		3.5		uA	
Digital Inputs						
Logic input high	V_{IH}	0.8V_{DD_io}		V_{DD_io}	V	
Logic input low	V_{IL}	0		0.8	V	
Input Capacitance	$C_{\_IN}$			10	pF	
Input Leakage Current	$I_{\_LEAK\_IN}$			10	uA	
Digital Outputs						
Logic output high	V_{OH}	0.8V_{DD_io}		V_{DD_io}	V	
Logic output low	V_{OL}			0.4	V	
Output Capacitance	$C_{\_OUT}$			10	pF	
Output Leakage Current	$I_{\_LEAK\_OUT}$			10	uA	
Rise/Fall Time	$T_{\_RISE\_OUT}$			5	nS	
Clock Signals						
BRCLK output frequency	F_{BRCLK}		1, 12, or xtal Freq.		MHz	Depends on Register settings. Always either: 1 MHz Tx clock, 12 MHz APLL clock (Tx, Rx, and Idle), or the buffered 12 MHz crystal oscillator frequency.
SPI_CLK rise, fall time	T_{r_spi}			200	nS	Requirement for error-free register reading, writing.
SPI_CLK frequency range	F_{SPI}	0	12		MHz	
Overall Transceiver						
Operating Frequency Range	$F_{\_OP}$	2402		2482	MHz	

Antenna port mismatch (Z_0=50Ω)	$VSWR_I$		<2:1		VSWR	Receive mode. Meas. using 50 ohm balun.
	$VSWR_O$		<2:1		VSWR	Transmit mode. Meas. using 50 ohm balun.

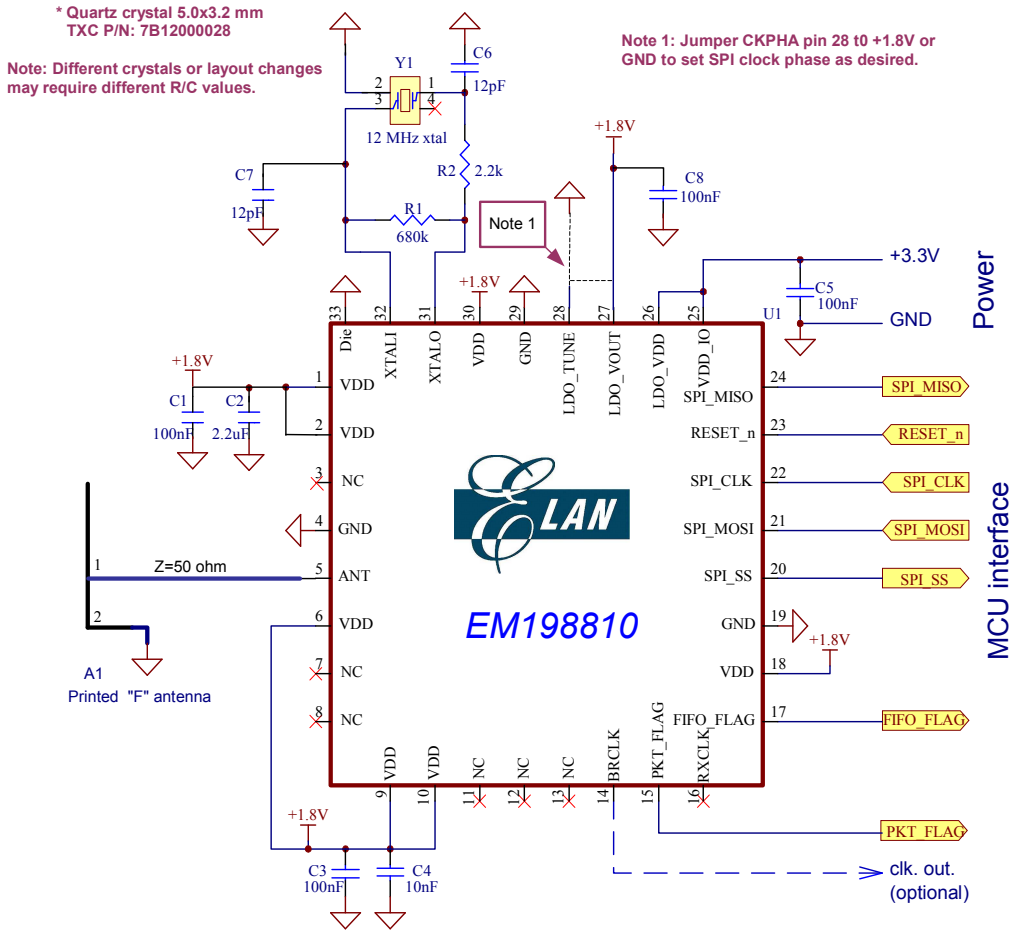
Receive Section: @ BER≦0.1%							
Receiver sensitivity				-85	-80	dBm	Meas. At antenna pin.
Maximum useable signal			-20			dBm	
Input 3rd order intercept point		IIP_3	-14	-11		dBm	
Data (Symbol) rate		T_S		1		uS	
Min. Carrier/Interference ratio: @ BER≦0.1%							
Co-Channel Interference		$CI_{cochannel}$		9	11	dB	-60 dBm desired signal.
Adjacent Ch. Interference, 1MHz offset		CI_{-1}		-1.5	0	dB	-60 dBm desired signal.
Adjacent Ch. Interference, 2MHz offset		CI_{-2}		-30		dB	-60 dBm desired signal. Interference at 2 MHz below desired signal.
Adjacent Ch. Interference, ≥ 3MHz offset		CI_{-3}		-40		dB	-67 dBm desired signal.
Image Frequency Interference		CI_{image}		-23	-9	dB	-60 dBm desired signal. Image freq. is always 2 MHz higher than desired signal.
Adjacent interference to Image (1MHz)		CI_{image_11}		-34	-20	dB	-67 dBm desired signal. Always 3 MHz higher than desired signal.
Out-of-Band Blocking		OBB_{-1}	-10			dBm	30 MHz to 2000 MHz; Meas. with ACX BF2520 ceramic filter on ant. pin. Desired sig.-70dBm.
		OBB_{-2}	-27			dBm	2000 MHz to 2400 MHz
		OBB_{-3}	-27			dBm	2500 MHz to 3000 MHz
		OBB_{-4}	-10			dBm	3000 MHz to 12.75 GHz
Transmit Section: Reg. 9, bits 15-8 set to 00000000							
RF Output Power		P_{AV}		+2		dBm	Power Level 0 Meas. Using ACX BL2012 balun.
Modulation Characteristics							
Peak FM Demodulation.	00001111 pattern	$\triangle f1_{avg}$	280	314	350	KHz	
	01010101 pattern	$\triangle f2_{max}$	230			KHz	For at least 99.9% of all $\Delta f2_{max}$ meas.
ISI, % Eye Open		$\triangle f2_{avg}/\triangle f1_{avg}$	80			%	1010 data sequence referenced to 00001111 data sequence
Zero Crossing Error		ZCERR	-125		+125	nS	+/- 1/8 of Symbol Period
In-Band Spurious Emission							
+/- 550kHz		IBS_1			-20	dBc	
2MHz offset		IBS_2			-40	dBm	
>3MHz offset		IBS_3			-60	dBm	
Out-of-Band Spurious Emission							
Operation		OBS_O_1		<-60	-36	dBm	30 MHz ~ 1 GHz
		OBS_O_2		-45	-30	dBm	1 GHz ~ 12.75 GHz, excludes desired signal.
		OBS_O_3		<-60	-47	dBm	1.8 GHz ~ 1.9 GHz
		OBS_O_4		<-65	-47	dBm	5.15 GHz ~ 5.3 GHz
RF VCO and PLL Section							
Typical PLL lock range		F_{LOCK}	2340		2560	MHz	
TX, RX Frequency Tolerance				--		ppm	Same as XTAL pins frequency tolerance
Channel (Step) Size				1		MHz	
SSB Phase Noise				-95		dBc/Hz	550KHz offset
				-115		dBc/Hz	2MHz offset

Crystal oscillator freq. range (Reference Frequency)			12		MHz	Designed for 12 MHz crystal reference freq.	
Crystal oscillator digital trim range, typ.		-12		+12	ppm		
RF PLL Settling Time	T_{HOP}		75	150	uS		
Out-of-Band Spur. Emissions	$OBS_{\_1}$		<-75	-57	dBm	30 MHz ~ 1 GHz	IDLE state, Synthesizer and VCO ON.
	$OBS_{\_2}$		-68	-47	dBm	1 GHz ~ 12.75 GHz	
LDO Voltage Regulator Section							
Dropout Voltage	V_{do}			TBD	V	Measured during Receive state	
Quiescent current	I_q			6	uA	No-load current consumed by LDO reg.	

- Table 6 -

6. Application Circuit

Typical Application



Simple, low-power (0dBm) 2.4GHz RF
Transceiver with Framing and Data buffers

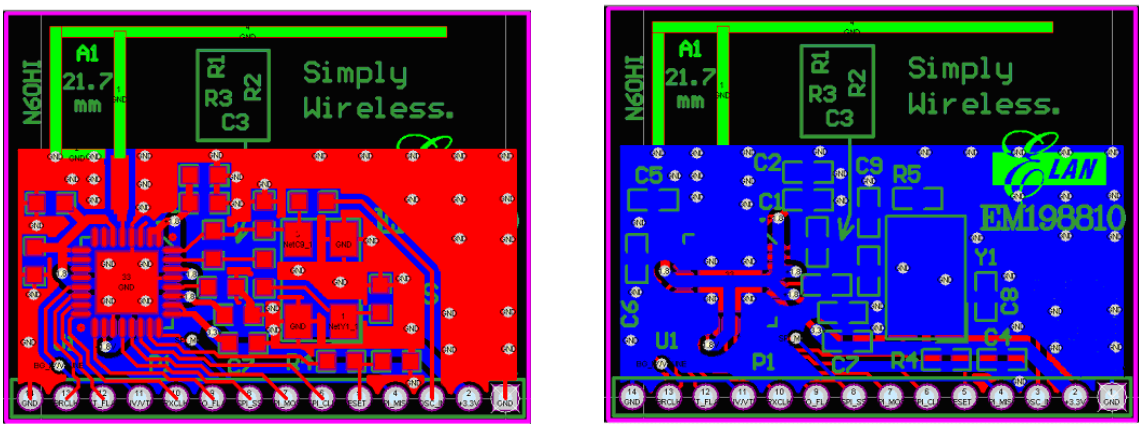
- Figure 6 -

BOM list

Comment	Description	Designator	Quantity	Footprint
10pF	Capacitor	C8	1	SMD-0603
12pF	Capacitor	C9	1	SMD-0603
10nF	Capacitor	C6	1	SMD-0603
100nF	Capacitor	C1 C3 C5 C7	4	SMD-0603
2.2uF	Capacitor	C2	1	SMD-0603
0 ohm	Resistor	R4	1	SMD-0603
2.2k	Resistor	R2	1	SMD-0603
680k	Resistor	R1	1	SMD-0603
12MHz	Crystal	Y1	1	OSC 5x3.2
EM198810	IC	U1	1	QFN 32 5x5
CON1x14	Connector	P1	1	HDR1x14

- Table 7 -

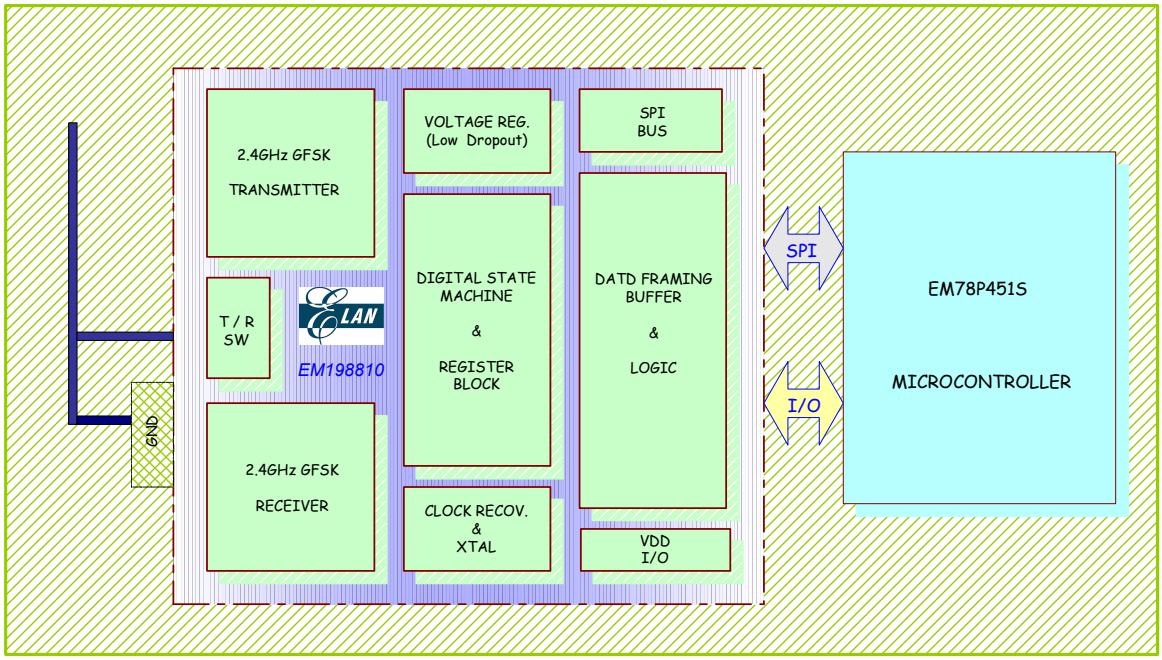
PCB layout



Top layer **Bottom layer**

- Figure 7 -

Wireless Personal Area Network Solution



Elan Wireless personal area network Total Solution

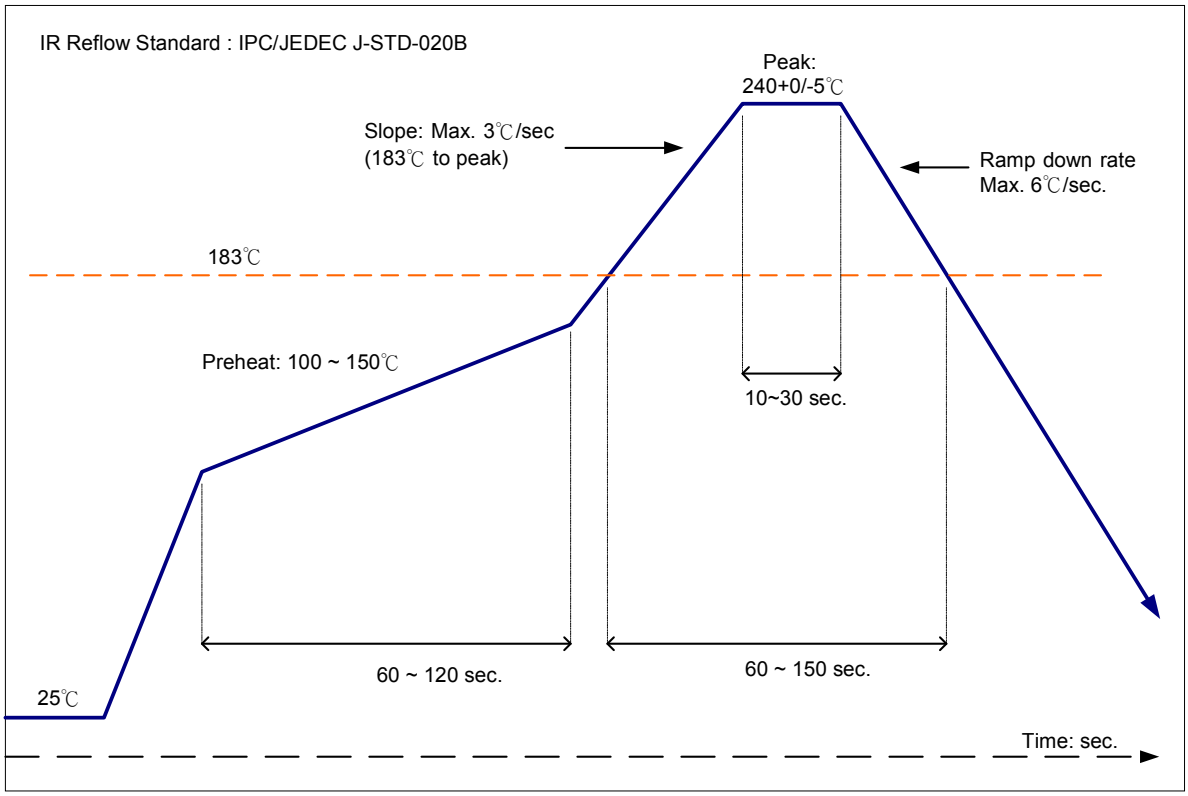
- Fig. 8 –

7. SOLDERING

Reflow soldering requires paste to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Several methods exist for reflowing, throughput times vary between 100 and 300 seconds depending on heating method.

Recommendation: Follow IPC/JEDEC J-STD-020B

Condition: Average ramp-up rate (183℃ to peak): 3℃/sec. max.
Preheat: 100 ~ 150℃ 60 ~ 120 sec.
Temperature maintained above 183℃: 60 ~ 150sec.
Time within 5℃ of actual peak temperature: 10 ~ 30sec.
Peak temperature: 240+0/-5℃
Ramp-down rate: 6℃/sec. max.
Time 25℃ to peak temperature: 6 minutes max.
Cycle interval: 5 minutes



- Fig. 9 -

DATA SHEET STATUS

Data Sheet Status	Product Status	Definitions
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