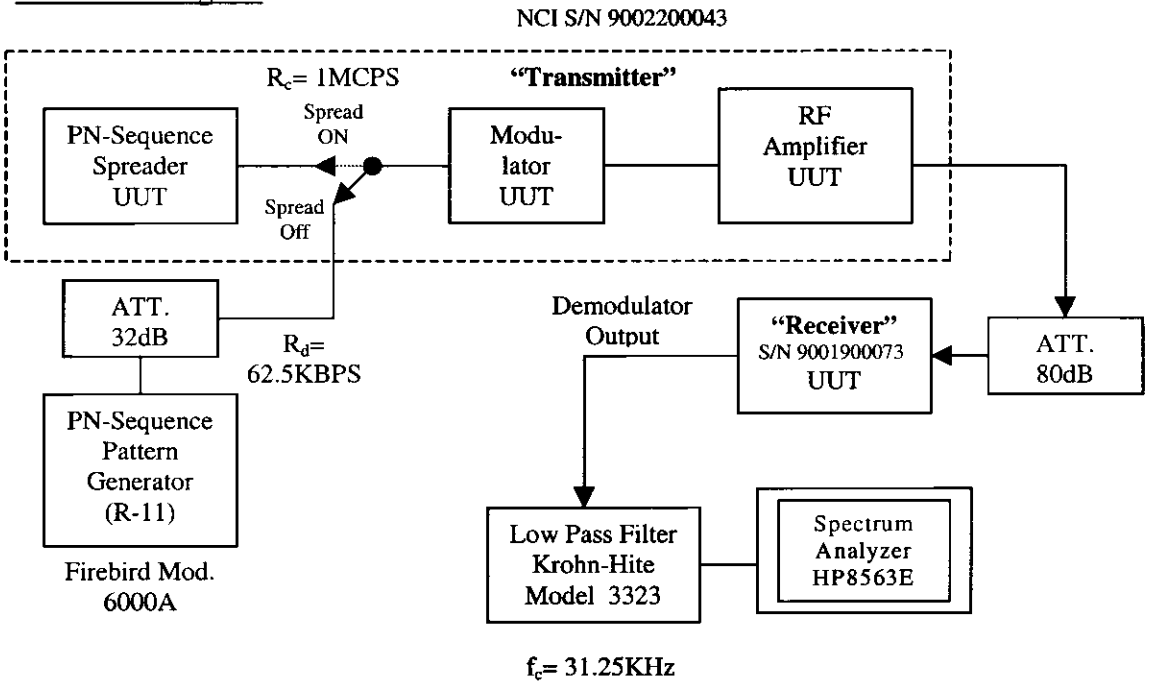
"Processing Gain Measurement"
Reference: FCC Requirements Part 15, Paragraph 15.247, (e), (1)

Test block diagram:

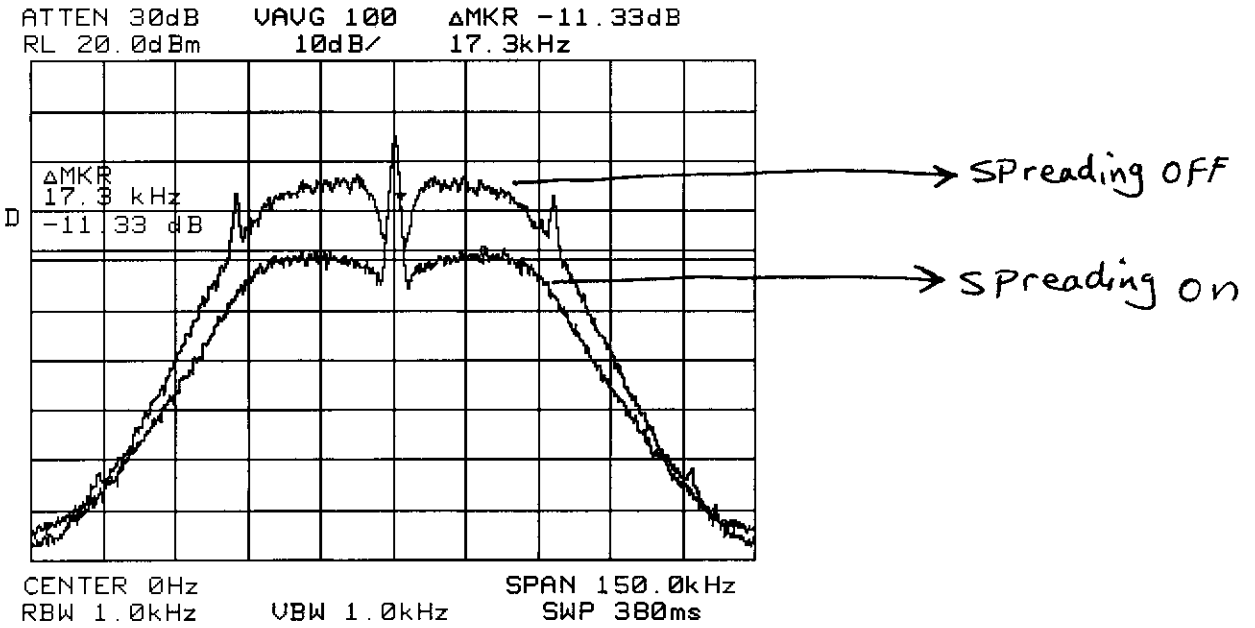


Test Parameters:

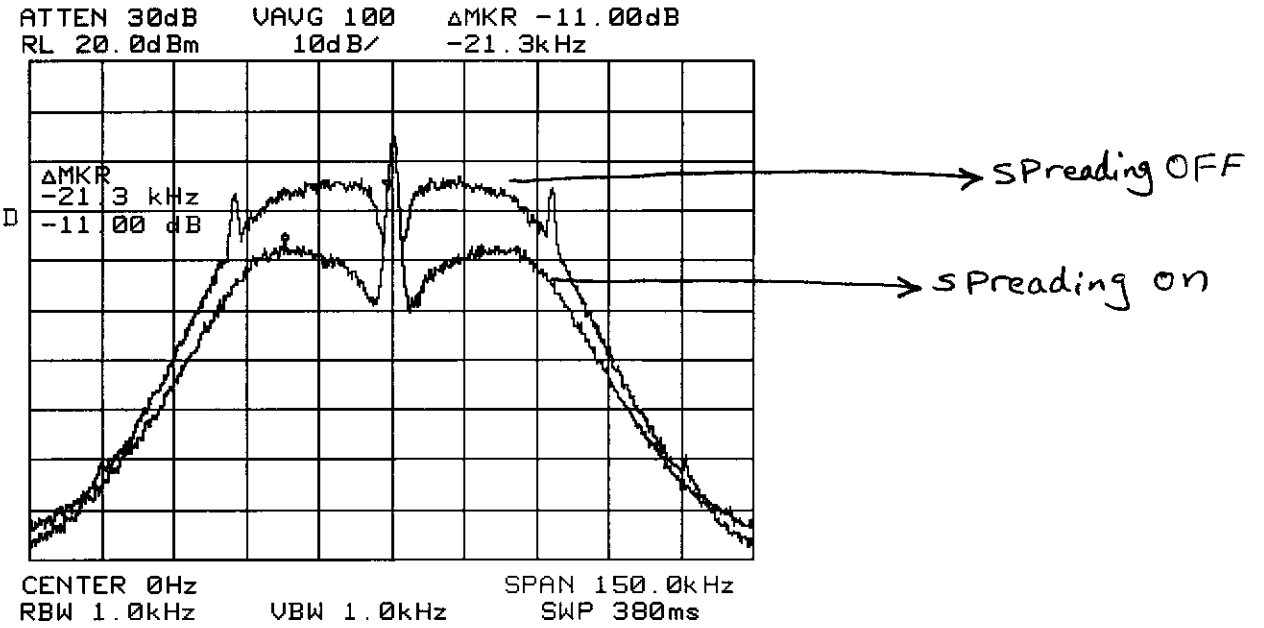
1) Data rate R_d= 62.5KBPS
   Symbol rate R_s= 31.25KSPS
2) Chip Rate R_c= 1MCPS
3) Processing gain G_p= 10*Log(R_c/R_d)= 12dB
4) Receiver lowpass filter cut-off frequency
   f_c= symbol rate= 31.25KHz
5) Lowpass filter characteristic: Maximally flat, 48dB/Octave

Test method (para. 15.247 (e) (1)):

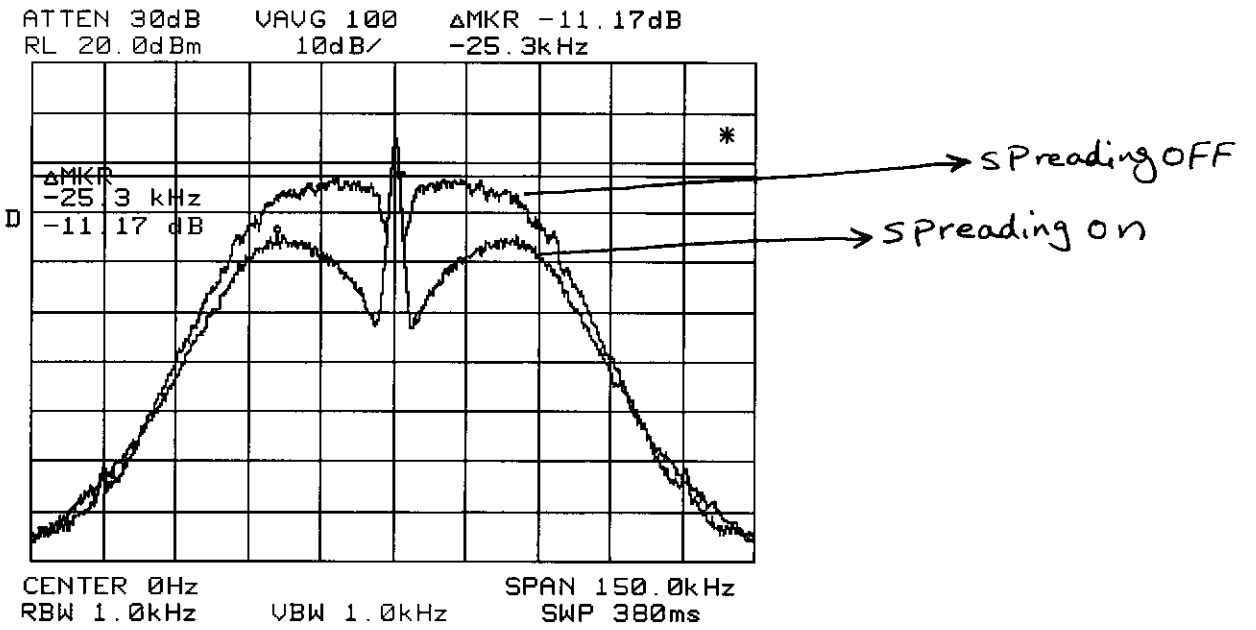
1) The data sequence is generated by the PN-Sequence pattern generator at 62.5KHz . This generator emulates the original data generated internally by the ASIC chip in the UUT. The test pattern used is a maximal sequence of length 2047 (R-11).
2) The processing gain is the difference between the unspread S/N to the spread S/N at the output of the lowpass filter, expressed in "dB".
3) Since the noise power at the output of the lowpass filter does not change when the signal is unspread or spread, the processing gain is measured by comparing the power spectrum of the unspread and spread signals.



Processing Gain > 11.33 dB @ chan ϕ



Processing Gain > 11.0 dB @ ch 8



Processing Gain > 11.17 dB @ ch 16