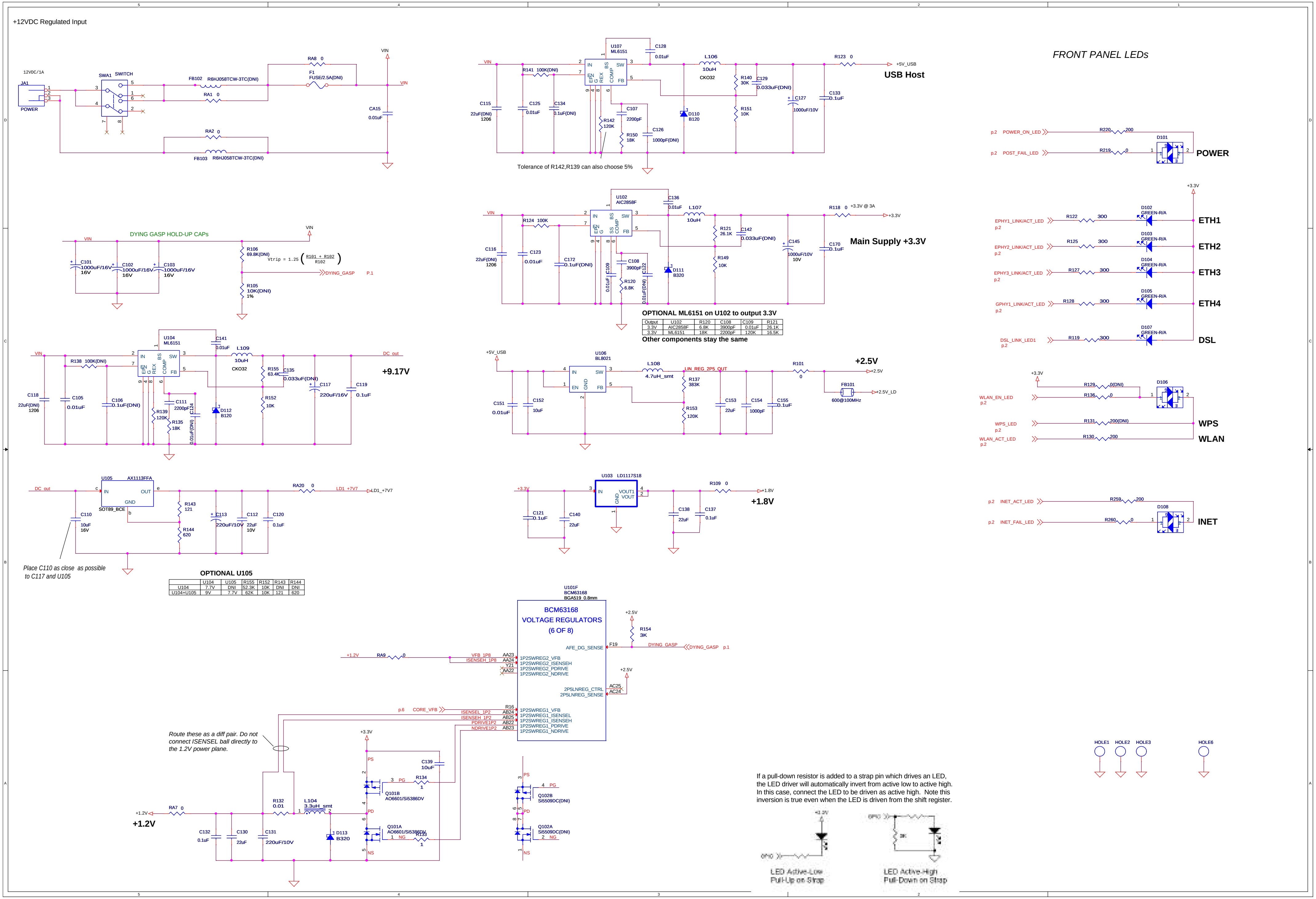


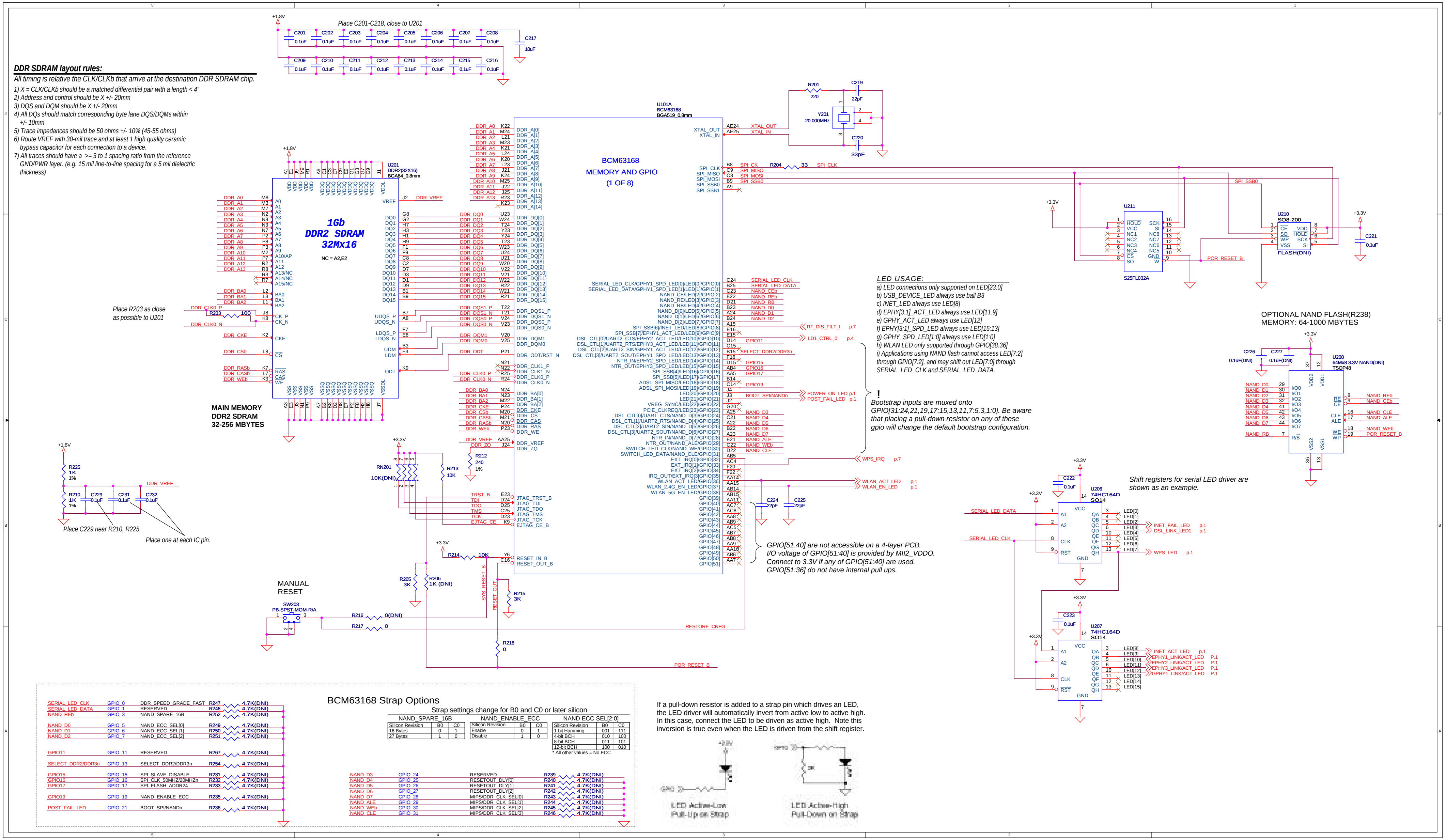
OPTIONAL ML6151 on U102 to output 3.3V

Output	U102	R120	C108	C109	R121
3.3V	AIC2858F	6.8K	3900pF	0.01uF	26.1K
3.3V	ML6151	18K	2200pF	120K	16.5K

Other components stay the same

OPTIONAL U105

	U104	U105	R155	R152	R143	R144
U104	7.7V	DNI	52.3K	10K	DNI	DNI
U104+U105	9V	7.7V	62K	10K	121	620



DDR SDRAM layout rules:

All timing is relative the CLK/CLKb that arrive at the destination DDR SDRAM chip.

1) X = CLK/CLKb should be a matched differential pair with a length < 4"
2) Address and control should be X +/- 20mm
3) DQS and DQM should be X +/- 20mm
4) All DQs should match corresponding byte lane DQS/DQMs within +/- 10mm
5) Trace impedances should be 50 ohms +/- 10% (45-55 ohms)
6) Route VREF with 30-mil trace and at least 1 high quality ceramic bypass capacitor for each connection to a device.
7) All traces should have a >= 3 to 1 spacing ratio from the reference GND/PWR layer. (e.g. 15 mil line-to-line spacing for a 5 mil dielectric thickness)

LED USAGE:

a) LED connections only supported on LED[23:0]
b) USB_DEVICE_LED always use ball B3
c) INET_LED always use LED[8]
d) EPHY[3:1]_ACT_LED always use LED[11:9]
e) GPHY_ACT_LED always use LED[12]
f) EPHY[3:1]_SPD_LED always use LED[15:13]
g) GPHY_SPD_LED[1:0] always use LED[1:0]
h) WLAN LED only supported through GPIO[38:36]
i) Applications using NAND flash cannot access LED[7:2] through GPIO[7:2], and may shift out LED[7:0] through SERIAL_LED_CLK and SERIAL_LED_DATA.

!
Bootstrap inputs are muxed onto GPIO[31:24,21,19,17:15,13,11,7:5,3,1:0]. Be aware that placing a pull-down resistor on any of these gpio will change the default bootstrap configuration.

GPIO[51:40] are not accessible on a 4-layer PCB. I/O voltage of GPIO[51:40] is provided by MII2_VDDO. Connect to 3.3V if any of GPIO[51:40] are used. GPIO[51:36] do not have internal pull ups.

Shift registers for serial LED driver are shown as an example.

OPTIONAL NAND FLASH(R238)
MEMORY: 64-1000 MBYTES

MAIN MEMORY
DDR2 SDRAM
32-256 MBYTES

BCM63168 Strap Options

Strap settings change for B0 and C0 or later silicon

NAND_SPARE_16B

Silicon Revision	B0	C0
16 Bytes	0	1
27 Bytes	1	0

NAND_ENABLE_ECC

Silicon Revision	B0	C0
Enable	0	1
Disable	1	0

NAND ECC SEL[2:0]

Silicon Revision	B0	C0
1-bit Hamming	001	111
4-bit BCH	010	100
8-bit BCH	011	101
12-bit BCH	100	010

* All other values = No ECC

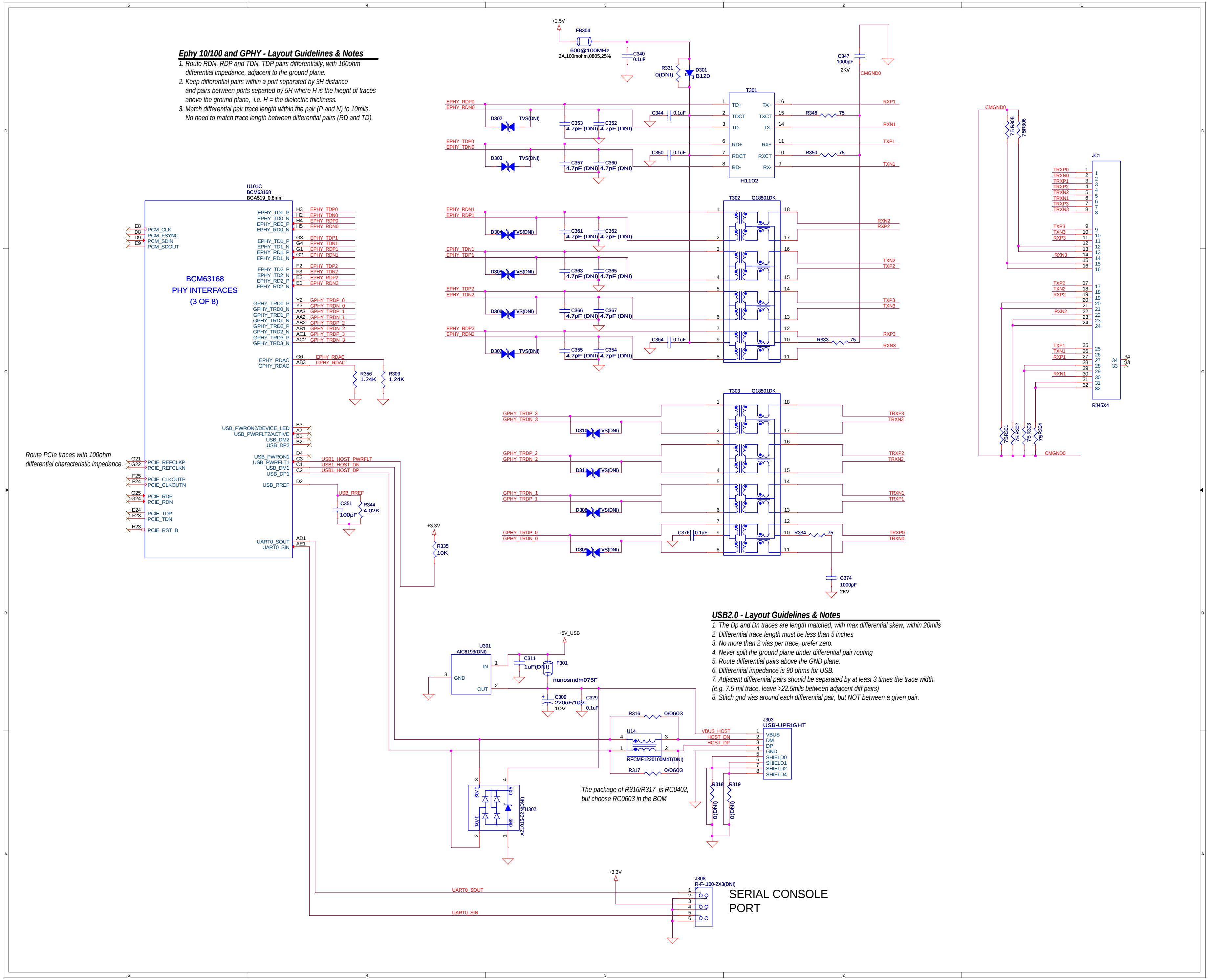
If a pull-down resistor is added to a strap pin which drives an LED, the LED driver will automatically invert from active low to active high. In this case, connect the LED to be driven as active high. Note this inversion is true even when the LED is driven from the shift register.

LED Active-Low
Pull-Up on Strap

LED Active-High
Pull-Down on Strap

Ephy 10/100 and GPHY - Layout Guidelines & Notes

1. Route RDN, RDP and TDN, TDP pairs differentially, with 100ohm differential impedance, adjacent to the ground plane.
2. Keep differential pairs within a port separated by 3H distance and pairs between ports separted by 5H where H is the hieght of traces above the ground plane, i.e. H = the dielectric thickness.
3. Match differential pair trace length within the pair (P and N) to 10mils. No need to match trace length between differential pairs (RD and TD).

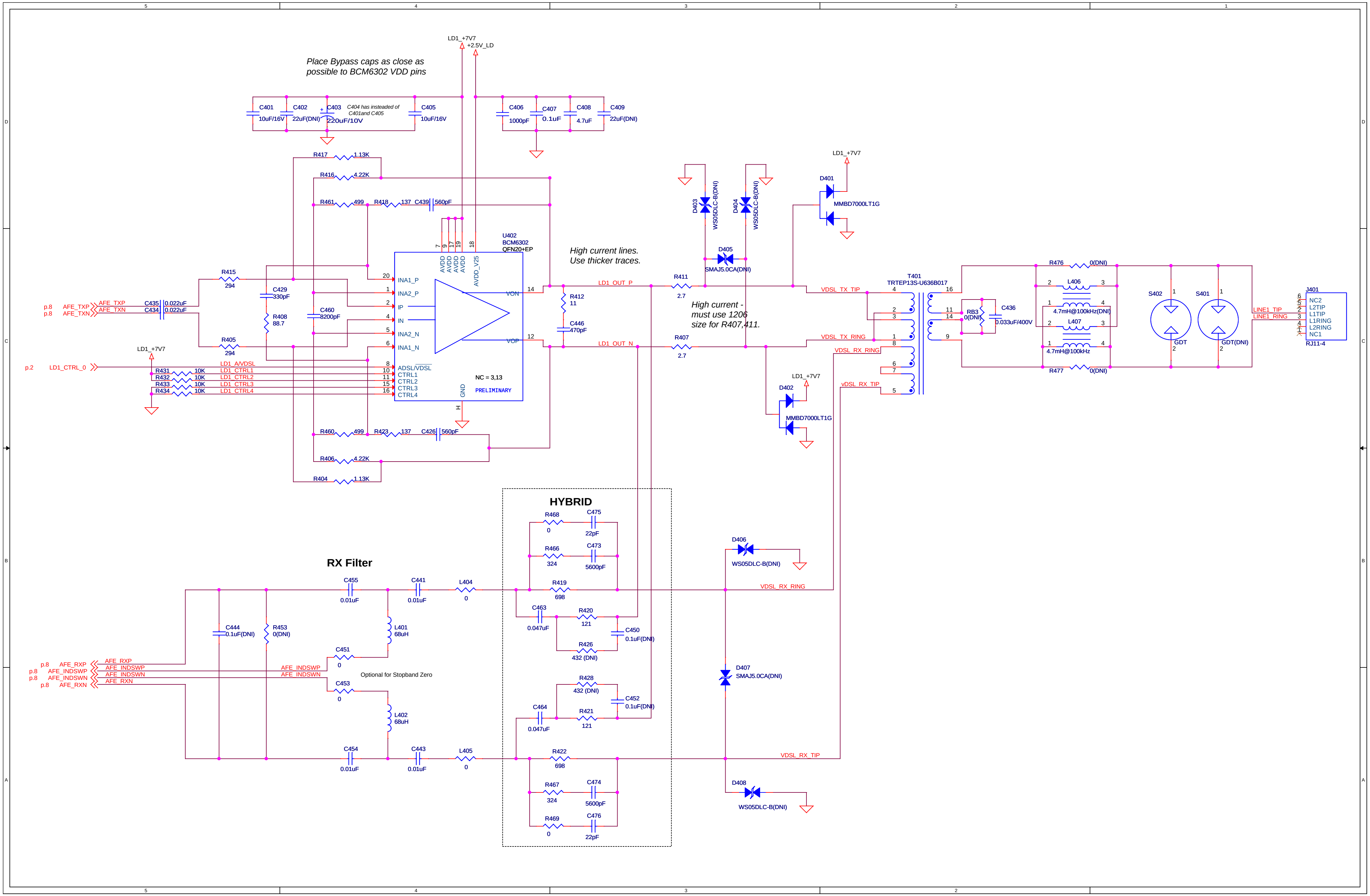


Route PCIe traces with 100ohm differential characteristic impedance.

The package of R316/R317 is RC0402, but choose RC0603 in the BOM

USB2.0 - Layout Guidelines & Notes

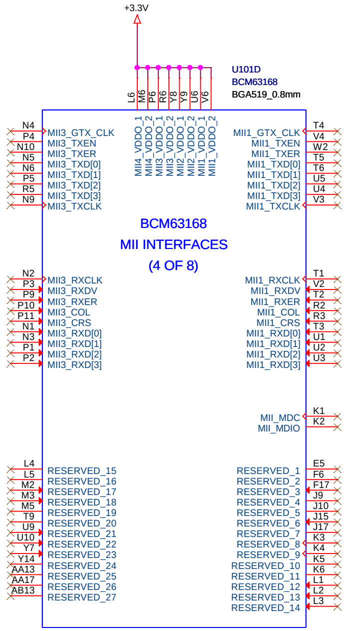
1. The Dp and Dn traces are length matched, with max differential skew, within 20mils
2. Differential trace length must be less than 5 inches
3. No more than 2 vias per trace, prefer zero.
4. Never split the ground plane under differential pair routing
5. Route differential pairs above the GND plane.
6. Differential impedance is 90 ohms for USB.
7. Adjacent differential pairs should be separated by at least 3 times the trace width. (e.g. 7.5 mil trace, leave >22.5mils between adjacent diff pairs)
8. Stitch gnd vias around each differential pair, but NOT between a given pair.

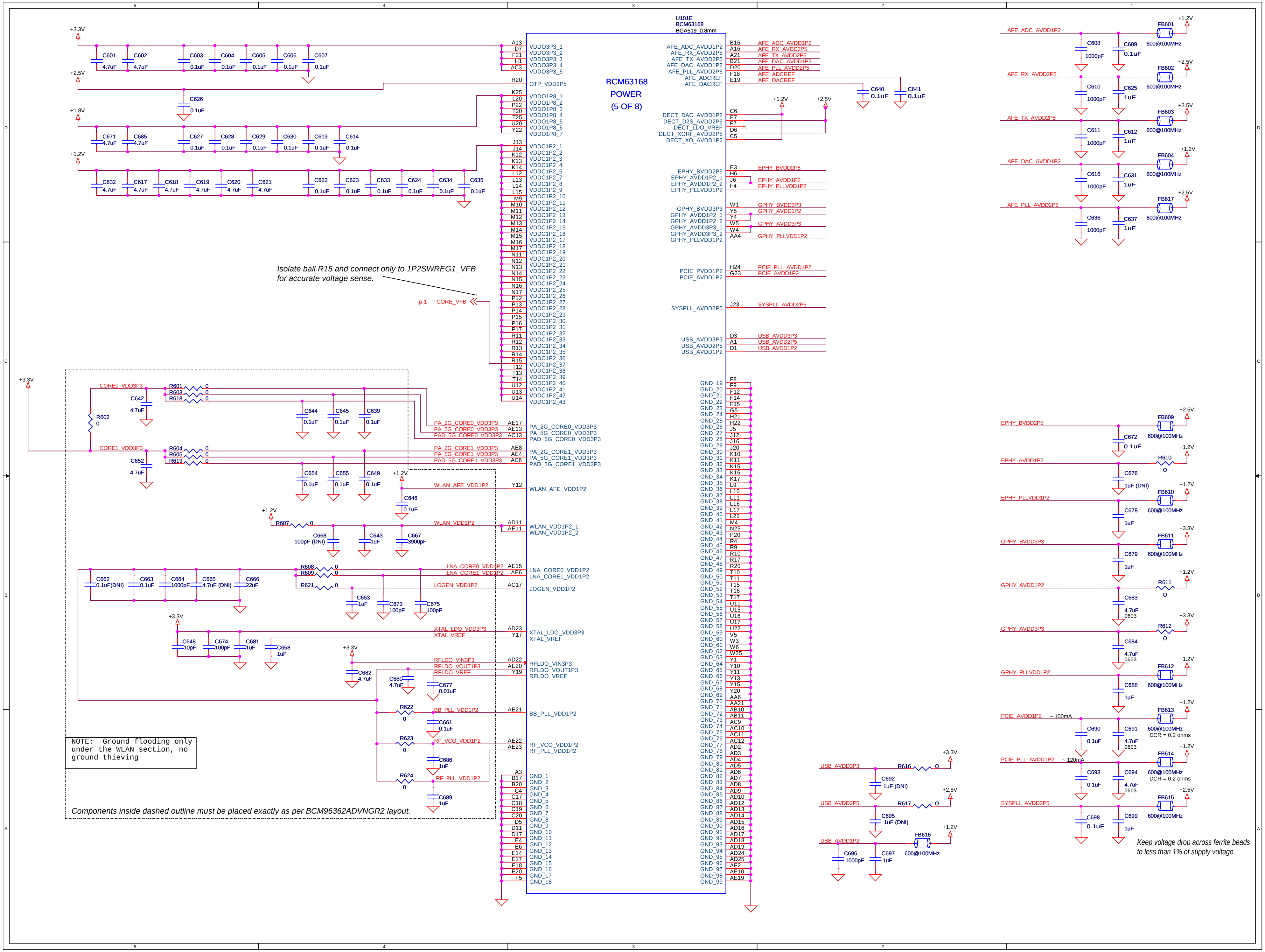


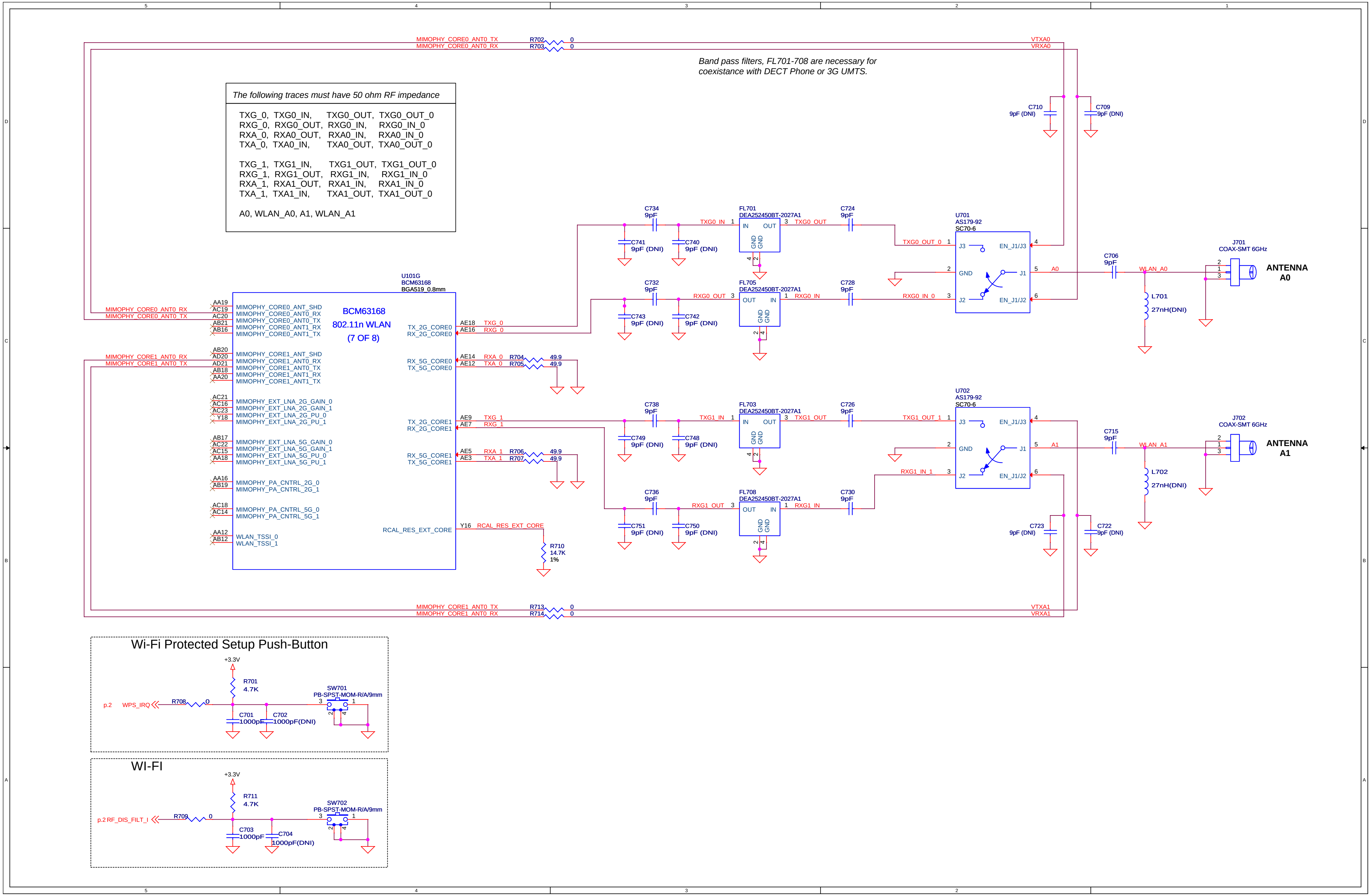
Place Bypass caps as close as possible to BCM6302 VDD pins
LD1_+7V7
+2.5V_LD
C401 10uF/16V
C402 22uF(DNI)
C403 220uF/10V
C404 has insteaded of C401and C405
C405 10uF/16V
C406 1000pF
C407 0.1uF
C408 4.7uF
C409 22uF(DNI)
R417 1.13K
R416 4.22K
R461 499
R418 137
C439 560pF
U402 BCM6302 QFN20+EP
AVDD AVDD AVDD AVDD AVDD_V25
INA1_P INA2_P IP IN INA2_N INA1_N
VON VOP
ADSL/VDSL CTRL1 CTRL2 CTRL3 CTRL4
NC = 3,13
PRELIMINARY
GND
R415 294
R405 294
C429 330pF
R408 88.7
C460 8200pF
C435 0.022uF
C434 0.022uF
p.8 AFE_TXP
p.8 AFE_TXN
p.2 LD1_CTRL_0
R431 10K LD1_CTRL1
R432 10K LD1_CTRL2
R433 10K LD1_CTRL3
R434 10K LD1_CTRL4
LD1_A/VDSL
R460 499
R423 137
C426 560pF
R406 4.22K
R404 1.13K
High current lines. Use thicker traces.
R412 11
C446 470pF
LD1_OUT_P
LD1_OUT_N
R411 2.7
R407 2.7
High current - must use 1206 size for R407,411.
D403 WS05DLC-B(DNI)
D404 WS05DLC-B(DNI)
D405 SMAJ5.0CA(DNI)
D401 MMBD7000LT1G
D402 MMBD7000LT1G
VDSL_TX_TIP
VDSL_TX_RING
VDSL_RX_RING
VDSL_RX_TIP
T401 TRTEP13S-U636B017
RB3 0(DNI)
C436 0.033uF/400V
R476 0(DNI)
R477 0(DNI)
L406 4.7mH@100kHz(DNI)
L407 4.7mH@100kHz
S402 GDT
S401 GDT(DNI)
LINE1_TIP
LINE1_RING
J401 RJ11-4
NC2 L2TIP L1TIP L1RING L2RING NC1
HYBRID
R468 0
C475 22pF
R466 324
C473 5600pF
R419 698
C463 0.047uF
R420 121
C450 0.1uF(DNI)
R426 432 (DNI)
R428 432 (DNI)
C452 0.1uF(DNI)
C464 0.047uF
R421 121
R422 698
R467 324
C474 5600pF
R469 0
C476 22pF
RX Filter
C455 0.01uF
C441 0.01uF
L404 0
C444 0.1uF(DNI)
R453 0(DNI)
L401 68uH
C451 0
Optional for Stopband Zero
C453 0
L402 68uH
C454 0.01uF
C443 0.01uF
L405 0
p.8 AFE_RXP
p.8 AFE_INDSWP
p.8 AFE_INDSWN
p.8 AFE_RXN
D406 WS05DLC-B(DNI)
D407 SMAJ5.0CA(DNI)
D408 WS05DLC-B(DNI)

CONNECT MIIx_VDDO_1 & _2 TO 3.3V WHEN USED IN MII, RvMII, TMII MODE, OR WHEN NOT USED
CONNECT MIIx_VDDO_1 & _2 TO 2.5V WHEN USED IN RGMII MODE, OR WHEN NOT USED

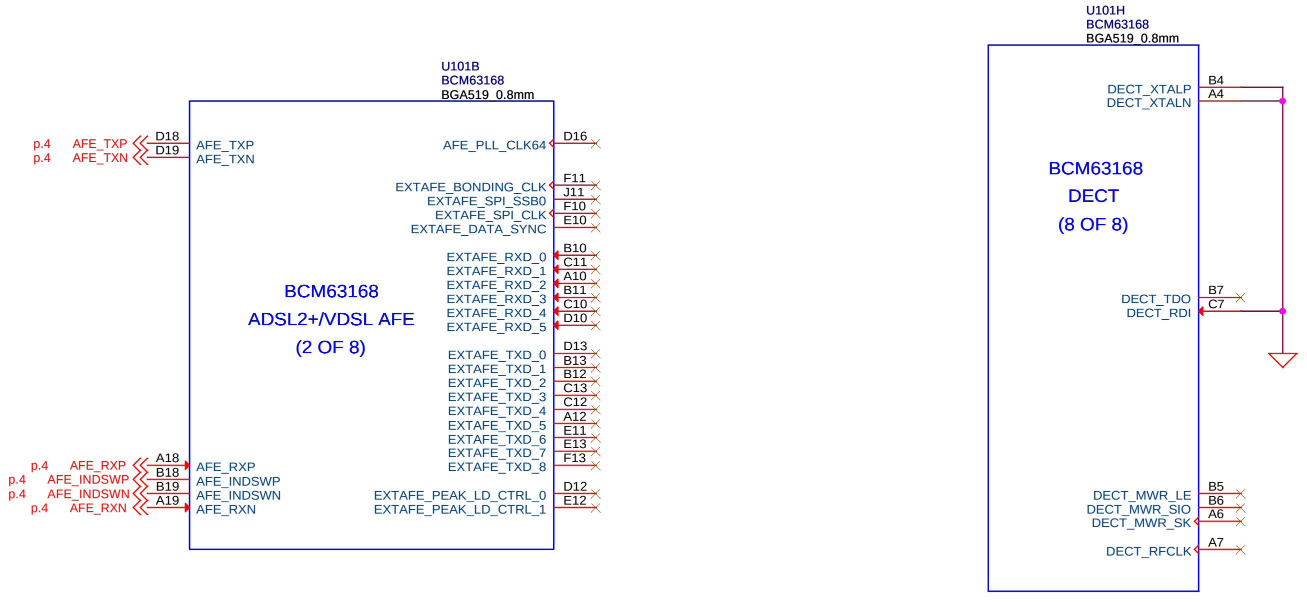
!
MII2_VDDO_1 & _2 PROVIDE THE I/O VOLTAGE FOR GPIO[51:40]. THEREFORE,
MII2_VDDO_1 & _2 MUST BE CONNECTED TO 3.3V WHEN ANY OF GPIO[51:40] ARE USED.




U101E
BCM63168
BGA519_0.8mm
BCM63168
POWER
(5 OF 8)
+3.3V
VDDO3P3_1
VDDO3P3_2
VDDO3P3_3
VDDO3P3_4
VDDO3P3_5
C601 4.7uF
C602 4.7uF
C603 0.1uF
C604 0.1uF
C605 0.1uF
C606 0.1uF
C607 0.1uF
+2.5V
OTP_VDD2P5
C626 0.1uF
+1.8V
VDDO1P8_1
VDDO1P8_2
VDDO1P8_3
VDDO1P8_4
VDDO1P8_5
VDDO1P8_6
VDDO1P8_7
C671 4.7uF
C685 4.7uF
C627 0.1uF
C628 0.1uF
C629 0.1uF
C630 0.1uF
C613 0.1uF
C614 0.1uF
+1.2V
VDDC1P2_1 … VDDC1P2_43
C632 4.7uF
C617 4.7uF
C618 4.7uF
C619 4.7uF
C620 4.7uF
C621 4.7uF
C622 0.1uF
C623 0.1uF
C633 0.1uF
C624 0.1uF
C634 0.1uF
C635 0.1uF
Isolate ball R15 and connect only to 1P2SWREG1_VFB for accurate voltage sense.
p.1 CORE_VFB
AFE_ADC_AVDD1P2
AFE_RX_AVDD2P5
AFE_TX_AVDD2P5
AFE_DAC_AVDD1P2
AFE_PLL_AVDD2P5
AFE_ADCREF
AFE_DACREF
C640 0.1uF
C641 0.1uF
DECT_DAC_AVDD1P2
DECT_D2S_AVDD2P5
DECT_LDO_VREF
DECT_XORF_AVDD2P5
DECT_XO_AVDD1P2
EPHY_BVDD2P5
EPHY_AVDD1P2_1
EPHY_AVDD1P2_2
EPHY_PLLVDD1P2
GPHY_BVDD3P3
GPHY_AVDD1P2_1
GPHY_AVDD1P2_2
GPHY_AVDD3P3_1
GPHY_AVDD3P3_2
GPHY_PLLVDD1P2
PCIE_PVDD1P2
PCIE_AVDD1P2
PCIE_PLL_AVDD1P2
SYSPLL_AVDD2P5
USB_AVDD3P3
USB_AVDD2P5
USB_AVDD1P2
GND_1 … GND_99
FB601 600@100MHz
C608 1000pF
C609 0.1uF
FB602 600@100MHz
C610 1000pF
C625 1uF
FB603 600@100MHz
C611 1000pF
C612 1uF
FB604 600@100MHz
C616 1000pF
C631 1uF
FB617 600@100MHz
C636 1000pF
C637 1uF
CORE0_VDD3P3
CORE1_VDD3P3
R601 0
R603 0
R618 0
R602 0
R604 0
R605 0
R619 0
C642 4.7uF
C652 4.7uF
C644 0.1uF
C645 0.1uF
C639 0.1uF
C654 0.1uF
C655 0.1uF
C649 0.1uF
PA_2G_CORE0_VDD3P3
PA_5G_CORE0_VDD3P3
PAD_5G_CORE0_VDD3P3
PA_2G_CORE1_VDD3P3
PA_5G_CORE1_VDD3P3
PAD_5G_CORE1_VDD3P3
WLAN_AFE_VDD1P2
C646 0.1uF
WLAN_VDD1P2
WLAN_VDD1P2_1
WLAN_VDD1P2_2
R607 0
C668 100pF (DNI)
C643 1uF
C667 3900pF
C662 0.1uF(DNI)
C663 0.1uF
C664 1000pF
C665 4.7uF (DNI)
C666 22uF
R608 0
R609 0
R621 0
LNA_CORE0_VDD1P2
LNA_CORE1_VDD1P2
LOGEN_VDD1P2
C653 1uF
C673 100pF
C675 100pF
XTAL_LDO_VDD3P3
XTAL_VREF
C648 10pF
C674 100pF
C681 1uF
C658 1uF
RFLDO_VIN3P3
RFLDO_VOUT1P3
RFLDO_VREF
C682 4.7uF
C680 4.7uF
C677 0.01uF
R622 0
BB_PLL_VDD1P2
C661 0.1uF
R623 0
RF_VCO_VDD1P2
RF_PLL_VDD1P2
C686 1uF
R624 0
C689 1uF
NOTE: Ground flooding only under the WLAN section, no ground thieving
Components inside dashed outline must be placed exactly as per BCM96362ADVNGR2 layout.
FB609 600@100MHz
C672 0.1uF
R610 0
C676 1uF (DNI)
FB610 600@100MHz
C678 1uF
FB611 600@100MHz
C679 1uF
R611 0
C683 4.7uF 0603
R612 0
C684 4.7uF 0603
FB612 600@100MHz
C688 1uF
PCIE_AVDD1P2 ~ 100mA
FB613 600@100MHz DCR = 0.2 ohms
C690 0.1uF
C691 4.7uF 0603
PCIE_PLL_AVDD1P2 ~ 120mA
FB614 600@100MHz DCR = 0.2 ohms
C693 0.1uF
C694 4.7uF 0603
FB615 600@100MHz
C698 0.1uF
C699 1uF
R616 0
C692 1uF (DNI)
R617 0
C695 1uF (DNI)
FB616 600@100MHz
C696 1000pF
C697 1uF
Keep voltage drop across ferrite beads to less than 1% of supply voltage.



Band pass filters, FL701-708 are necessary for coexistance with DECT Phone or 3G UMTS.
The following traces must have 50 ohm RF impedance
TXG_0, TXG0_IN, TXG0_OUT, TXG0_OUT_0
RXG_0, RXG0_OUT, RXG0_IN, RXG0_IN_0
RXA_0, RXA0_OUT, RXA0_IN, RXA0_IN_0
TXA_0, TXA0_IN, TXA0_OUT, TXA0_OUT_0
TXG_1, TXG1_IN, TXG1_OUT, TXG1_OUT_0
RXG_1, RXG1_OUT, RXG1_IN, RXG1_IN_0
RXA_1, RXA1_OUT, RXA1_IN, RXA1_IN_0
TXA_1, TXA1_IN, TXA1_OUT, TXA1_OUT_0
A0, WLAN_A0, A1, WLAN_A1
MIMOPHY_CORE0_ANT0_TX R702 0 VTXA0
MIMOPHY_CORE0_ANT0_RX R703 0 VRXA0
C710 9pF (DNI)
C709 9pF (DNI)
U101G
BCM63168
BGA519_0.8mm
BCM63168
802.11n WLAN
(7 OF 8)
AA19 MIMOPHY_CORE0_ANT_SHD
AC19 MIMOPHY_CORE0_ANT0_RX
AC20 MIMOPHY_CORE0_ANT0_TX
AB21 MIMOPHY_CORE0_ANT1_RX
AB16 MIMOPHY_CORE0_ANT1_TX
AB20 MIMOPHY_CORE1_ANT_SHD
AD20 MIMOPHY_CORE1_ANT0_RX
AD21 MIMOPHY_CORE1_ANT0_TX
AB18 MIMOPHY_CORE1_ANT1_RX
AA20 MIMOPHY_CORE1_ANT1_TX
AC21 MIMOPHY_EXT_LNA_2G_GAIN_0
AC16 MIMOPHY_EXT_LNA_2G_GAIN_1
AC23 MIMOPHY_EXT_LNA_2G_PU_0
Y18 MIMOPHY_EXT_LNA_2G_PU_1
AB17 MIMOPHY_EXT_LNA_5G_GAIN_0
AC22 MIMOPHY_EXT_LNA_5G_GAIN_1
AC15 MIMOPHY_EXT_LNA_5G_PU_0
AA18 MIMOPHY_EXT_LNA_5G_PU_1
AA16 MIMOPHY_PA_CNTRL_2G_0
AB19 MIMOPHY_PA_CNTRL_2G_1
AC18 MIMOPHY_PA_CNTRL_5G_0
AC14 MIMOPHY_PA_CNTRL_5G_1
AA12 WLAN_TSSI_0
AB12 WLAN_TSSI_1
TX_2G_CORE0 AE18 TXG_0
RX_2G_CORE0 AE16 RXG_0
RX_5G_CORE0 AE14 RXA_0 R704 49.9
TX_5G_CORE0 AE12 TXA_0 R705 49.9
TX_2G_CORE1 AE9 TXG_1
RX_2G_CORE1 AE7 RXG_1
RX_5G_CORE1 AE5 RXA_1 R706 49.9
TX_5G_CORE1 AE3 TXA_1 R707 49.9
RCAL_RES_EXT_CORE Y16 RCAL_RES_EXT_CORE
R710 14.7K 1%
C734 9pF
C741 9pF (DNI)
C740 9pF (DNI)
FL701 DEA252450BT-2027A1
TXG0_IN 1 IN OUT 3 TXG0_OUT
C724 9pF
U701 AS179-92 SC70-6
TXG0_OUT_0 1 J3 EN_J1/J3 4
2 GND J1 5 A0
RXG0_IN_0 3 J2 EN_J1/J2 6
C706 9pF
WLAN_A0
L701 27nH(DNI)
J701 COAX-SMT 6GHz
ANTENNA A0
C732 9pF
C743 9pF (DNI)
C742 9pF (DNI)
FL705 DEA252450BT-2027A1
RXG0_OUT 3 OUT IN 1 RXG0_IN
C728 9pF
U702 AS179-92 SC70-6
C738 9pF
C749 9pF (DNI)
C748 9pF (DNI)
FL703 DEA252450BT-2027A1
TXG1_IN 1 IN OUT 3 TXG1_OUT
C726 9pF
TXG1_OUT_1 1 J3 EN_J1/J3 4
2 GND J1 5 A1
RXG1_IN_1 3 J2 EN_J1/J2 6
C715 9pF
WLAN_A1
L702 27nH(DNI)
J702 COAX-SMT 6GHz
ANTENNA A1
C736 9pF
C751 9pF (DNI)
C750 9pF (DNI)
FL708 DEA252450BT-2027A1
RXG1_OUT 3 OUT IN 1 RXG1_IN
C730 9pF
C723 9pF (DNI)
C722 9pF (DNI)
MIMOPHY_CORE1_ANT0_TX R713 0 VTXA1
MIMOPHY_CORE1_ANT0_RX R714 0 VRXA1
Wi-Fi Protected Setup Push-Button
+3.3V
R701 4.7K
p.2 WPS_IRQ R708 0
SW701 PB-SPST-MOM-R/A/9mm
C701 1000pF
C702 1000pF(DNI)
WI-FI
+3.3V
R711 4.7K
p.2 RF_DIS_FILT_I R709 0
SW702 PB-SPST-MOM-R/A/9mm
C703 1000pF
C704 1000pF(DNI)



U101B
BCM63168
BGA519_0.8mm
BCM63168
ADSL2+/VDSL AFE
(2 OF 8)
p.4 AFE_TXP
p.4 AFE_TXN
D18 AFE_TXP
D19 AFE_TXN
p.4 AFE_RXP
p.4 AFE_INDSWP
p.4 AFE_INDSWN
p.4 AFE_RXN
A18 AFE_RXP
B18 AFE_INDSWP
B19 AFE_INDSWN
A19 AFE_RXN
AFE_PLL_CLK64 D16
EXTAFE_BONDING_CLK F11
EXTAFE_SPI_SSB0 J11
EXTAFE_SPI_CLK F10
EXTAFE_DATA_SYNC E10
EXTAFE_RXD_0 B10
EXTAFE_RXD_1 C11
EXTAFE_RXD_2 A10
EXTAFE_RXD_3 B11
EXTAFE_RXD_4 C10
EXTAFE_RXD_5 D10
EXTAFE_TXD_0 D13
EXTAFE_TXD_1 B13
EXTAFE_TXD_2 B12
EXTAFE_TXD_3 C13
EXTAFE_TXD_4 C12
EXTAFE_TXD_5 A12
EXTAFE_TXD_6 E11
EXTAFE_TXD_7 E13
EXTAFE_TXD_8 F13
EXTAFE_PEAK_LD_CTRL_0 D12
EXTAFE_PEAK_LD_CTRL_1 E12
U101H
BCM63168
BGA519_0.8mm
BCM63168
DECT
(8 OF 8)
DECT_XTALP B4
DECT_XTALN A4
DECT_TDO B7
DECT_RDI C7
DECT_MWR_LE B5
DECT_MWR_SIO B6
DECT_MWR_SK A6
DECT_RFCLK A7