APPENDIX B: OPERATIONAL DESCRIPTION

Please refer to the following pages.

The A/L & IF UNIT consists of the following Block.

[IF Block]

- 1st IF amplifier, 1st IF filter
- 2nd Local VCO, 2nd Local PLL circuit
- 2nd Mixer, 2nd IF filter, 2nd IF amplifier

[Logic circuit]

- Analog Digital Converter: ADC (IC812)
- CONTROLLER ASIC: HILLARY (IC701)
- Flash ROM (IC702)
- SRAM (IC703, IC704)
- EEPROM (IC706)
- Serial Number ROM (IC709)
- MIXED SIGNAL ASIC: PATTI (IC801)
- Complex Programmable Logic Device: CPLD (IC811)
- Digital Signal Processor: DSP (IC901)
- RS-485 (IC708)
- RS-232 (IC707)
- Reset Circuit (IC710)

[Audio circuit]

- Audio Amplifier (IC802)
- Analog Switch (IC803)

[Power supply circuit]

- Voltage Regulator (IC941, IC942, IC943, IC951, IC952, IC953, IC954)

CIRCUIT DESCRIPTION

1. IF Block

This block's function is conversion from 1st IF signal to 2nd IF signal. 2nd IF signal is sent to Controller ASIC, or 2nd IF AMPL (IC1309) for digital sampling by Analog Digital Converter, through the 2nd IF filters (FL1303 or FL1304 or FL1306+FL1307) according to each radio operational mode. And if route for digital sampling by Analog Digital Converter is selected, the 2nd IF signal is propagated to Analog Digital Converter through the 2nd IF AMPL (IC1309) and another Ceramic Filter (FL1308). Then each operational mode of this radio is Conventional wide band, Conventional narrow band and C4FM.

1-1. 1st IF amplifier, 1st IF filter

The 1st IF output signal from J201 of TRX/SYNTHESIZER UNIT is input to J1301 of IF block of A/L&IF Unit.

The 1st IF signal is input to TR1303 of the IF AMP through TR1309 and TR1310.

That signal is filtered by Crystal-Band-pass-filter (FL1301 and FL1302) and propagated to FM demodulation IC (IC1303) .

1-2. 2nd Local VCO, 2nd Local PLL circuit

The 2nd Local signal is generated by PLL synthesizer block that is composed of VCO circuit and PLL circuit.

The 2nd local VCO generates the IF signal (44.65MHz or 45.55MHz).

Then the 2nd PLL circuit controls the frequency of this IF signal with the high stability.

1-3. 2nd Mixer, 2nd IF filter, 2nd IF amplifier

The IF Receiver (IC1303) is a one-chip IC for radio communication system. This IC includes 2nd Mixer, 2nd IF amplifier and Limiter. The 1st IF signal is amplified by 2nd IF amplifier and propagated to the input-port of 2nd Mixer in IC1303. The 2nd local frequency (45.1MHz) is propagated from 2nd local amplifier (TR1202) to another input-port of the 2nd Mixer. The 2nd Mixer converts 1st IF signal (45.1MHz) to 2nd IF frequency (450KHz).

The 2nd IF signal is propagated to Ceramic Filters (FL1303 or FL1304 or FL1306+FL1307), which are switched by order of Controller ASIC.

2. Logic circuit

The main microcomputer circuit in M7100 radio consists of Hillary (IC701), Flash ROM (IC702), SRAM (IC703 and IC704), EEPROM (IC706) and Serial Number ROM (IC709). This circuit is synchronized by TCXO (XU701) whose frequency is 19.2 MHz.

MIXED SIGNAL ASIC: PATTI (IC801) is used for voltage control for TRX/SYNTHESIZER-Unit and Audio interface.

Complex Programmable Logic Device: CPLD (IC811) is used for interface of ADC, DSP and HILLARY.

Digital Signal Processor: DSP (IC901) is used for modulation, de-modulation and voice-codec.

RS-485 (IC708) and RS-232 (IC707) is external interface for man-machine interface.

Reset Circuit (IC710) is used for resetting radio at power ramped up timing.

2-1. Analog Digital Converter: ADC (IC812)

ADC (IC812) is used for Analog-signal to Digital-signal to convert 2nd IF-signal.

2-2. CONTROLLER ASIC: HILLARY (IC701)

Main functions of HILLARY are following.

- PATTI, FLASH ROM, EEPROM, SRAM and DSP control.
- Data load to the frequency synthesizer.
- Fetch and process of PTT, monitor, channel, selection and volume control.
- TRX/SYNTHESIZER Unit Control.
- Squelch Decoding.
- Channel Guard and Digital Channel Guard Encoding/Decoding.
- External interface control for the radio data. (Ex. Channel number and signaling)

2-3. FLASH ROM (IC702)

This memory contains the software to control the radio. This Flash ROM has a storage capacity of 2 M x 8 bits.

2-4. SRAM (IC703, IC704)

These Flash ROM' total storage capacity is 1M x 8 bits.

2-5. EEPROM (IC706)

The EEPROM has a storage capacity of 16 K bits, and contains the user configurable parameters.

This memory is used for storing tracking data, variable personalities and mainly contains the following data:

- Channel Frequency Data
- Channel Guard/Digital Channel Guard Data
- TX power, TX Modulation Data
- Squelch Data
- Display Data, etc.

2-6. Serial Number ROM (IC709)

The Serial Number ROM has an electronic registration number that provides absolutely unique identity, which can be determined with minimal electronic interface. The IC contains the factory-recorded numbers that is consisted of a unique 48bit serial number, an 8bit CRC, and an 8bit Family code (01h).

2-7. MIXED SIGNAL ASIC, PATTI (IC801)

PATTI has three major functions. These functions are as follows:

- Fast digitizer
- Voice CODEC by 13bit PCM
- Two 8bit DAC and a 10bit DAC

2-8. Complex Programmable Logic Device: CPLD (IC811)

The CPLD is used for changing the parallel data to serial data.

And this IC has function of the interface between DSP to HILLARY and ADC.

2-9. Digital Signal Processor DSP (IC901)

The DSP has almost functions of digital signal processing for this radio.

And HILLARY controls this IC's function.

2-10. RS-485 (IC708)

This IC is used for a high-speed differential tri-state bus/line transceiver to meet the requirements of EIA standard RS-485 specification. This interface is used for Control Unit.

2-11. RS-232 (IC707)

The IC is used for line driver/receivers to meet the requirements of EIA standard RS-232 specifications. The IC707 is located between the radio unit and the ORCC connector.

2-12. Reset Circuit (IC710)

This IC's function is resetting radio system. The signal is generated at the timing of ramped up voltage level of 5VD.

And it is possible to adjust delay time from ramped up timing by external capacitor. The generated signal is injected to HILLARY.

3. Audio circuit

This block is used for Audio Output to speaker.

3-1. Audio Amplifier (IC802)

The audio amplifier is located between the ASIC and speaker. The amplifier (IC802) amplifies the output signal from the MIXED SIGNAL ASIC (PATTI:IC801) to the adequate level for driving speaker.

3-2. Analog Switch (IC803)

This Analog switch uses for mute a voice line. When a control signal is “H”, a voice line is active.

4. Power supply circuit

This block is used for Power supply to each block. The supplied voltage from external battery is regulated to adequate voltage for each device.

4-1. Voltage Regulators (IC941, IC942, IC943, IC951, IC952, IC953 and IC954)

The radio needs some kinds of voltage regulator.

Two Voltage regulators (IC951 and IC952) generate each 5Vdc for mostly the System Control. Other two Voltage regulators (IC953 and IC954) generate each 9Vdc for mostly the TRX/SYNTHESIZER Unit and Audio Amp (IC802). And other Voltage regulator (IC943) generates a 3.3Vdc for the DSP. Another Voltage regulator (IC942) generates a 1.5Vdc for the DSP.

The TRX/SYNTHSYZER Unit consists of the following Block.

[Receiver Circuit]

- Receiver Front-End
- 1'st Mixer
- 1'st IF

[Transmitter Circuit]

- RF Amplifier
- Pre-Driver
- PA Modules
- Power compositor
- Automatic Power Control
- Antenna Switch and Low Pass Filter

[Synthesizer circuit]

- 1st Local Synthesizer Circuit
- Reference Oscillator
- PLL Frequency Synthesizer chip
- Loop filter
- Rx VCO
- TX VCO
- Feedback Buffer Amplifier
- Dual-Modulus Prescaler
- Lock Detect

CIRCUIT DESCRIPTION

1. Receiver Circuit

The FM Double Super Heterodyne Receiver is designed for operation in the 136-174MHz-frequency range.

The Receiver uses intermediate frequencies (IF) of 45.1MHz and 450KHz.

Two bands pass filters, 45.1MHz crystal filter and a 450KHz ceramic filter keep adjacent channel selectivity.

The FM-detector is internal Quadrature discriminator in ASIC and 14bit ADC on Audio Logic Unit.

1-1. Receiver Front-End

A RF signal from antenna is propagated through the low pass filters, antenna switch and 1st band pass filter to the input of low noise amplifier (TR201).

The output of TR201 is propagated through 2nd band pass filter to the input of low noise amplifier (TR203).

The output of TR203 is propagated through 3rd band pass filter to input of 1'st Mixer (HC201).

These band pass filters keep Front-End selectivity.

1-2. 1st Mixer

The 1st Mixer is a Double-Balanced-Mixer (DBM: HC201) that converts a RF-signal range, from the 136 to 174MHz frequency, to 1st IF frequency (45.1MHz).

In the mixer, a RF signal from the Front-End RF filter is propagated to the input-port of the DBM.

1st IF signal is output from the IF port of DBM.

The 1st IF output signal from J201 of TRX/SYNTHESIZER UNIT is input to J1301 of IF block of Audio Logic Unit.

2. Transmitter Circuit

The Transmitter Circuit consists of Circuits of following.

(1) RF Amplifier (TR300 and TR101)
(2) Pre-Driver (TR102)
(3) PA Module (IC101 and IC102)
(4) Automatic Power Control Circuit (IC105)
(5) Combiner (L105, L106, L107, L108, R119)
(6) Antenna Switch (CD101, CD102-CD104-CD106)
(7) Low Pass Filter (Micro Strip Line and C122-C141).

2-1. RF Amplifier

The RF input signal (136MHz-174MHz) is input to attenuator (ATT: R370-R372) from Synthesizer output-port .
The output of the ATT is input to the RF-amplifier (TR300 and TR101), and the signal is amplified.
RF input level to TX Amplifier (TR300) is about 0dBm, and the signal is amplified to +6dBm by TX amplifier (TR300).
And that RF signal through Attenuator (R101-R103) is amplified by Exciter Amplifier (TR101) to +16dBm.
Those amplifiers are controlled by TXENB+.

2-2. Pre-Driver

The output signal of TR101 is input to the Pre-Driver (TR102) through attenuator (R109-R111). And the signal is amplified to +23dBm. This amplifier is also controlled by TXENB+.

2-3. PA Modules

The RF output of TR102 is input to the dividers circuit (R116-R118). And divided RF signal is input to two PA-modules (IC101 and IC102). Each RF signal is amplified to about 65W respectively by PA-modules.
Then Power control circuit controls the gain control voltage to PA Module. The PA modules' power supply voltages are supplied from +A. Internal amplifiers, those are consist of three stages, in PA Module are operated in Class-AB.

2-4. Combiner

The each PA-module output signals are input to the Combiner circuit (L105, L106, L107, L108, R119).
The Combiner is used the Wilkinson Type which is consist of Coils and Capacitors
The Final RF output signal level from Combiner circuit is about 110W.

2-5. Automatic Power Control

The Automatic-Power-Control circuit (APC) operates the output power to the antenna to maintain a constant power level over the VHF frequency band.

The APC circuit controls the gate voltage (Vgg) of the first stage for gain in the PA Module (IC101 and IC102).

A Power Detector (Directional coupler) picks up TX-power and the detected power is supplied to CD110. The picked up TX-power is rectified in CD110 (the rectifying circuit). The Diode (CD110) produces a positive DC voltage proportional to the TX-power level. Also, when the RF-load is caused mismatch, this circuit detects the reflected power from antenna port. And that reflected power is rectified in CD109 (the rectifying circuit).

Each power-rectified signals are summed by the adder circuit (IC105). And the added signal is compared to “APCREF”, that's source is produced from DAC in PATTI on Audio Logic Unit. The output signal of IC105 is connected to Vgg of the IC101 and IC102. The Vgg is control port for TX-power and the TX-power is controlled with this compared signal.

Temperature monitor circuit (RT101 and TR104) makes thermal screening and detection for PA-module protection.

When the temperature of the PA heat sink is more than +100degC, this circuit senses the temperature of PA heat sink.

And the temperature monitor circuit drops TX-power with the operation.

2-6. Antenna Switch and Low Pass Filter

The Antenna Switch consists of CD101, CD102, and CD104-CD106. And the Low Pass Filter consists of the micro-strip line and C122-C141.

During the RX operation, "TXENB+" signal is low level. The impedance of Antenna switch diode become high.

The receiver RF signal from Antenna port input to 5W DET circuit through Low Pass Filter.

During the TX operation, also "TXENB+" signal is switched high level.

"TXENB+" signal from Audio Logic Unit is connected to the Base of TR106.

The status of "TR106 and TR105" as switch is ON while "TXENB+" is high level.

At the same time the +9VT line becomes the 9V. Then the switches (CD101, CD102, CD104-CD106) and the diode impedance for Antenna Switch are produced low, the output power from Combiner pass to Low Pass Filter.

3. Synthesizer circuit

3-1. 1st Local Synthesizer Circuit

The Frequency Synthesizer circuit receives PLL data and control information from the microcomputer. Then this circuit generates the TX/RX RF frequencies.

And at once, the circuit provides locked frequency information to A/L&IF Unit. The circuit consists of the Reference Oscillator, PLL Frequency Synthesizer IC (IC501), Loop filter, RX VCO (TR401), TX VCO (TR405), and Feedback Buffer Amplifier. RX VCO and TX VCO are locked on the divided frequency of the Reference Oscillator by a single synthesis loop consisting of the Feedback Buffer and PLL Frequency Synthesizer IC that has internal divider and pre-scalars.

The TX VCO operates frequency range of 136-174MHz.

The RX VCO operates frequency range of 181.1MHz-219.1MHz

3-2. Reference Oscillator

The reference oscillator is a VC-TCXO (Voltage Control Temperature Controlled Compensated Crystal Oscillator) that has +/-1.5ppm of variable range. The standard reference oscillator frequency is 19.2MHz.

The VC-TCXO is enclosed in a shielded can for RF guard. The VC-TCXO is compensated with internal temperature compensated circuit against both low and high temperature. Then the VC-TCXO is compensated in +/-1.5ppm frequency range with temperature from -30degC to +60degC.

3-3. PLL Frequency Synthesizer IC

PLL Frequency Synthesizer IC (IC501) consists of a programmable reference oscillator divider (that uses “R” counter), phase detector and programmable VCO dividers (that uses “+N” and “A” counter).

A fixed integer number divides the reference frequency (19.2MHz) from the reference oscillator to obtain a channel reference (6.25KHz or 5KHz) for the synthesizer.

The internal phase detector compares the output from the reference divider with the output from internal “+N”, “A” counter. The “+N”, “A” counter receive divided signal, whose source is VCO output signal, by Pre-scalar, and those counters are programmed by the microcomputer.

The phase detector shifts output voltage when phase error is detected, during comparison with divided signal and current signal. If a phase error is detected, the error voltage as DC offset is shifted and supplied to correct the VCO output frequency toward the VCO and loop filter. The count value of the “+N”, “A” counters are controlled by Audio Logic Unit with “SCK+”, “SDT+” and “PLLENB+”.

When a different channel is selected or switched to the TX or RX from another operation by user operation, the error voltage is shifted by the phase-detector for changing to RF frequency.

3-4. Loop filter

The Loop-filter consists of IC503, TR505 and some passive devices toward VCO.

This filter controls the bandwidth and stability of the synthesizer loop.

The FET-switches (TR503 and TR504) in the loop filter circuit is controlled by "PLLFST2-" for the speeding up of PLL-Lockup-time.

The output signal of the filter is input to the variable capacitor in the TRX VCO and TRX frequency is controlled and maintained.

3-5. Rx VCO

The VCO is an oscillator with tank circuit that consists of the various capacitors and coils. And this is the Colpitsu type oscillator.

The output level of each VCO is typically -10dBm for coupled buffer amplifier inputs.

The RX VCO consists of FET oscillator (TR601 and TR611) and other various devices.

The RX VCO output is connected to input port of the high gain buffer amplifier (RX VCO AMP: TR616).

The output of RX VCO AMP is connected to RX LOCAL AMP1 and 2.

Those LOCAL AMPs are controlled by "DPTT-", that is sent from Audio Logic Unit.

The "DPTT-" status is high level during RX operation. The "DPTT-" status is inverted by TR604 and the inverted signal is used as "RXVCO_ENB" signal. Then "RXVCO_ENB" status is low level, so the RX VCO amplifier circuit is started operating.

And, RXVCO is controlled by also "BUF_SPLTSW-" for switching L-Band or H-Band operation.

While the "BUF_SPLTSW-" status is high level, the RX VCO oscillates with H-Band (198.1MHz-219.1MHz).

And while the "BUF_SPLTSW-" status is low level, the RX VCO oscillates with L-Band (188.1MHz-198.1MHz).

Each split VCO bands are split to 3-Bands, moreover. Those 3-Bands are controlled with "VA", "VB", "VC" and "VD" from BAND SHIFT CONTROL.

3-6 TX VCO

The TX VCO is basically similar to the RX VCO.

The TX VCO consists of FET oscillator (TR401 and TR405) and other various devices.

The TX VCO output is connected to input port of the high gain buffer amplifier (TX VCO AMP1 and 2: TR411 and TR412). Those AMPs are controlled by "BUF_DPTT+".

The "BUF_DPTT+" status is high level during TX operation. The "BUF_DPTT+" status is inverted by TR407 and the inverted signal is used as "VCO_DPTT" signal. Then "VCO_DPTT" status is low level, so the TX VCO amplifier circuit is started operating.

And, TXVCO is controlled by also "BUF_SPLTSW-" for switching L-Band or H-Band operation.

While the "BUF_SPLTSW-" status is high level, the TX VCO oscillates with H-Band (153.0MHz-174.0MHz).

And while the "BUF_SPLTSW-" status is low level, the TX VCO oscillates with L-Band (136.0MHz-153.0MHz).

Each split VCO bands are split to 4-Bands, moreover. Those 3-Bands are controlled with "VA"-"VF"from BAND SHIFT CONTROL.

3-7. Feedback Buffer Amplifier

The output signals of each VCO (TX and RX VCO) are combined by R561, R562, and R560.

The combined signal level is amplified to -10dBm by FEEDBACK amplifier (TR511).

3-8. Dual-Modulus Pre-scalar

The Dual-Modulus Pre-scalar is included in PLL Frequency synthesizer IC.

The Pre-scalar divides the RF frequency by 64 or 65 under control of the PLL Frequency synthesizer IC. The output of the Pre-scalar is supplied to internal "+N", "A" counter for divided down to 5KHz or 6.25KHz, the phase is compared between the divided-down frequency and the internal Reference Oscillator. The result of this comparison is voltage of detected phase error that is used to lock on frequency. The "+N", "A" counter value is provided from the Audio Logic Unit. The DC voltage, which depends on operating frequency, at Test Point TP501 should be within 1.5 to 6.5 Vdc when the PLL is locked on.

3-9. Lock Detect

The "Lock Detect" signal is output from IC504.

If the large frequency-error is occurred, the stability of RF frequency will be disrupted and then the frequency will be locked off.