APPENDIX B: OPERATIONAL DESCRIPTION

Please see the following pages.

7 CIRCUIT ANALYSIS

The UHF-L P7100^{IP} is a dual-conversion super heterodyne FM transceiver (see Table 1 for model number and frequency band information).

7.1 VOLTAGE REGULATOR / BIAS SUPPLY OVERVIEW

U402 provides the +5.5V bias (VSYN) for the Tx & Rx VCO's, the main charge pump on the PLL IC, the reference oscillator, and analog gates U304 & U309. U403 provides the +5.5V bias (VRX) for the receiver circuitry, plus supplies the bias for the "SW-5V" signal. [Note that U403 remains powered on during both Rx & Tx states because "RXON" remains high.] The "SW-5V" signal is provided by the "DPTT" signal from Hillary being input into a dual driver & pass transistor, Q402. The "SW-5V" signal provides the bias for the pre-driver amplifier (U202), the transmit power control circuitry (U404) and reference voltage into the directional coupler within antenna switch module (Z302). U405 provides the +3.0V bias (VSYN-2) for the PLL IC's digital logic, internal oscillator, & divider chain. The "SW-B" signal is a switched on battery voltage. It is provided by the "DPTT" signal from Hillary being input into driver transistor & pass transistor Q403. The "SW-B" signal provides the bias into the antenna switch module (Z302) to turn on or off the pin diodes in the Tx/Rx antenna switch. During Rx mode, U406 takes the VSYN output voltage and doubles it to ~ 11 VDC. This provides the bias for the U104 op-amps.

U900 provides the +5V bias to drive the analog portion of the baseband circuitry. U902 provides the +3V bias to drive the DSP portion of the logic circuitry. U903 provides the +1.5V bias to drive the "core" portion of the DSP. U904 provides the +5V bias to drive the 5 V logic circuitry.

Note: All of the voltage regulators are linear regulators except for U406 & U904, which are switching voltage regulators.

Transistors Q703-Q705 provide a current limited, switched battery voltage to the UDC connector for bias of external audio accessories.

7.2 RECEIVER CIRCUITS

The UHF-L P7100^{IP} receiver is designed for operation in the 378.000-430.000 MHz frequency range. The receiver has intermediate frequencies (IF) of 115.65 MHz and 450 kHz. Adjacent channel selectivity is obtained by using band pass filters- a 115.65 MHz crystal filter and two 450 kHz ceramic filters. The receive demodulator is the phase digitizer located within Hillary (U700).

7.2.1 Receiver Front End

A RF signal from the antenna is coupled through the Tx low pass filter & antenna switch in the antenna switch module (Z302), and the bandpass filter (FL101A) to the input of low noise RF pre-amplifier Q101. The output of Q101 is coupled through another bandpass filter (FL101B) to an attenuator pad. Its output is routed through an elliptic filter (C106, C126, C127, C148-C151, L110, L153, L155, L157, & R127) to the input of first mixer Z101. Front End selectivity is provided by the bandpass & elliptic filters.

The bandpass filters are tunable. The “BPFcontV” from U500-62 (“Patti’s” DAC01) output is input into a buffer amplifier (U104A) and then a voltage doubler (U104B). This voltage is then input into FL101, pins 3 & 7, to optimally tune the bandpass filters for suppression of undesired spurious responses.

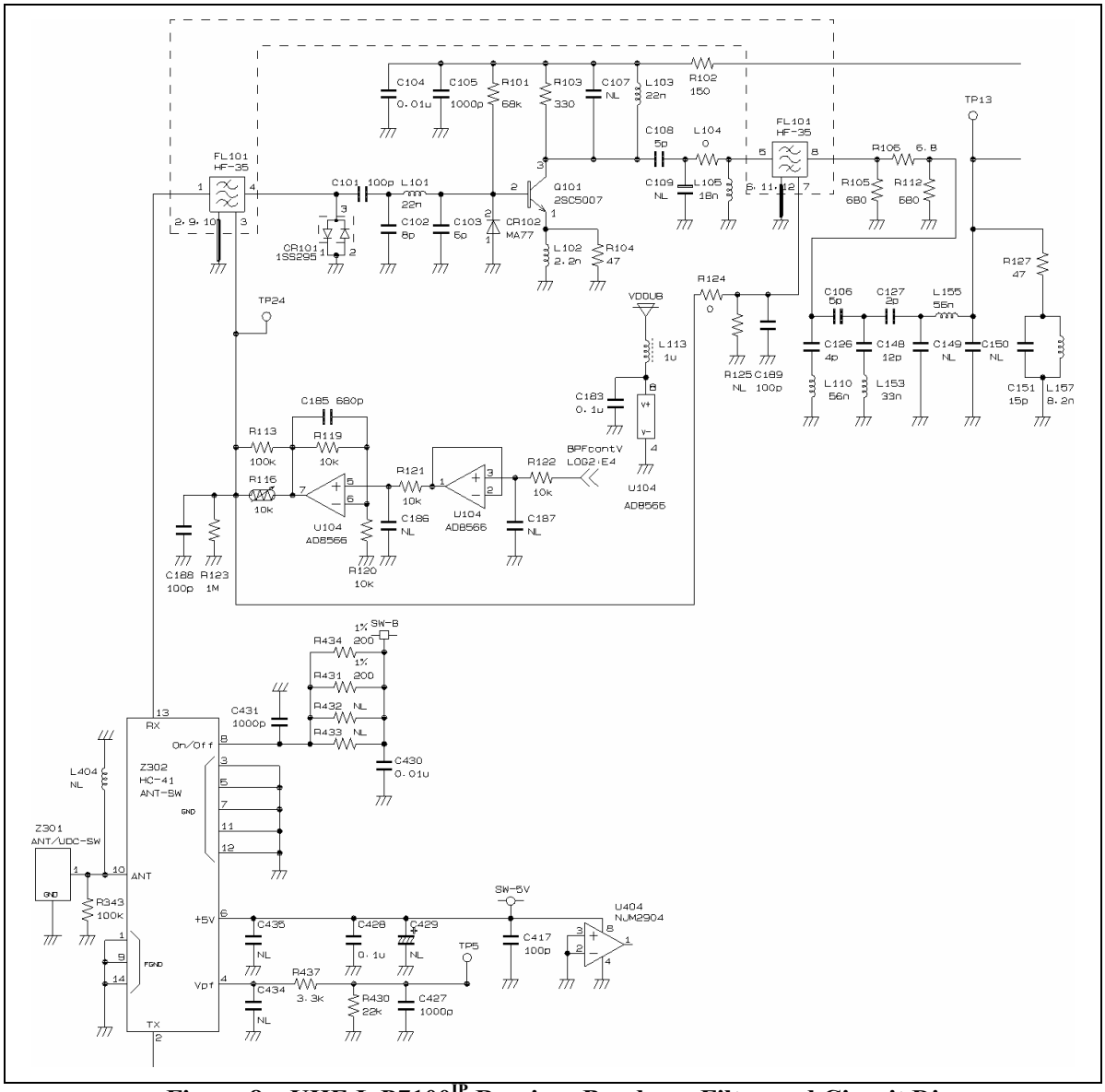

Figure 8 – UHF-L P7100^{IP} Receiver Bandpass Filter and Circuit Diagram

7.2.2 First Mixer Circuit

The first mixer is a Double-Balanced-Mixer (Z101) that converts a RF signal in the 378-430 MHz range to the 115.65 MHz first IF frequency. The Rx L.O. signal is derived from the Rx VCO, amplified by Q103, and input into Z101, pin 6. The signal at the output of Z101 is provided to the input of the first IF amplifier, Q102.

7.2.3 First IF Circuit

The first IF signal from the output of the first Mixer is coupled through first IF amplifier Q102 to crystal filter FL103. The highly selective crystal filter provides the first portion of the receiver IF selectivity. The output of the filter is coupled through an impedance-matching network to the Rx back end IC (U101).

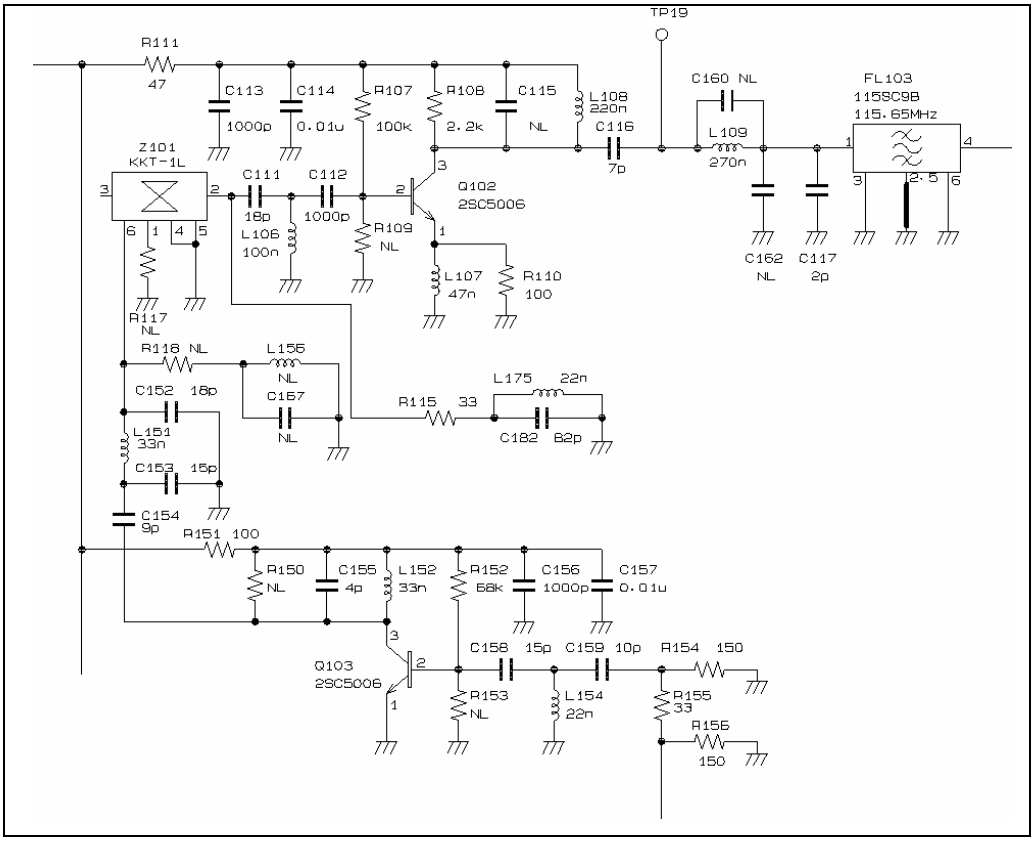

Figure 9 – UHF-L P7100^{IP} First Mixer and First I.F. Circuit Diagram

7.2.4 Second Mixer, Second IF Filters and Second IF Amplifier

The receiver back end IC (U101) is a single chip digital communication systems IC. It includes the second mixer, second IF amplifier and the limiter amplifier. Within the internal circuits of U101, the first IF signal is amplified and applied to the input of the second mixer. The second local injection frequency, 115.2 MHz, is applied from the second L.O. amplifier (Q106) to the local oscillator input of the second mixer. [Note that the 115.2 MHz second L.O. signal is the sixth harmonic of the 19.2 MHz reference oscillator.] The second mixer converts the first IF signal (115.65 MHz) down to the second IF frequency, 450 kHz. The second IF signal is applied to Ceramic Filter FL105 (wideband mode) or FL106 (narrowband or Project 25 mode), which provide the first part of the 450 kHz selectivity. Selection of FL105 or FL106 filters are controlled by the IF.NARROW signal from the microcomputer ("Hillary", i.e. U700). The output of the second IF filter is amplified through the second IF amplifier and back to ceramic filter FL104 (wideband or narrowband mode) or FL107 (Project 25 mode), which provide the second part of the 450 kHz selectivity. Selection of FL104 or FL107 filters are controlled by the C4FM.DATA signal from the microcomputer ("Hillary": U700). The output is then run to a limiter amplifier where the IF signal is amplified/limited, balanced, and output at RXIF and RXIF (bar). These two lines, one with a positive phase and the other with a negative phase, are used to cancel out any noise that might be on the line. These balanced outputs are applied to the phase digitizer in Hillary and demodulated.

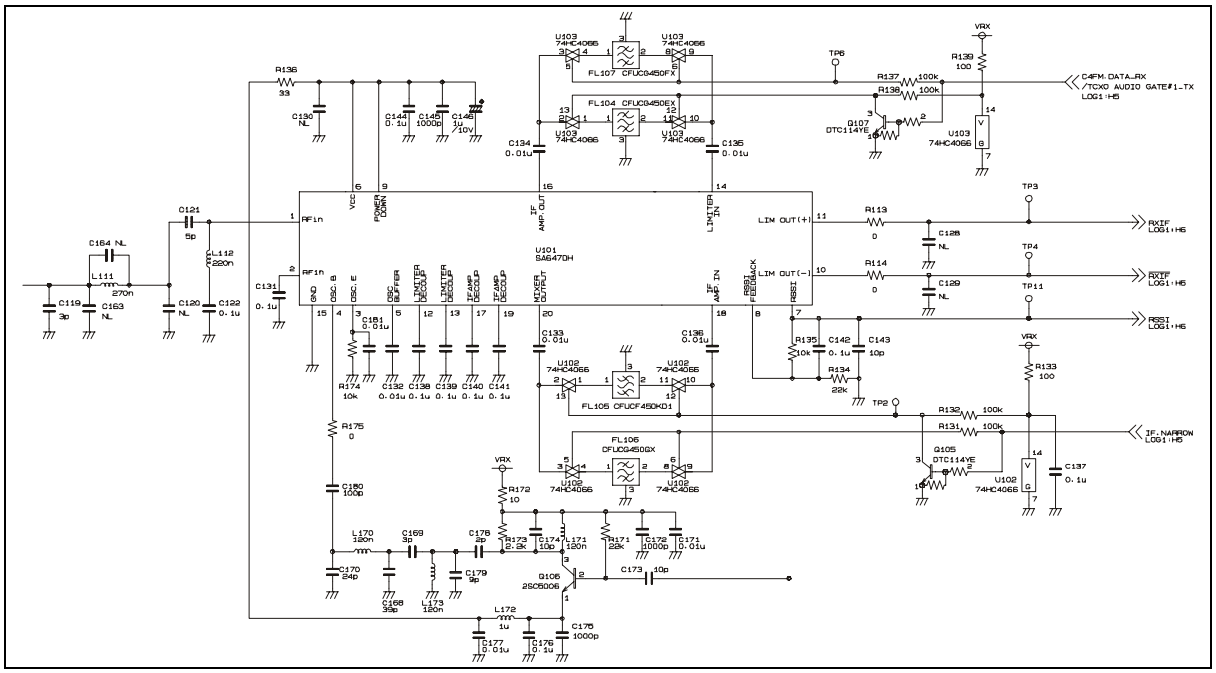

Figure 10 – UHF-L P7100 Second Mixer and Second IF Circuit Diagram

7.3 TRANSMITTER CIRCUIT

The UHF-L P7100^{IP} transmitter circuit consists of Tx VCO (Z304), pre-driver amplifier (U202), driver amplifier (Q202), PA module (U201), automatic power control circuitry (U404, Q422), and antenna switch module (Z302).

7.3.1 Tx VCO

The Tx VCO in the synthesizer circuit is programmed to generate low phase noise transmitter carrier frequencies from 378 to 430 MHz. The output of the Tx VCO is applied to filter attenuator pads R332-R334 & R221-R223. The typical output level is 0 dBm.

7.3.2 Pre-Driver & Driver Ampliers

The output of the two filter attenuator pads is applied to pre-driver amplifier U202 and is amplified to +11.5 dBm. The output from the pre-driver amplifier is applied to driver amplifier Q202, and amplified to +21 dBm.

7.3.3 PA Module

The +15.5 dBm input into PA Module U201 is amplified to about 5.4 watts. The PA Module is a two stage RF amplifier. The first stage's bias voltage is supplied by the power control circuitry. The output of the PA module is regulated by this bias voltage. The second stage's RF amplifier operates in Class C. Its bias is the battery voltage [B+ (7.5 VDC)] that is connected to U201 through RF choke L251.

7.3.4 Automatic Power Control

The automatic power control circuit samples the forward output power to the antenna to maintain a constant power level across the band. The automatic power control circuit controls the voltage "Vcont" to PA Module U201, pin 2.

A directional coupler is included in the antenna switch module. This directional coupler provides a sample of transmitted forward power for diode detection. The diode produces a positive DC voltage proportional to the transmitter output power level. This DC voltage (Z302, pin 4) is compared at comparator U404 to the "TX POWER CONT" signal from the Patti IC (U500, pin 62). [Note: the TX POWER CONT signal out of Patti is set by RF Power tracking data.] The output of U404 is applied to DC driver amplifier Q421, and over to DC amplifier Q422. The output voltage of Q422 is applied to the Vcont input of PA Module U201, pin 2 to provide a constant output power level.

7.3.5 Antenna Switch Module

The Antenna Switch Module also consists of the transmit/receive switch circuitry and a low pass filter. During transmit, the DPTT signal from Hillary is high. Transistor Q402 turns on the "SW-5V" supply to antenna switch module Z302, pin 6. When transmitting, the antenna switch pin diodes are in a low impedance state. During receive mode, the antenna switch pin diodes are in a high impedance state.

The losses through the power control circuitry and the antenna switch module reduce the PA output power from 5.4 W down to around 4.2 W at the antenna connector. This provides the rated 4 Watts output power.

7.3.6 Frequency Synthesizer Circuit

The frequency synthesizer circuit consists of the reference oscillator, PLL frequency synthesizer chip U305 (CX72301), the loop filter, Rx VCO Z303, and Tx VCO Z304.
The PLL frequency synthesizer chip receives PLL data, clock, and control information from the microcomputer and from this generates the Tx carrier or Rx L.O. frequencies. It also provides frequency lock status back to the microcomputer.

The output of 19.2 MHz reference oscillator Z305 clock signal is fed into the PLL IC at U305, pin 14.

The Rx VCO and the Tx VCO are locked to the reference oscillator by a fractional–N synthesizer loop consisting of the loop filter, and the PLL frequency synthesizer chip.

The Tx VCO operates over a frequency range of 378-430 MHz. The Rx VCO operates as a low side injection source over a frequency range of 262.35-314.35 MHz.

7.3.7 Reference Oscillator

The 19.2 MHz reference oscillator consists of a ±1.5 ppm TCXO (Temperature Compensated Crystal Oscillator). The TCXO is enclosed in a RF shielded can. The TCXO is internally temperature compensated for both low and high temperatures. The nominal temperature is +25 ^{o}C (+77 ^{o}F). With no additional compensation, the oscillator will provide ±1.5-ppm stability from –30 ^{o}C to +60 ^{o}C (-22 ^{o}F to 140 ^{o}F).

7.3.8 PLL Frequency Synthesizer

PLL frequency synthesizer chip U305 (CX72301) provides fractionality through the use of its main sigma-delta modulator. (Note: the auxiliary sigma-delta modulator is not used.) The PLL IC is programmed in fractional-N mode with the main sigma-delta modulation programmed into its 18 bit configuration.

The 19.2 MHz reference source derived from the reference oscillator is divided by a programmed ratio from 1 to 32 to create a reference frequency for the main phase detector. The divide ratio is programmed into the Reference Frequency Divider Register.

The output from the external Tx or Rx VCO is input into a VCO pre-scalar on the IC. The pre-scalar provides low noise signal conditioning before it is input into the main divider. The main divider's divide ratios are programmable in range from 37.5 to 537.5.

The contents of the Reference Frequency Divider register, Main Divider register, MSB & LSB Dividend registers, the setting of the PLL IC into fractional-N instead of Integer-N mode, and the setting of the main modulator into 18 bit instead of 10 bit mode are established by data sent to the CX72301 from the Hillary microprocessor. The received data is transmitted via the SC.CLK, SC.DATA, and SC.SYN1LE lines.

The dividend is the Desired VCO division ratio in Fractional-N applications. This number is a real number and can be interpreted as the reference frequency (Fref) multiplying factor such that the resulting frequency is equal to the desired VCO frequency. With the sigma-delta modulator in 18 bit mode, the 18 bit signed input value to the modulator, ranging from –131,072 to +131,071, provides 262,144 steps. Each step size is 9.6 MHz/2^{18} (= 36.6 Hz). The signed input value is provided by the contents of the MSB & LSB Main Dividend registers. The Main Divider register's contents are set to 262,144.

The divided down VCO signal out of the VCO main divider and the divided down 9.6 MHz derived reference oscillator signal are input into the main phase/frequency detector. If the frequencies differ, then a phase error is detected, and an error voltage results. This developed error voltage is applied as a VCO DC offset voltage to an external loop filter to reset the VCO on frequency. When the VCO has adjusted on frequency, the error voltage is diminished and replace with a constant output voltage.

When a different channel is selected or when changing to the transmit or receive mode, an error voltage is generated and appears at the phase detector output, causing the Phase Locked Loop to acquire the new frequency.

During the transition to the new frequency, the LOCK DETECT signal is an active low, pulsing, open collector signal. After lock has occurred, the LOCK DETECT signal is a high impedance output. In the P7100^{IP} Radio & Logic schematics this signal is labeled as "UNLOCK" & sent over to the Hillary microprocessor (U500, pin 27). If the uP detects that the PLL IC is in an unlock state, then the transmitter is disabled.

7.3.9 Loop Filter

The loop filter consists of R322, R323, R325-R327, R331, C332, C336-C338, C340, C341, U304, & U309. This filter controls the bandwidth, stability, & switching speed of the synthesizer loop. The loop filter's bandwidth is switched via audio gates U304 & U309 which are controlled by signal "VCO.RX/TX" from the microcontroller. The output of the loop filter is applied to the varicaps in the transmit and receive VCO's to adjust and maintain the VCO frequency. The use of two VCO's allows rapid, independent, selection of transmit and receive frequencies across the frequency band.

7.3.10 Rx VCO and Tx VCO

The VCO's consist of low-noise silicon transistor oscillators followed by high-gain buffers. When changing to a different channel or changing from transmit or receive mode, signal "VCO.Rx/Tx" is used to control analog switches U304 & U309. These switches are used to either turn on the Rx VCO or the Tx VCO.

When the "VCO.RX/TX" signal is low, the U307 inverter and analog switch U304 turn on transistor Q301, which turns on Rx VCO Z303. When the "VCO.RX/TX" signal is high, analog switch U309 turns on transistor Q302, which turns on Tx VCO Z304. Both pass transistors Q301 and Q302 provide a low noise bias voltage to the VCO's via the "VSYN" bias line to provide optimized low phase noise performance.

The VCO's output powers are typically 0 dBm. The output is applied back to the PLL IC (U305, pin 7) for VCO frequency control via C367 & R321. The Rx VCO output is used as the local oscillator frequency by the receiver first mixer through the first local oscillator buffer amplifier (Q103). The Tx VCO output is applied to the pre-driver input.

The VCO voltages need only be set once at any frequency within the band and split. After that they will operate correctly over the entire split with no additional tuning.

7.4 INTEGRATED CIRUIT OVERVIEW

The RF circuitry is dominated by two (2) integrated circuits. These IC's are described as follows:

- **U101** (SA647) – This Rx back end IC contains the second mixer and the second IF (450 kHz) amplifier and limiter chain. The L.O. for the second mixer is the sixth harmonic of the 19.2 MHz reference oscillator. External ports are provided between the second mixer output and the I.F. amplifier input, and between the I.F. amplifier output and the limiter input to provide appropriate second I.F. selectivity. The limiter circuit provides a balanced output to HILLARY. The IC also provides the **R**eceiver **S**ignal **S**trength **I**ndicator (**RSSI**) signal.

- **U305** (CX72301) – This PLL IC provides the main frequency synthesizer for the Rx VCO to provide the L.O. for the first mixer and for the Tx VCO to provide the drive signal to the pre-driver transistor U202.

The digital circuitry is dominated by three (3) integrated circuits. These IC's are described as follows:

- U500 ("Patti") – Provides the CODEC that digitizes Tx analog baseband signals. It also provides the CODEC to convert digitized Rx signals back to analog signals for driving the internal audio amplifier and audio accessories via the UDC connector. It also provides the coarse tuning of the volume control for the receive audio. Digitized Tx/Rx signals are interfaced with Hillary. This IC also contains D/A converters for setting the Tx frequency on channel, generating sub-audible encode signals (CG, DCG, & EDACS low speed data), and setting the Tx RF power to the proper level. This IC contains an A/D converter for an RSSI input from the Rx backend IC. This IC also handles part of the Rx volume control function.

- **U600** (TMS320VC5416) – The DSP performs Digital Signal Processing on Tx/Rx analog and/or digital signals. Specifically, it provides the pre-emphasis filter, limiter, and post-limiter filter for Tx analog signals. It provides the digital data filter for Tx data. It provides de-emphasis and fine-tuning of the volume control for Rx analog signals. The DSP also provides all sub-audible baseband filtering.

- U700 ("Hillary") – Contains the microprocessor, phase digitizer, timing & logic control, frequency discriminator and sigma/delta modulator to provide digital modulation.

7.5 BASEBAND CIRCUITRY OVERVIEW

Internal mic audio is input through audio gate U505 into the MICIP port at U500, pin 14. If an external speaker/mic is attached to the UDC connector, then U505 is open-circuited to disable the internal mic. Mic audio from an external audio accessory is amplified in op-amp U501 (Av = 13.2 dB) and then input into the AUXI1 port at U500, pin 19. Note: the internal mic is part of the front cover assembly.

The Patti IC (U500) digitizes the signal at 8K samples/second into a 13 bit PCM signal. The digitized Tx baseband signal is input into the DSP (U600) where it is filtered and limited. The digitized output from the DSP is input into the Dual DAC IC (U601) where it is converted back into an analog signal. The Dual DAC's Channel A output (U601, pin 4) is routed through single pole double throw audio gate U602. If the radio is in Rx mode, a +1.6 V output from U706-4 is routed through the SPDT switch. In Tx mode, the Channel A output is routed to a 2-pole Low Pass filter consisting of R650, R652, C650, & C652. The filtered "MODI" signal is then fed to op-amps U205 & U310 to be mixed as inputs for reference oscillator and Tx VCO modulation. For the Tx VCO modulation, further filtering is provided by an elliptic filter consisting of L301, L303, C356, & C358. The signal is then AC coupled & translated down in level before being input into the Tx VCO at Z304, pin 7. Two inputs (AFC) & (TCG.DCG) are used for reference oscillator modulation. The Patti IC (at U500, pin 60) generates a DC voltage which is used to set the reference oscillator exactly at 19.2 MHz. [This DC voltage is derived from the reference oscillator tracking data.] The TCG.DCG signal is generated from the DA converter output at U500, pin 61. This signal is used to generate analog Channel Guard tones, Digital Channel Guard codewords, and EDACS Low Speed Data. The TCG.DCG signal is mixed through op-amps U205 & U310 over to reference oscillator Z305.

Analog receive signals are output from the AUX02 port at U500, pin 22. The receive signal is then attenuated by either –3.3 or –21.2 dB in op-amp U504. The decision on switching the gain is part of the receive volume control process. The additional 17.9 dB of loss is actuated by turning on one of the 2 transistors in dual transistor Q500 and shorting R524 in parallel with R523. The output of U504 can be delivered via R530 & C537 to the UDC connector for use as a driver signal for audio accessories. The output of U504 is also the input to audio amplifier U502. U502 amplifies the driver signal to provide 0.5 W rated power to the 16 Ω internal speaker (SP1). The audio amplifier is turned on and off by providing or removing battery voltage supplied through pass transistor Q501. Q501 is on or off by the second transistor in dual transistor Q500, which is controlled from U700, pin 128. Note: the internal speaker is part of the front cover assembly.