Circuit Analysis of JAGUAR700M 800MHz Synthesizer Block (TG-0038LS)

1. Frequency Synthesizer Circuit

The Frequency Synthesizer circuit receives PLL data, and control information from the microcomputer and from this generates the Tx / Rx RF frequencies.

It also provides frequency lock status to A/L & IF UNIT. It consist of the Reference Oscillator, PLL Frequency Synthesizer chip IC501, Loop filter, Rx VCO TR401, Tx VCO TR405, Feedback Buffer Amplifier. Rx VCO and Tx VCO are locked to the Reference Oscillator by a single direct-divide synthesis loop consisting of the Feedback Buffer, and PLL Frequency Synthesizer chip.

The Tx VCO operates over a frequency range of 403-412.5MHz and 425.5-435MHz.

The Rx VCO operates over a frequency range of 384.4-393.9MHz.

1-1. Reference Oscillator

The reference oscillator consists of a 1.5PPM TCXO (Temperature Controlled Compensated Crystal Oscillator). The standard reference oscillator frequency is 19.2MHz.

The TCXO is enclosed in a RF shielded can. The TCXO is compensated by internal temperature compensated circuit for both low and high temperature. With no additional compensated the oscillator will provide 1.5 PPM stability from -30°C to +60°C.

1-2. PLL Frequency Synthesizer chip

PLL Frequency Synthesizer chip IC501 contains a programmable reference oscillator divider (R), phase detector, and programmable VCO dividers (+N, A).

A fixed integer number to obtain a 6.25KHz or 5KHz channel reference for the synthesizer divides the reference frequency 19.2MHz from the reference oscillator.

EDACS4 can change this divide value.

The internal phase detector compares the output of the reference divider with the output of internal +N,A counter. The +N, A counter receives as its input the VCO frequency divided by the Prescaler and programmed by the microcomputer.

This results in an error voltage when the phase differ and a constant output voltage when phase-detector input compare in frequency and phase.

If a phase error is detected, an error voltage is developed and applied to the VCO DC offset and loop filter to reset the VCO frequency. The count of the +N, A counters is controlled by the frequency data received on the SCK+, SDT+ and PLLENB+ line from A/L & IF UNIT.

When a different channel is selected or when changing to the transmit or receive mode an error voltage is generated and appears at the phase-detector output, APD(IC305-2pin), causing the Phase Locked Loop to acquire the new frequency.

1-3. Loop filter

The Loop filter consists of R518 through R523 and C524, C532 through C534.

This filter controls the bandwidth and stability of the synthesizer loop.

When a different channel changing or changing to the transmit or receive mode, FET switch is controlled by PLLFST2- for PLL lock up first.

The output of the filter is applied to the varicaps in the transmitter and receiver VCO's to adjust and maintain the VCO frequency. The use of to VCO's allows rapid independent selection of transmit and receive frequencies across the frequency split.

1-4. Rx VCO

The Rx VCO consists of FET oscillator TR401, and followed by high-gain buffer TR402. TR402 prevents external loading and provides power gain.

The VCO is a colpitts oscillator with the various varactors, capacitors and coil the tank circuit.

The VCO is switched on and off VCOENB+ line. When VCOENB+ is high, the Rx VCO is turned on, transistor TR401 and TR402 is on. The output of the Rx VCO after 2 times(through R302) is typically 0dBm. The output is applied to the feedback buffer for the VCO frequency control and as the Receiver frequency to Rx 1'st Mixer through the Local oscillator buffer amplifier. The VCO voltage need only be set once at some frequency of the band and split, after which it operates over the entire split with no additional tuning.

1-5 Tx VCO

The Tx VCO is basically the same as the Rx VCO. The VCO consists of FET oscillator TR304 followed by high-gain buffer amplifier TR303. When DPTT- is low, the Tx VCO is turned on, transistor TR303 and TR304 is on. The output of the Tx VCO after 2 times(through R301) is typically 0dBm.

1-6. Common Doubler

The common doubler consists of TR317. The common doubler does the oscillation frequency of the reception/transmission VCO 2 times.

1-7. Feedback Buffer Amplifier

The output of Rx VCO and Tx VCO, from transistor TR402 and TR407 respectively, are supplied to Feedback Buffer Amplifier IC404 and TR404

1-8. Dual-Modulus Prescaler

The Dual-Modulus Prescaler completes the Phase Lock Loop(PLL) feedback path from the PLL Frequency synthesizer chip to the Loop Filter, to the VCO's and Feedback Buffers and then back to the PLL Frequency synthesizer chip through the Prescaler.

The Prescaler divides the VCO by 64 or 65 under control of MC(IC306-6pin) from the PLL Frequency synthesizer chip. The output of the Prescaler is applied to the PLL Frequency synthesizer chip where it is divided down 5KHz or 6.25KHz by and internal +N, A counter and compared in frequency and phase with the divided-down frequency for the Reference Oscillator. The result of this comparison is the error voltage used to maintain frequency lock. The +N, A counter is controlled by data received from the A/L UNIT. Depending on the operating frequency, the DC voltage at Test Point TP501 should be within 1.5 to 6.5 Vdc when the PLL is locked.

1-9. Lock Detect

The Lock Detect circuit consists of transistor IC501.

If a large frequency error exists, then unlock, PLLLOCK+ goes to low.