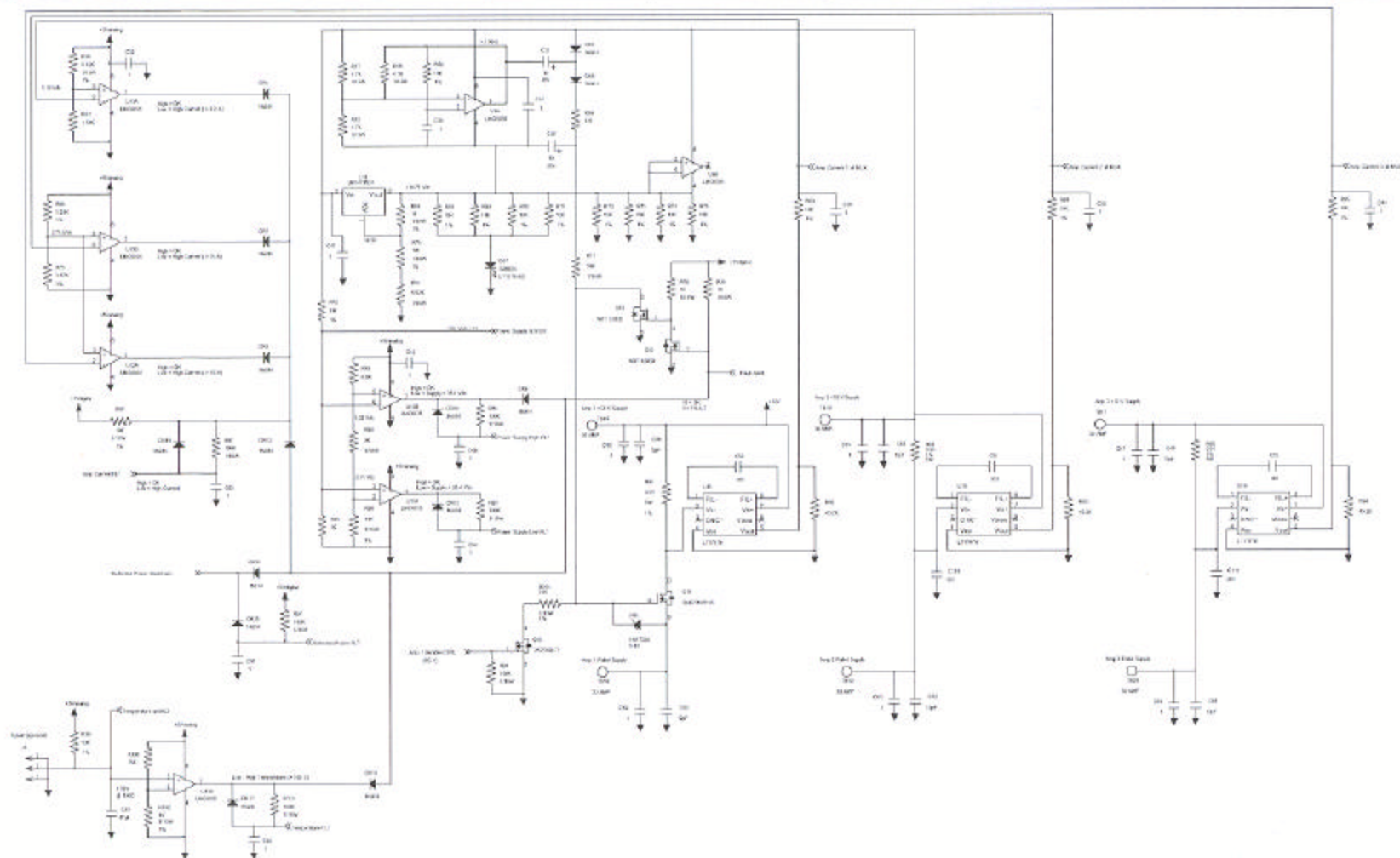
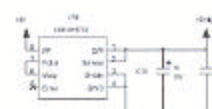
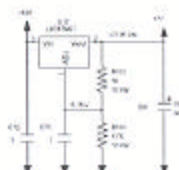


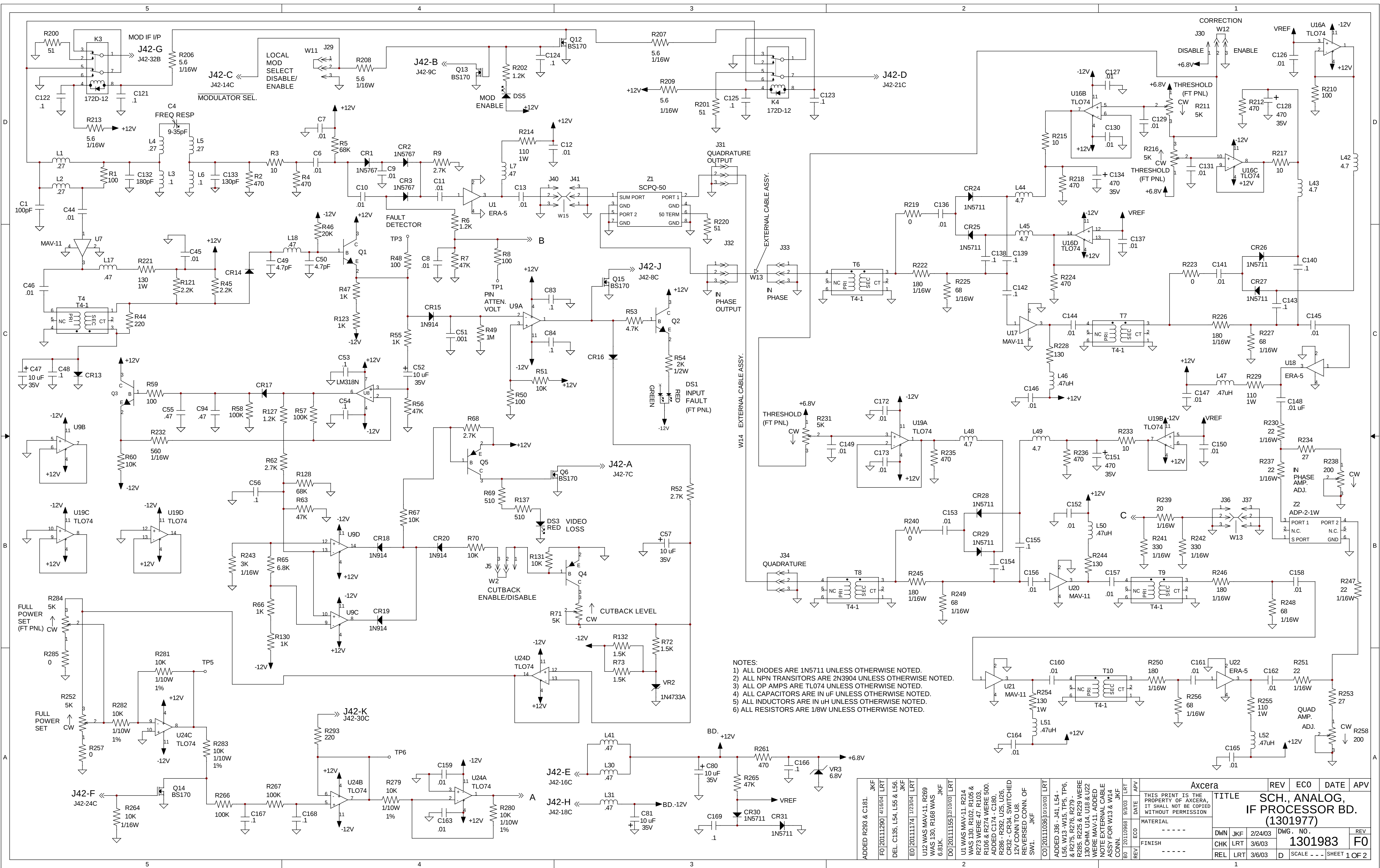


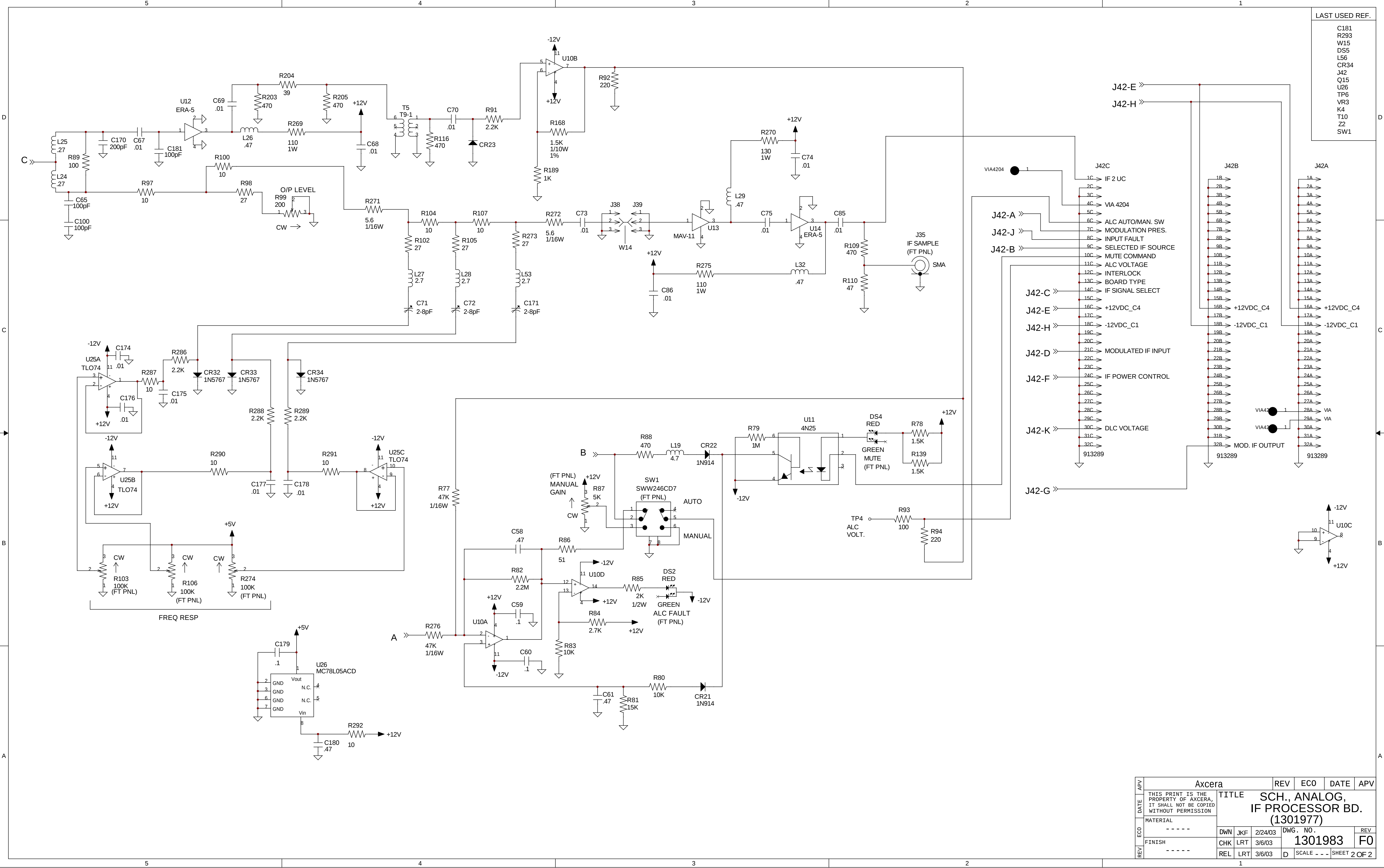
NOTE:

A track width of 3 mils is needed between power input vias and series resistors R55, R56, R57. 0.3 inch track width is also needed between the output of the series resistors and the output vias that provide power to the amplifier palette.



Access				REV	ECO	DATE	APP
SCH_AMP				1			
CONTROL, INNOVATOR LX							
(1303662)							
1303663							
G0							





600W pep –27dBc min LDMOS Technology

Designed for analog and digital TV transposers and transmitters, this amplifier incorporates micro-strip technology and push-pull LDMOS to enhance ruggedness and reliability. Patented bias control and matching circuit.

- 470 - 862 MHz
- (42 ÷ 50 Volt) 43 Nominal
- Input/Output 50Ω - 50Ω
- P_{out} : 600W pep –27 dBc min (2-tone test 100KHz spacing)
- Gain : 14 dB min; 16 dB typ
- Class AB
- Devices: BLF878 or equivalent
- Connectorized version available (SMA/N Output)
- No mechanical trimmers - maximizes MTBF



ABSOLUTE MAXIMUM RATINGS (Device Flange T = 70 °C)

Symbol	Parameter	Value	Unit
V _S	Drain-Source Voltage (without RF)	80	V dc
I _S	Current Supply	40	A dc
T _{stg}	Storage Temperature Range	-20 + 80	°C
T _c	Operating Base Plate Temperature ¹	0 + 75 ²	°C
ψ	VSWR max	3:1 all phase angle	-
	Max input power	See note ³	-
	Max cw output power	400	Watt

ELECTRICAL SPECIFICATIONS (Base Plate T_c = 45 °C, 50Ω loaded, V_d = 43 V)

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ.	Max	
BW	Bandwidth	P _{out} = 300 W (CW)	470		862	MHz
G _p	Power gain	P _{ref} = 200 W (CW)	14	16	-	dB
1dB cp	Power Output @ 1dB cp	Referred to P _{out} = 80W (CW) ⁴	500	650	-	W
I _q *	Quiescent Current	P _{out} = 0 W – Total * ⁵	-	-	4.0	A
I _{tot}	@ P _{Max}	500W Ps Black Level Video + Audio	-	-	30	A
I _{rl}	Input return loss	P _{out} = 300 W CW	15	20	-	dB
ψ	Load mismatch	P _{ref} = 300 W CW, f= 862MHz, load VSWR = 2:1, all phase angles ⁶	No degradation in P _{out}			
Gr	Gain Flatness	P _{ref} = 300 W CW, BW: 470-862MHz		±0.5	±1.5	dB
η	Drain Efficiency	P _{out} = 400 W ⁷ (CW)	40	45	-	%
	P _{out} DVB-T	P _{out} 140Wrms without precorrection		140		W rms
	IMD (Inside the Channel)	P _{out} 450W ps common ampl. dual sound, with Red Field sound 1 @ -13dB and sound 2 @ -20dB without precorrection	-46	-50		dBc
	P _{out} common ampl	P _{out} 450W ps common ampl. dual sound, with Red Field sound 1 @ -13dB and sound 2 @ -20dB without precorrection	-46	-50		dBc
	Shoulders @ +/-4.2MHz	P _{out} 140Wrms (DVB-T) without precorrection	-28	-32		dBc

¹ A temperature sensor is mounted on the circuit to have an immediate working temperature measurement.

² **Warning:** The base plate temperature must be 75 °C max, using an appropriate heatsink.

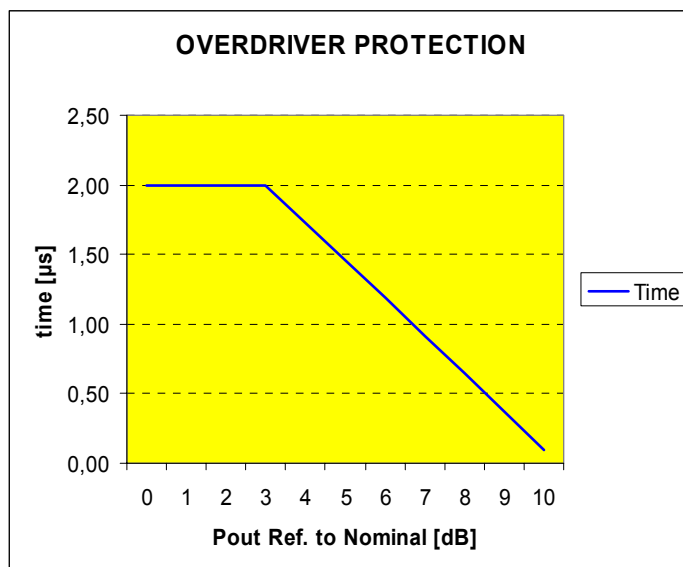
³ **Warning:** The input power must not exceed +6dB, for 300 nanosecond, the nominal input power referred to the 1dBcp power output, or nominal input power to obtain 100W DVB-T Output. Power, See plot "A"

⁴ Max 400W CW continuous work

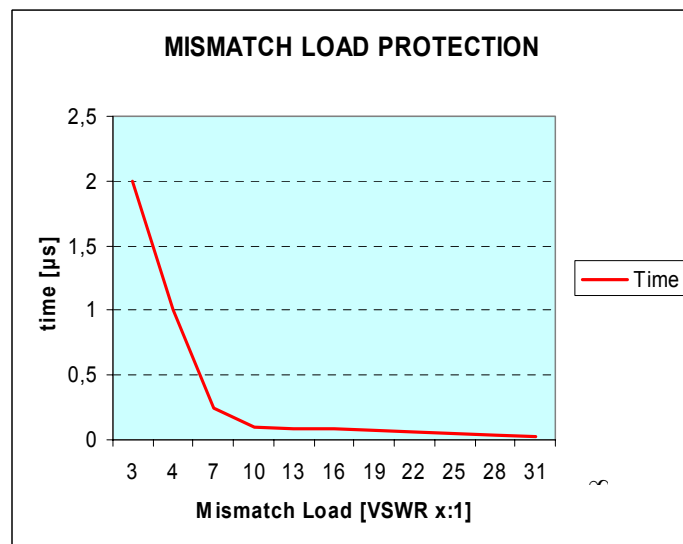
⁵ The Quiescent Current is set at optimal value, in factory. This parameter can be fine adjusted by means of the IR Bias Control Unit (option) depending on the applied signal and/or frequency and output power (See LDMOS Technology Note). (**Warning:** Do not exceed the specified max I_q value).

⁶ **Warning:** In case of DVB-T or DTV application nominal performance are warrant up to 1,8 : 1 load VSWR . If load mismatch exceed this value a specific protection circuit must be used, typical shutting down answer time is showed in the plot "B"

⁷ Do not keep the amplifier working at this P_{out} for more than one minute.



PLOT "A"



PLOT "B"



SMART BIAS SPECIAL FEATURES

- No mechanical trimmers to increase reliability
- Unmatched stability of the rest current (I_q) in the range of -30 to +100 deg.C (flange temperature)
- Built-in over temperature protection
- Built-in soft start for switch-on at extreme low temperatures (for outdoor application)
- Bias factory settings stored in memory

IR COMMANDS

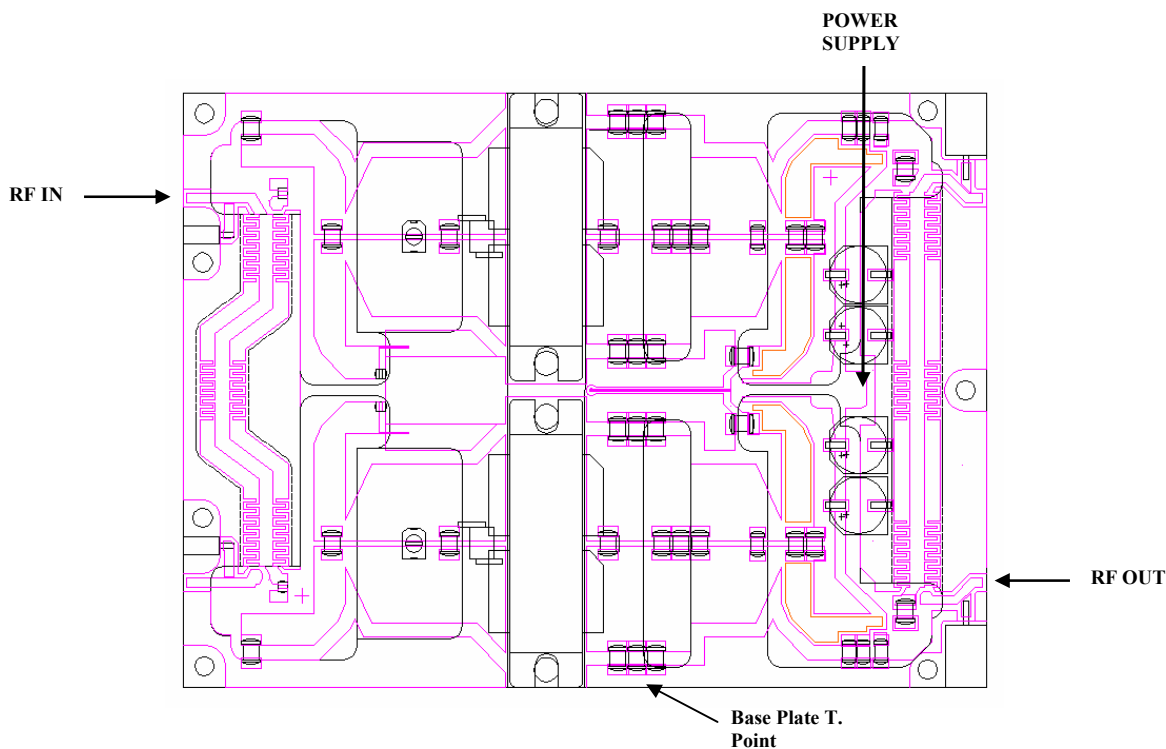
- Current control (Left and right power device)
- Shut down (pallet switch-off)
- Look-up table bias values activation via IR port (Bias factory settings stored in memory)

Note

IR bias control unit (shown above with LDU661C) is available upon request. (OPTIONAL)
The picture here above do not necessary represent the final version of the Ir Bias Control Unit

Contacts: Res-Ingenium, +39 0763 316333 Fax +39 0763316002- or visit www.res-ingenum.com

LDU661C Layout and Connections⁸



NOTE. In response to customer request, this pallet has been designed to allow two different positions of IN/OUT connections: /TL = connection on the left side, /TR = connection on the right side.

HEATSINK MOUNTING/HARDWARE

1. HEATSINK TOOLING

- Planarity: typical value 0.8
- Roughness: better than 0.03 mm

2. THERMAL COMPOUND

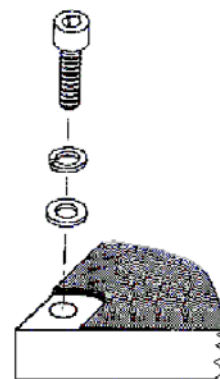
- Paste with silicones
- Thickness: optimum between 0.06 mm and 0.15 mm, on the whole back surface of the amplifier.

3. SCREWS

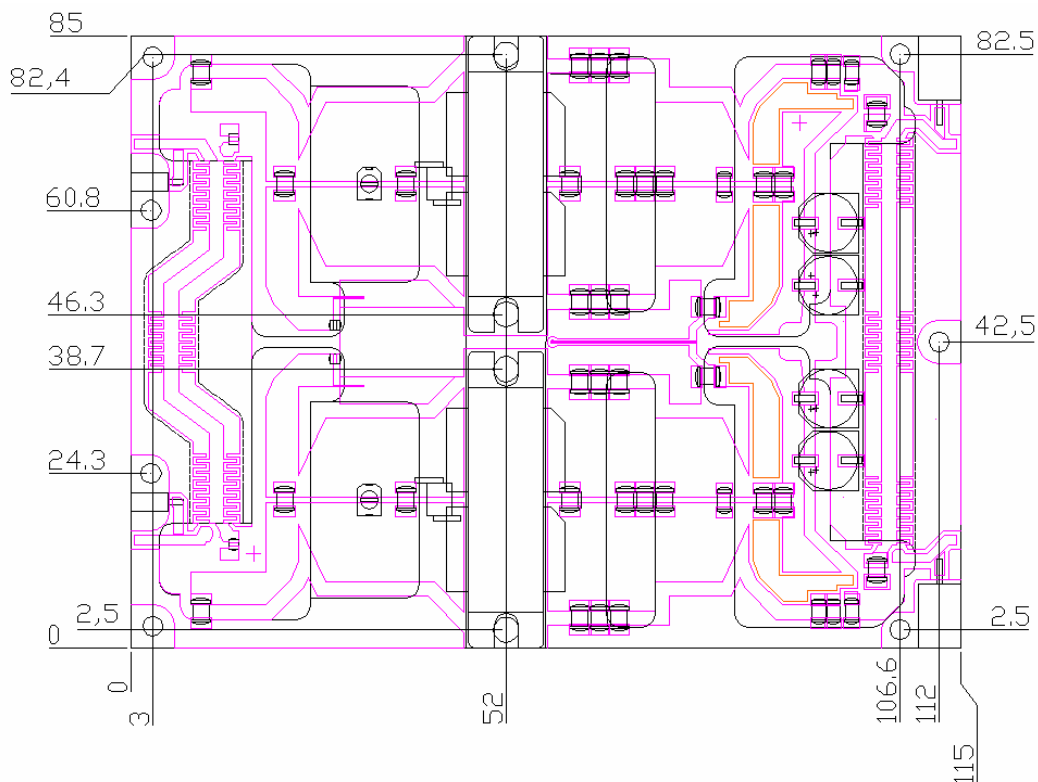
- 11 x M2.5 - Socket head cap screws.
- 8 Split lock washers WZ Ø3 + 8 Flat washers ZU Ø3.
- The recommended Torque is 12 Kg/cm for M3 type screws and 10 Kg/cm for M2.5 type screws.

4. TIGHTENING ORDER

- See next figure:



⁸ RES provides the pallet without unbalanced load resistors (input 50 Ohm 20W/output 50 Ohm 100W. Dimensions: 13 x 6.3mm, about, 1 hole).



Dimensions in mm.

WARNING

In the interest of continual product improvement all specifications are subject to change without notice

Res-Ingenium

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05018 Orvieto (TR)
Italy
Telephone: +39 0736 316333
Fax: +39 0763 316002
Internet: res-ingenum.com
E-Mail: map@res-ingenum.com

IMPORTANT NOTICE

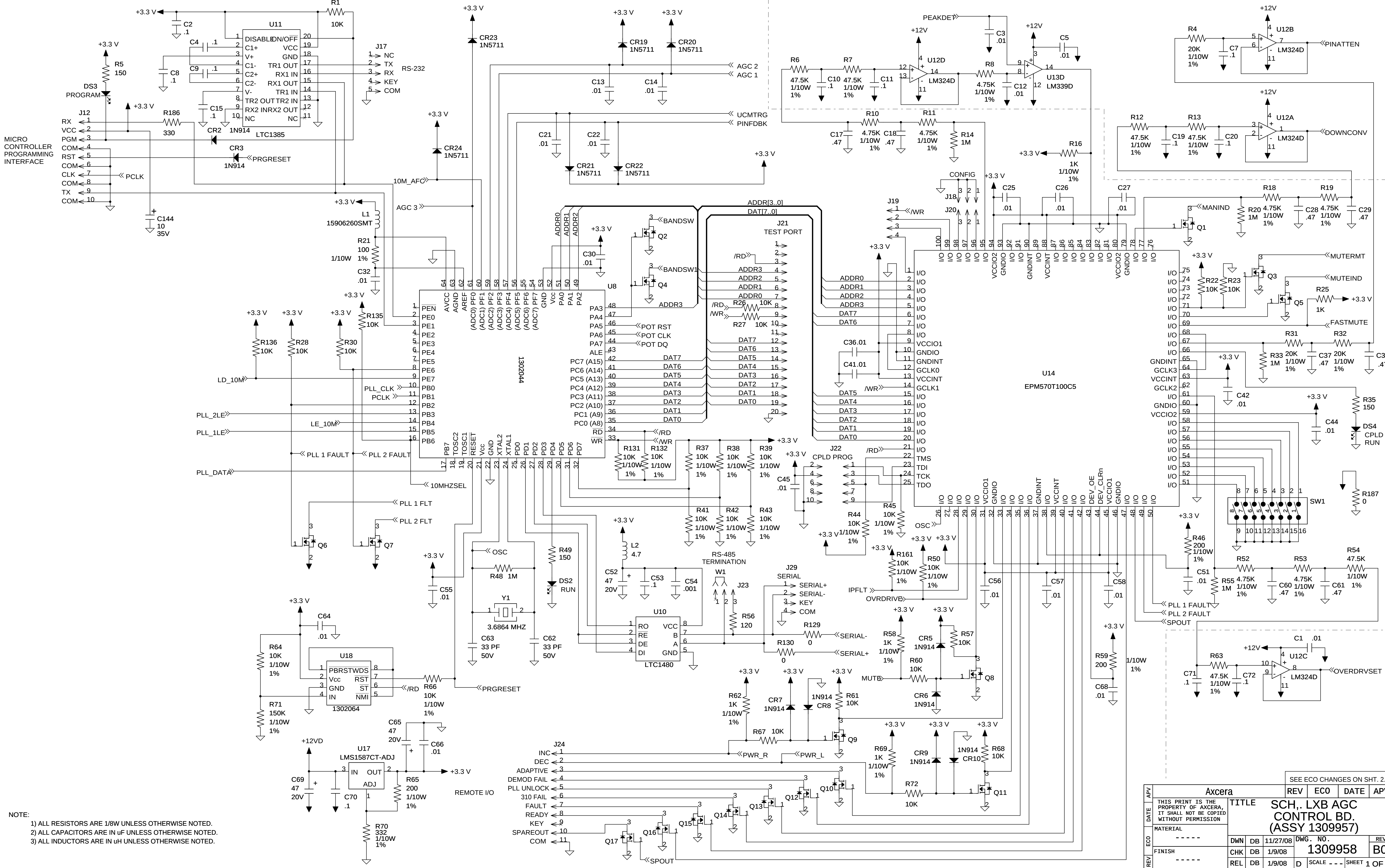
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WARNING

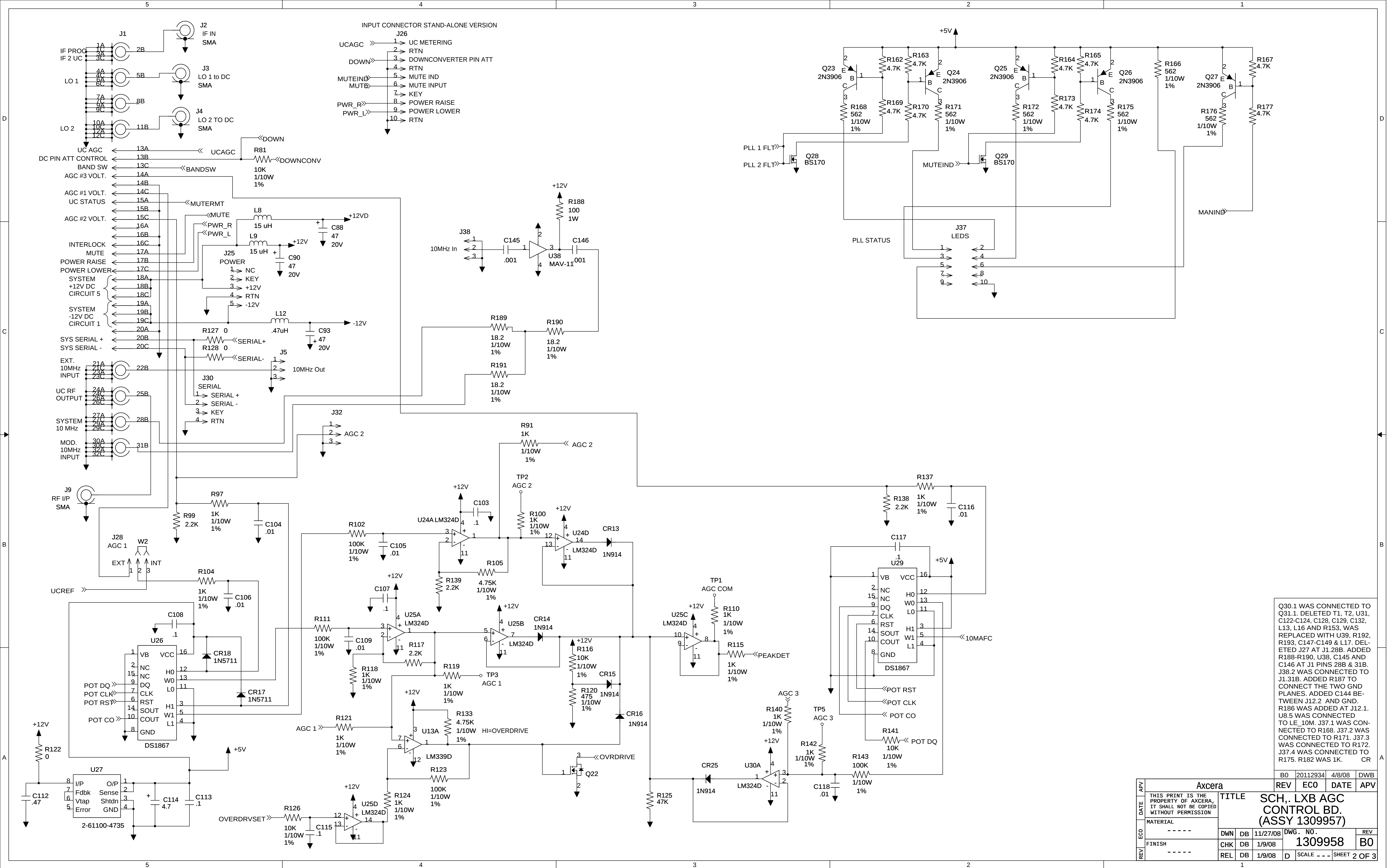
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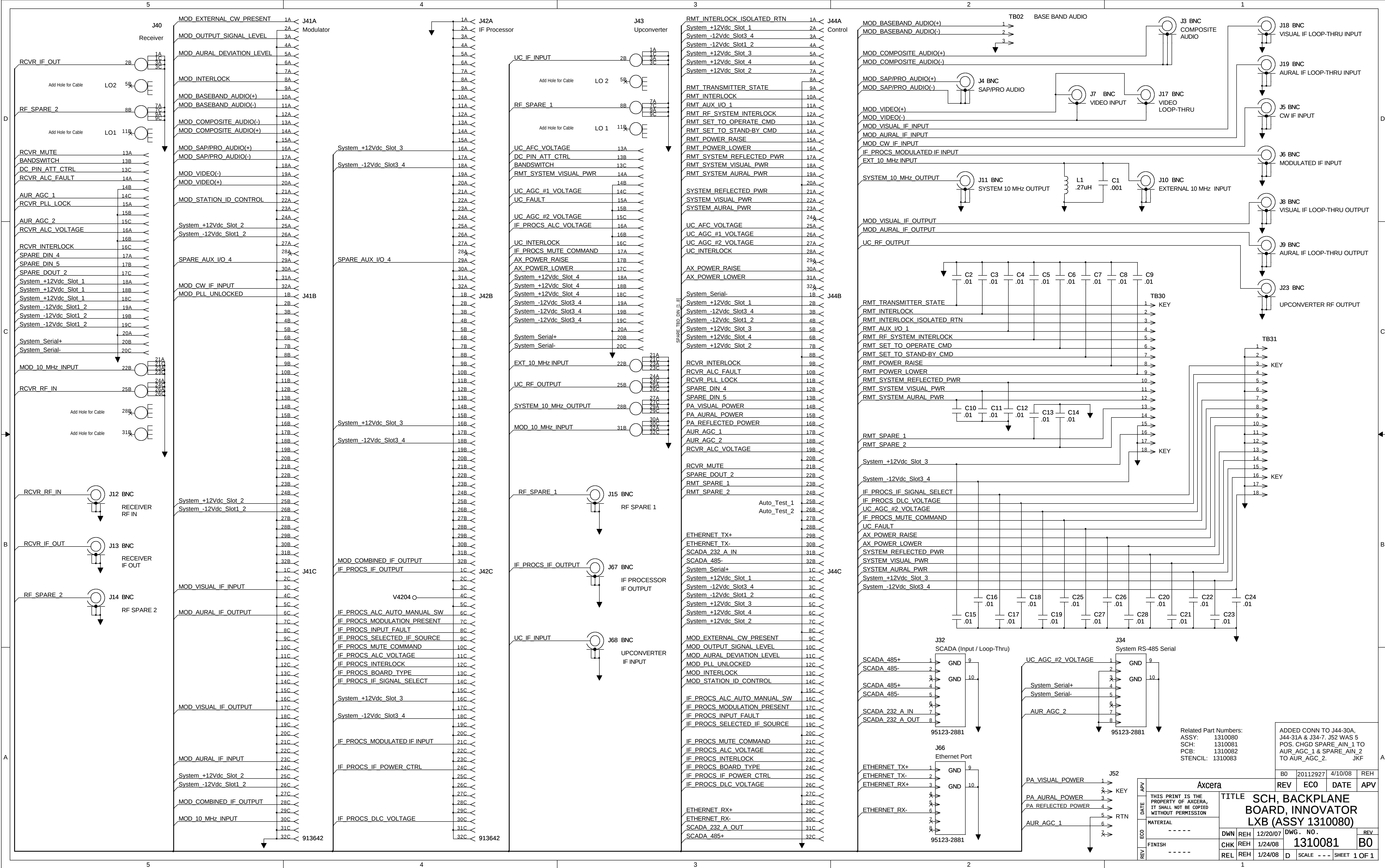


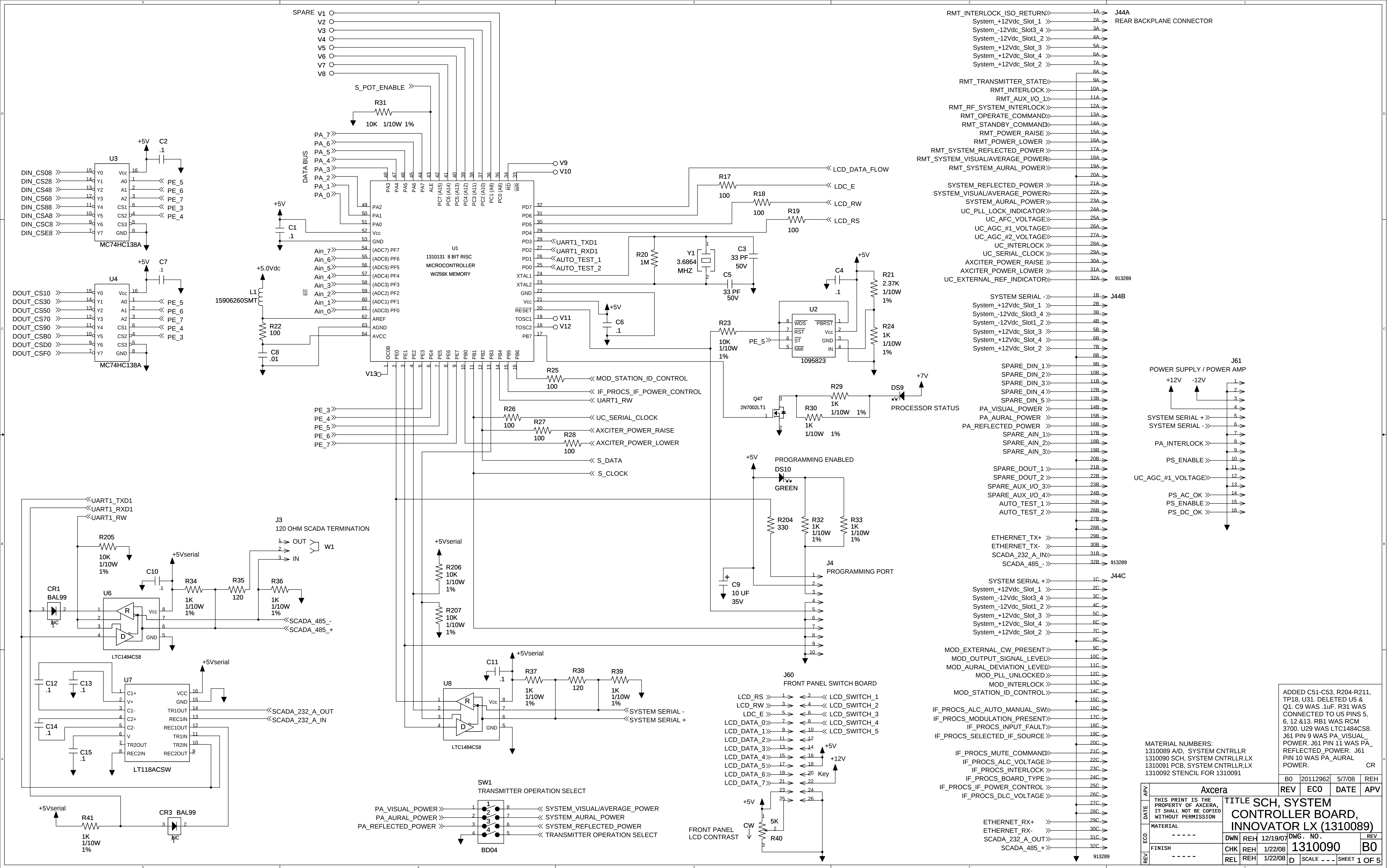
NOTE:

- 1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
- 2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
- 3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.

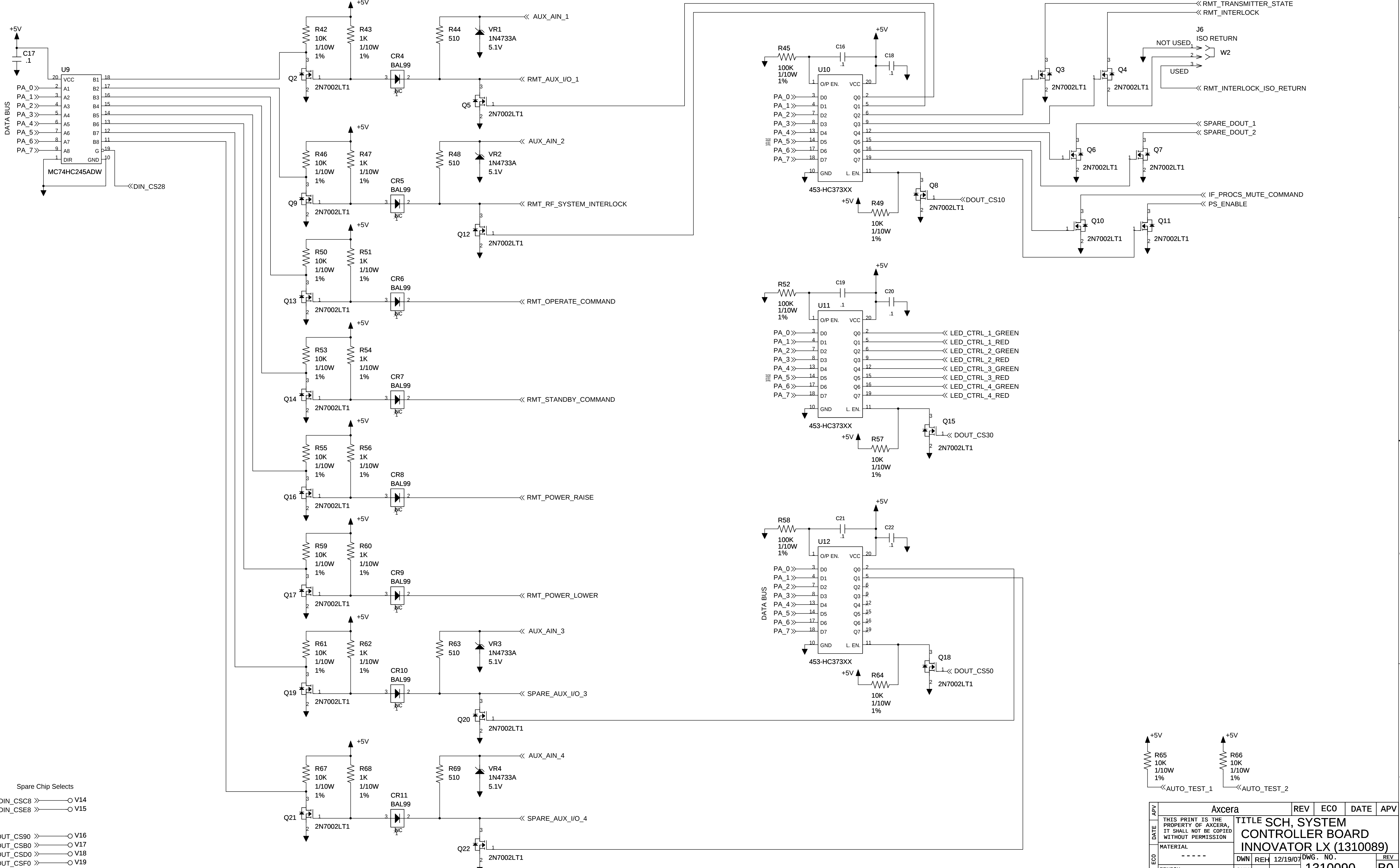
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MATERIAL		DWN		DB	11/27/08	DWG. NO.	REV
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REV		REL		DB	1/9/08	D	SCALE - - - SHEET 1 OF 3





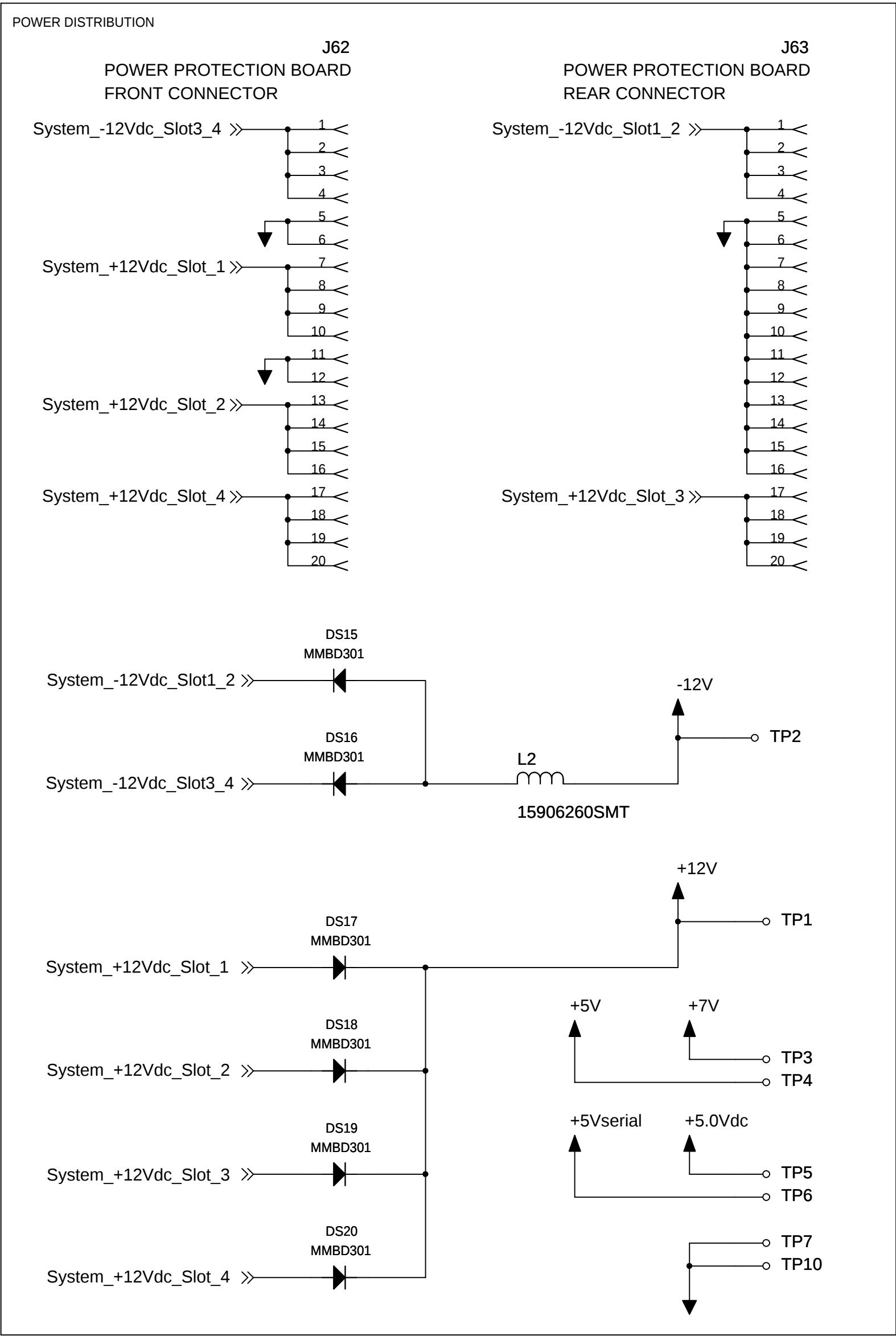
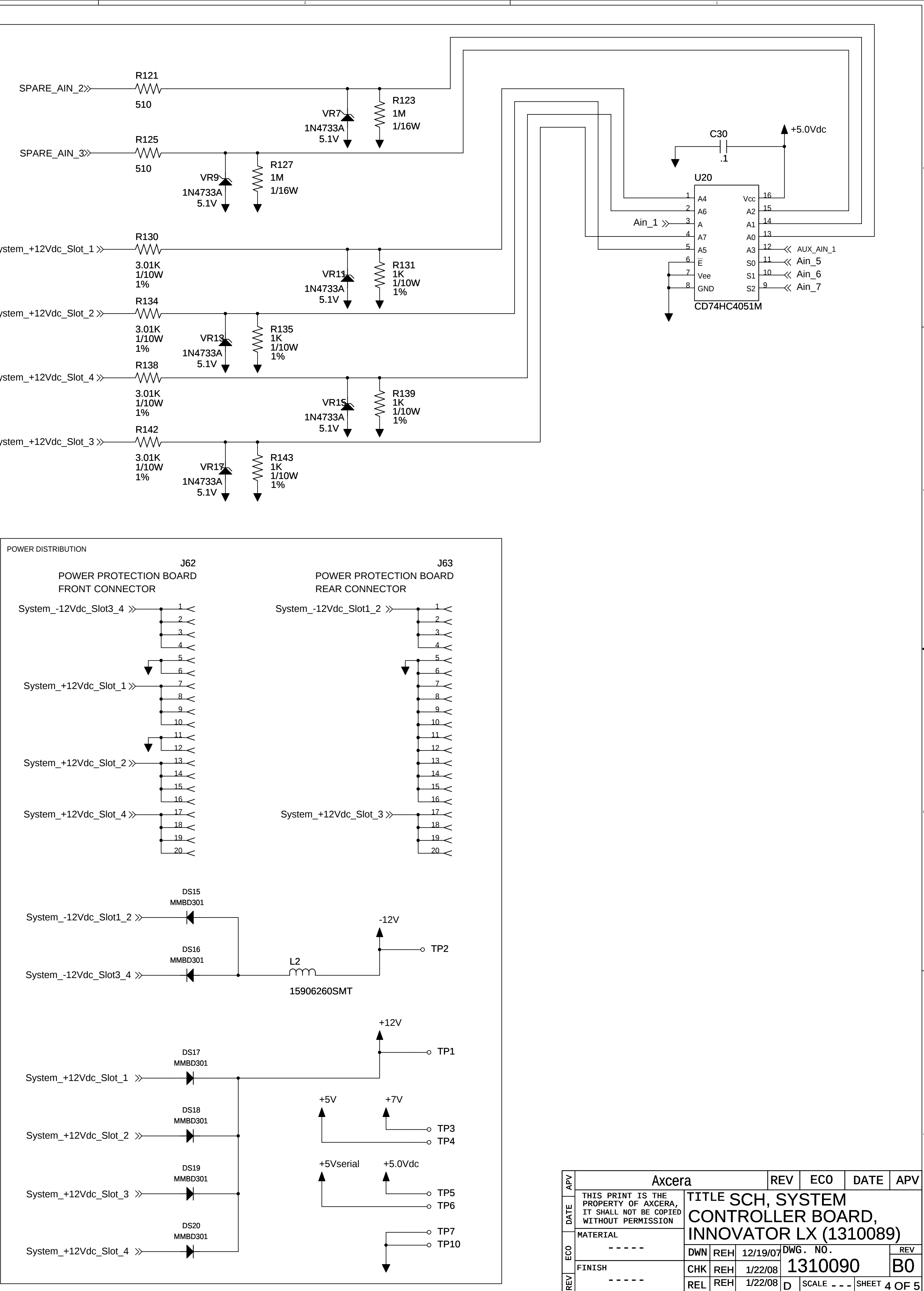


MATERIAL NUMBERS: 1310089 A/D, SYSTEM CNTRLR 1310090 SCH, SYSTEM CNTRLR,LX 1310091 PCB, SYSTEM CNTRLR,LX 1310092 STENCIL FOR 1310091				CR			
B0				20112962			
5/7/08				REH			
APV				REV			
THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION				TITLE SCH, SYSTEM CONTROLLER BOARD, INNOVATOR LX (1310089)			
DWN				REH			
12/19/07				DWG. NO.			
1/22/08				1310090			
CHK				REV			
REL				B0			
1/22/08				D			
SCALE				SHEET 1 OF 5			



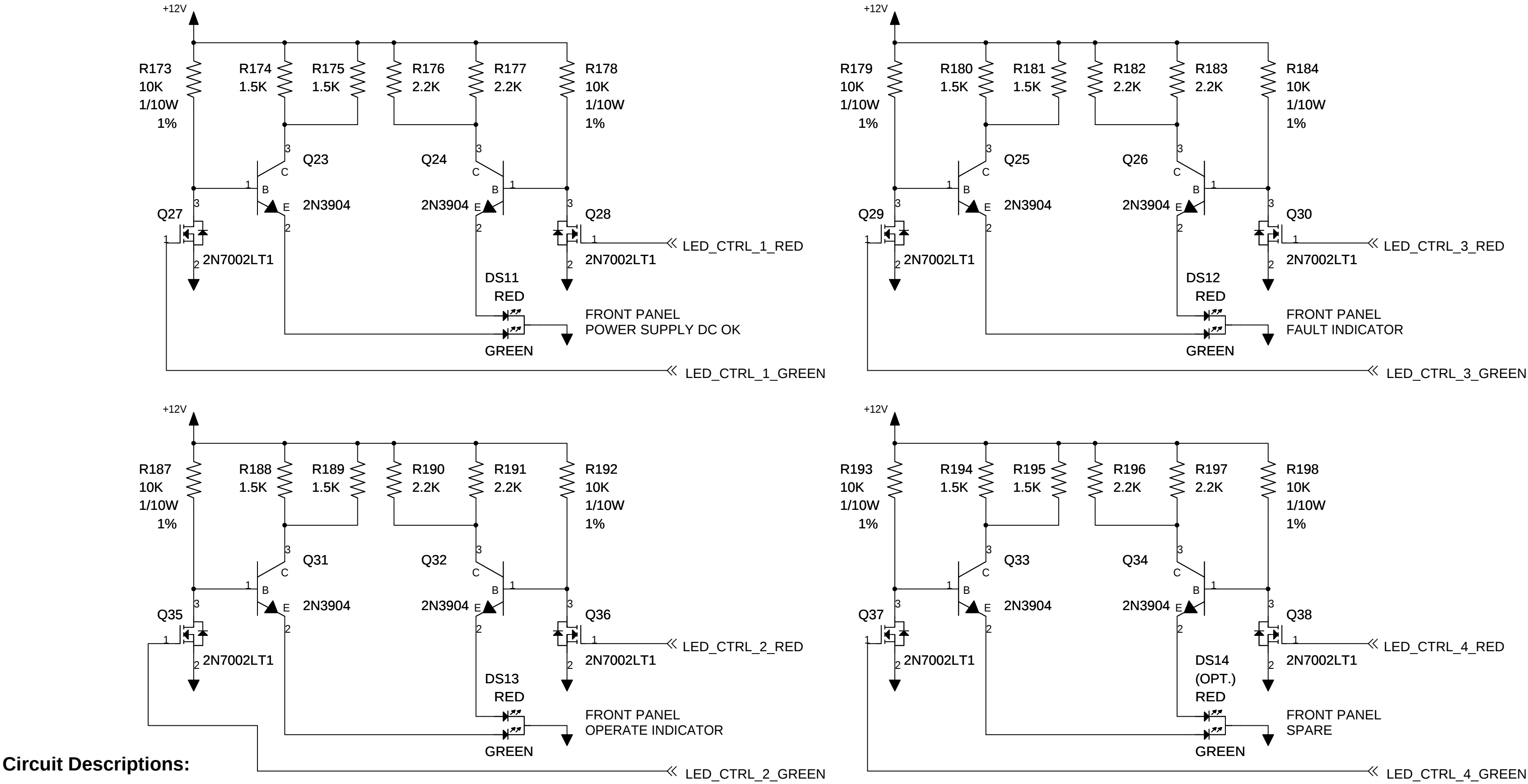
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	-----				REL	REH	1/22/08	B0
					SCALE	---	SHEET 2 OF 5	

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ECO	MATERIAL -----				DWN	REH	12/19/07	DWG. NO.
REV	FINISH -----				CHK	REH	1/22/08	1310090
					REL	REH	1/22/08	B0
						D	SCALE ---	SHEET 3 OF 3



APV	Axcera				REV	ECO	DATE	APV
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ECO	MATERIAL		DWG. NO.					
	-----		DWN	REH	12/19/07			REV
REV	FINISH		1310090					
	-----		CHK	REH	1/22/08			B0
			REL	REH	1/22/08	D	SCALE ---	SHEET 4 OF 5

R211
C53
Q47
DS20
U31
VR22
J64
TP18
V23
SW2
CR11
W2
Y1
L2



Circuit Descriptions:

PAGE 1:

U1 is an Atmel Atmega2561 microcontroller. This part is in-circuit programmed using the serial programming port.

U2 is a watchdog IC used to hold the microcontroller in reset if the supply voltage is less than 4.21 Vdc; (1.25 Vdc < Pin 4 (IN) < Pin 2 (Vcc)). The watchdog momentarily resets the microcontroller if Pin 6 (IST) is not clocked every second.

A test board is used to execute self test routines. When the test board is installed, Auto_Test_1 is held low and Auto_Test_2 is allowed to float at 5 Vdc. This is the signal to start the auto test routines.

U3 and U4 are used to selectively enable various input and output ICs found on page 2 and 3 of the schematic.

U1 has two serial ports available. In this application, one port is used to communicate with transmitter system components where U1 is the master of a RS-485 serial bus. The other serial port is used to provide serial data I/O where U1 is not the master of the data port. A dual RS-232 port driver IC and a RS-485 port driver is also in the second serial data I/O system. The serial ports are wired such that serial data input can come through either the RS-232 or RS-485 channels. Data output is sent out through each of the two serial port channels.

Switch SW1 is used to select either transmitter operation or exciter driver operation. When the switches of SW1 are on, transmitter operation is selected and the power monitoring lines of the transmitter's power amplifier are routed to the system power monitoring lines.

PAGE 2:

Digital output latches are used to control system devices. Remote output circuits are implemented using open drain FETs with greater than 60 Volt drain to source voltage ratings.

Remote digital inputs are diode protected with a 1 Kohm pull-up resistor to 5Vdc. If the remote input voltage is greater than about 2 volts or floating, a FET is turned on and a logic low is applied to the digital input buffer. If the remote input voltage is less than the turn on threshold of the FET (about 2 Vdc), a logic high is applied to the digital input buffer.

Four of the circuits on page two are auxiliary I/O connections wired for future use. They are wired similar to the remote digital inputs but include a FET for digital output operation. To operate these signals as an input, the associated output FET must be turned off. These circuits are also connected to an analog input multiplexer IC.

PAGE 3:

Several ICs are used as input buffers to allow the microcontroller to monitor various digital input values. Most digital inputs use a 10 Kohm pull-up resistor. The buffer IC used for data transfer to the display is wired for read and write control.

RB1 is the connector to a Rabbit Semiconductor RCM4300. This ethernet enabled controller polls the U1 microcontroller on the same serial lines as a remote computer. The controller only gets data and sets conditions through the serial communication port.

PAGE 4:

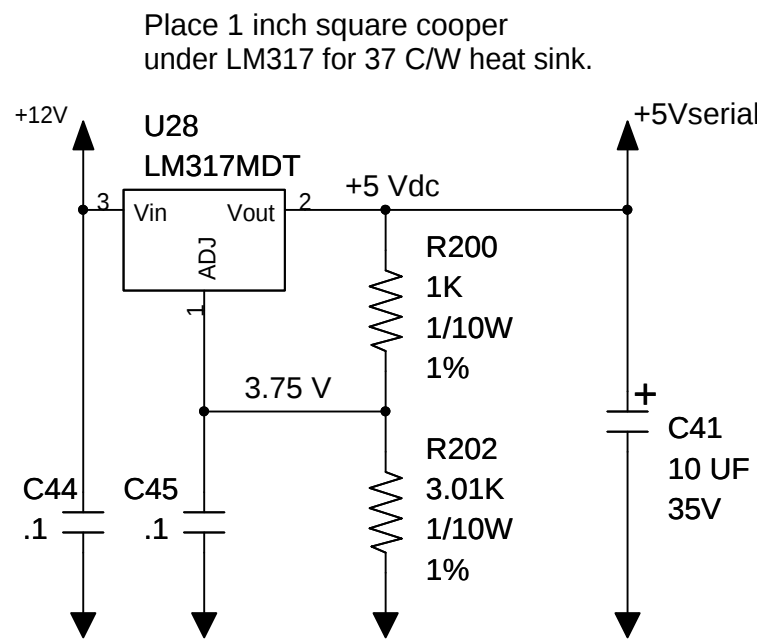
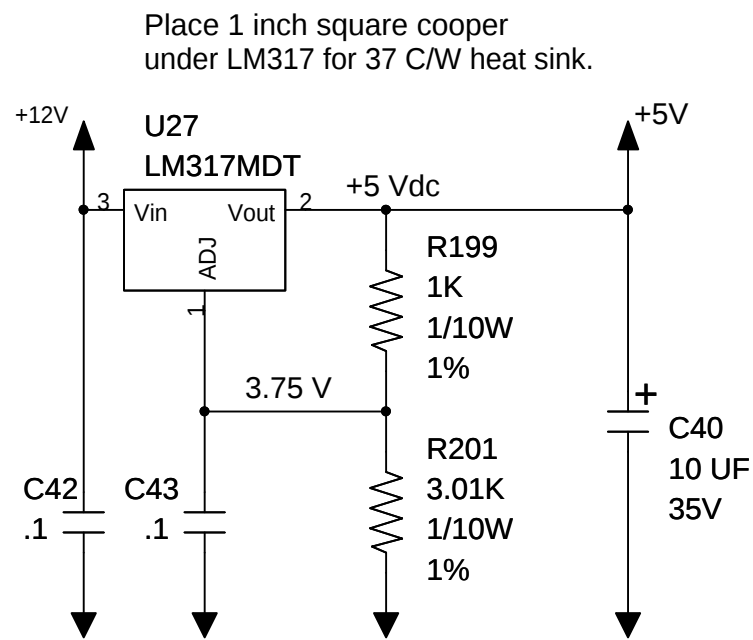
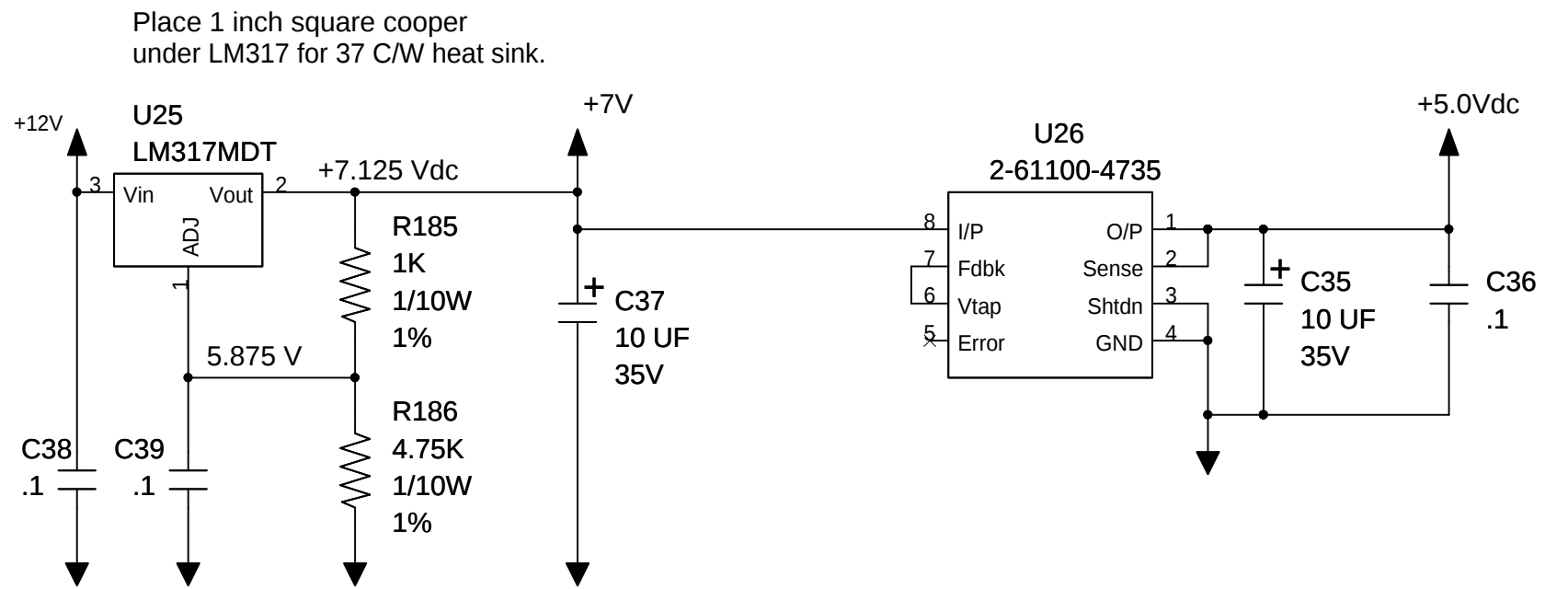
Each analog input is expected to be between 0 and 5 Vdc. If a signal exceeds 5.1 Vdc, a 0.225 Watt zenor diode clamps the signals voltage. Most signals are calibrated at their source however two dual serial potentiometer ICs are used to calibrate four signals. For these four circuits, the input value is divided in half before it is applied to an op-amp. The serial potentiometer is used to adjust the input signal between 80 and 120% of the input signal. Serial data to the second serial potentiometer is transferred through the first IC. The wiper position of the digital potentiometer circuit is used to set the gain of the op-amp. Lower digital values for the wiper setting increases the gain of the op-amp. If N= 0, gain = 6.0. If N = 255, gain = 3.00. If Vin = 1.0 at spare_Ain_1 and N = 128, U21A out = 4.0V with gain = 4.

Two 20 position connectors are used to provide power to the backplane. J62 and J63 get power from the power supply after a nominal 3 amp resettable fuse. The Raychem polyswitch resettable fuses may open on a current as low as 2.43 amps at 50C, 3 amps at 25 C or 3.3 amps at 0C. They definately will open when the current is 4.86 amps at 50C, 6 amps at 20C, or 6.6 amps at 0C. Trace widths of these circuits are 0.140" (designed for maximum current).

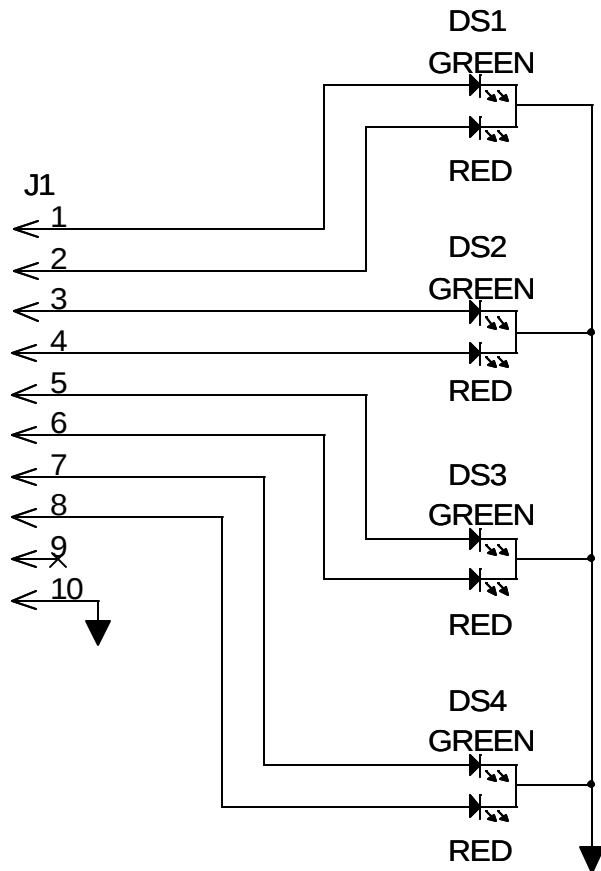
PAGE 5:

Each of the four LED circuits drive a dual element common cathode LED. To make a good amber color, the current applied to the green element is slightly greater than the red element.

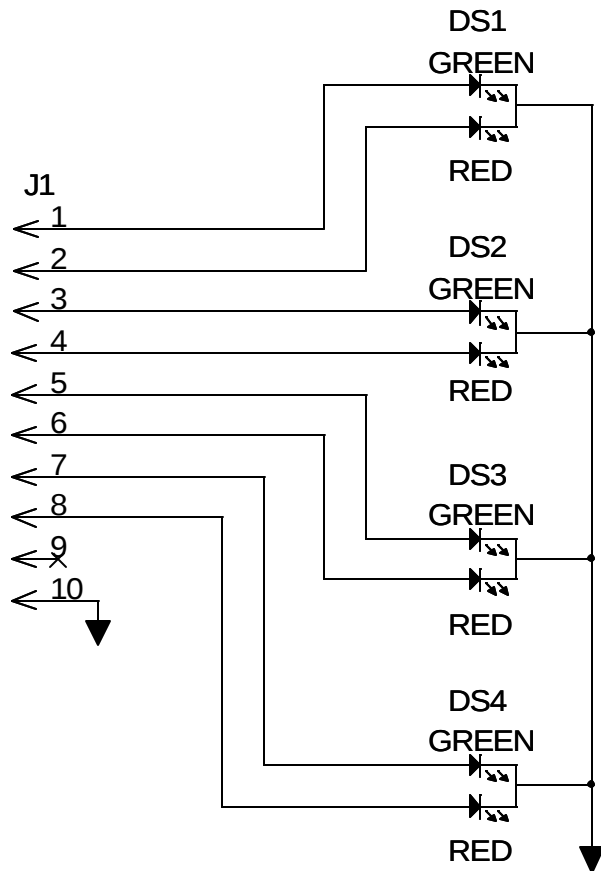
Several voltage regulators are used to power the board. Seven volts is typically applied to board LEDs and to the input of a precision 5.0 volt regulator. The 5.0 volt regulator is used for analog circuits and the microcontroller analog reference voltage. Another two 5 volt regulator circuits are used for most other board circuits.



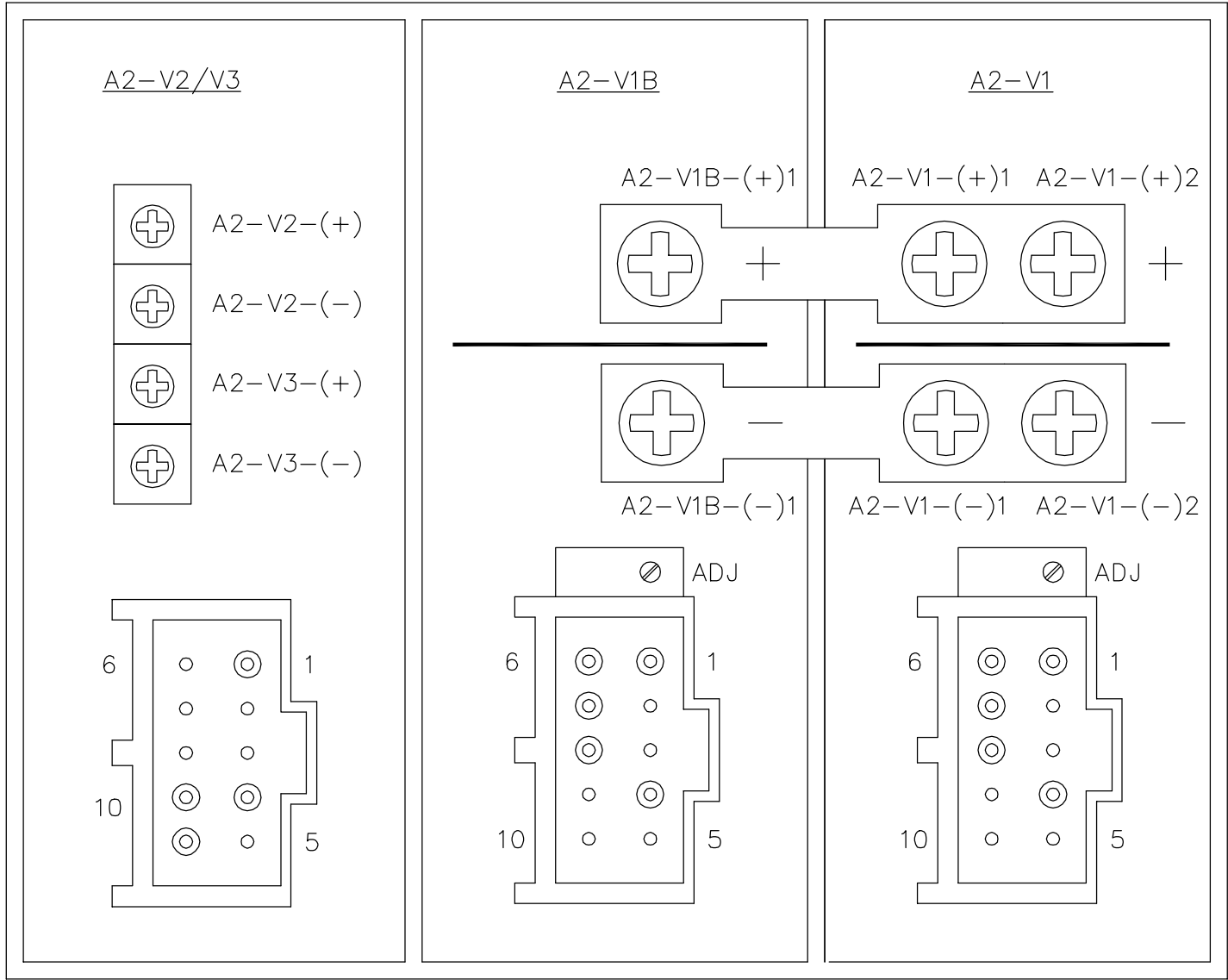
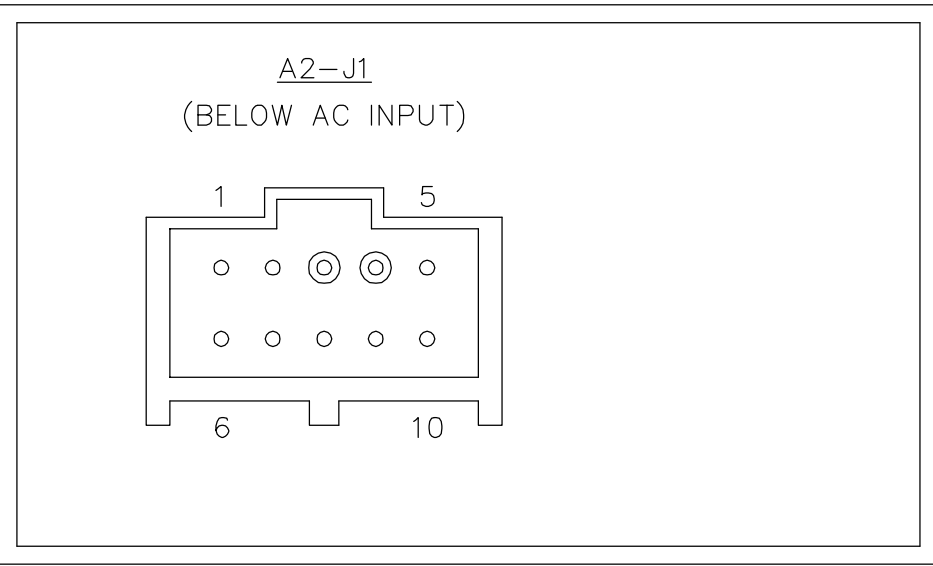
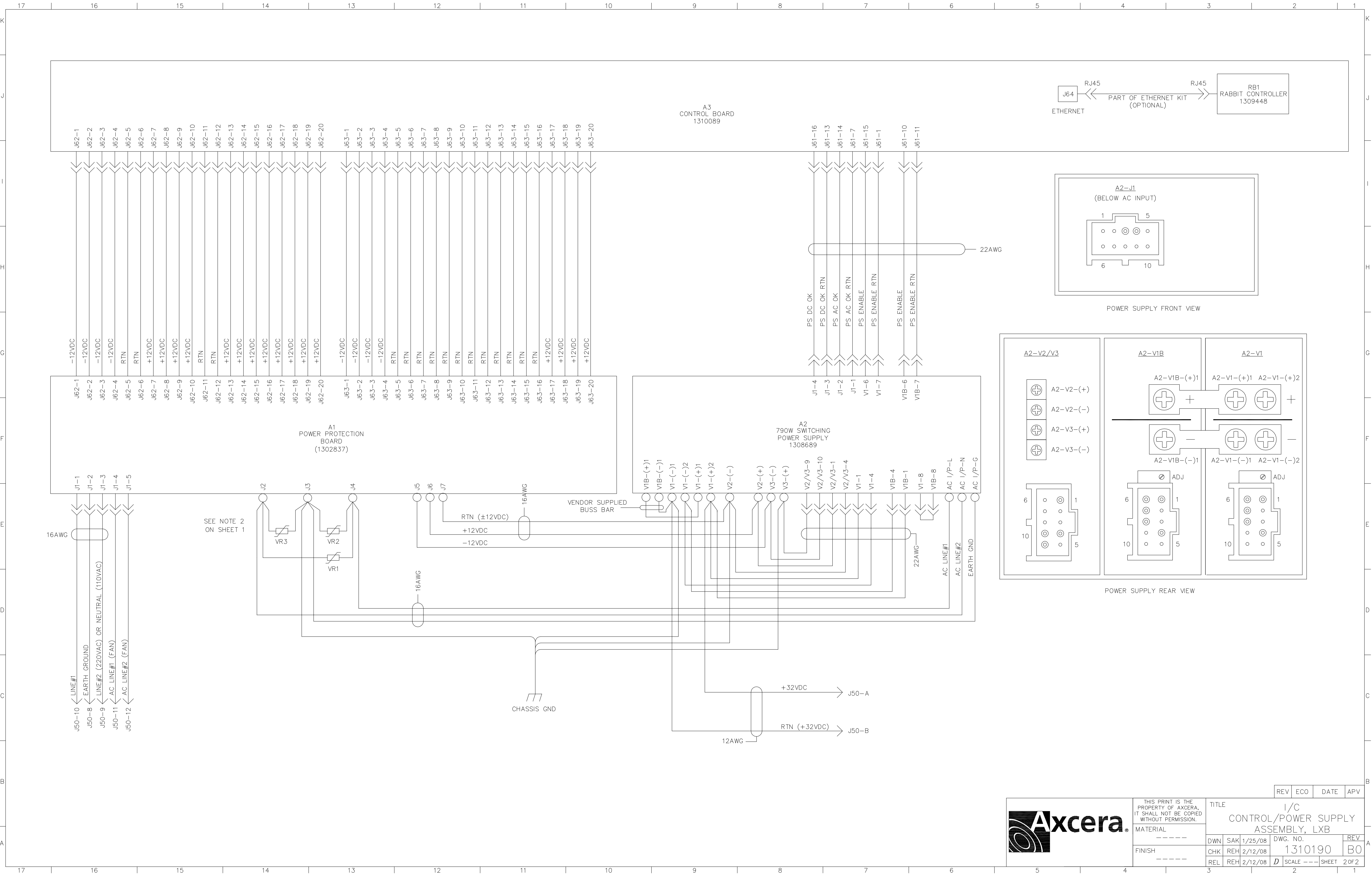
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ECO	MATERIAL				DWN	REH	12/19/07	REV
REV	FINISH				CHK	REH	1/22/08	B0
	-----				REL	REH	1/22/08	D
							SCALE ---	SHEET 5 OF 5

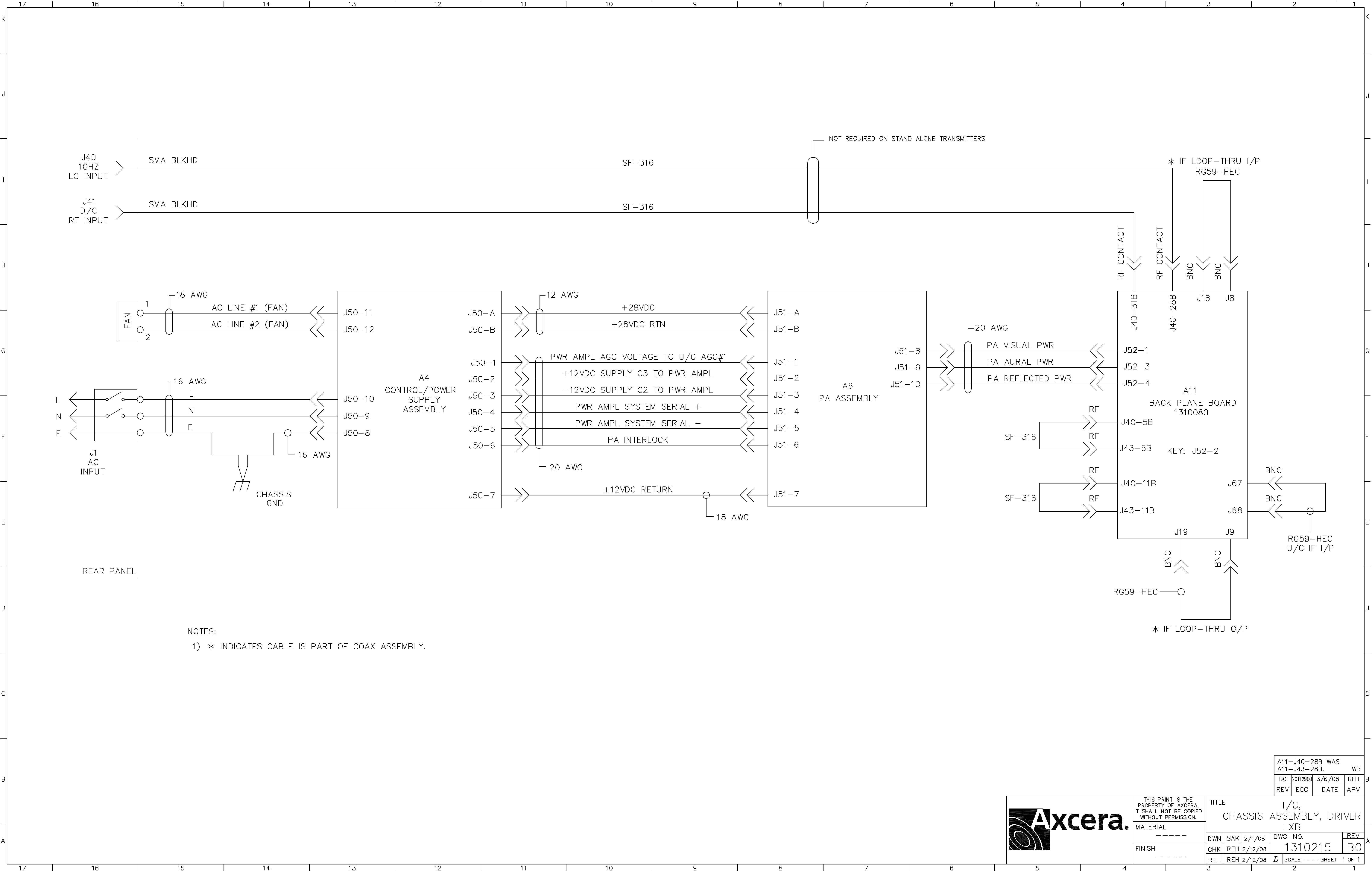


APV	Axcera			REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION			TITLE SCH, LED DISPLAY BD. (ASSY 1310123)			
ECO							
REV	FINISH			DWN	JKF	1/10/08	DWG. NO. 1310124
	-----			CHK	DWB	1/10/08	REV A0
	-----			REL	DWB	1/10/08	A SCALE - - - SHEET 1 OF 1



APV	Axcera			REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION			TITLE SCH, LED DISPLAY BD. (ASSY 1310123)			
ECO							
REV	FINISH			DWN	JKF	1/10/08	DWG. NO. 1310124
	-----			CHK	DWB	1/10/08	REV A0
	-----			REL	DWB	1/10/08	A SCALE - - - SHEET 1 OF 1





A11-J40-28B WAS				WB	
A11-J43-28B.				REH	
BO	20112900	3/6/08	REH		
REV	ECO	DATE	APV		



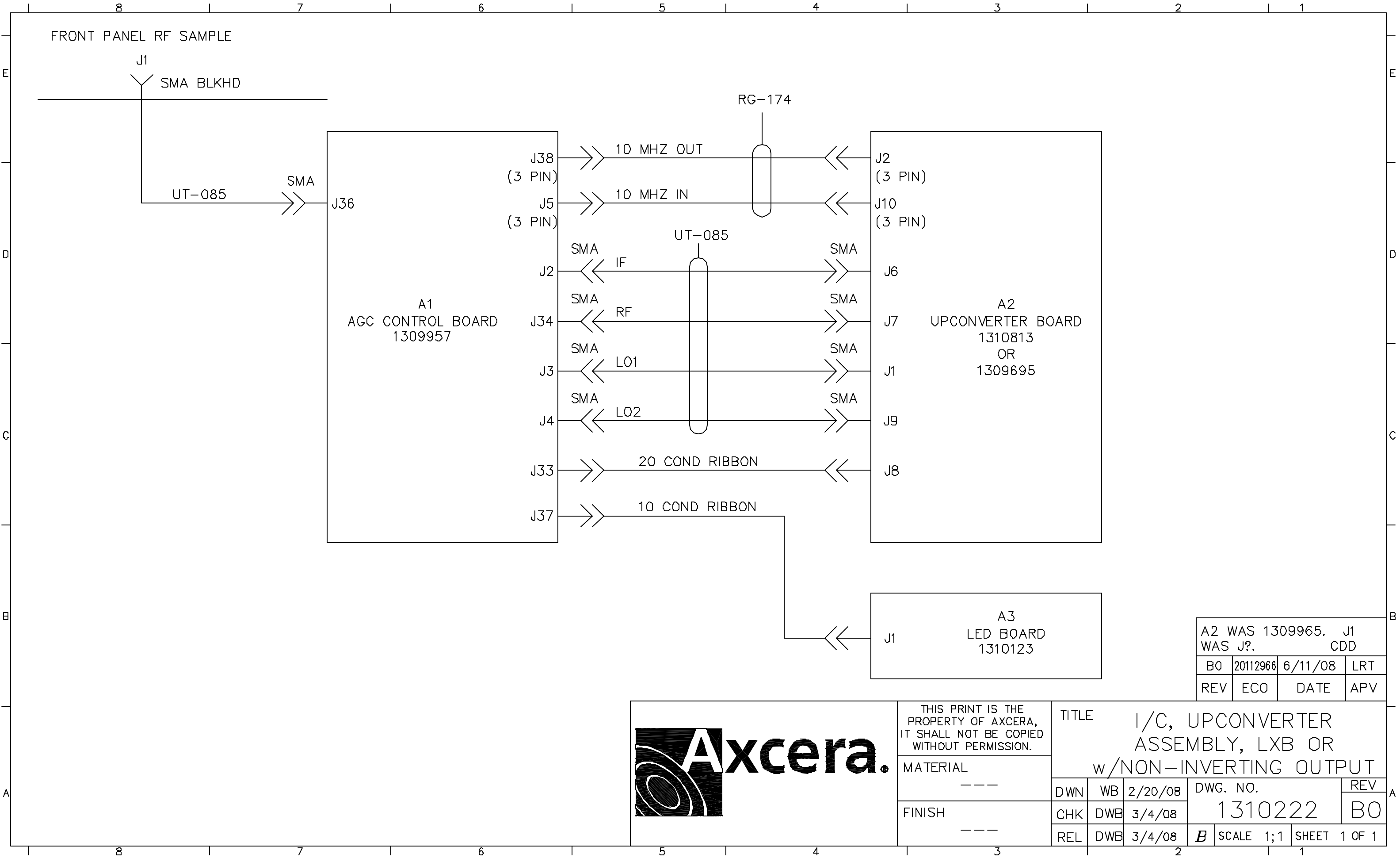
THIS PRINT IS THE
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MATERIAL

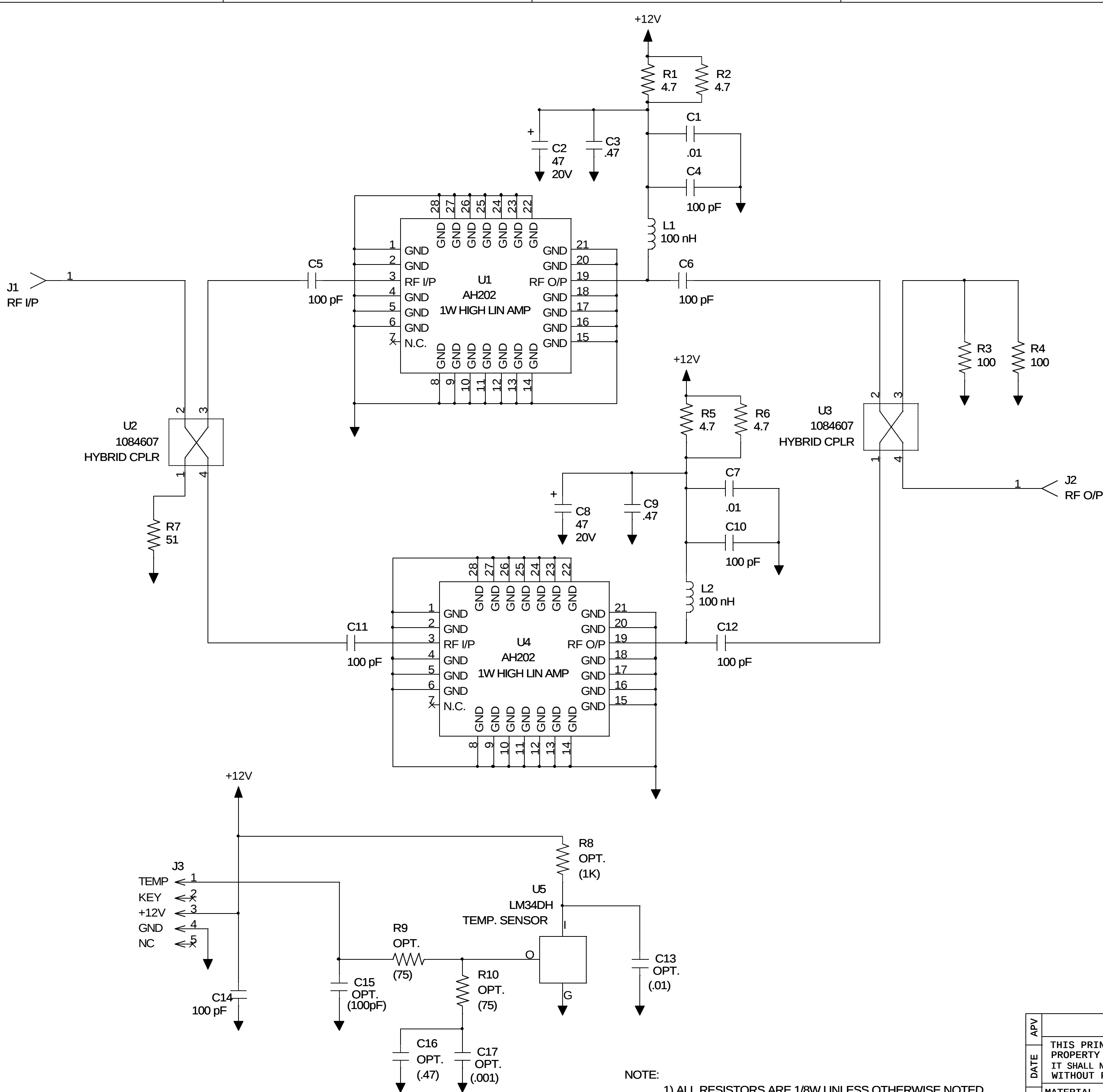
FINISH

TITLE
I/C,
CHASSIS ASSEMBLY, DRIVER
LXB

DWN	SAK	2/1/08	DWG. NO.	REV
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REL	REH	2/12/08	D	SCALE --- SHEET 1 OF 1



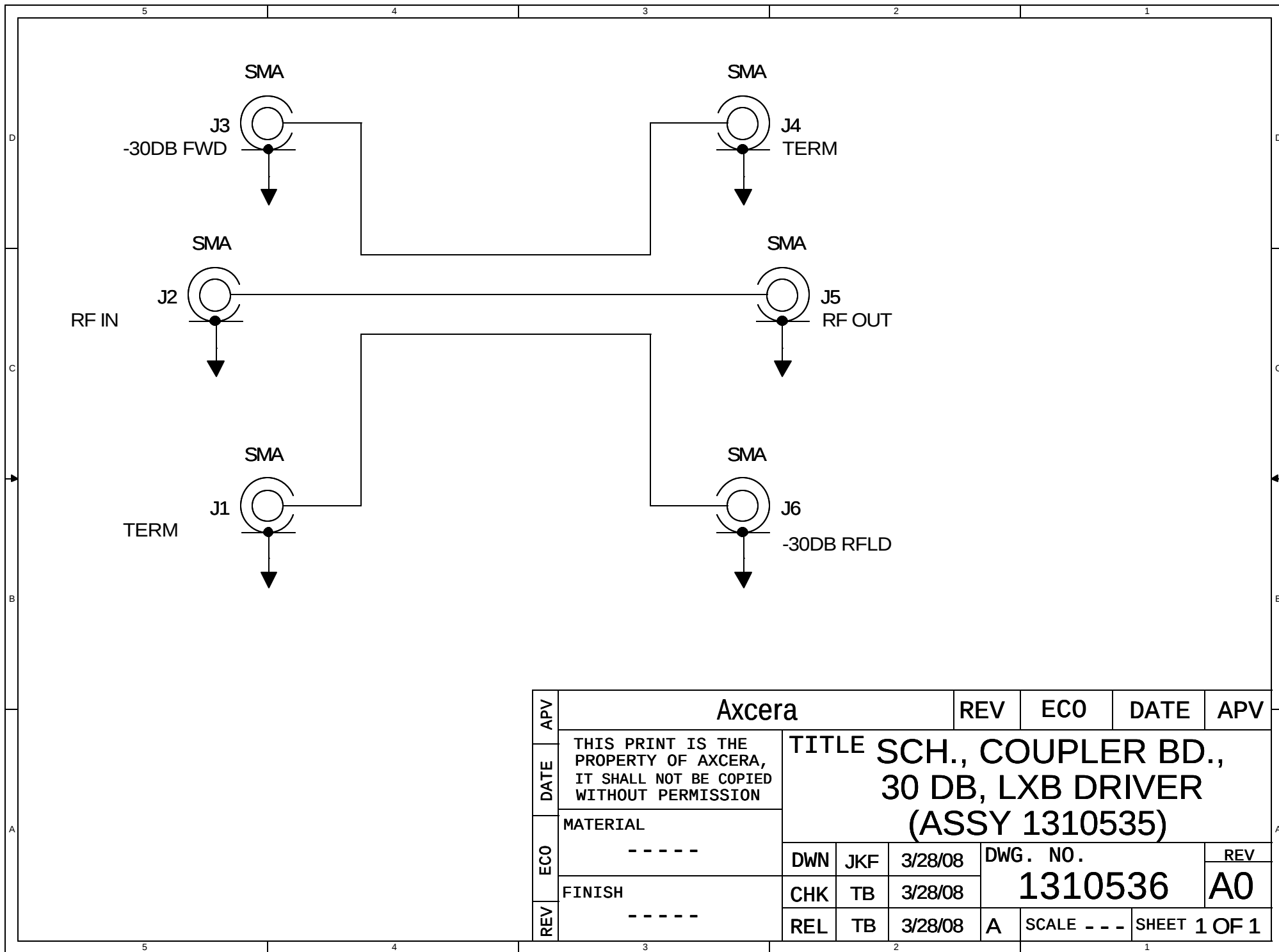
LAST USED REF
R10
C17
U5
L2
J3



NOTE:

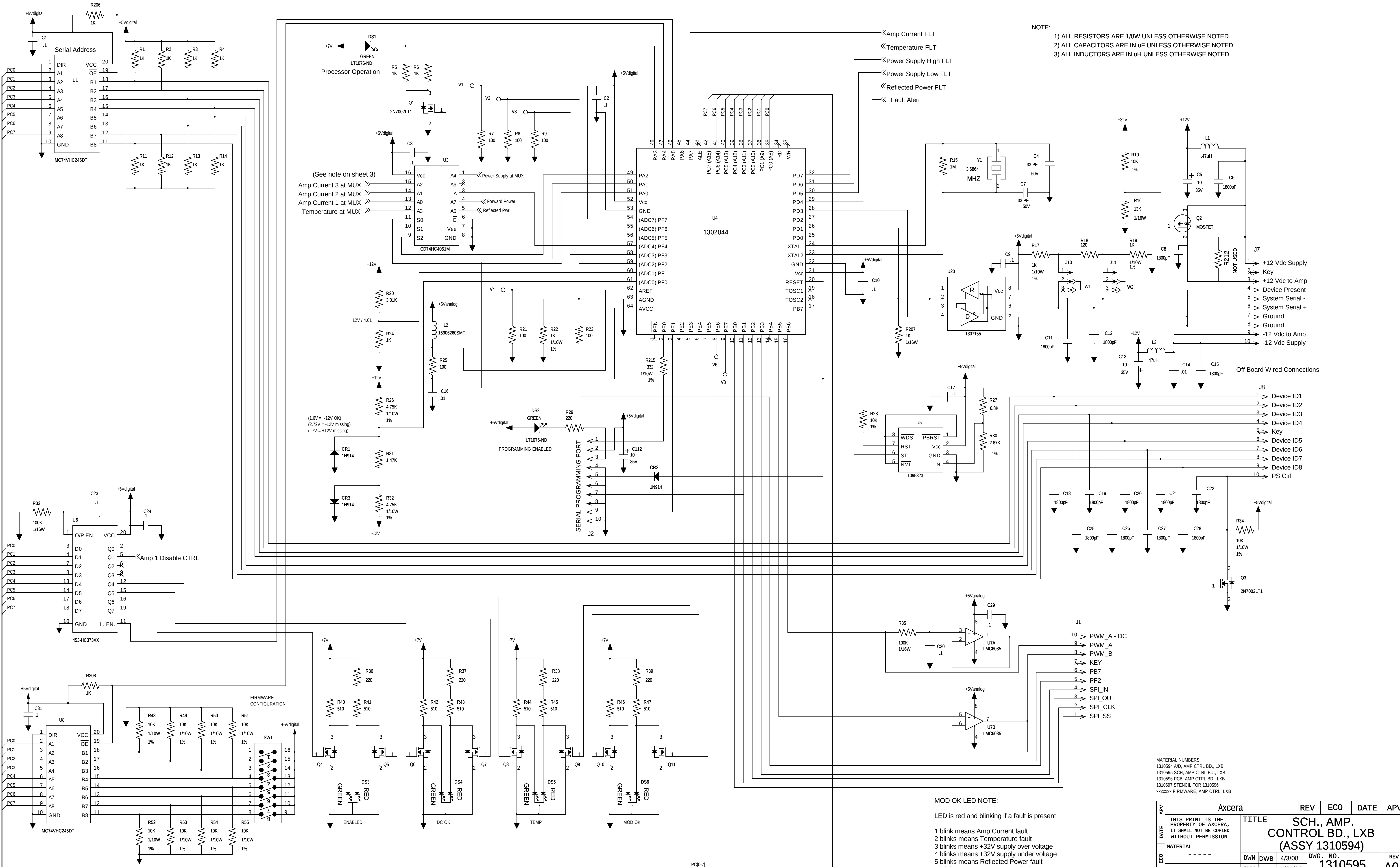
- 1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
- 2) ALL CAPACITORS ARE IN μ F UNLESS OTHERWISE NOTED.
- 3) ALL INDUCTORS ARE IN μ H UNLESS OTHERWISE NOTED.

APV	Axcera				REV	ECO	DATE	APV
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ECO	MATERIAL -----				DWN	JKF	2/21/08	DWG. NO.
REV	FINISH -----				CHK	DWB	2/25/08	1310283
					REL	DWB	2/25/08	C
					SCALE ---		SHEET 1 OF 1	



APV	Axcera			REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION			TITLE SCH., COUPLER BD., 30 DB, LXB DRIVER (ASSY 1310535)			
ECO							
REV	FINISH			DWN	JKF	3/28/08	DWG. NO.
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						SCALE - - -	SHEET 1 OF 1

A0

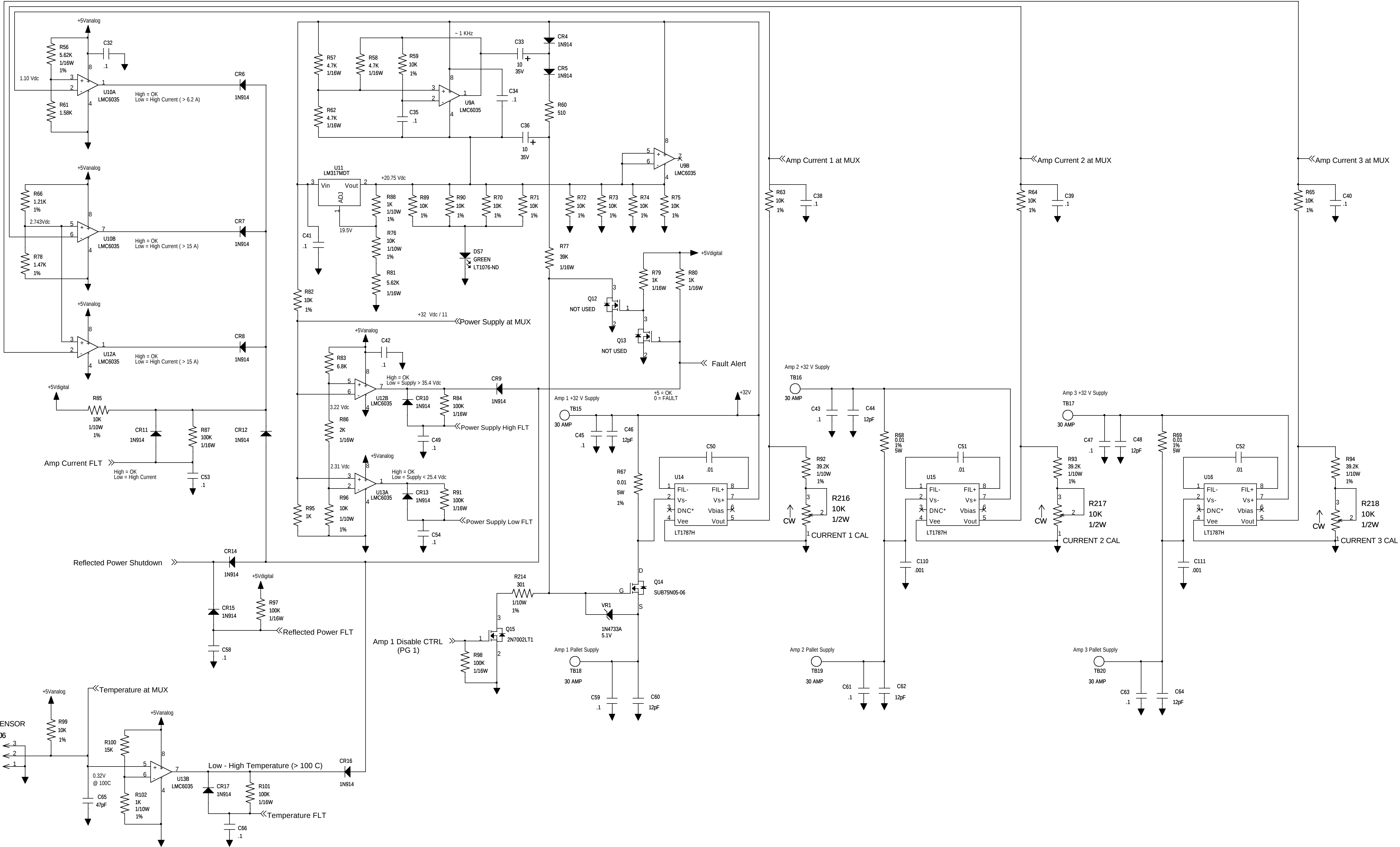


NOTE:
1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.

MOD OK LED NOTE:
LED is red and blinking if a fault is present
1 blink means Amp Current fault
2 blinks means Temperature fault
3 blinks means +32V supply over voltage
4 blinks means +32V supply under voltage
5 blinks means Reflected Power fault
6 blinks means +12V or -12V fault

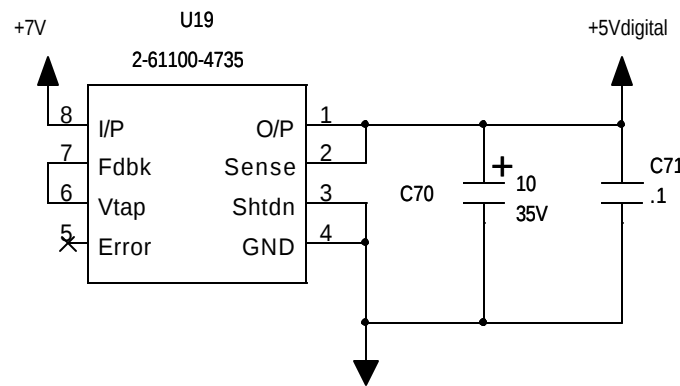
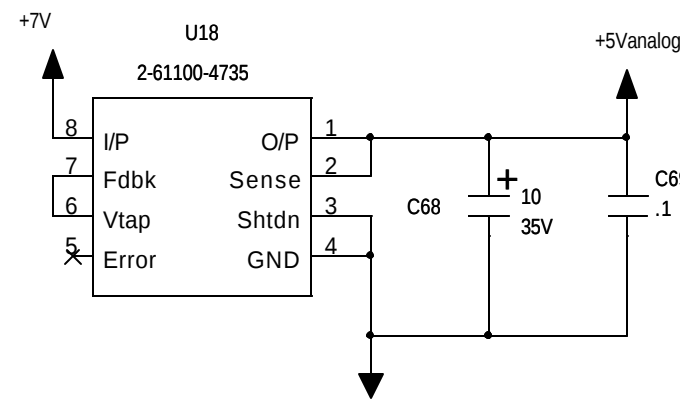
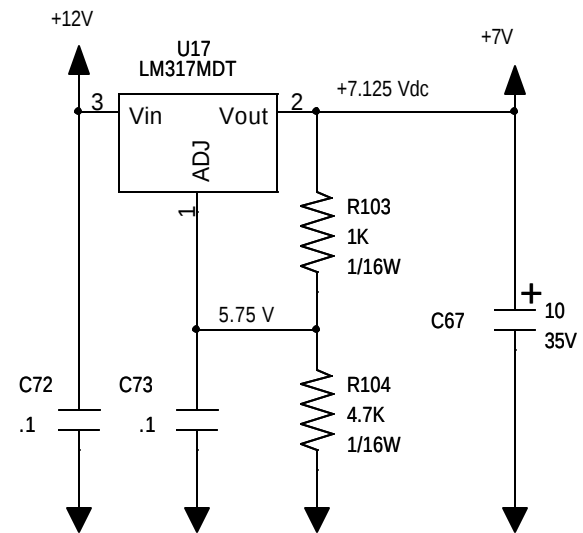
MATERIAL NUMBERS:
1310594 A/D, AMP CTRL BD., LXB
1310595 SCH, AMP CTRL BD., LXB
1310596 PCB, AMP CTRL BD., LXB
1310597 STENCIL FOR 1310596
XXXXXXXX FIRMWARE, AMP CTRL., LXB

APV	Axcera				REV	ECO	DATE	APV	
DATE	THIS PRINT IS THE PROPERTY OF AXCERA. IT SHALL NOT BE COPIED WITHOUT PERMISSION		TITLE SCH., AMP. CONTROL BD., LXB (ASSY 1310594)						
ECO									-----
REV	FINISH		-----		CHK	DWB	4/24/08	1310595	1
					REL	DWB	4/24/08	D	SCALE --- SHEET 1 OF 3



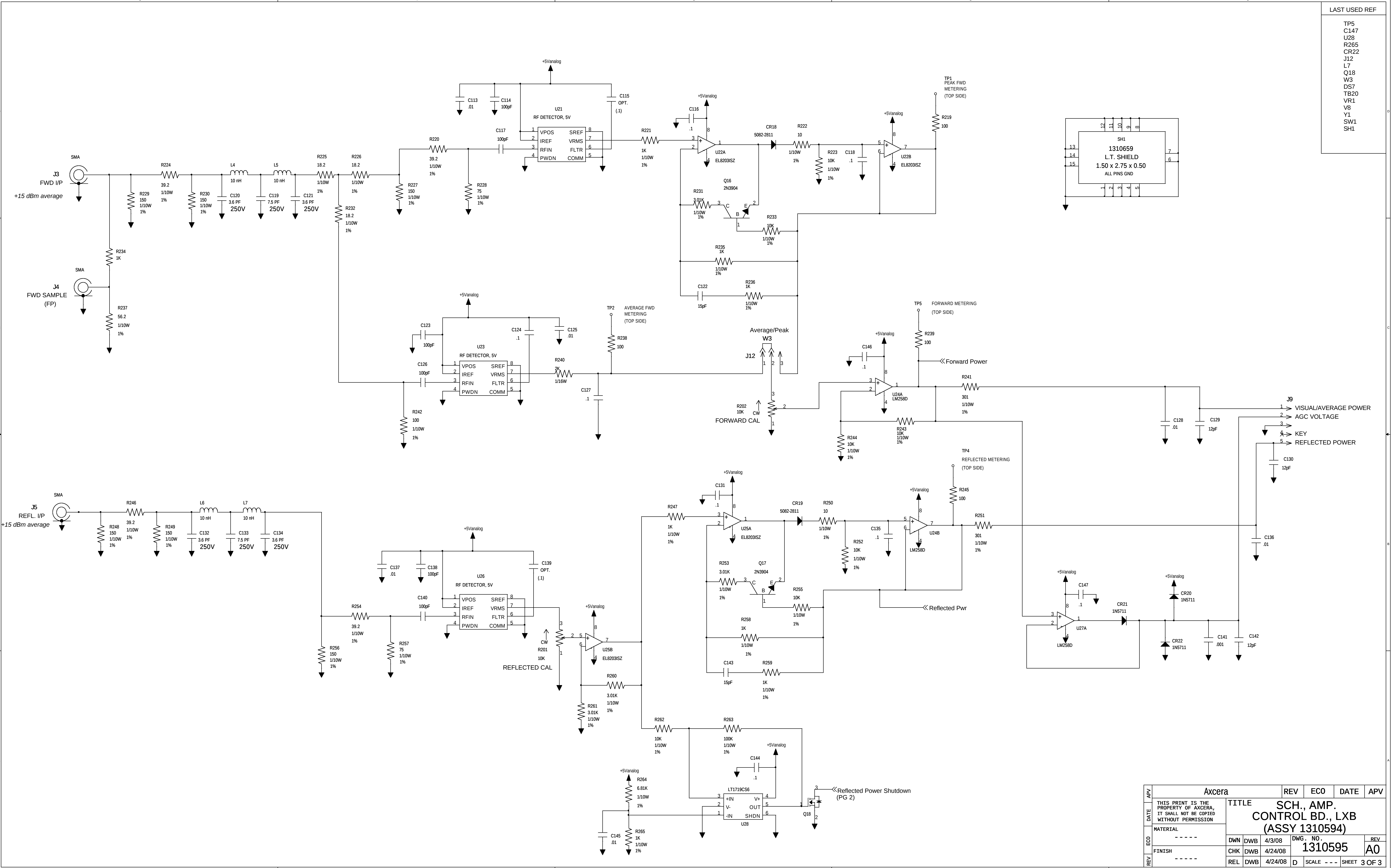
NOTE:

A track width of 0.3 inch is needed between power input vias and sense resistors R55,R56,R57. 0.3 inch track width is also needed between the output of the sense resistors and the output vias that provide power to the amplifier pallets.

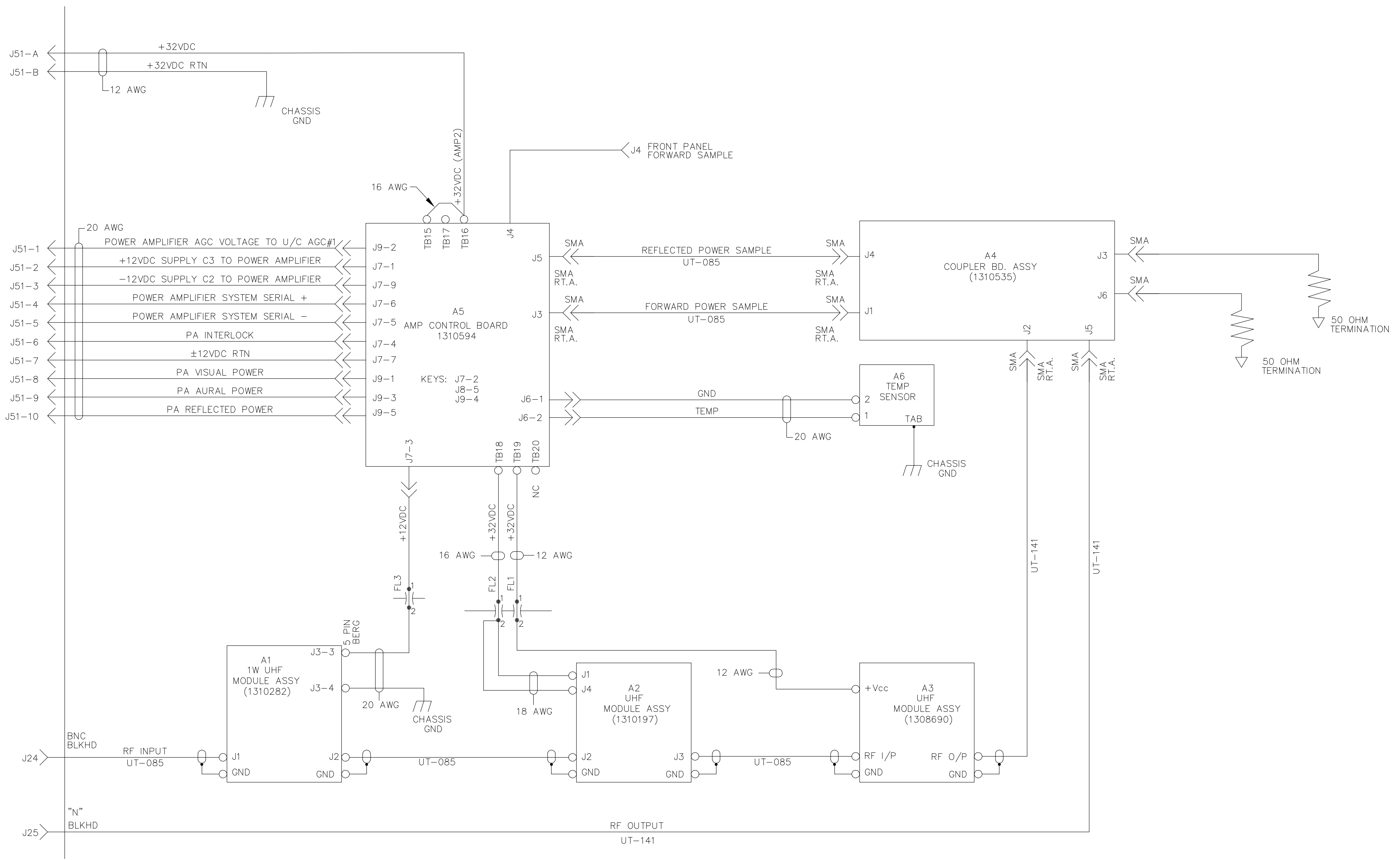


Axcera		REV	ECO	DATE	APV
THIS PRINT IS THE PROPERTY OF AXCERA. IT SHALL NOT BE COPIED WITHOUT PERMISSION		TITLE SCH., AMP. CONTROL BD., LXB (ASSY 1310594)			
DATE	4/3/08	DWN	DWB	DWG. NO. 1310595	REV
ECO	4/24/08	CHK	DWB	A0	
REV	4/24/08	REL	DWB	SCALE - - -	SHEET 2 OF 3

LAST USED REF	
TP5	
C147	
U28	
R265	
CR22	
J12	
L7	
Q18	
W3	
DS7	
TB20	
VR1	
V8	
Y1	
SW1	
SH1	



APV		REV		ECO		DATE		APV	
THIS PRINT IS THE PROPERTY OF AXCERA. IT SHALL NOT BE COPIED WITHOUT PERMISSION		TITLE		SCH., AMP. CONTROL BD., LXB (ASSY 1310594)		DWG. NO.		REV	
MATERIAL		DWN		4/3/08		1310595		A0	
FINISH		CHK		4/24/08		REL		D	
REL		DWB		4/24/08		SCALE		3 OF 3	



NOTE:
1. ALL WIRE IS 18AWG UNLESS OTHERWISE NOTED.



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MATERIAL -----				DWN	SAK	5/7/08	DWG. NO. 1310752
FINISH -----				CHK	TB	5/12/08	REV A0
REL				TB	5/12/08	D	SCALE --- SHEET 1 OF 1