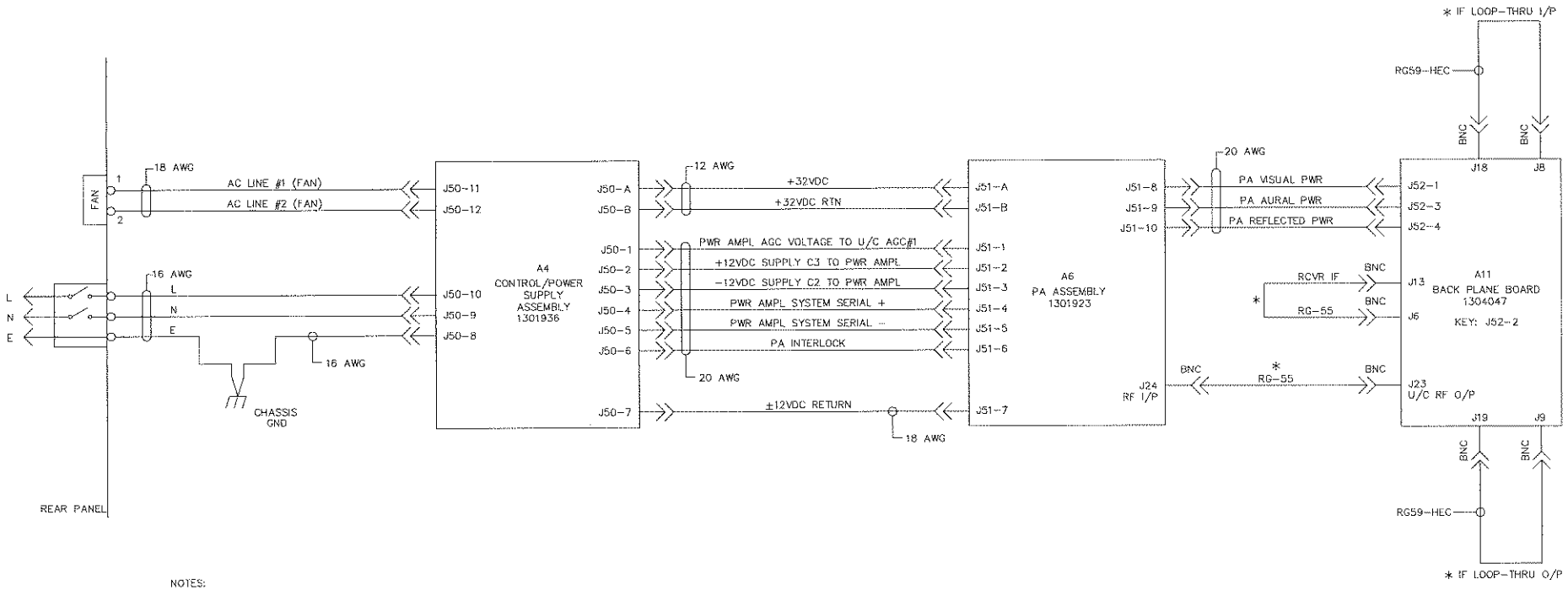


NOTES:

* INDICATES CABLE IS PART OF COAX ASSEMBLY.

REV	ECO	DATE	APV

Axcera

MATERIAL

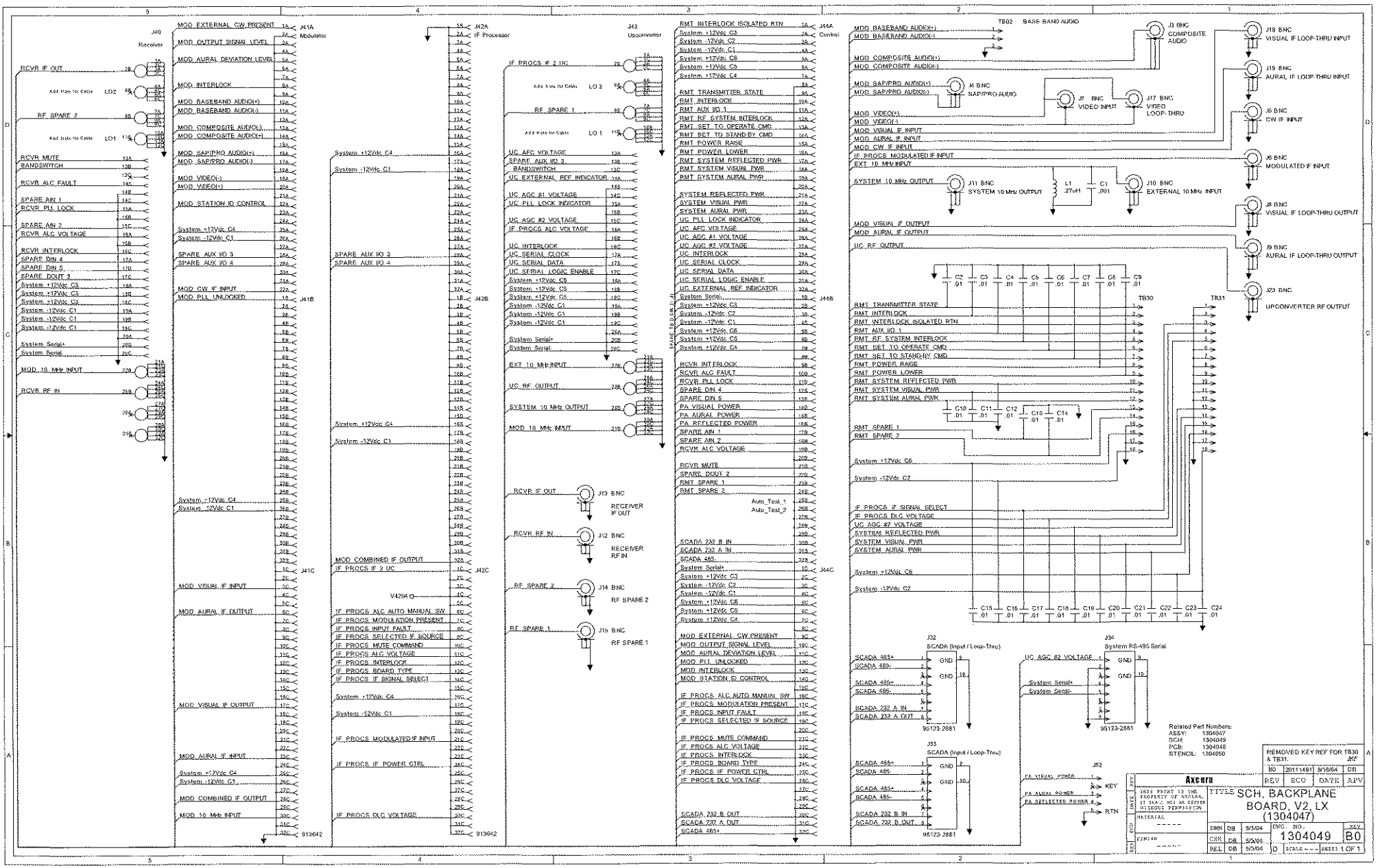
FINISH

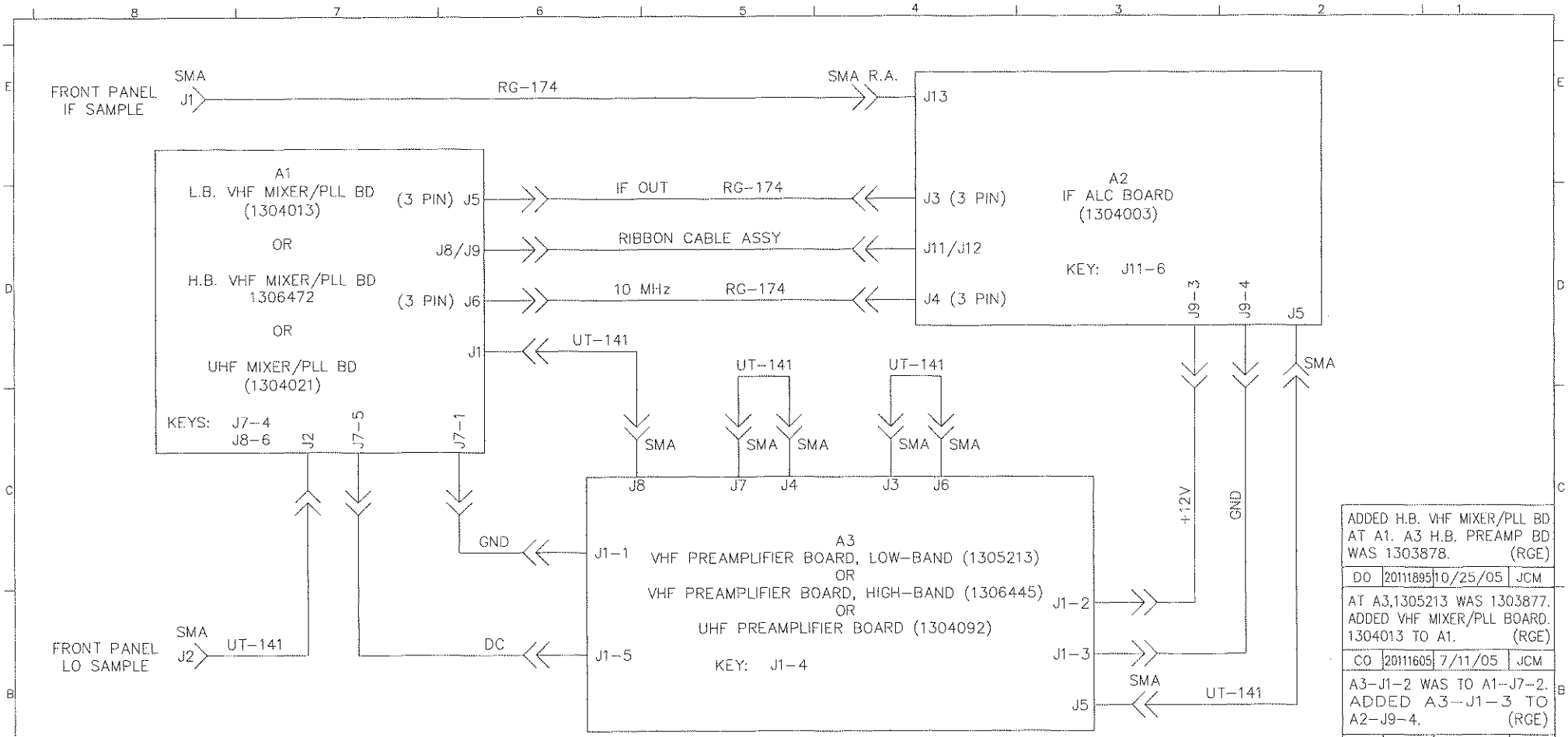
TITLE: I/C, CHASSIS ASSEMBLY INNOVATOR LX, V2

DWN	ROS	8/7/04	
CHK	JCM	8/18/04	
REL	JCM	8/18/04	

DWG. NO. 1304064 REV A0

D SCALE --- SHEET 1 OF 1


J40 Receiver
J41A Modulator
J42A IF Processor
J43 Upconverter
J44A Control
J41B
J42B
J44B
J41C
J42C
J44C
RCVR IF OUT
RF SPARE 2
RCVR MUTE
BANDSWITCH
RCVR ALC FAULT
SPARE AIN 1
RCVR PLL LOCK
SPARE AIN 2
RCVR ALC VOLTAGE
RCVR INTERLOCK
SPARE DIN 4
SPARE DIN 5
SPARE DOUT 2
System +12Vdc C3
System -12Vdc C3
System -12Vdc C1
System -12Vdc C1
System Serial+
System Serial-
MOD 10 MHz INPUT
RCVR RF IN
MOD EXTERNAL CW PRESENT
MOD OUTPUT SIGNAL LEVEL
MOD AURAL DEVIATION LEVEL
MOD INTERLOCK
MOD BASEBAND AUDIO(+)
MOD BASEBAND AUDIO(-)
MOD COMPOSITE AUDIO(+)
MOD COMPOSITE AUDIO(-)
MOD SAP/PRO AUDIO(+)
MOD SAP/PRO AUDIO(-)
MOD VIDEO(-)
MOD VIDEO(+)
MOD STATION ID CONTROL
System +12Vdc C4
System -12Vdc C1
SPARE AUX I/O 3
SPARE AUX I/O 4
MOD CW IF INPUT
MOD PLL UNLOCKED
MOD VISUAL IF INPUT
MOD AURAL IF INPUT
MOD COMBINED IF OUTPUT
MOD 10 MHz INPUT
013642
IF PROCS IF 2 I/C
LO 2
RF SPARE 1
LO 1
UC AFC VOLTAGE
SPARE AUX I/O 5
UC AGC #1 VOLTAGE
UC PLL LOCK INDICATOR
UC AGC #2 VOLTAGE
IF PROCS ALC VOLTAGE
UC INTERLOCK
UC SERIAL CLOCK
UC SERIAL DATA
UC SERIAL LOGIC ENABLE
EXT 10 MHz INPUT
UC RF OUTPUT
SYSTEM 10 MHz OUTPUT
MOD 10 MHz INPUT
RCVR IF OUT
RCVR RF IN
RF SPARE 2
RF SPARE 1
J13 BNC RECEIVER IF OUT
J12 BNC RECEIVER RF IN
J14 BNC RF SPARE 2
J15 BNC RF SPARE 1
V4204
IF PROCS ALC AUTO MANUAL SW
IF PROCS MODULATION PRESENT
IF PROCS INPUT FAULT
IF PROCS SELECTED IF SOURCE
IF PROCS MUTE COMMAND
IF PROCS ALC VOLTAGE
IF PROCS INTERLOCK
IF PROCS BOARD TYPE
IF PROCS IF SIGNAL SELECT
IF PROCS MODULATED IF INPUT
IF PROCS IF POWER CTRL
IF PROCS DLC VOLTAGE
RMT INTERLOCK ISOLATED RTN
RMT TRANSMITTER STATE
RMT INTERLOCK
RMT AUX I/O 1
RMT RF SYSTEM INTERLOCK
RMT SET TO OPERATE CMD
RMT SET TO STAND-BY CMD
RMT POWER RAISE
RMT POWER LOWER
RMT SYSTEM REFLECTED PWR
RMT SYSTEM VISUAL PWR
RMT SYSTEM AURAL PWR
SYSTEM REFLECTED PWR
SYSTEM VISUAL PWR
SYSTEM AURAL PWR
UC PLL LOCK INDICATOR
UC AFC VOLTAGE
UC AGC #1 VOLTAGE
UC AGC #2 VOLTAGE
UC INTERLOCK
UC SERIAL CLOCK
UC SERIAL DATA
UC SERIAL LOGIC ENABLE
UC EXTERNAL REF INDICATOR
System Serial-
RCVR INTERLOCK
RCVR ALC FAULT
RCVR PLL LOCK
SPARE DIN 4
SPARE DIN 5
PA VISUAL POWER
PA AURAL POWER
PA REFLECTED POWER
SPARE AIN 1
SPARE AIN 2
RCVR ALC VOLTAGE
RCVR MUTE
SPARE DOUT 2
RMT SPARE 1
RMT SPARE 2
Auto_Test_1
Auto_Test_2
SCADA 232 B IN
SCADA 232 A IN
SCADA 485-
SPARE DIN 5
MOD EXTERNAL CW PRESENT
MOD OUTPUT SIGNAL LEVEL
MOD AURAL DEVIATION LEVEL
MOD PLL UNLOCKED
MOD INTERLOCK
MOD STATION ID CONTROL
IF PROCS ALC AUTO MANUAL SW
IF PROCS MODULATION PRESENT
IF PROCS INPUT FAULT
IF PROCS SELECTED IF SOURCE
IF PROCS MUTE COMMAND
IF PROCS ALC VOLTAGE
IF PROCS INTERLOCK
IF PROCS BOARD TYPE
IF PROCS IF POWER CTRL
IF PROCS DLC VOLTAGE
SCADA 232 B OUT
SCADA 232 A OUT
SCADA 485+
SPARE DIN 1 - SPARE DIN 4
TB02 BASE BAND AUDIO
MOD BASEBAND AUDIO(+)
MOD BASEBAND AUDIO(-)
MOD COMPOSITE AUDIO(+)
MOD COMPOSITE AUDIO(-)
MOD SAP/PRO AUDIO(+)
MOD SAP/PRO AUDIO(-)
MOD VIDEO(+)
MOD VIDEO(-)
MOD VISUAL IF INPUT
MOD AURAL IF INPUT
MOD CW IF INPUT
IF PROCS MODULATED IF INPUT
EXT 10 MHz INPUT
SYSTEM 10 MHz OUTPUT
MOD VISUAL IF OUTPUT
MOD AURAL IF OUTPUT
UC RF OUTPUT
J3 BNC COMPOSITE AUDIO
J4 BNC SAP/PRO AUDIO
J7 BNC VIDEO INPUT
J17 BNC VIDEO LOOP-THRU
J11 BNC SYSTEM 10 MHz OUTPUT
L1 .27uH
C1 .001
J10 BNC EXTERNAL 10 MHz INPUT
J18 BNC VISUAL IF LOOP-THRU INPUT
J19 BNC AURAL IF LOOP-THRU INPUT
J6 BNC CW IF INPUT
J5 BNC MODULATED IF INPUT
J8 BNC VISUAL IF LOOP-THRU OUTPUT
J9 BNC AURAL IF LOOP-THRU OUTPUT
J23 BNC UPCONVERTER RF OUTPUT
C2 C3 C4 C5 C6 C7 C8 C9 .01
C10 C11 C12 C13 C14 .01
C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 .01
TB30
TB31
RMT TRANSMITTER STATE
RMT INTERLOCK
RMT INTERLOCK ISOLATED RTN
RMT AUX I/O 1
RMT RF SYSTEM INTERLOCK
RMT SET TO OPERATE CMD
RMT SET TO STAND-BY CMD
RMT POWER RAISE
RMT POWER LOWER
RMT SYSTEM REFLECTED PWR
RMT SYSTEM VISUAL PWR
RMT SYSTEM AURAL PWR
RMT SPARE 1
RMT SPARE 2
System +12Vdc C6
System -12Vdc C2
IF PROCS IF SIGNAL SELECT
IF PROCS DLC VOLTAGE
UC AGC #2 VOLTAGE
SYSTEM REFLECTED PWR
SYSTEM VISUAL PWR
SYSTEM AURAL PWR
J32 SCADA (Input / Loop-Thru)
J33 SCADA (Input / Loop-Thru)
J34 System RS-485 Serial
J52
KEY
RTN
96123-2861
Related Part Numbers:
ASSY: 1304047
SCH: 1304049
PCB: 1304048
STENCIL: 1304050
REMOVED KEY REF FOR TB30 & TB31. JKF
B0 20111491 9/15/04 DB
Axcera
REV ECO DATE APV
THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION
TITLE: SCH, BACKPLANE BOARD, V2, LX (1304047)
DWN DB 5/3/04
CHK DB 5/3/06
APV
DWG. NO. 1304049
REV B0
SCALE - - - SHEET 1 OF 1



ADDED H.B. VHF MIXER/PLL BD AT A1. A3 H.B. PREAMP BD WAS 1303878. (RGE)			
DO	20111895	10/25/05	JCM
AT A3,1305213 WAS 1303877. ADDED VHF MIXER/PLL BOARD. 1304013 TO A1. (RGE)			
CO	20111605	7/11/05	JCM
A3-J1-2 WAS TO A1-J7-2. ADDED A3-J1-3 TO A2-J9-4. (RGE)			
BO	20111504	10/13/04	DWB
REV	ECO	DATE	APV

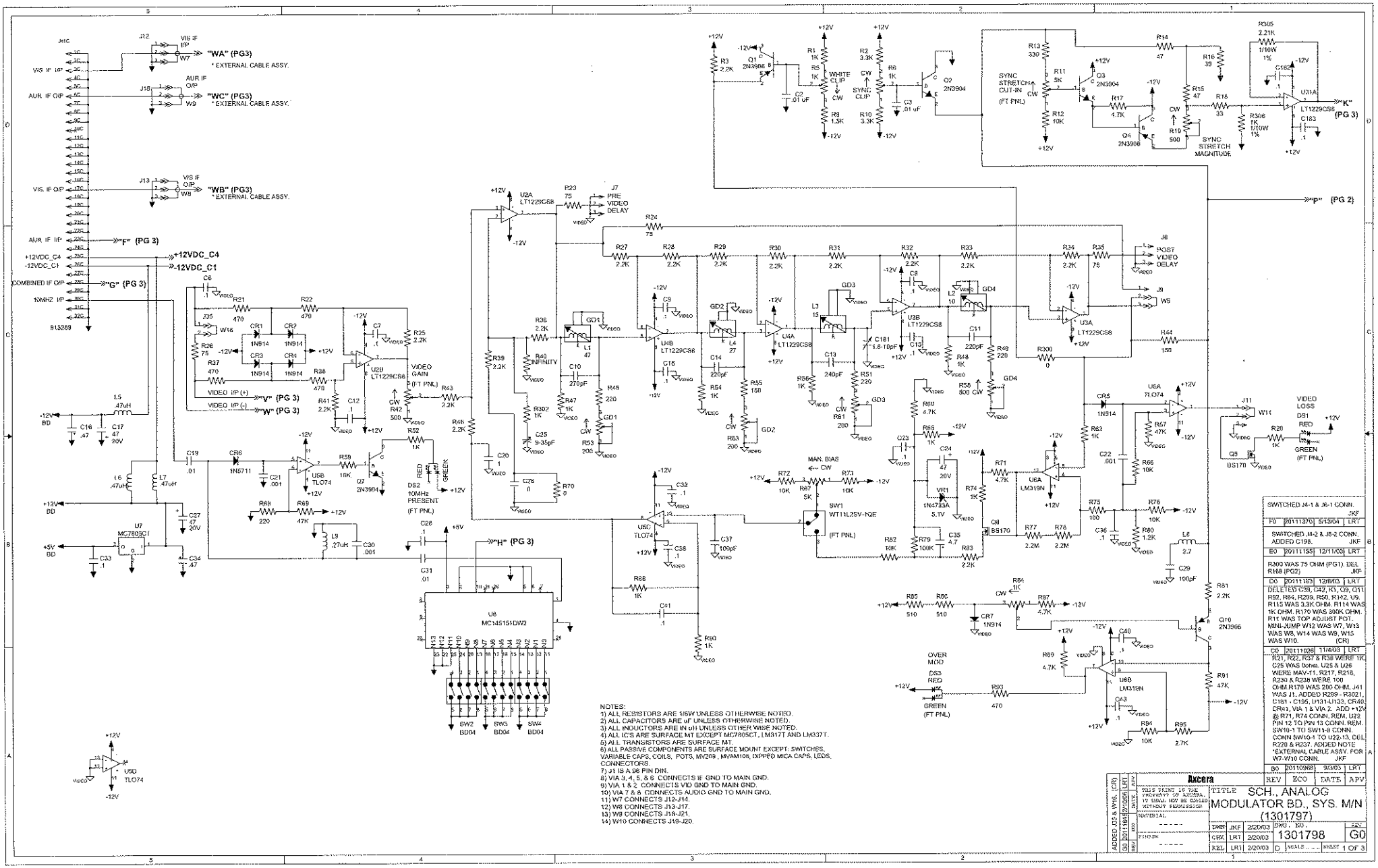
Axcera

MATERIAL ---

FINISH ---

TITLE: I/C, RECEIVER ASSY, VHF/UHF, LX

DWN	RGE	4/6/04	DWG. NO. 1304005	REV D0
CHK	JCM	8/4/04		
REL	JCM	8/4/04	B SCALE ---	SHEET 1 OF 1



NOTES:
1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHER WISE NOTED.
4) ALL IC'S ARE SURFACE MT EXCEPT MC7805CT, LM317T AND LM337T.
5) ALL TRANSISTORS ARE SURFACE MT.
6) ALL PASSIVE COMPONENTS ARE SURFACE MOUNT EXCEPT: SWITCHES, VARIABLE CAPS, COILS, POTS, MV209 , MVAM108, DIPPED MICA CAPS, LEDS, CONNECTORS.
7) J1 IS A 96 PIN DIN.
8) VIA 3, 4, 5, & 6 CONNECTS IF GND TO MAIN GND.
9) VIA 1 & 2 CONNECTS VID GND TO MAIN GND.
10) VIA 7 & 8 CONNECTS AUDIO GND TO MAIN GND.
11) W7 CONNECTS J12-J14.
12) W8 CONNECTS J13-J17.
13) W9 CONNECTS J18-J21.
14) W10 CONNECTS J18-J20.

	SWITCHED J4-1 & J6-1 CONN.	JKF	
F0	20111370	5/13/04	LRT
	SWITCHED J4-2 & J6-2 CONN. ADDED C198.	JKF	
E0	20111155	12/11/03	LRT
	R300 WAS 75 OHM (PG1). DEL R168 (PG2)	JKF	
D0	20111163	12/8/03	LRT
	DELETED C59, C42, R1, C9, C11, R97, R64, R295, R56, R42, U9, R115 WAS 3.3K OHM. R114 WAS 1K OHM. R170 WAS 300K OHM. R11 WAS TOP ADJUST POT. MINI-JUMP W12 WAS W7, W13 WAS W8, W14 WAS W9, W15 WAS W10. (CR)		
C0	20111026	11/4/03	LRT
	R21, R22, R37 & R38 WERE 1K. C25 WAS 0ohm. U25 & U26 WERE MAY-11. R217, R218, R230 & R236 WERE 100 OHM R170 WAS 200 OHM. J41 WAS J1. ADDED R299 - R3021, C181 - C195, U31-U133, CR40, CR43, VIA 1 & VIA 2. ADD +12V @ R71, R74 CONN, REM, U22 PIN 12 TO PIN 13 CONN. REM. SW10-1 TO SW11-8 CONN. CONN SW10-1 TO U22-13. DEL R220 & R237. ADDED NOTE *EXTERNAL CABLE ASSY. FOR W7-W10 CONN.	JKF	
B0	20110968	9/3/03	LRT

ADDED J25 & W16 (CR) G0 20111094 12/10/03 LRT

Axcera

REV | ECO | DATE | APV

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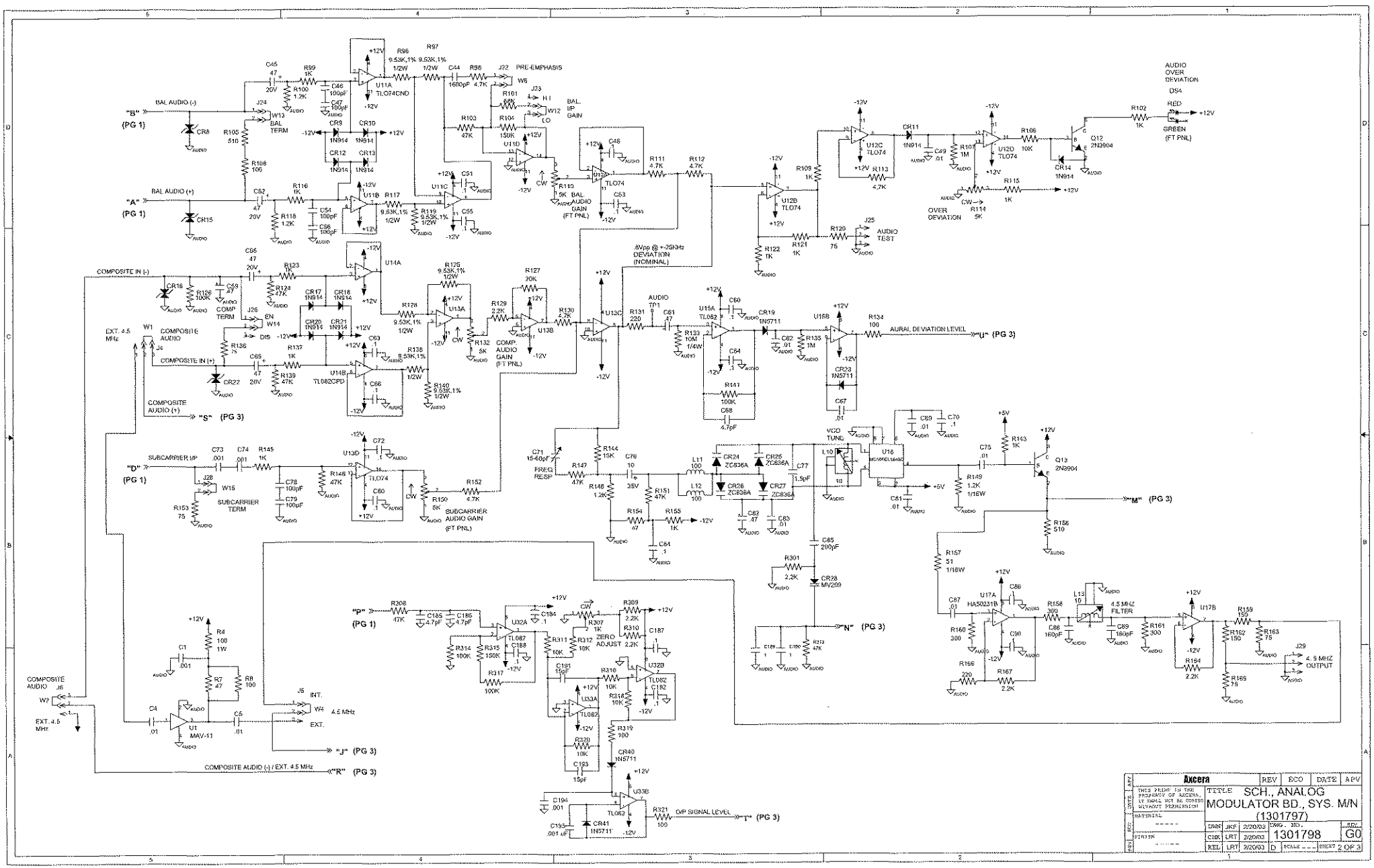
TITLE: SCH., ANALOG MODULATOR BD., SYS. M/N (1301797)

DWN	JKF	2/20/03	DWG. NO. 1301798 REV G0
CHK	LRT	2/20/03	
REL	LRT	2/20/03	D SCALE - - - SHEET 1 OF 3


"B" (PG 1)
BAL AUDIO (-)
"A" (PG 1)
BAL AUDIO (+)
BAL TERM
PRE-EMPHASIS
BAL. UP GAIN
BAL AUDIO GAIN (FT PNL)
AUDIO OVER DEVIATION
OVER DEVIATION
AUDIO TEST
8Vpp @ +-25KHz DEVIATION (NOMINAL)
COMPOSITE IN (-)
COMPOSITE IN (+)
COMP TERM
COMPOSITE AUDIO
COMPOSITE AUDIO (+)
EXT. 4.5 MHz
"S" (PG 3)
COMP. AUDIO GAIN (FT PNL)
AURAL DEVIATION LEVEL
"U" (PG 3)
"D" (PG 1)
SUBCARRIER I/P
SUBCARRIER TERM
SUBCARRIER AUDIO GAIN (FT PNL)
VCO TUNE
FREQ RESP
"M" (PG 3)
"P" (PG 1)
"N" (PG 3)
4.5 MHZ FILTER
4.5 MHZ OUTPUT
COMPOSITE AUDIO J6
INT.
EXT.
4.5 MHz
"J" (PG 3)
COMPOSITE AUDIO (-) / EXT. 4.5 MHz
"R" (PG 3)
O/P SIGNAL LEVEL
"T" (PG 3)
Axcera
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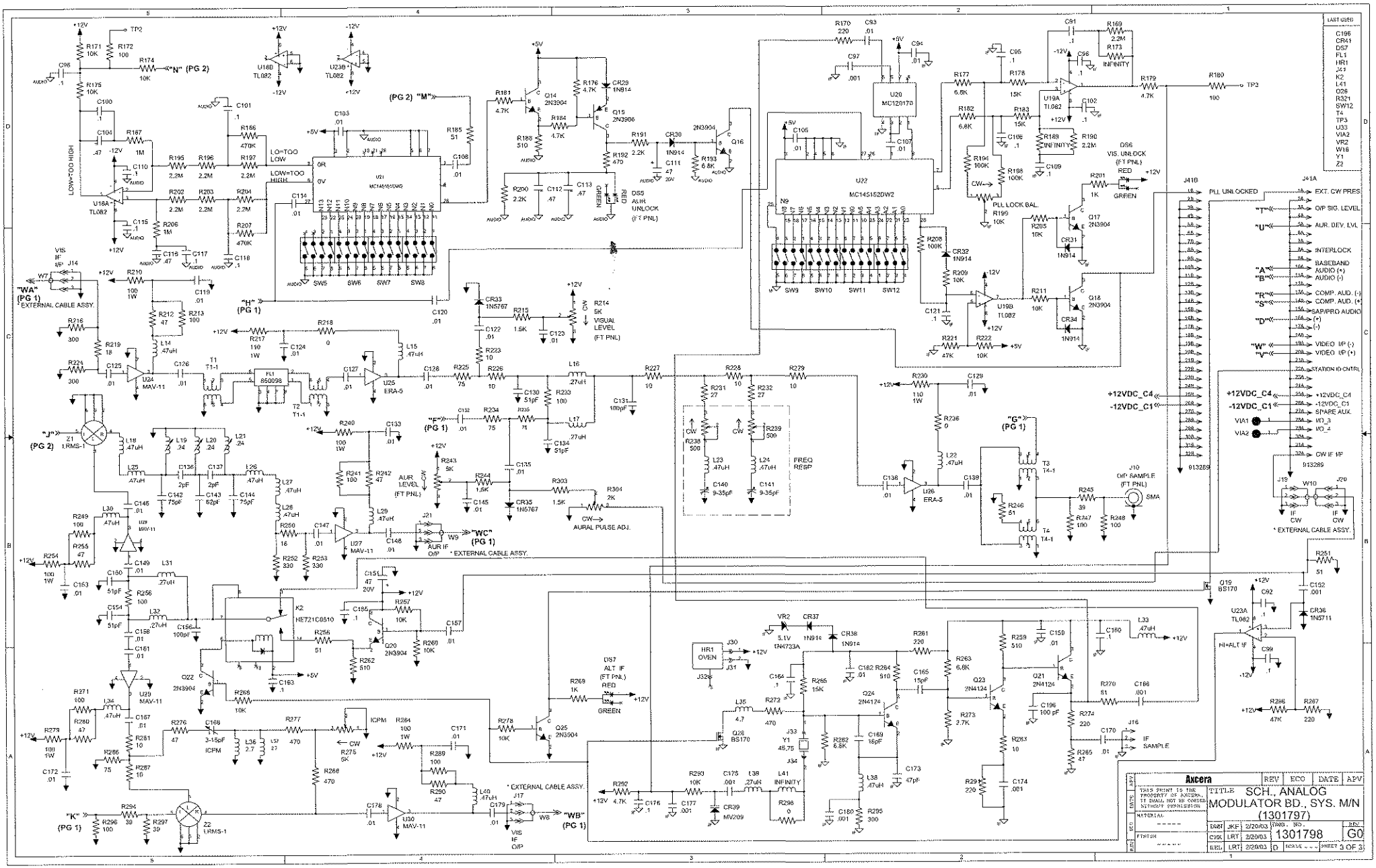
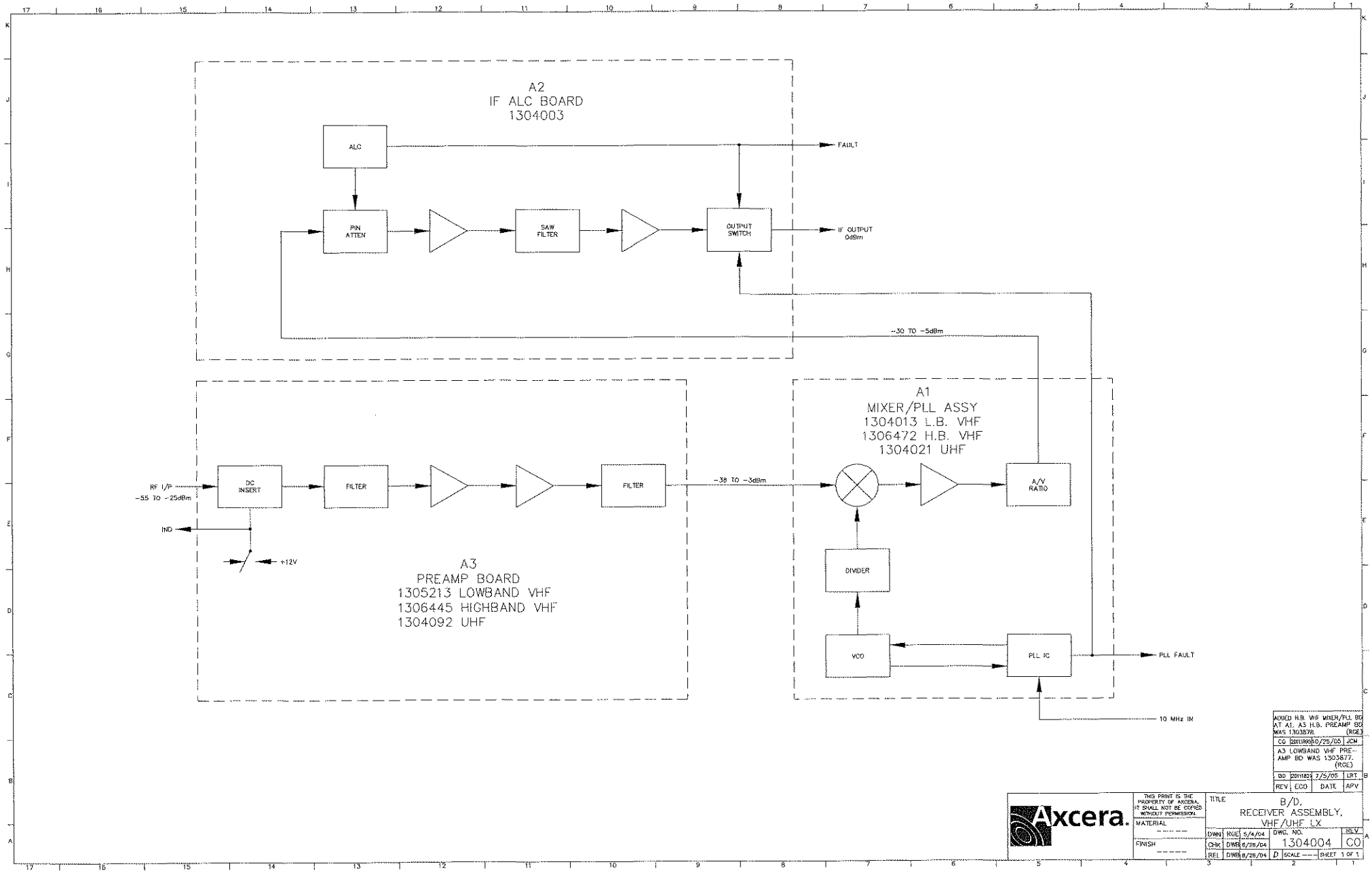
MATERIAL
FINISH
REV
ECO
DATE
APV
TITLE
SCH., ANALOG MODULATOR BD., SYS. M/N (1301797)
DWN JRF 2/20/03
CHK LRT 2/20/03
REL LRT 3/20/03
DWG. NO. 1301798
SIZE D
SCALE
SHEET 2 OF 3


Axcera
TITLE
SCH., ANALOG MODULATOR BD., SYS. M/N (1301797)
1301798
G0
SHEET 3 OF 3
"WA" (PG 1)
"WB" (PG 1)
"WC" (PG 1)
"H" (PG 1)
"J" (PG 2)
"K" (PG 1)
"M" (PG 2)
"N" (PG 2)
"E" (PG 1)
"G" (PG 1)
PLL UNLOCKED
EXT. CW PRES
O/P SIG. LEVEL
AUR. DEV. LVL
INTERLOCK
BASEBAND AUDIO (+)
AUDIO (-)
COMP. AUD. (-)
COMP. AUD. (+)
SAP/PRO AUDIO (+)
(-)
VIDEO I/P (-)
VIDEO I/P (+)
STATION ID CNTRL
+12VDC_C4
-12VDC_C1
SPARE AUX.
I/O_1
I/O_2
CW IF I/P
913289
+12VDC_C4
-12VDC_C1
VIA1
VIA2
LOW=TOO HIGH
LO=TOO LOW
VIS. UNLOCK (FT PNL)
ALT. UNLOCK (FT PNL)
VISUAL LEVEL (FT PNL)
AUR. LEVEL (FT PNL)
O/P SAMPLE (FT PNL)
AURAL PULSE ADJ.
PLL LOCK BAL.
FREQ RESP
AUR IF O/P
IF SAMPLE
* EXTERNAL CABLE ASSY.
LAST USED
C195
CR41
DS7
FL1
HR1
J41
K2
L41
Q28
R321
SW12
T4
TP3
U33
VIA2
VR2
W16
Y1
Z2



REV	ECO	DATE	APV
B0	2011823	7/5/05	LRT
			(RGE)
A3 LOWBAND VHF PRE-AMP BD WAS 1303877.			
C0	2011995	10/25/05	JCM
ADDED H.B. VHF MIXER/PLL BD AT A1, A3 H.B. PREAMP BD WAS 1303878.			(RGE)

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MATERIAL ------

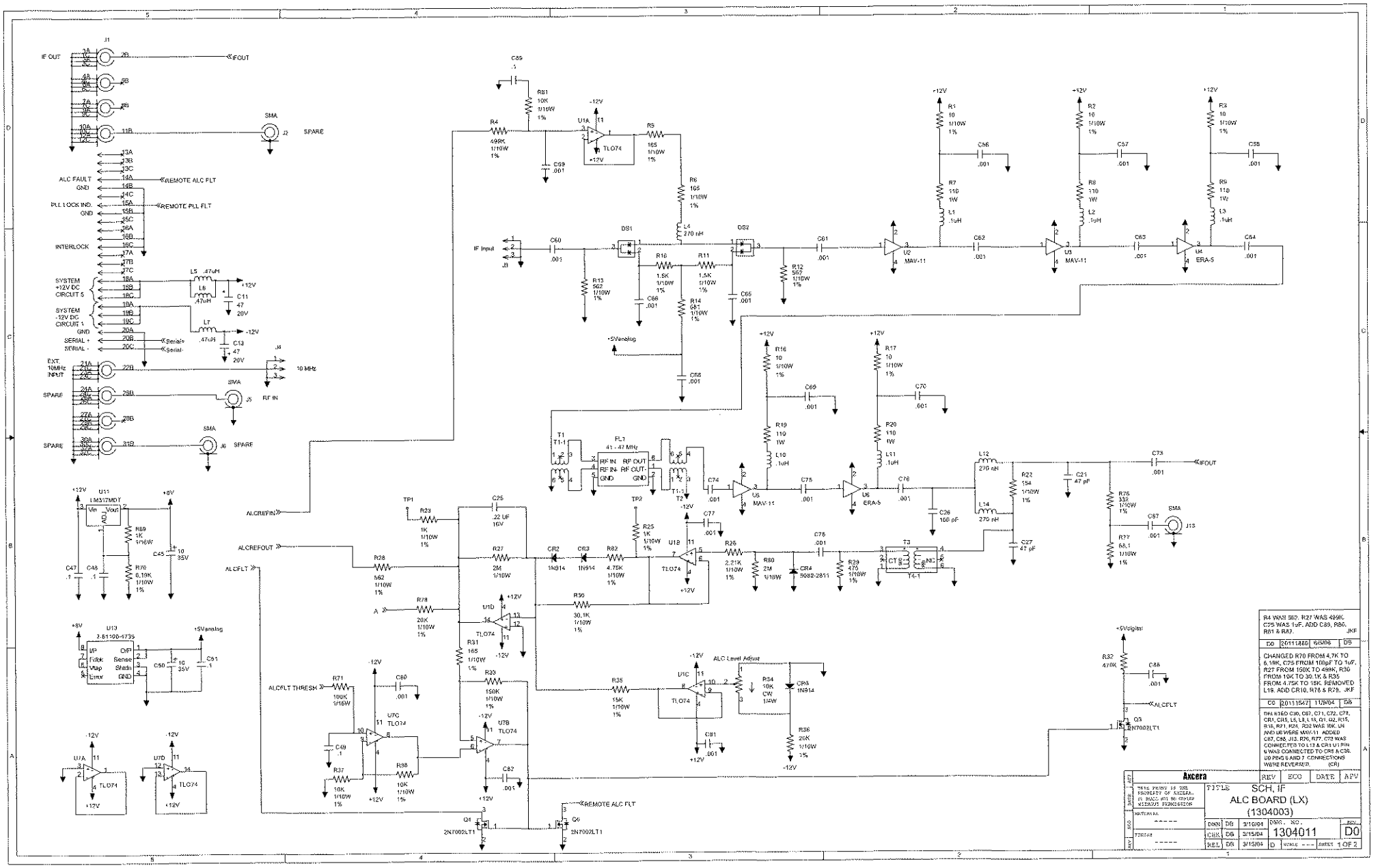
FINISH ------

TITLE: B/D, RECEIVER ASSEMBLY, VHF/UHF LX

DWN	RGE	5/4/04
CHK	DWR	6/26/04
REL	DWR	6/26/04

DWG. NO. 1304004 REV C0

D SCALE ---- SHEET 1 OF 1



R4 WAS 5K, R27 WAS 499K. C25 WAS 1uF, ADD C89, R80, R81 & R87. JKF

DD	20111880	6/5/06	DS

CHANGED R70 FROM 4.7K TO 6.19K, C75 FROM 100pF TO 1uF, R27 FROM 150K TO 499K, R30 FROM 10K TO 30.1K & R35 FROM 4.75K TO 15K. REMOVED L19. ADD CR10, R76 & R79. JKF

CC	20111547	1/26/04	SB

R44 R160 C80, C87, C71, C72, C78, CR1, CR5, L5, L9, L15, Q1, Q2, R15, R18, R21, R24, R32 WAS 10K. U4 AND U6 WERE MAV-11. ADDED C67, C86, J13, R76, R77. CR3 WAS CONNECTED TO L13 & CR1 U1 PIN 6 WAS CONNECTED TO CR5 & C56. U9 PINS 6 AND 7 CONNECTIONS WERE REVERSED. (CR)

REV	ECO	DATE	APV

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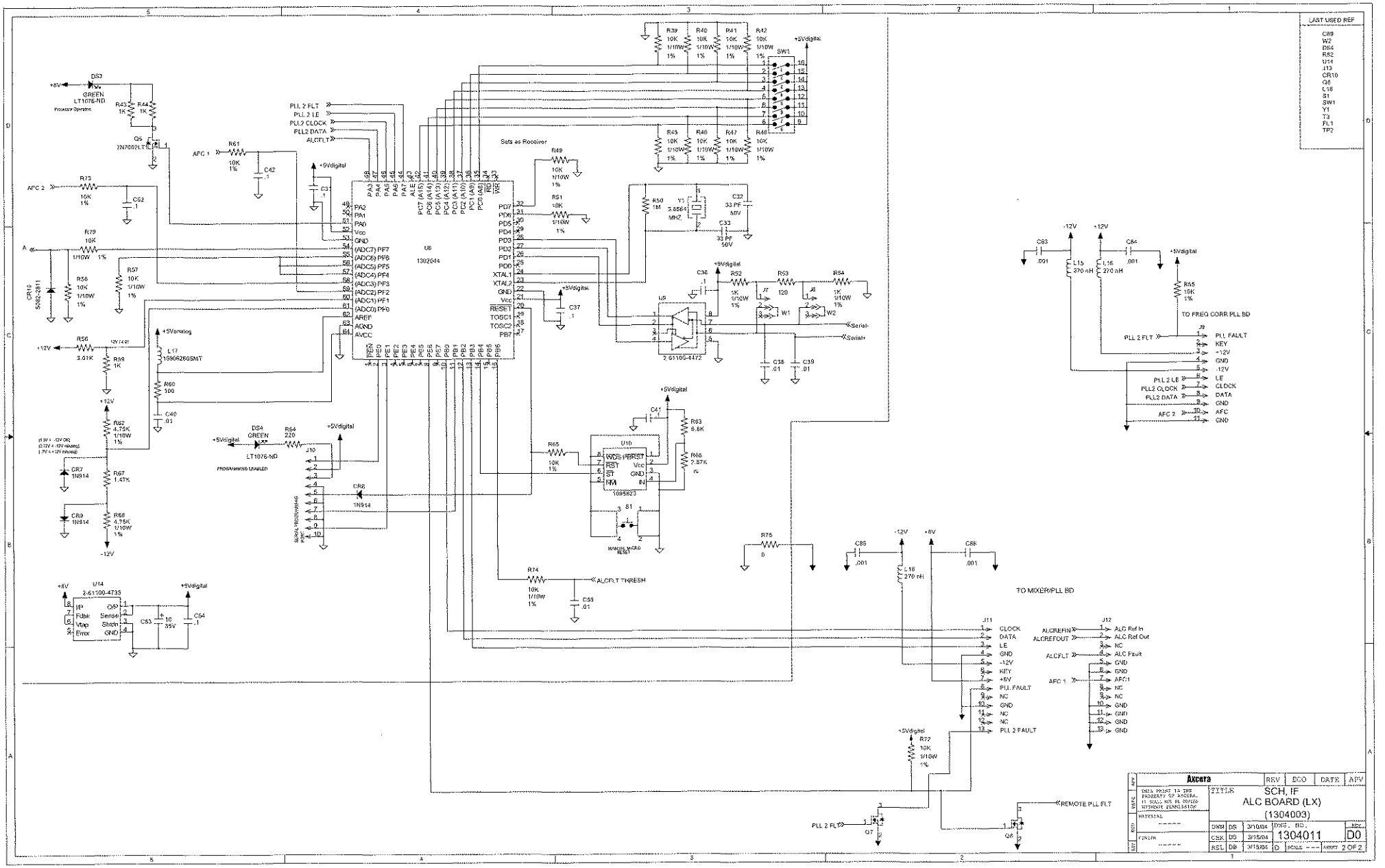
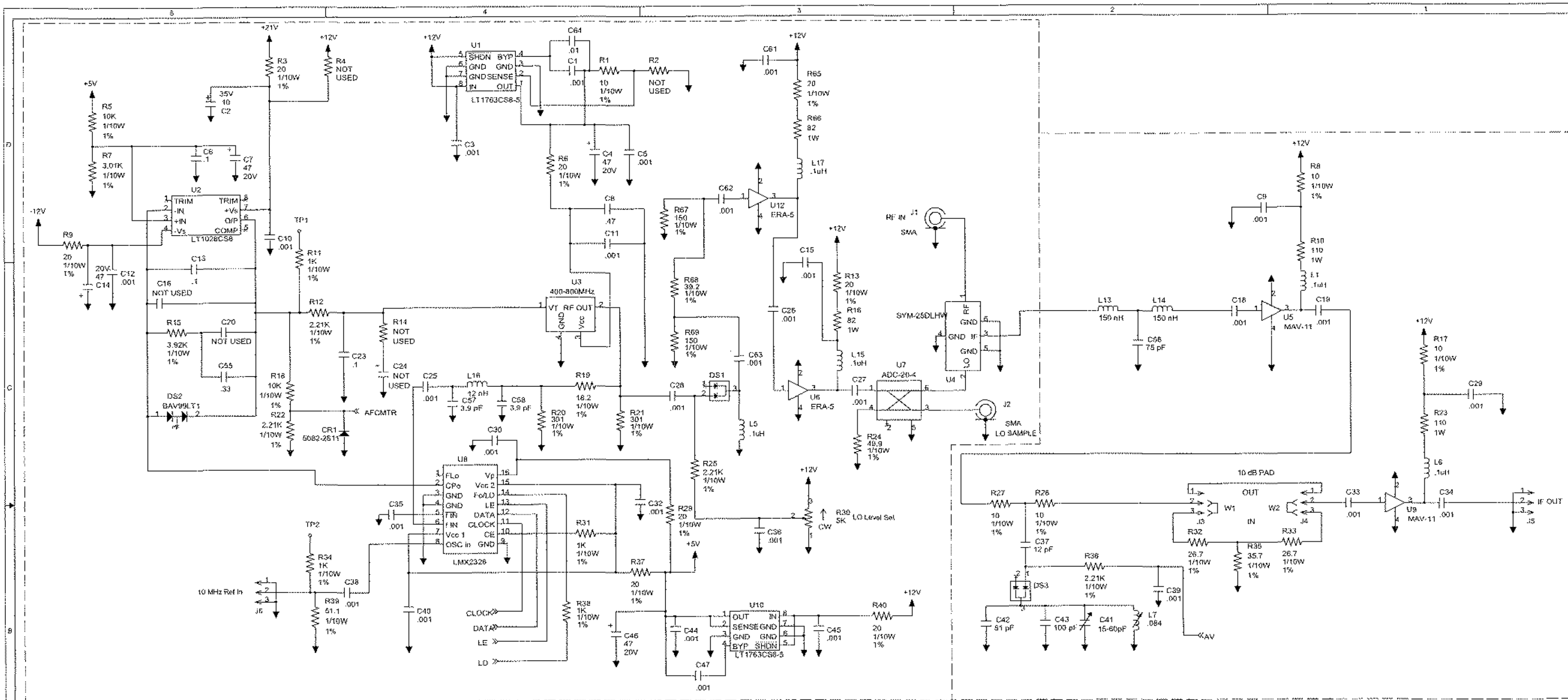
TITLE: SCH, IF ALC BOARD (LX) (1304003)

DWN	DB	3/15/04	DWG. NO. 1304011 REV D0
CHK	DB	3/15/04	
REL	DB	3/15/04	D SCALE --- SHEET 1 OF 2

MATERIAL: ---

FINISH: ---


LAST USED REF
C89
W2
DS4
R62
U14
J13
CR10
Q6
L18
S1
SW1
Y1
T3
FL1
TP2
DS3
GREEN
LT1076-ND
Processor Operates
R43
R44
Q5
2N7002LT1
PLL 2 FLT
PLL 2 LE
PLL2 CLOCK
PLL2 DATA
ALCFLT
AFC 1
R61
C42
AFC 2
R73
C52
R79
CR10
5082-2811
R56
R57
+5Vanalog
+12V
L17
1996266SMT
R58
R59
R60
C40
R62
4.75K
CR7
1N914
R67
1.47K
CR9
R68
-12V
DS4
GREEN
LT1076-ND
PROGRAMMING ENABLED
R64
220
J10
CR8
1N914
R65
10K
U10
1085823
MANUAL MODE RESET
S1
R63
6.8K
R65
2.87K
R74
ALCFLT THRESH
C55
.01
R75
0
C85
.001
C86
.001
L18
270 nH
TO MIXER/PLL BD
U14
2-61100-4735
C53
10
35V
C54
.1
R72
10K
REMOTE PLL FLT
PLL 2 FLT
Q7
Q6
R39
R40
R41
R42
SW1
R45
R46
R47
R48
Sets as Receiver
R49
RS1
U6
1302044
C31
C32
33 PF
50V
C33
Y1
5.6644
MHZ
R50
1M
C34
U5
2.61100-4472
RS2
RS3
RS4
J7
J8
W1
W2
Serial-
Serial+
C37
C38
C39
C83
.001
L15
270 nH
L16
270 nH
C84
.001
R55
10K
TO FREQ CORR PLL BD
J9
PLL FAULT
KEY
-12V
GND
+12V
LE
CLOCK
DATA
GND
AFC
GND
J11
CLOCK
DATA
LE
GND
-12V
KEY
+8V
PLL FAULT
NC
NC
GND
NC
NC
PLL 2 FAULT
J12
ALC Ref In
ALC Ref Out
NC
ALC Fault
GND
GND
AFC1
NC
NC
GND
GND
GND
GND
ALCREFIN
ALCREFOUT
ALCFLT
AFC 1
Axcera
REV
ECO
DATE
APV
SCH, IF
ALC BOARD (LX)
(1304003)
DRN DS 3/10/04
CHK DS 3/15/04
RSL DB 3/15/04
1304011
D0
SHEET 2 OF 2



NOTE:

1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.
4) Bd Material 30 mil FR4

ADDED NOTE "NOT USED" AT C16, C20. R12 WAS 1K, R15 WAS 3.01K, C55 WAS 0.33UF. U2 WAS AD797BR C13 & C23 WERE SURFACE MOUNT. ADDED C61, C62, C63, L17, R65 THRU R70, U12. C15 WAS CONNECTED TO +12V. (CR)

C0	20111504	09/28/04	DB

DELETED R26, C17, C21, C22, C31, L2, L3, L4. ADDED NOTE "NOT USED" AT R2, R14, C24. R1 WAS 243 OHM, R13 WAS 82 OHM, R15 WAS 18 OHM. C6 & C51 WERE 0.1UF, C20 WAS 10UF, U1 & U10 WERE LT1763CS8, U3 WAS RDS-1500 (1000-1500 MHz), L9 WAS 15 UH. ADDED C56 THRU C60, L13 THRU L16, R64. REWIRED SW1. (CR)

REV	ECO	DATE	APV
B0	20111456	07/16/04	DB

REV	ECO	DATE	APV	DESCRIPTION
E0	20111854	2/20/06	DB	R62 & R63 WERE 2.21K. ADDED C64. CR
D0	20111577	11/8/04	DB	R43 WAS 150K. JKF

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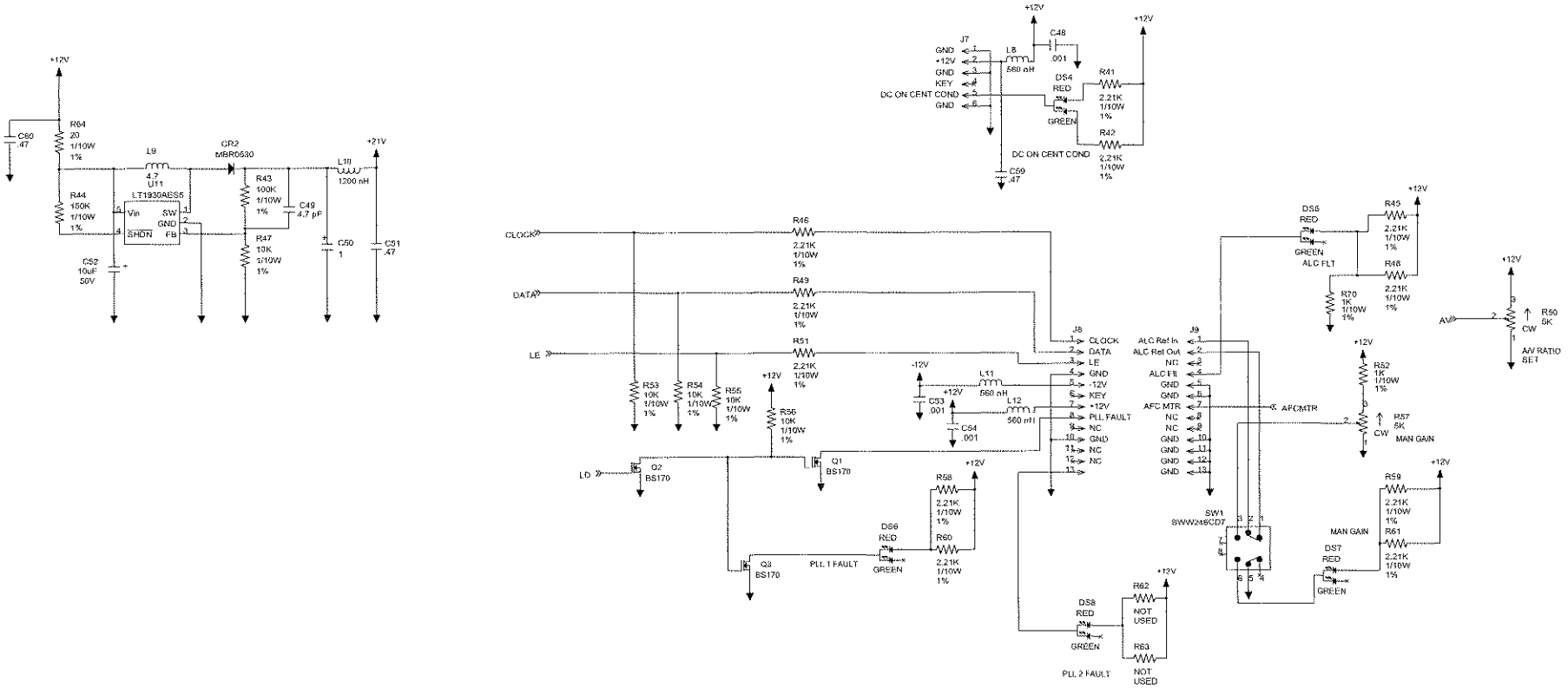
MATERIAL: ------

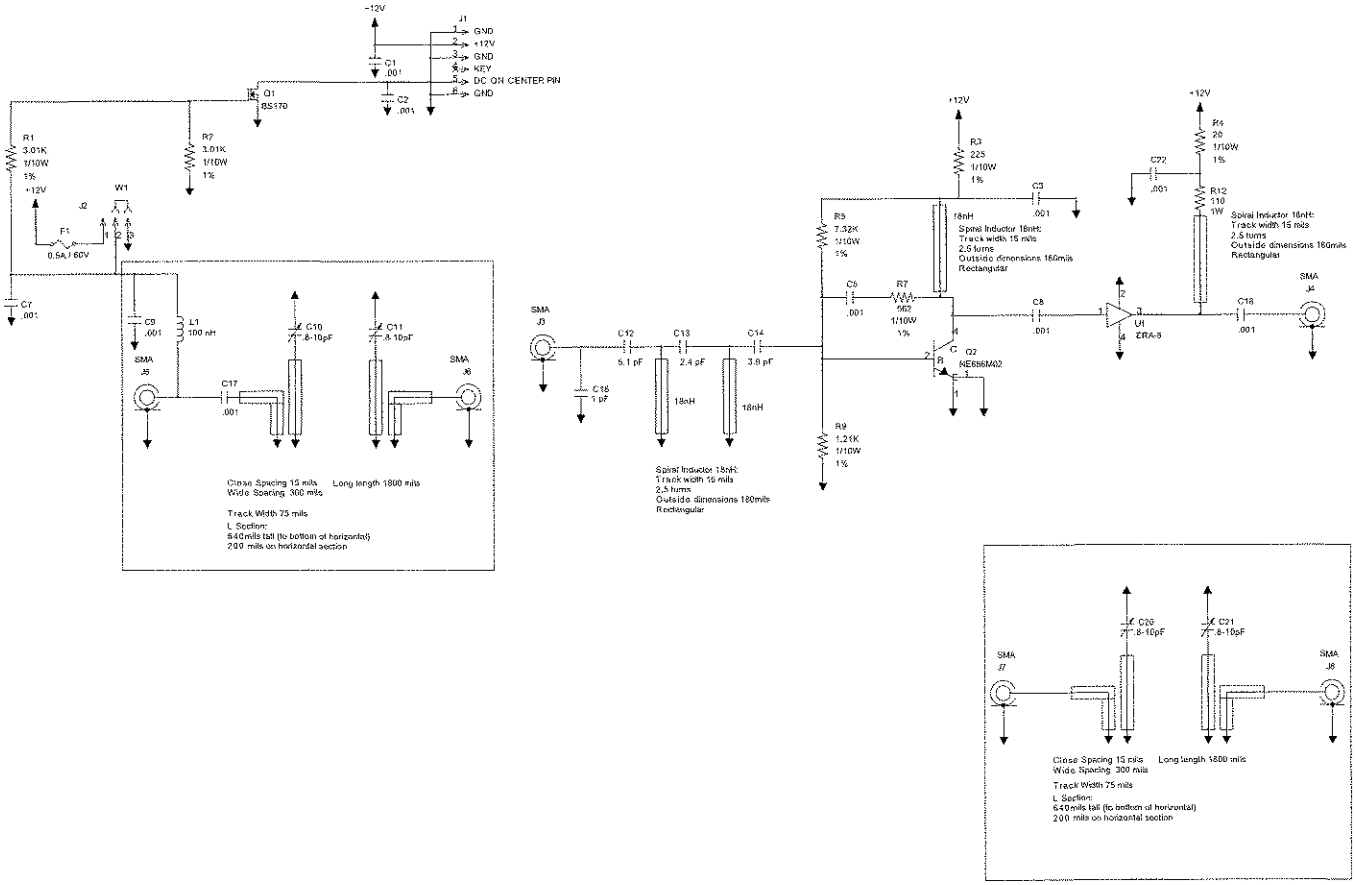
FINISH: ------

TITLE: SCH, UHF MIXER PLL BOARD (1304021)

DWN	DB	2/27/04	DWG. NO. 1304023 — REV E0
CHK	DB	2/27/04	
REL	DB	2/27/04	D — SCALE ---- — SHEET 1 OF 2



Axcera		REV	ECO	DATE	APV
THIS PRINT IS THE PROPERTY OF AXCERA. IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH, UHF MIXER/ PLL BOARD (1304021)				
MATERIAL -----	DWN DB 2/27/04	DWG. NO. 1304023		REV E0	
FINISH -----	CHK DB 2/27/04				
	REL DB 2/27/04	D	SCALE ----	SHEET 2 OF 2	



Notes:
BD Material is TLX-8 60 mils

REV	ECO	DATE	APV
C0	20111574	11/10/04	LRT
B9	20111489	07/20/04	DB

MOVED W1 FROM J2 1-2 TO J2 2-3. JKF

DELETED C4, C8, C15, C16, C3, R6, R9, R10, R11. C16 WAS 3.9 PF, R4 WAS 225 OHM. ADDED C22, R12. U1, SPIRAL INDUCTOR 18 NH WAS CONNECTED FROM C8 TO GND "LONG LENGTH" NOTE WAS 1800 MILS. L SECTION NOTE WAS 740 MILS TALL (TO BOTTOM OF HORIZONTAL. (DB)

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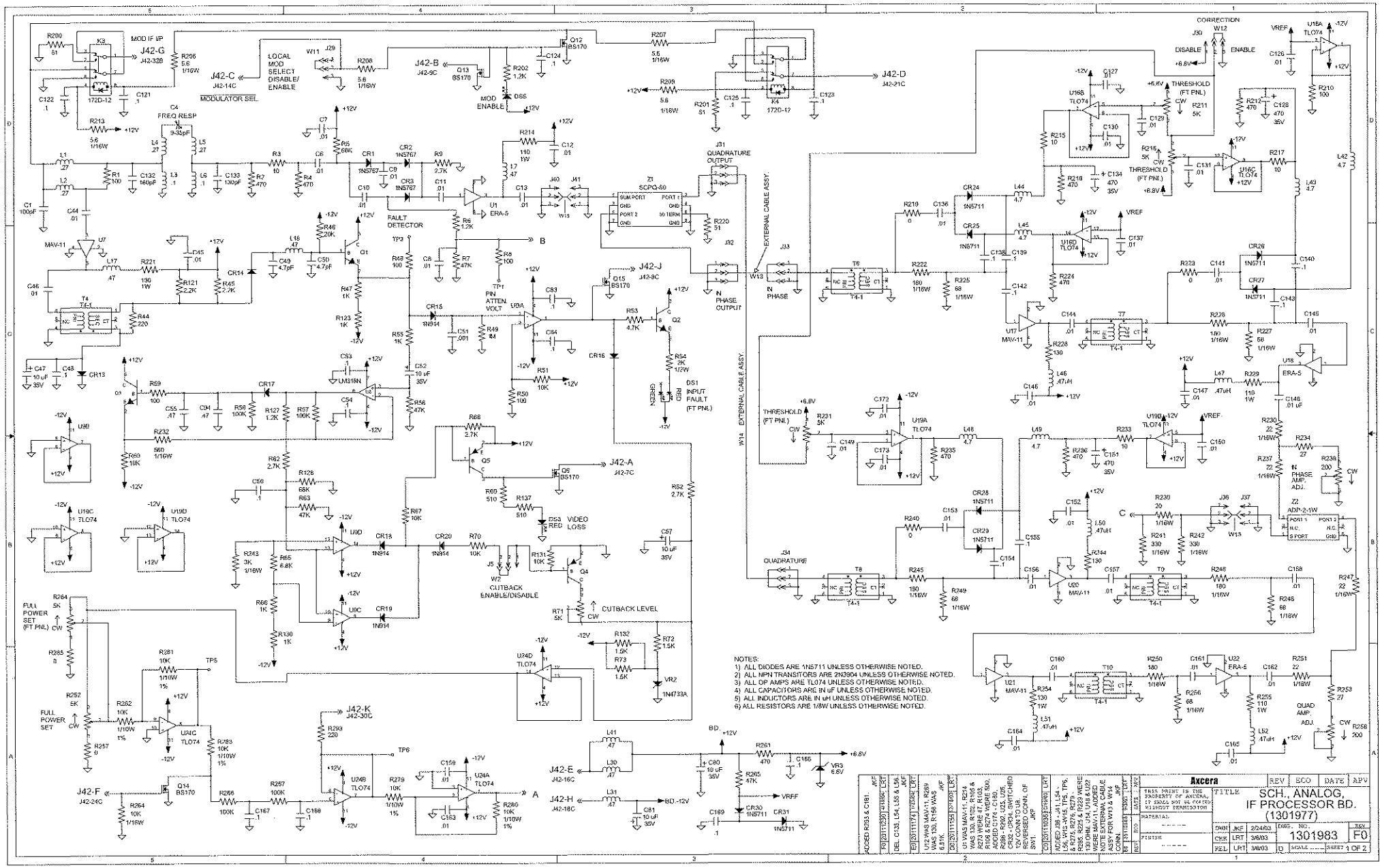
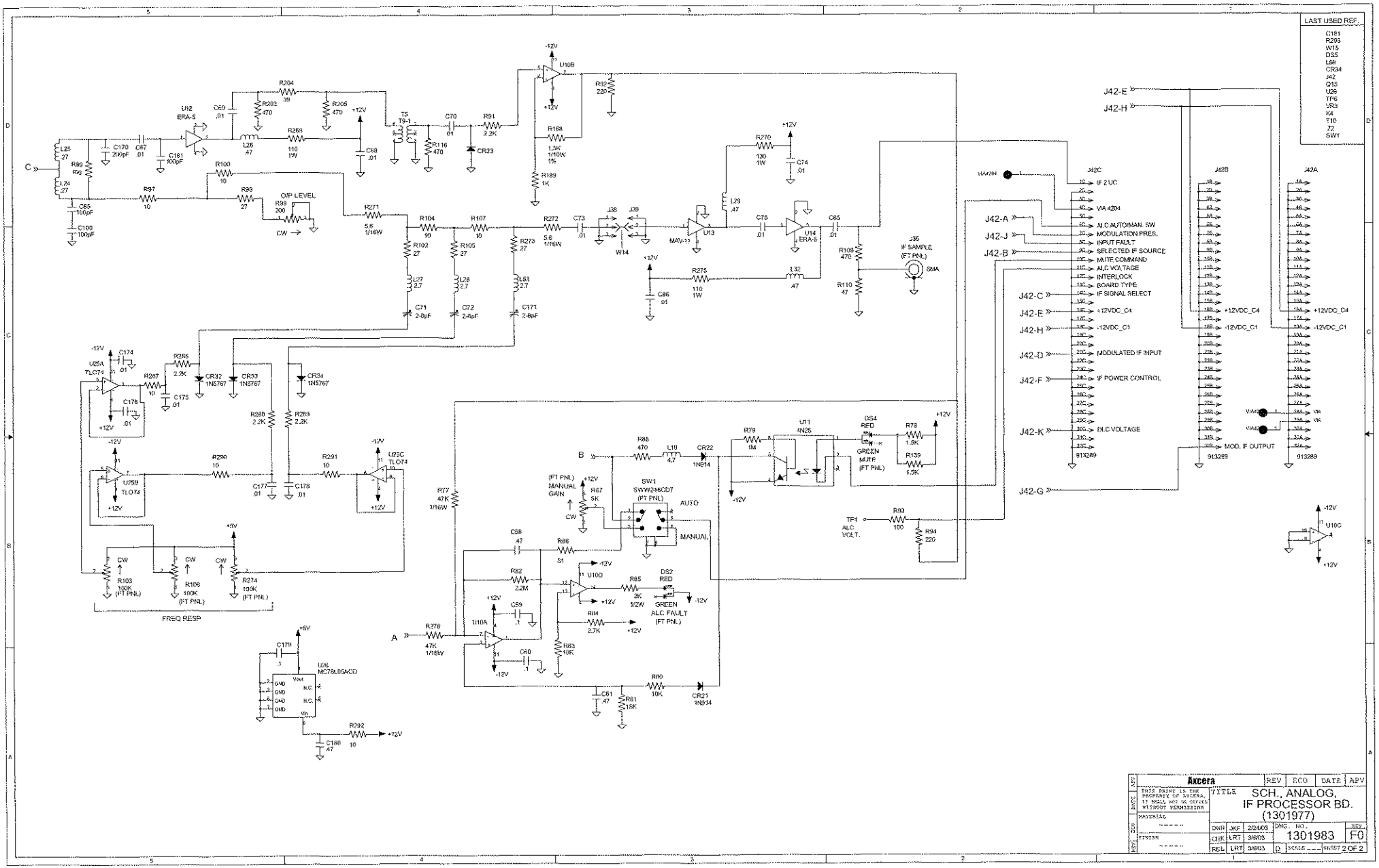
MATERIAL

FINISH

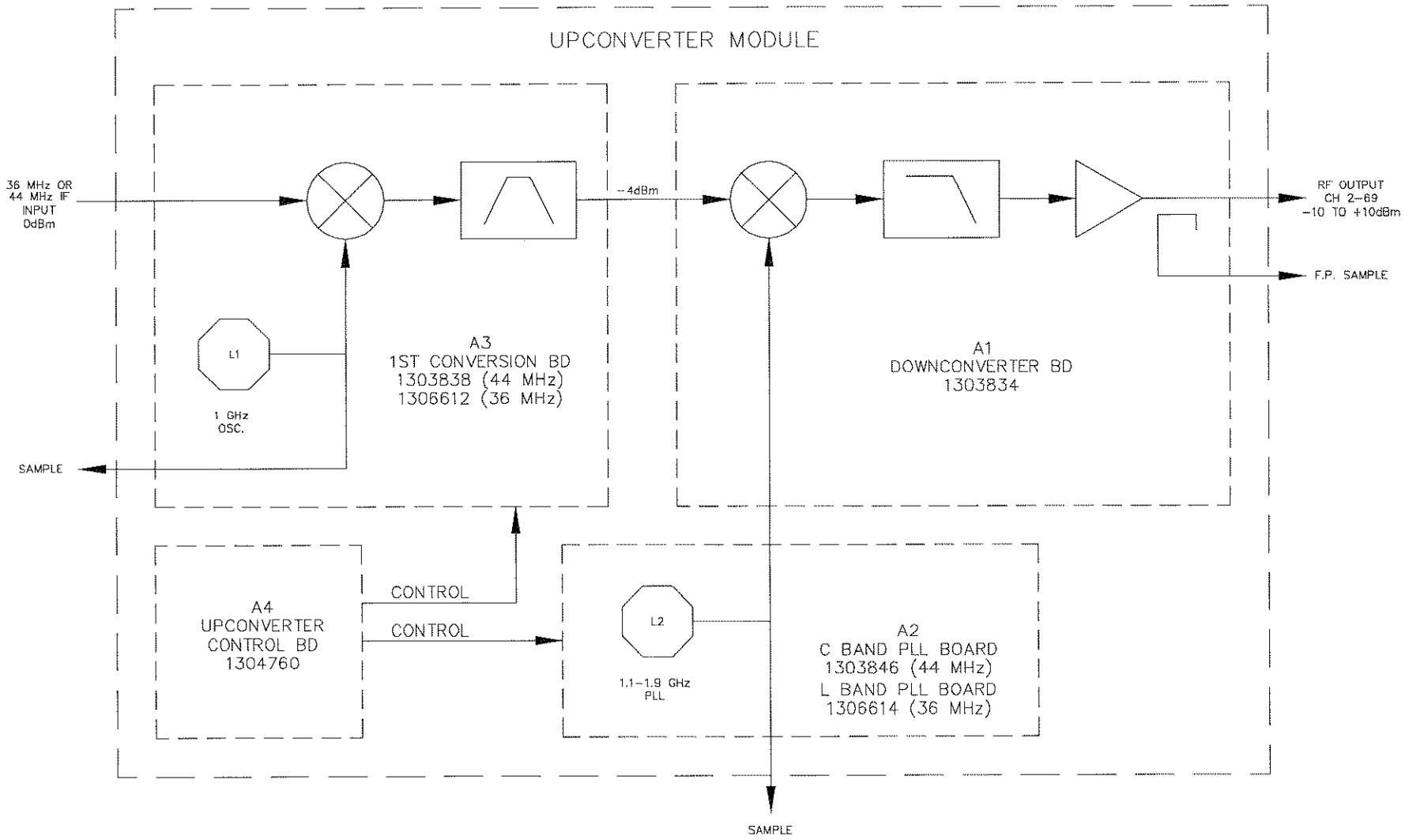
TITLE: SCHEMATIC, UHF PREAMPLIFIER (1304092)

DRN	DB	2/10/04	DWG. NO. 1304091 REV. C0
CHK	DB	2/26/04	
REL	DB	2/26/04	D SCALE --- SHEET 1 OF 1


J42-G
J42-32B
J42-C
J42-14C
J42-B
J42-9C
J42-D
J42-21C
J42-J
J42-8C
J42-A
J42-7C
J42-K
J42-30C
J42-F
J42-24C
J42-E
J42-16C
J42-H
J42-18C
LOCAL MOD SELECT DISABLE/ ENABLE
MODULATOR SEL.
MOD IF I/P
MOD ENABLE
FREQ RESP
FAULT DETECTOR
PIN ATTEN. VOLT
QUADRATURE OUTPUT
EXTERNAL CABLE ASSY.
W14 EXTERNAL CABLE ASSY.
N PHASE
N PHASE OUTPUT
CORRECTION
DISABLE
ENABLE
THRESHOLD (FT PNL)
THRESHOLD (FT PNL)
N PHASE ADJ.
QUAD AMP ADJ.
QUADRATURE
VIDEO LOSS
CUTBACK ENABLE/DISABLE
CUTBACK LEVEL
FULL POWER SET (FT PNL)
FULL POWER SET
INPUT FAULT (FT PNL)
NOTES:
1) ALL DIODES ARE 1N5711 UNLESS OTHERWISE NOTED.
2) ALL NPN TRANSISTORS ARE 2N3904 UNLESS OTHERWISE NOTED.
3) ALL OP AMPS ARE TL074 UNLESS OTHERWISE NOTED.
4) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
5) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.
6) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
Axcera
TITLE
SCH., ANALOG, IF PROCESSOR BD. (1301977)
REV
ECO
DATE
APV
DWN JKF 2/24/03
CHK LRT 3/6/03
REL LRT 3/6/03
DWG. NO. 1301983
REV F0
SCALE
SHEET 1 OF 2



	Axcera	REV	ECO	DATE	APV
	TITLE: SCH., ANALOG, IF PROCESSOR BD. (1301977)				
	DWN JKF 2/24/03	DWG. NO. 1301983		REV F0	
	CHK LRT 3/6/03				
	REL LRT 3/6/03	D	SCALE ---	SHEET 2 OF 2	



REV	ECO	DATE	APV

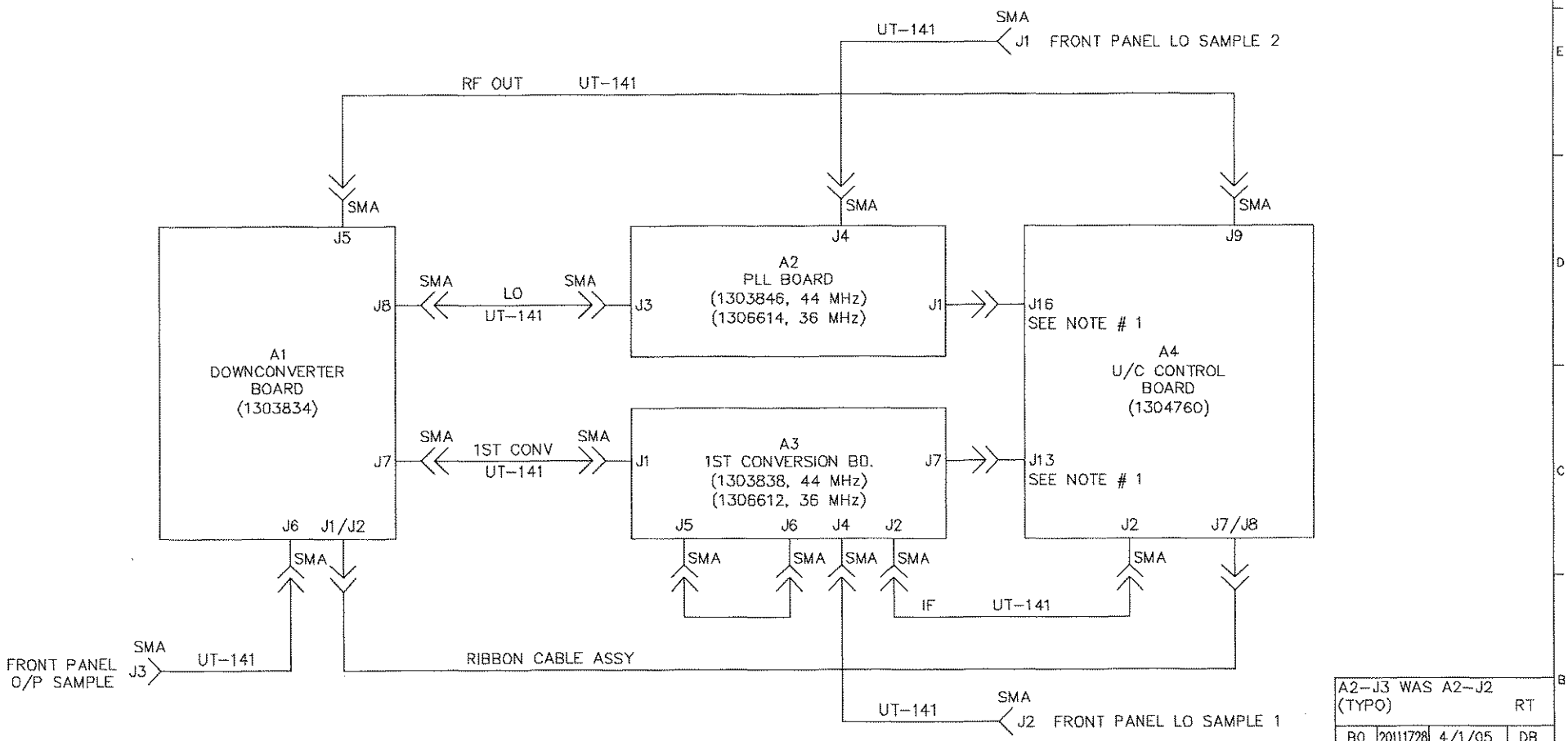
Axcera.

MATERIAL ---

FINISH ---

TITLE: B/D, U/C ASSEMBLY, VHF/UHF LX

DWN	RGE	5/7/04	DWG. NO. 1303830	REV A0
CHK	DWB	9/30/04		
REL	DWB	9/30/04	C	SCALE ---- SHEET 1 OF 1



NOTES:
1. CONNECTORS ARE BOARD TO BOARD AND NOT PART OF THE HARNESS.

A2-J3 WAS A2-J2 (TYPO)			RT
B0	20111728	4/1/05	DB
REV	ECO	DATE	APV

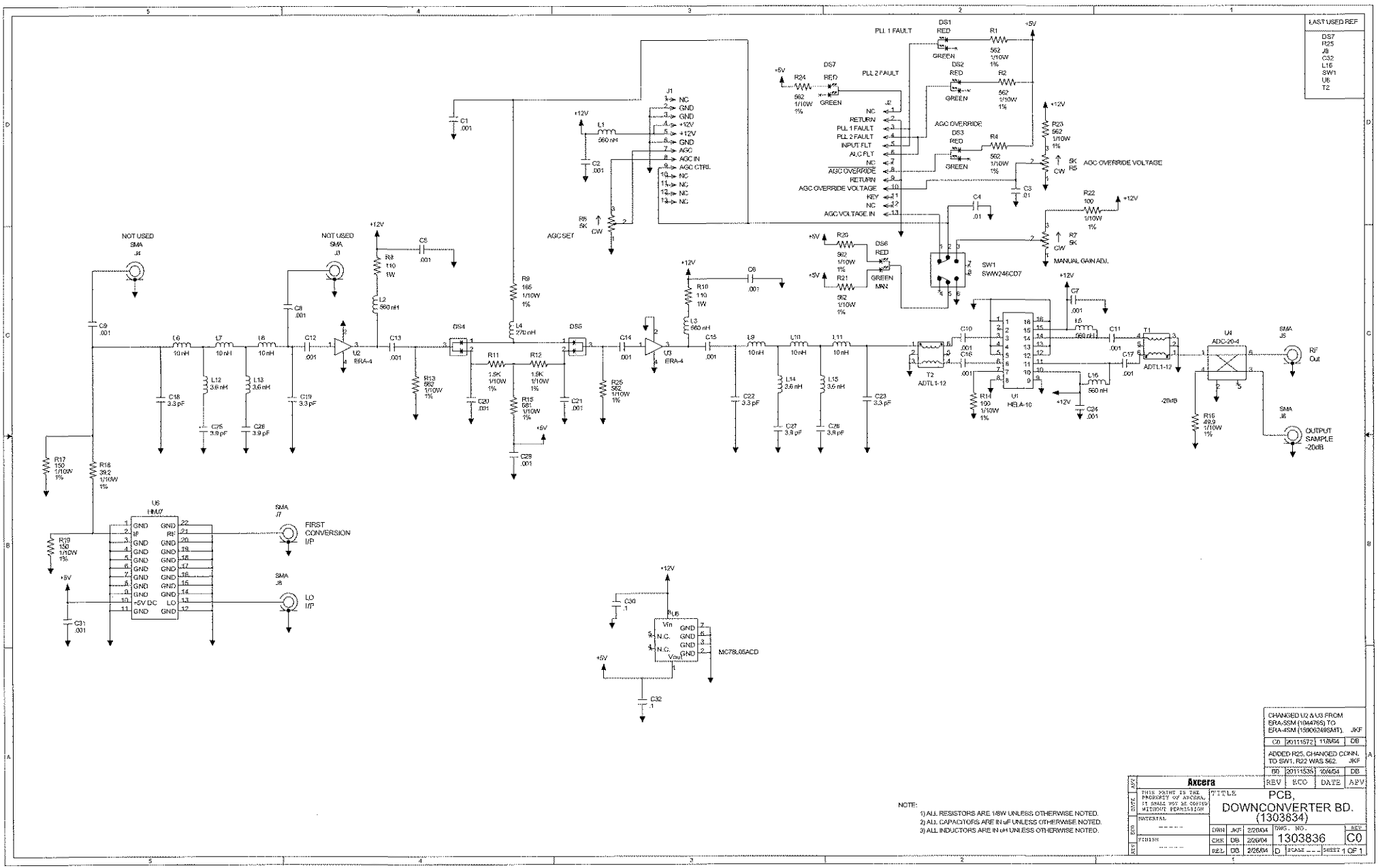
Axcera.

MATERIAL ------

FINISH ------

TITLE I/C, UPCONVERTER ASSY, VHF/UHF, LX

DWN	RGE	04/06/04	DWG. NO. 1303831	REV B0
CHK	DWB	9/30/04		
REL	DWB	9/30/04	B SCALE ---	SHEET 1 OF 1


LAST USED REF
DS7
R25
J9
C32
L16
SW1
U6
T2
PLL 1 FAULT
PLL 2 FAULT
AGC OVERRIDE
AGC OVERRIDE VOLTAGE
MANUAL GAIN ADJ.
AGC SET
NOT USED SMA J4
NOT USED SMA J3
SMA J7 FIRST CONVERSION I/P
SMA J8 LO I/P
SMA J5 RF Out
SMA J6 OUTPUT SAMPLE -20dB
ERA-4
ADTL1-12
HMJ7
MC78L05ACD
NOTE:
1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN nH UNLESS OTHERWISE NOTED.
CHANGED U2 & U3 FROM ERA-5SM (1004765) TO ERA-4SM (15006248SMT), JKF
C0 20111572 11/8/04 DB
ADDED R25, CHANGED CONN. TO SW1, R22 WAS 562. JKF
B0 20111535 10/4/04 DB
Axcera
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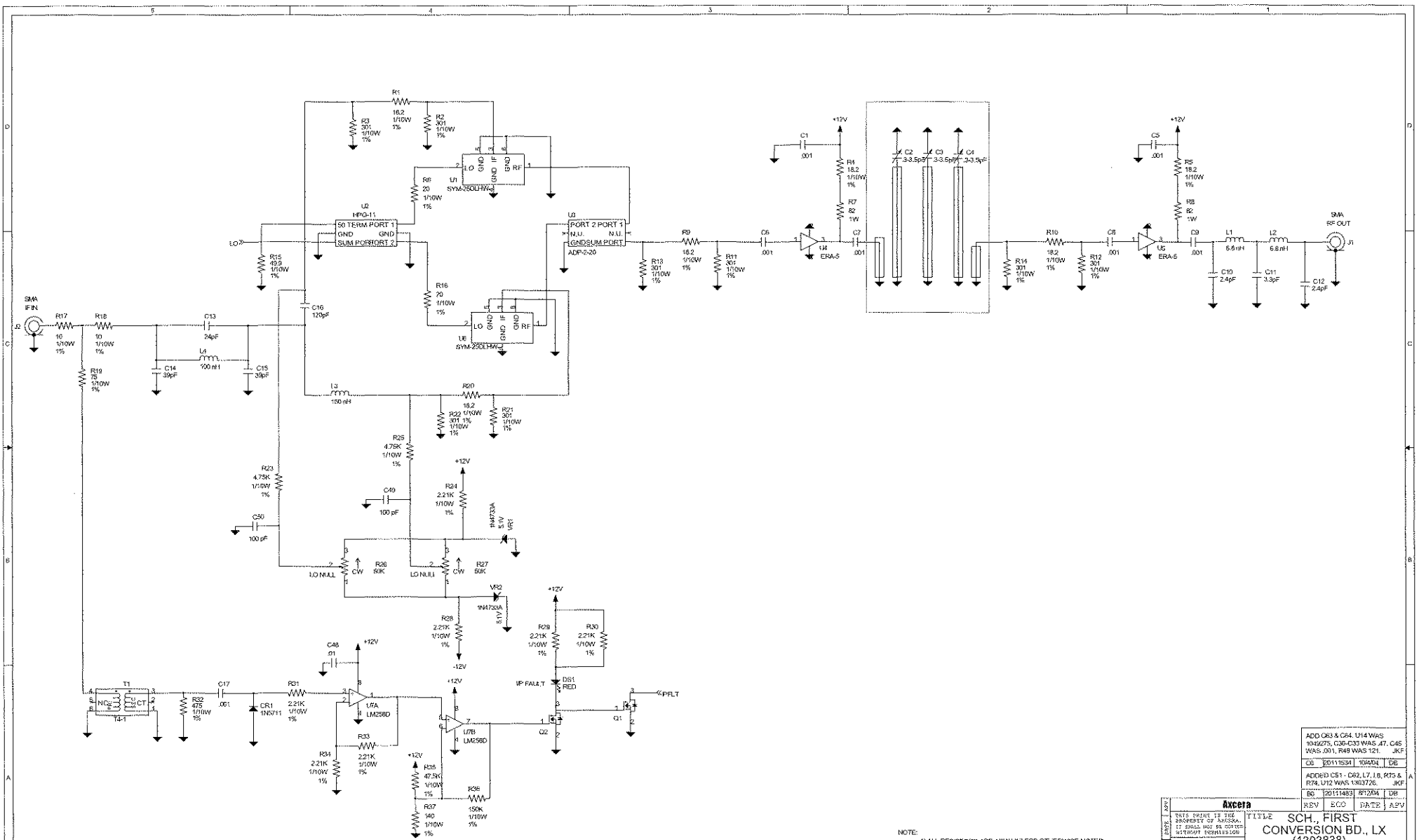
MATERIAL
FINISH
TITLE PCB, DOWNCONVERTER BD. (1303834)
DRN JKF 2/2/04
CHK DB 2/26/04
APV DB 2/26/04
DWG. NO. 1303836
REV C0
SCALE
SHEET 1 OF 1



NOTE:
1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN nH UNLESS OTHERWISE NOTED.

REV	ECO	DATE	APV
C0	20111534	10/4/04	DB
ADDED C51 - C62, L7, L8, R75 & R74, U12 WAS 1303726.			JKF
B0	20111483	8/12/04	DB

ADD C63 & C64, U14 WAS 1049275, C30-C33 WAS .47, C45 WAS .001, R48 WAS 121. JKF

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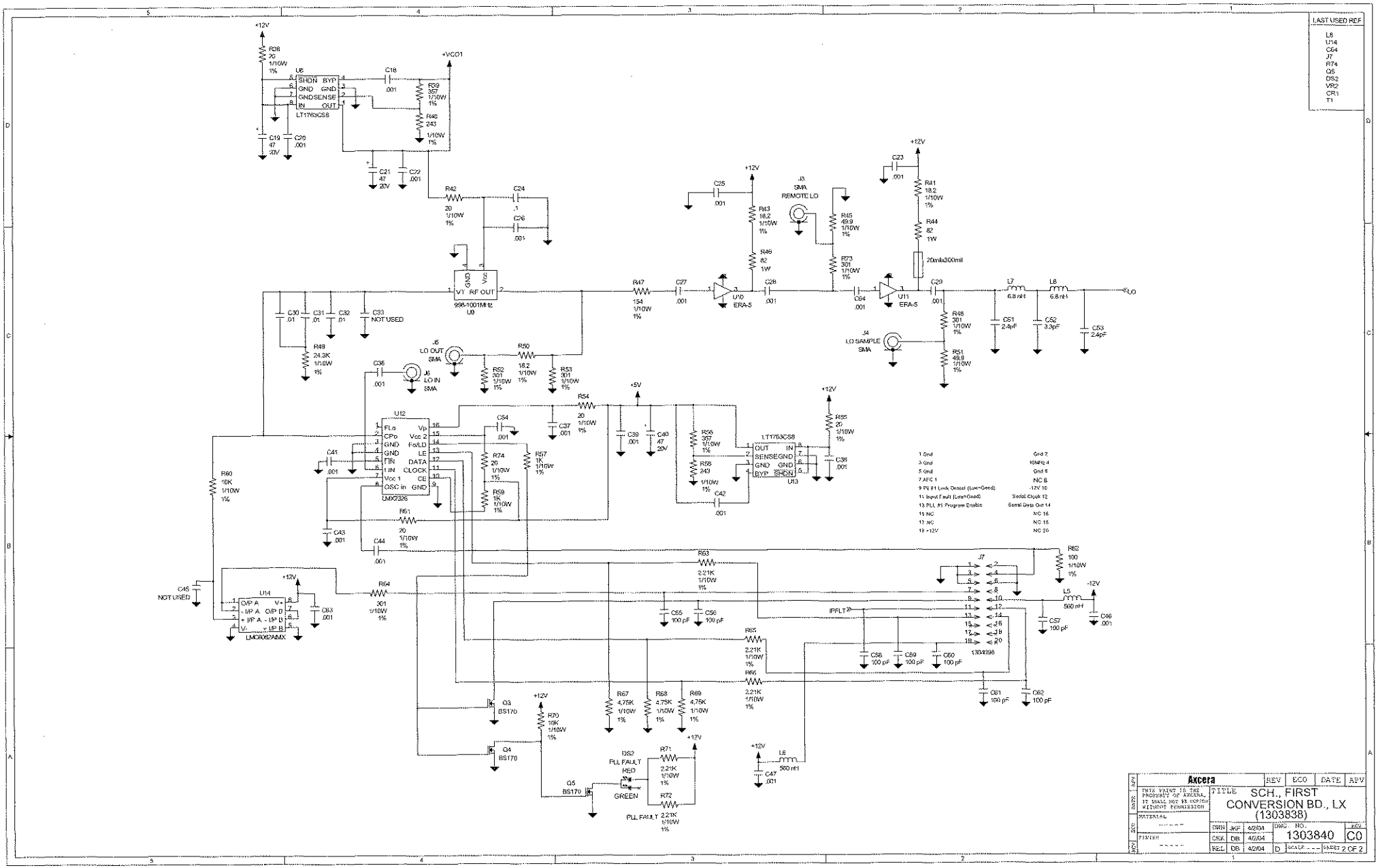
TITLE: SCH., FIRST CONVERSION BD., LX (1303838)

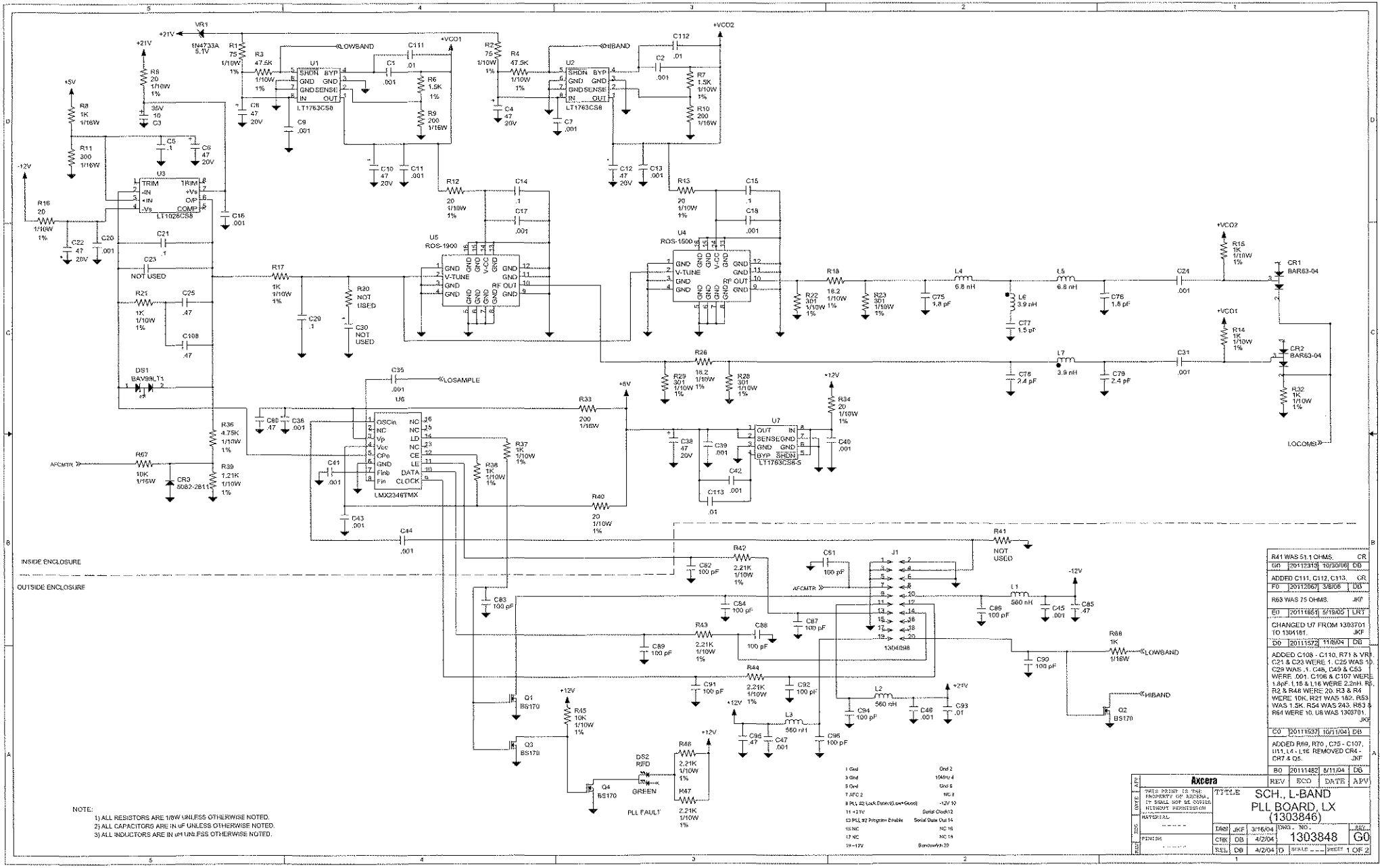
DWN	JKF	4/2/04	
CHK	DB	4/2/04	
PEL	DB	4/2/04	

MATERIAL: ------
FINISH: ------

DWG. NO. 1303840 REV C0

D SCALE: ---- SHEET 1 OF 2


LAST USED REF
L8
U14
C84
J7
R74
Q5
DS2
VR2
CR1
T1
+12V
+VCO1
U8
LT1763CS8
R38 20 1/10W 1%
C16 .001
R39 357 1/10W 1%
R40 243 1/10W 1%
C19 47 20V
C20 .001
C21 47 20V
C22 .001
R42 20 1/10W 1%
C24 .1
C26 .001
U0 936-1001MHz
C30 .01
C31 .01
C32 .01
C33 NOT USED
R49 24.3K 1/10W 1%
J5 LO OUT SMA
J6 LO IN SMA
C36 .001
R50 18.2 1/10W 1%
R52 301 1/10W 1%
R53 301 1/10W 1%
R47 154 1/10W 1%
C27 .001
U10 ERA-5
C28 .001
C25 .001
R43 18.2 1/10W 1%
R46 82 1W
J3 SMA REMOTE LO
R45 49.9 1/10W 1%
R73 301 1/10W 1%
C23 .001
R41 18.2 1/10W 1%
R44 82 1W
20mils/30mil
C64 .001
U11 ERA-5
C29 .001
L7 6.8 nH
L8 6.8 nH
LO
J4 LO SAMPLE SMA
R48 301 1/10W 1%
R51 49.9 1/10W 1%
C51 2.4pF
C52 3.3pF
C53 2.4pF
+5V
R54 20 1/10W 1%
C39 .001
C40 47 20V
R56 357 1/10W 1%
R58 243 1/10W 1%
C42 .001
LT1763CS8
C38 .001
R55 20 1/10W 1%
U12 LMX2326
C54 .001
C37 .001
C41 .001
R74 20 1/10W 1%
R57 1K 1/10W 1%
R59 1K 1/10W 1%
R60 10K 1/10W 1%
R61 20 1/10W 1%
C43 .001
C44 .001
1 Gnd
3 Gnd
5 Gnd
7 AFC 1
9 PE #1 Lock Detect (Low=Good)
11 Input Fault (Low=Good)
13 PLL #1 Program Enable
15 NC
17 NC
19 +12V
Gnd 2
10MHz 4
Gnd 6
NC 8
+12V 10
Serial Clock 12
Serial Data Out 14
NC 16
NC 18
NC 20
R63 2.21K 1/10W 1%
R62 100 1/10W 1%
J7
L5 560 nH
C57 100 pF
C46 .001
C45 NOT USED
U14 LMC6082AIMX
R64 301 1/10W 1%
C63 .001
C55 100 pF
C56 100 pF
IPFLT
R65 2.21K 1/10W 1%
R66 2.21K 1/10W 1%
C56 100 pF
C59 100 pF
C60 100 pF
1304398
C61 100 pF
C62 100 pF
Q3 BS170
Q4 BS170
R67 4.75K 1/10W 1%
R68 4.75K 1/10W 1%
R69 4.75K 1/10W 1%
R70 10K 1/10W 1%
Q5 BS170
DS2 PLL FAULT RED GREEN
R71 2.21K 1/10W 1%
RT2 2.21K 1/10W 1%
PLL FAULT
L6 560 nH
C47 .001
Axcera
REV ECO DATE APV
THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION
TITLE SCH., FIRST CONVERSION BD., LX (1303838)
MATERIAL
FINISH
DWN JKF 4/2/04
CHK DB 4/2/04
REL DB 4/2/04
DWG. NO. 1303840
REV C0
D
SCALE ---
SHEET 2 OF 2



NOTE:
1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.

REV	ECO	DATE	APV
R41 WAS 51.1 OHMS.			CR
G0	20112313	10/30/06	DB
ADDED C111, C112, C113.			CR
F0	20112067	3/8/06	DB
R63 WAS 75 OHMS.			JKF
E0	20111651	5/19/05	LR1
CHANGED U7 FROM 1303701 TO 1304181.			JKF
D0	20111572	11/8/04	DB
ADDED C108 - C110, R71 & VR1. C21 & C23 WERE 1. C25 WAS 10. C29 WAS .1. C48, C49 & C53 WERE .001. C106 & C107 WERE 1.8pF. L15 & L16 WERE 2.2nH. R1, R2 & R48 WERE 20. R3 & R4 WERE 10K. R21 WAS 182. R53 WAS 1.5K. R54 WAS 243. R63 & R64 WERE 10. U8 WAS 1303701.			JKF
C0	20111537	10/11/04	DB
ADDED R69, R70 , C75 - C107, L11, L4 - L16 REMOVED CR4 - CR7 & Q5.			JKF
B0	20111482	8/11/04	DB

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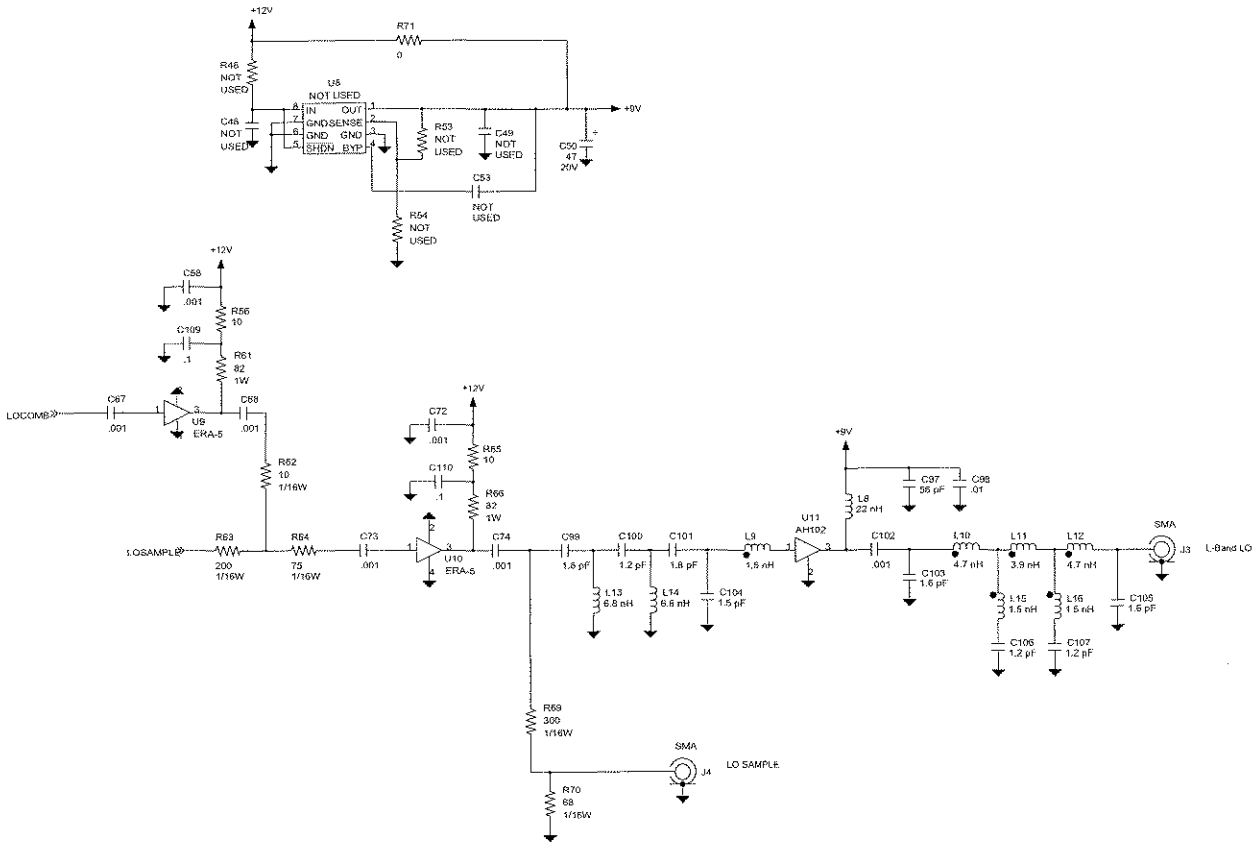
MATERIAL

FINISH

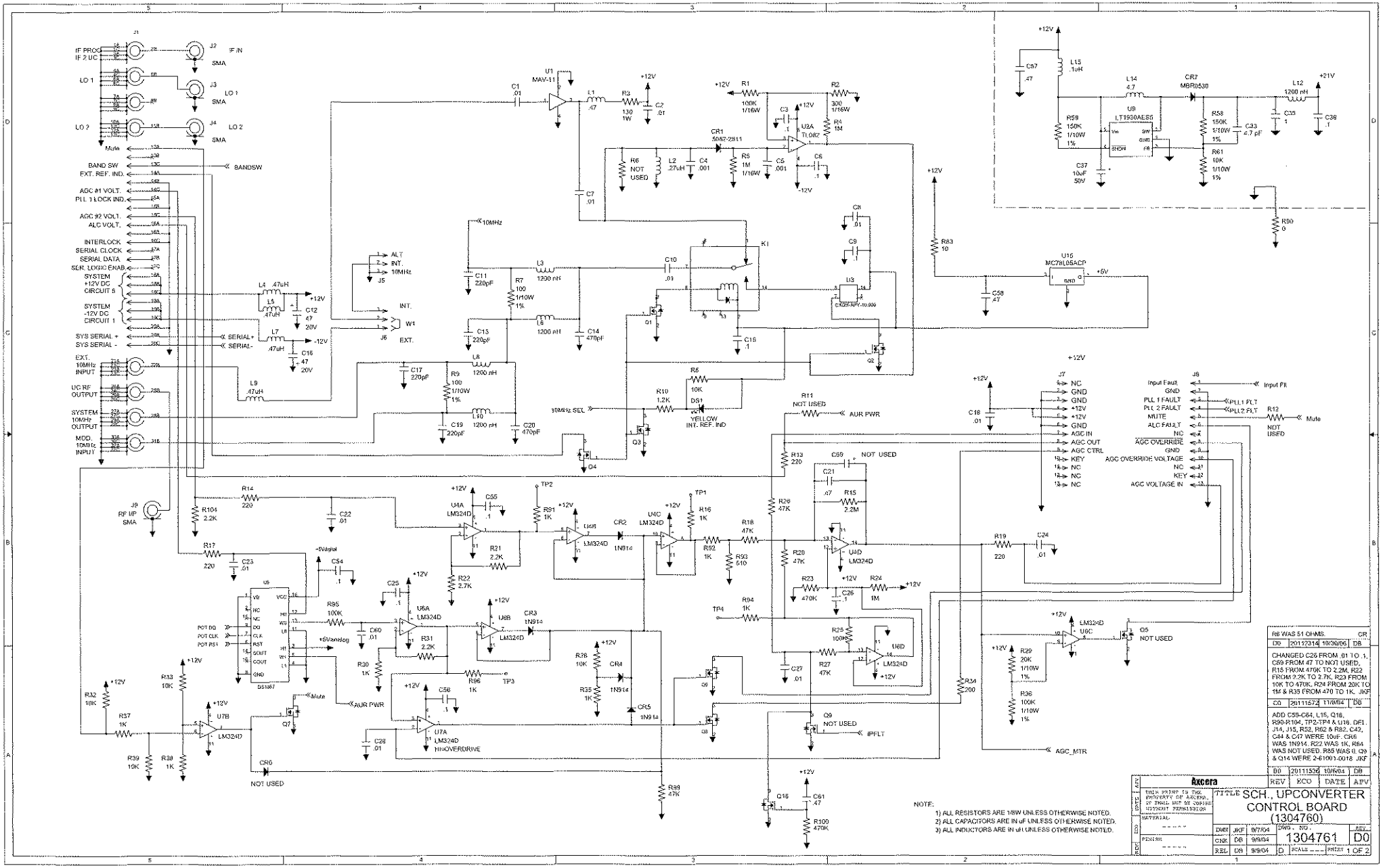
TITLE: SCH., L-BAND PLL BOARD, LX (1303846)

DRN	JKF	3/16/04	SIZE: D — NO.: 1303848 — REV: G0
CHK	DB	4/2/04	
ENGR	DB	4/2/04	SCALE: — SHEET 1 OF 2

LAST USED REF
C113
L16
U11
R71
J4
Q4
CR3
DS2
VR1



	Axcera	REV	ECO	DATE	APV
APV	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE	SCH., L-BAND PLL BOARD, LX (1303846)		
DATE	MATERIAL -----	DWN	JKF	3/16/04	DWG. NO. 1303848 REV G0
REV	FINISH -----	CHK	DB	4/2/04	
DES		REL	DB	4/2/04	D SCALE ---- SHEET 2 OF 2


IF PROC
IF 2 UC
LO 1
LO 2
J2 IF IN SMA
J3 LO 1 SMA
J4 LO 2 SMA
Mute
BAND SW
EXT. REF. IND.
AGC #1 VOLT.
PLL 1 LOCK IND.
AGC #2 VOLT.
ALC VOLT.
INTERLOCK
SERIAL CLOCK
SERIAL DATA
SER. LOGIC ENAB
SYSTEM +12V DC CIRCUIT 6
SYSTEM -12V DC CIRCUIT 1
SYS SERIAL +
SYS SERIAL -
EXT. 10MHz INPUT
UC RF OUTPUT
SYSTEM 10MHz OUTPUT
MOD. 10MHz INPUT
BANDSW
SERIAL+
SERIAL-
U1 MAV-11
U2A TL082
U3 CXO-53PV-10.000
U5 DS1867
U6A LM324D
U6B LM324D
U6C LM324D
U6D LM324D
U7A LM324D HIOVERDRIVE
U7B LM324D
U8 LT1930AES5
U9 LT1930AES5
U10 MC78L05ACP
CR1 5082-2811
CR2 1N914
CR3 1N914
CR4 1N914
CR5 1N914
CR6 NOT USED
CR7 MBR0530
DS1 YELLOW INT. REF. IND
Q1
Q2
Q3
Q4
Q5 NOT USED
Q6
Q7
Q8
Q9 NOT USED
Q15
Q16
K1
ALT
INT.
10MHz
EXT.
J5
J6
J7
J8 RF I/F SMA
J9
10MHz SEL
AUX PWR
#PLL1 FLT
#PLL2 FLT
Input Flt
Mute
AGC_MTR
#PFLT
+5Vdigital
+5Vanalog
POT DQ
POT CLK
POT RS1
NOT USED
NOTE:
1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.
R6 WAS 51 OHMS. CR D0 20117314 10/30/06 DB
CHANGED C26 FROM .01 TO .1, C59 FROM 47 TO NOT USED, R15 FROM 470K TO 2.2M, R22 FROM 2.2K TO 2.7K, R23 FROM 10K TO 470K, R24 FROM 20K TO 1M & R35 FROM 470 TO 1K. JKF
C0 20111572 11/8/04 DB
ADD C59-C64, L15, Q16, R90-R104, TP2-TP4 & U10. DF1, J14, J15, R52, R62 & R82. C42, C44 & C47 WERE 10uF. C66 WAS 1N914. R22 WAS 1K, R64 WAS NOT USED. R65 WAS 0. Q9 & Q14 WERE 2-61001-0018 JKF
B0 20111536 10/6/04 DB
Axcera
REV ECO DATE APV
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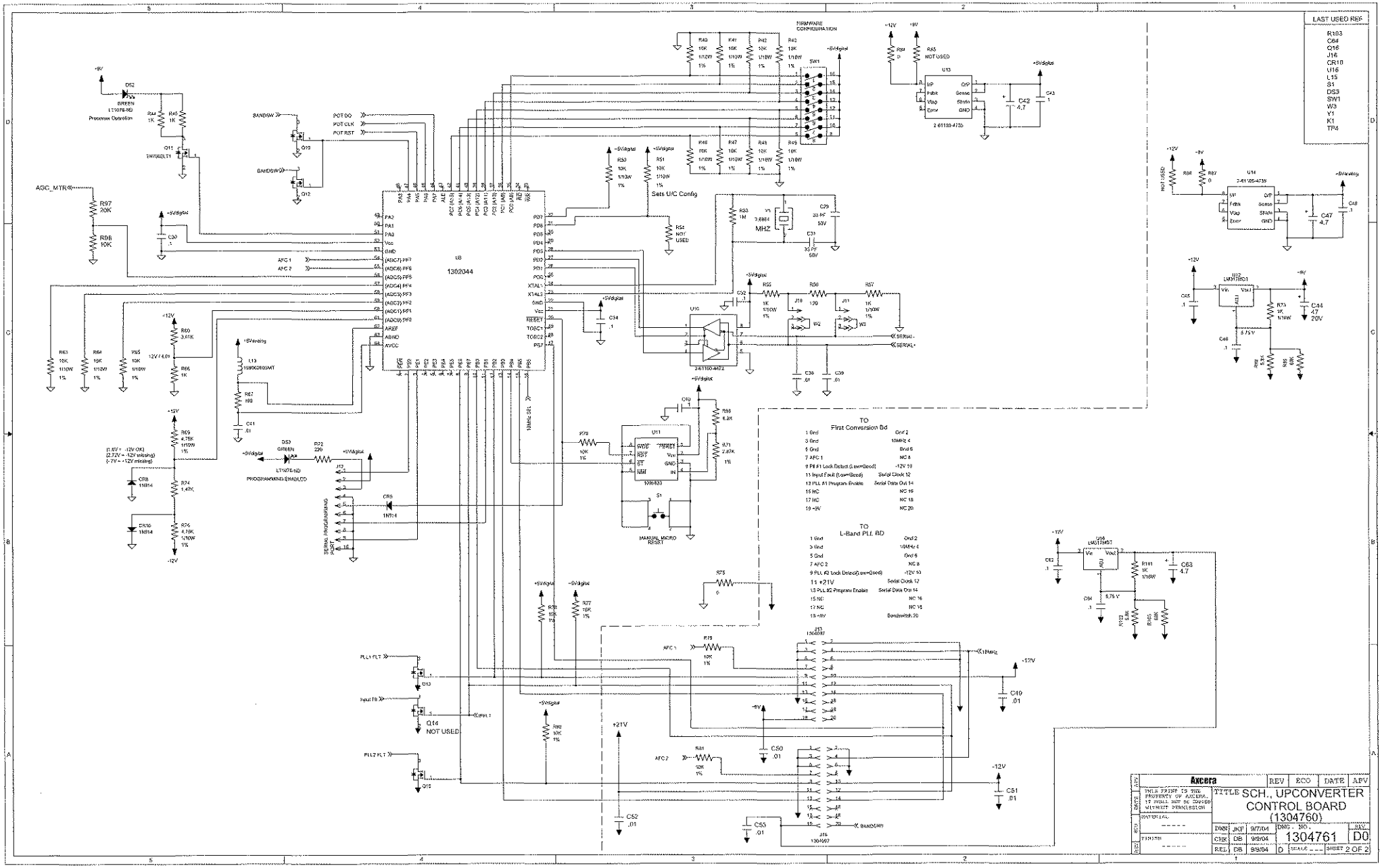
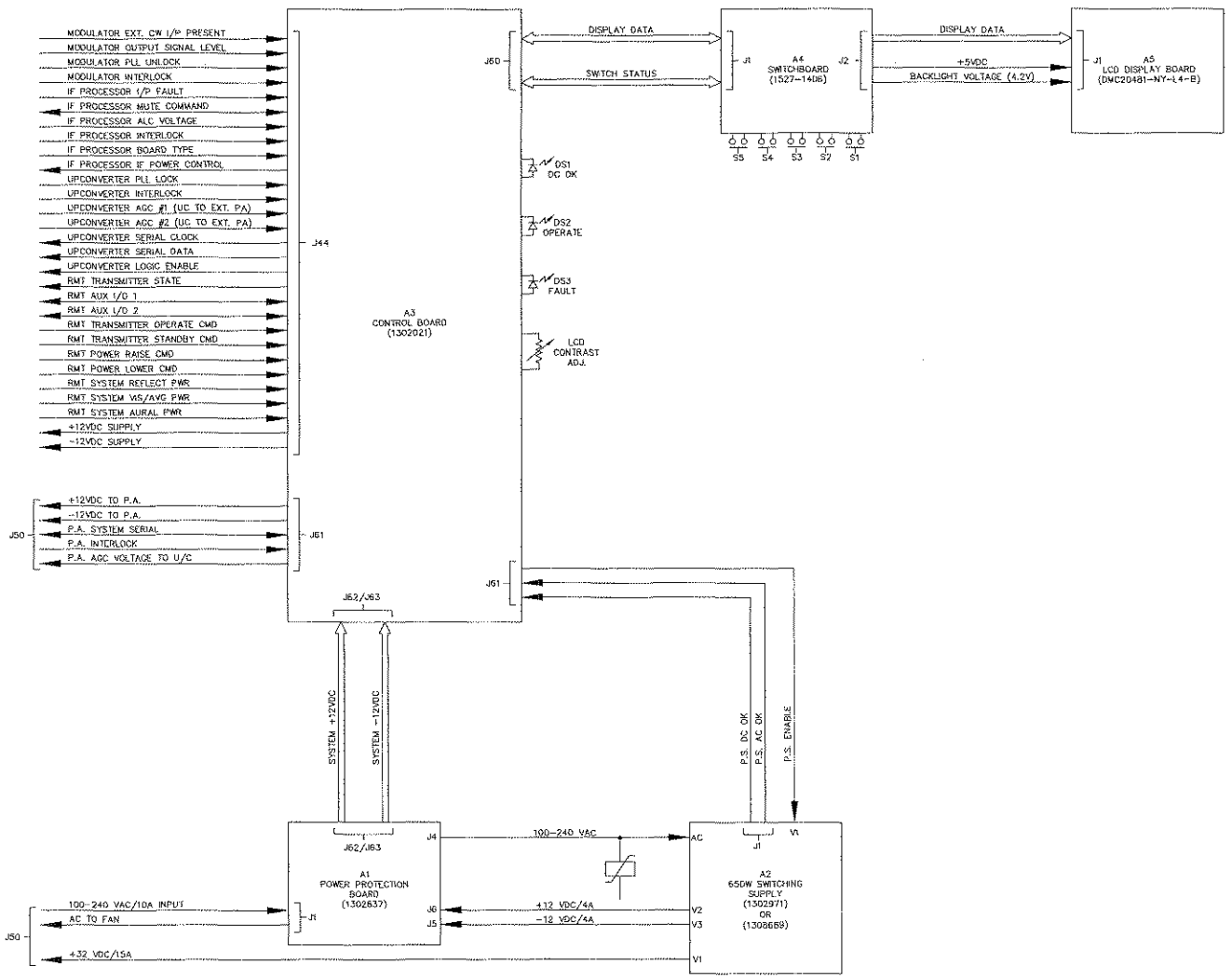
MATERIAL: ------
FINISH: ------
TITLE SCH., UPCONVERTER CONTROL BOARD (1304760)
DWN JKF 9/7/04
CHK DB 9/9/04
REL DB 9/9/04
DWG. NO. 1304761
REV D0
SCALE ---
SHEET 1 OF 2


LAST USED REF
R103
C84
Q16
J16
CR10
U16
L15
S1
DS3
SW1
W3
Y1
K1
TP4
FIRMWARE CONFIGURATION
Sets U/C Config
U8
1302044
TO First Conversion Bd
TO L-Band PLL BD
Axcera
TITLE SCH., UPCONVERTER CONTROL BOARD (1304760)
1304761
D0
SHEET 2 OF 2



REV	ECO	DATE	APV

Axcera.

MATERIAL ----

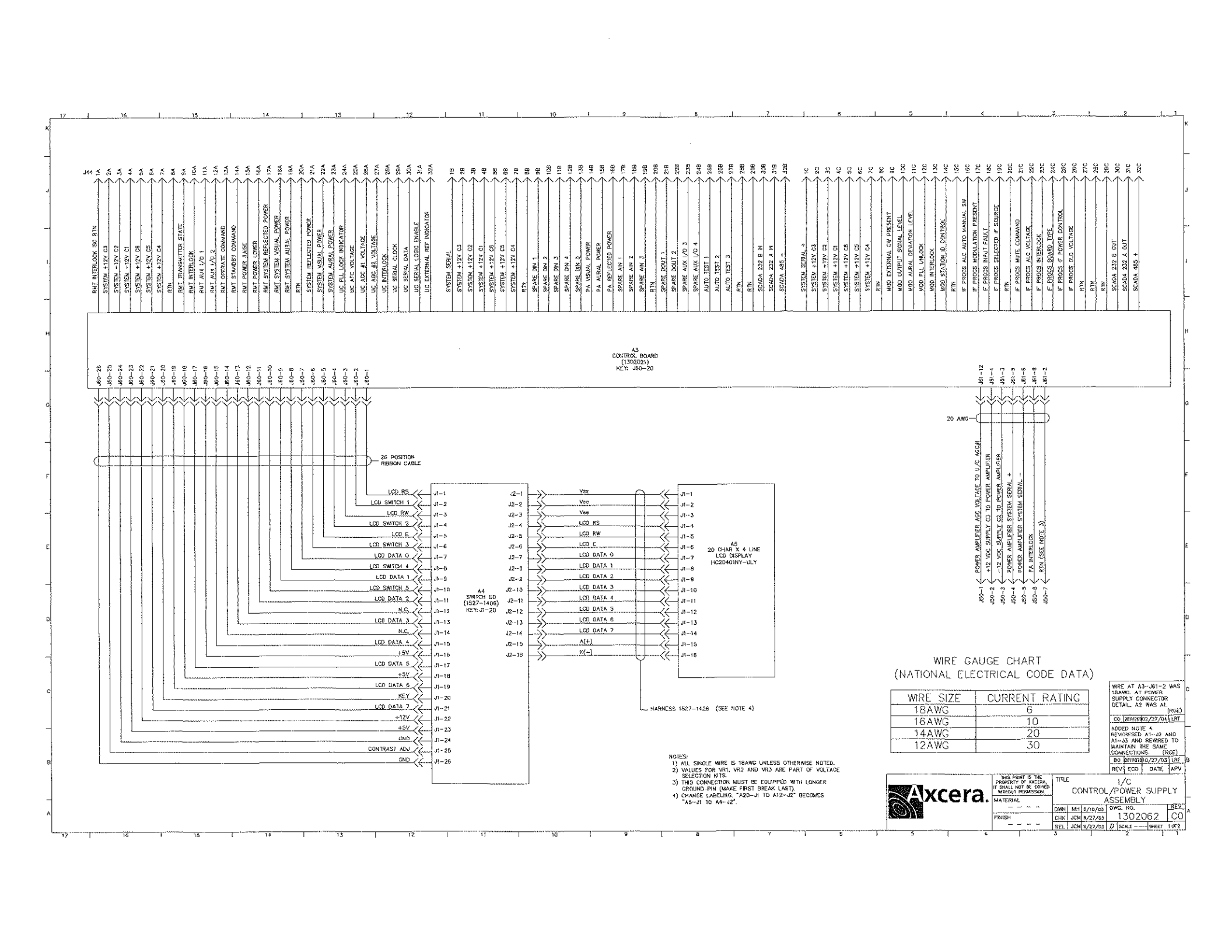
FINISH ----

TITLE: B/D, CONTROL/POWER SUPPLY ASSEMBLY, INNOVATOR LX

DWN	RGE	1/28/04
CHK	JCM	2/2/04
REL	JCM	2/2/04

DWG. NO. 1303889 REV A0

D SCALE --- SHEET 1 OF 1



NOTES:
1) ALL SINGLE WIRE IS 18AWG UNLESS OTHERWISE NOTED.
2) VALUES FOR VR1, VR2 AND VR3 ARE PART OF VOLTAGE SELECTION KITS.
3) THIS CONNECTION MUST BE EQUIPPED WITH LONGER GROUND PIN (MAKE FIRST BREAK LAST).
4) CHANGE LABELING, "A20-J1 TO A12-J2" BECOMES "A5-J1 TO A4-J2".

WIRE GAUGE CHART
(NATIONAL ELECTRICAL CODE DATA)

WIRE SIZE	CURRENT RATING
18AWG	6
16AWG	10
14AWG	20
12AWG	30

WIRE AT A3-J61-2 WAS 18AWG. AT POWER SUPPLY CONNECTOR DETAIL, A2 WAS A1. (RGE)

CO 20112618 02/27/03 LNT

ADDED NOTE 4. REVERSED A1-J2 AND A1-J3 AND REWIRED TO MAINTAIN THE SAME CONNECTIONS. (RGE)

BO 20111078 10/27/03 LNT

REV	ECO	DATE	APV

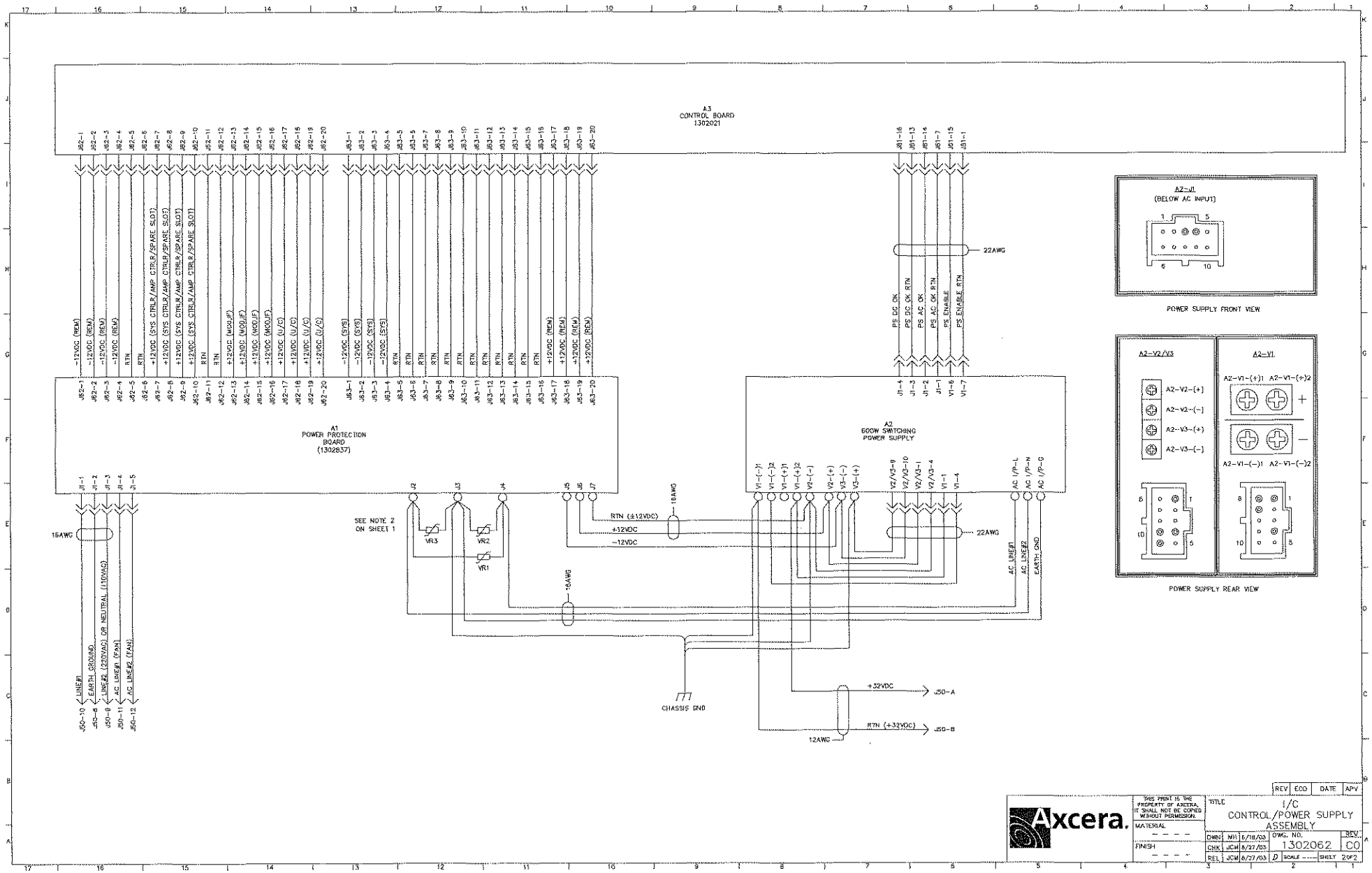
Axcera.

MATERIAL — — —

FINISH — — —

TITLE I/C CONTROL/POWER SUPPLY ASSEMBLY

			DWG. NO.	REV.
DWN	MH	6/18/03	1302062	C0
CHK	JCM	6/27/03		
REL	JCM	6/27/03	D SCALE — — — SHEET 1 OF 2	



REV	ECO	DATE	APV

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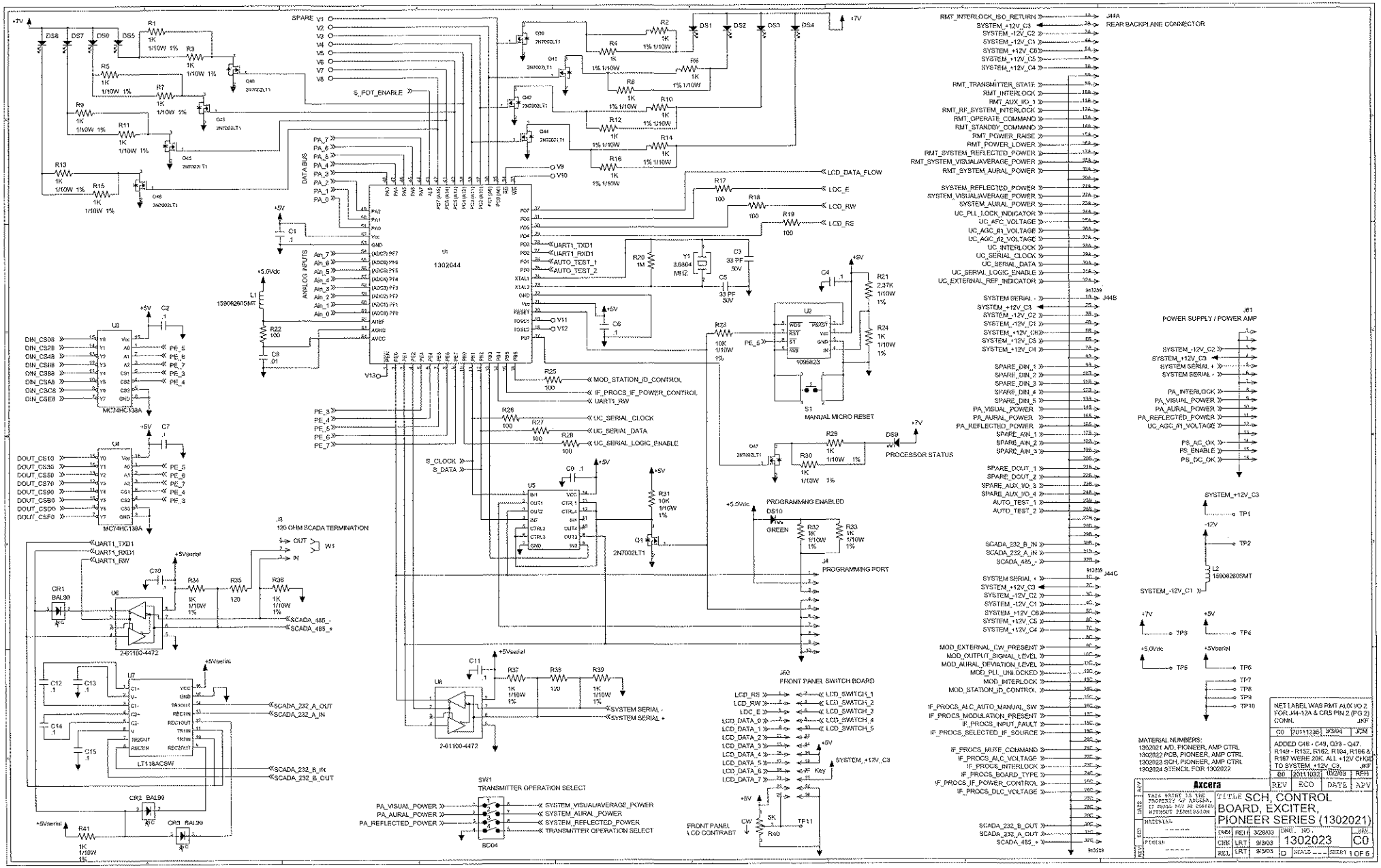
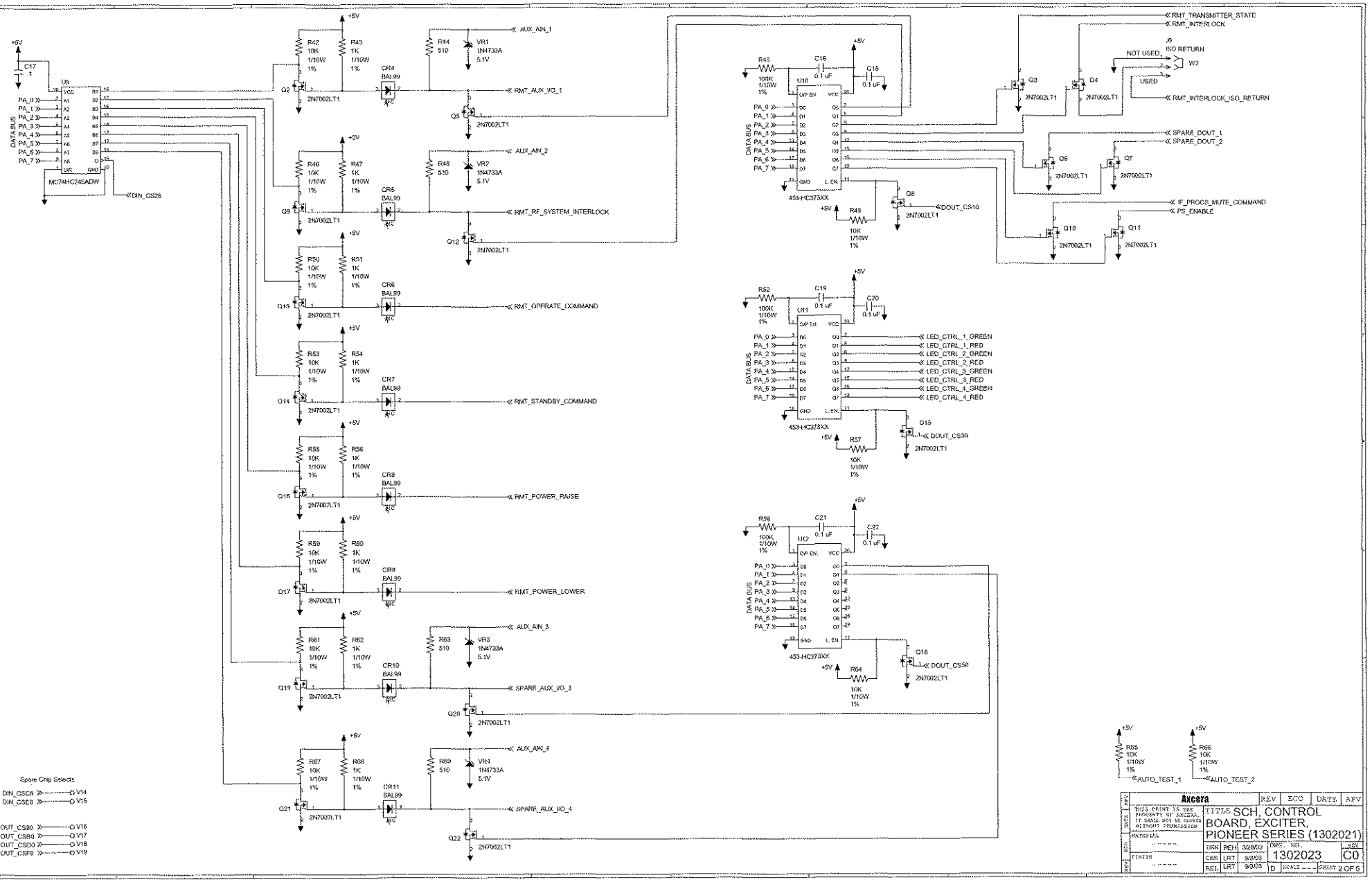
MATERIAL

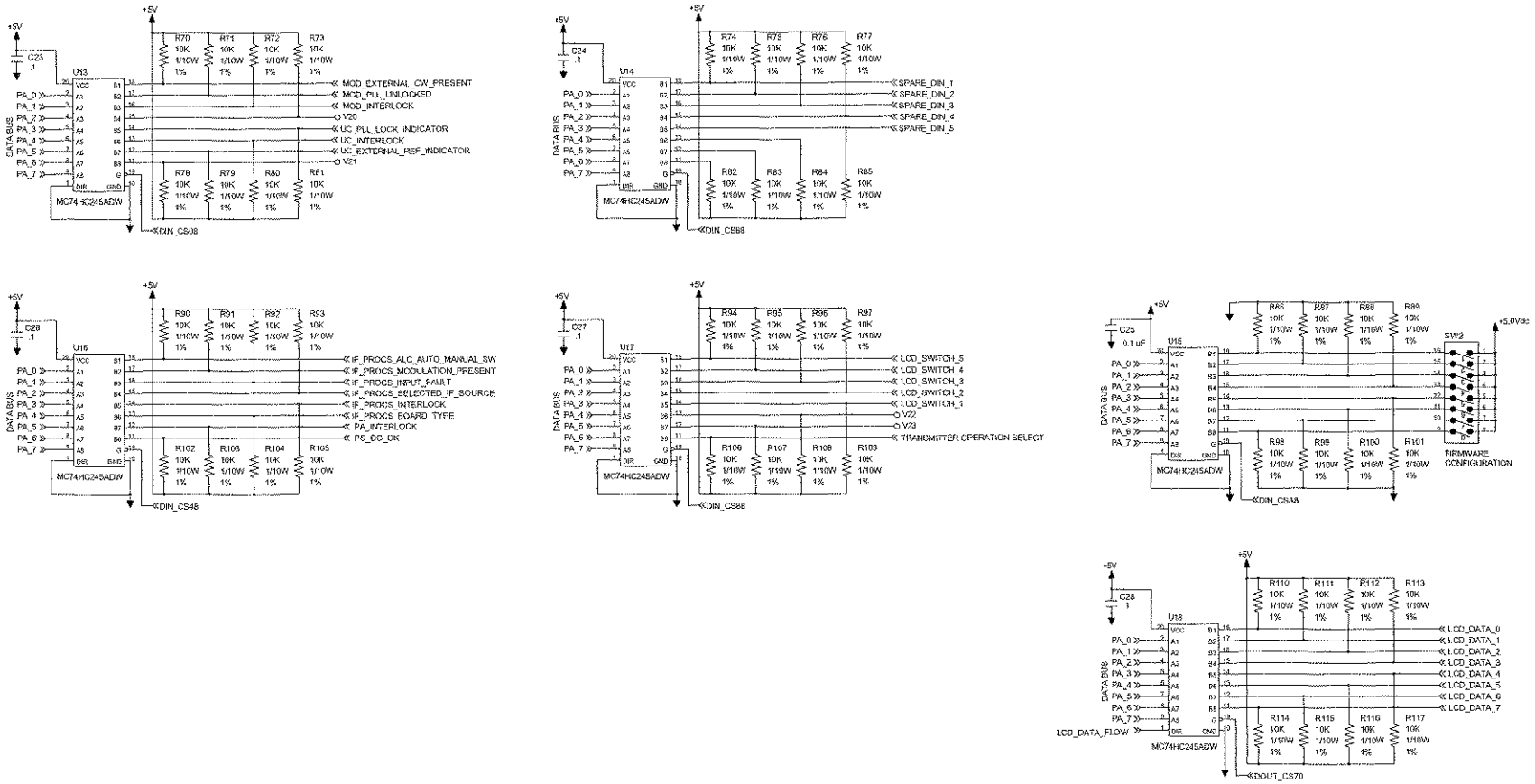
FINISH

TITLE: I/C CONTROL/POWER SUPPLY ASSEMBLY

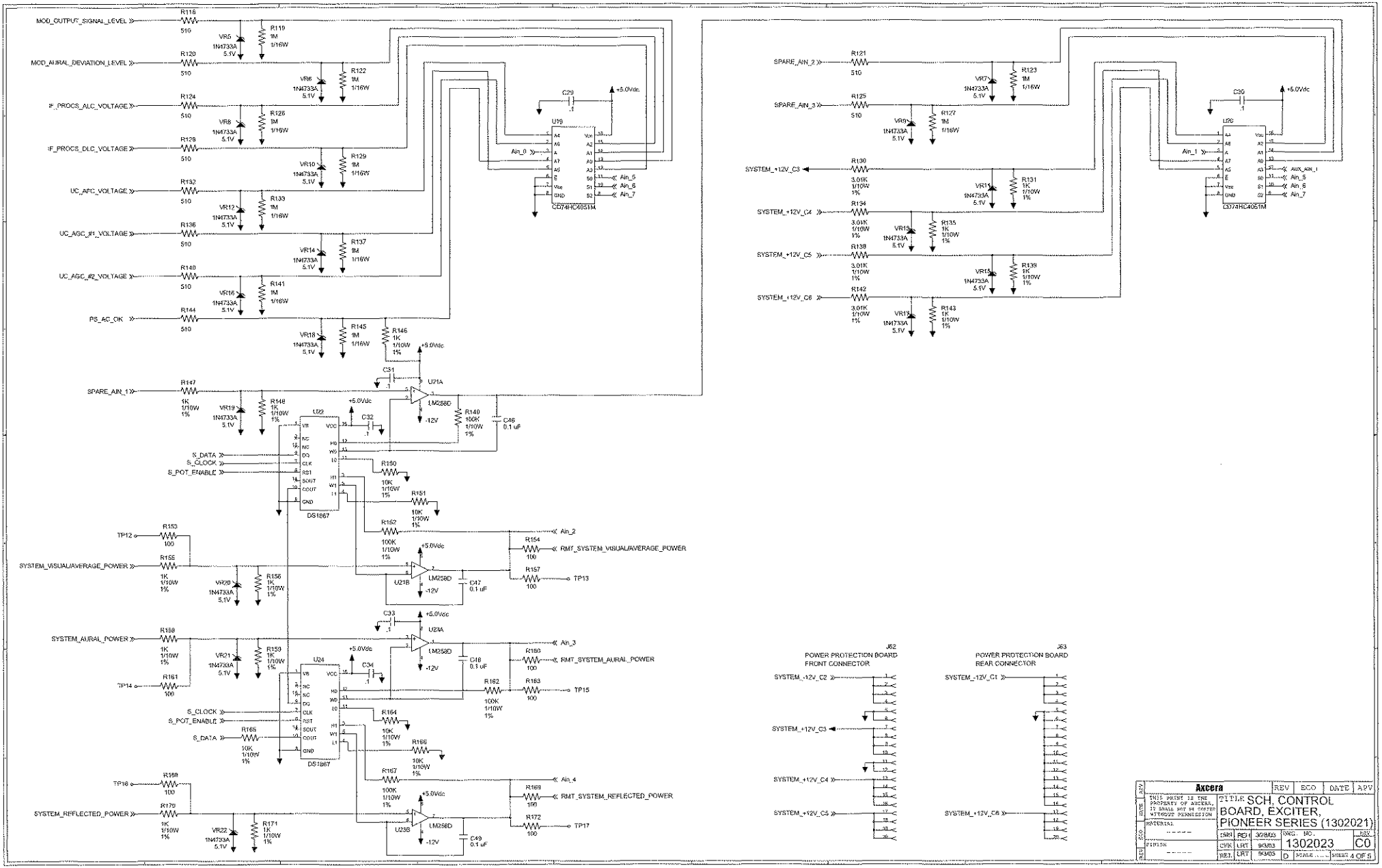
DWN	NH	6/18/03	DWG. NO. 1302062 REV. C0
CHK	JCM	8/27/03	
REL	JCM	8/27/03	D SCALE ---- SHEET 2OF2


J44A
REAR BACKPLANE CONNECTOR
J44B
J44C
J61
POWER SUPPLY / POWER AMP
J4
PROGRAMMING PORT
J3
120 OHM SCADA TERMINATION
J63
FRONT PANEL SWITCH BOARD
U1
1302044
MANUAL MICRO RESET
PROCESSOR STATUS
PROGRAMMING ENABLED
SW1
TRANSMITTER OPERATION SELECT
BD04
FRONT PANEL LCD CONTRAST
MATERIAL NUMBERS:
1302021 A/D, PIONEER, AMP CTRL
1302022 PCB, PIONEER, AMP CTRL
1302023 SCH, PIONEER, AMP CTRL
1302024 STENCIL FOR 1302022
NET LABEL WAS RMT AUX I/O 2 FOR J44-12A & CR8 PIN 2 (PG 2) CONN.
ADDED C48 - C49, Q39 - Q47. R149 - R152, R162, R164, R166 & R167 WERE 20K. ALL +12V CHGD TO SYSTEM_+12V_C3.
Axcera
TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)
DWG. NO. 1302023
REV C0
SCALE ---
SHEET 1 OF 5


+5V
C17
U8
MC74HC245ADW
DATA BUS
PA_0
PA_1
PA_2
PA_3
PA_4
PA_5
PA_6
PA_7
DIN_CS28
R42 10K 1/10W 1%
R43 1K 1/10W 1%
R44 510
VR1 1N4733A 5.1V
AUX_AIN_1
Q2 2N7002LT1
CR4 BAL99
RMT_AUX_I/O_1
Q5 2N7002LT1
R46 10K 1/10W 1%
R47 1K 1/10W 1%
R48 510
VR2 1N4733A 5.1V
AUX_AIN_2
Q9 2N7002LT1
CR5 BAL99
RMT_RF_SYSTEM_INTERLOCK
Q12 2N7002LT1
R50 10K 1/10W 1%
R51 1K 1/10W 1%
Q13 2N7002LT1
CR6 BAL99
RMT_OPERATE_COMMAND
R53 10K 1/10W 1%
R54 1K 1/10W 1%
Q14 2N7002LT1
CR7 BAL99
RMT_STANDBY_COMMAND
R55 10K 1/10W 1%
R56 1K 1/10W 1%
Q16 2N7002LT1
CR8 BAL99
RMT_POWER_RAISE
R59 10K 1/10W 1%
R60 1K 1/10W 1%
Q17 2N7002LT1
CR9 BAL99
RMT_POWER_LOWER
R61 10K 1/10W 1%
R62 1K 1/10W 1%
R63 510
VR3 1N4733A 5.1V
AUX_AIN_3
Q19 2N7002LT1
CR10 BAL99
SPARE_AUX_I/O_3
Q20 2N7002LT1
R67 10K 1/10W 1%
R68 1K 1/10W 1%
R69 510
VR4 1N4733A 5.1V
AUX_AIN_4
Q21 2N7002LT1
CR11 BAL99
SPARE_AUX_I/O_4
Q22 2N7002LT1
R45 100K 1/10W 1%
C16 0.1 uF
C15 0.1 uF
U10
OUT EN.
VCC
GND
L EN.
453-HC373XX
R49 10K 1/10W 1%
Q8 2N7002LT1
DOUT_CS10
Q3 2N7002LT1
Q4 2N7002LT1
Q6 2N7002LT1
Q7 2N7002LT1
Q10 2N7002LT1
Q11 2N7002LT1
RMT_TRANSMITTER_STATE
RMT_INTERLOCK
J5
ISO RETURN
NOT USED
W2
USED
RMT_INTERLOCK_ISO_RETURN
SPARE_DOUT_1
SPARE_DOUT_2
IF_PROCS_MUTE_COMMAND
PS_ENABLE
R52 100K 1/10W 1%
C19 0.1 uF
C20 0.1 uF
U11
LED_CTRL_1_GREEN
LED_CTRL_1_RED
LED_CTRL_2_GREEN
LED_CTRL_2_RED
LED_CTRL_3_GREEN
LED_CTRL_3_RED
LED_CTRL_4_GREEN
LED_CTRL_4_RED
R57 10K 1/10W 1%
Q15 2N7002LT1
DOUT_CS30
R58 100K 1/10W 1%
C21 0.1 uF
C22 0.1 uF
U12
R64 10K 1/10W 1%
Q18 2N7002LT1
DOUT_CS50
R65 10K 1/10W 1%
AUTO_TEST_1
R66 10K 1/10W 1%
AUTO_TEST_2
Spare Chip Selects
DIN_CS26
DIN_CS27
DOUT_CS60
DOUT_CS80
DOUT_CSD0
DOUT_CSF0
Axcera
REV
ECO
DATE
APV
THIS PRINT IS THE PROPERTY OF AXCERA. IT SHALL NOT BE COPIED WITHOUT PERMISSION
MATERIAL
FINISH
TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)
DRN REH 3/28/03
CHK LRT 9/3/03
REL LRT 9/3/03
DWG. NO. 1302023
REV C0
SCALE ---
SHEET 2 OF 5

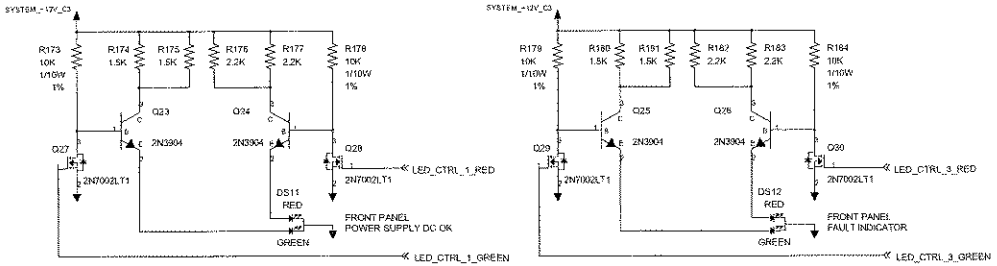


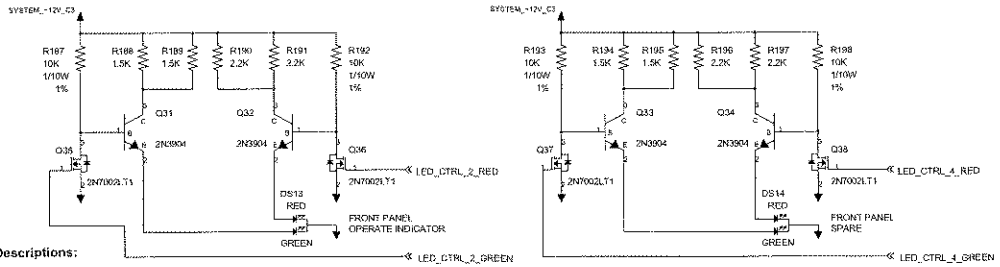
	Axcera	REV	ECO	DATE	APP
	THIS SHEET IS THE PROPERTY OF AXCERA. IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE: SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)			
	MATERIAL: ----	DRN REH 3/28/03	DWG. NO. 1302023		REV C0
	FINISH: ----	CHK LRT 9/3/03			
		APP LRT 9/3/03	D	SCALE: ----	SHEET 3 OF 5

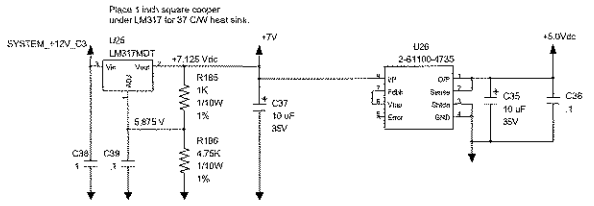

MOD_OUTPUT_SIGNAL_LEVEL
MOD_AURAL_DEVIATION_LEVEL
IF_PROCS_ALC_VOLTAGE
IF_PROCS_DLC_VOLTAGE
UC_APC_VOLTAGE
UC_AGC_#1_VOLTAGE
UC_AGC_#2_VOLTAGE
PS_AC_OK
SPARE_AIN_1
SPARE_AIN_2
SPARE_AIN_3
SYSTEM_+12V_C3
SYSTEM_+12V_C4
SYSTEM_+12V_C5
SYSTEM_+12V_C6
SYSTEM_VISUAL/AVERAGE_POWER
SYSTEM_AURAL_POWER
SYSTEM_REFLECTED_POWER
S_DATA
S_CLOCK
S_POT_ENABLE
+5.0Vdc
-12V
CD74HC4051M
DS1867
LM258D
Ain_0
Ain_1
Ain_2
Ain_3
Ain_4
Ain_5
Ain_6
Ain_7
AUX_AIN_1
RMT_SYSTEM_VISUAL/AVERAGE_POWER
RMT_SYSTEM_AURAL_POWER
RMT_SYSTEM_REFLECTED_POWER
J62
POWER PROTECTION BOARD
FRONT CONNECTOR
J63
POWER PROTECTION BOARD
REAR CONNECTOR
Axcera
TITLE: SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)
DWG. NO. 1302023
REV C0
SHEET 4 OF 5

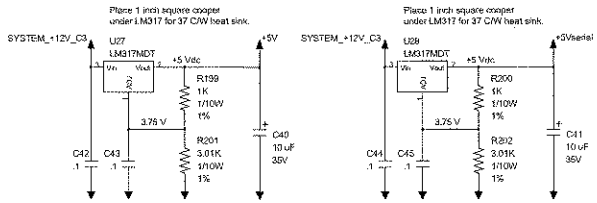
LAST USED REF.

R202
C49
Q47
DS14
U28
VR22
J63
TP17
V23
SW2
CR11
W21
Y1
L2
S1









Circuit Descriptions:

PAGE 1:

U1 is an Atmel Atmega128 microcontroller. This part is in-circuit programmed using the serial programming port. When the microcontroller is held in reset by either the programming port or the external watchdog IC, a transistor inverts the reset signal while serial programming lines are connected to U1 through analog switch U5.

U2 is a watchdog IC used to hold the microcontroller in reset if the supply voltage is less than 4.21 Vdc; (1.25 Vdc < Pin 4 (IN) < Pin 2 (Vcc)). The watchdog momentarily resets the microcontroller if Pin 6 (!ST) is not clocked every second. A manual reset switch is provided but should not be needed.

Diodes DS1 through DS8 are used for display of auto test results. A test board is used to execute self test routines. When the test board is installed, Auto_Test_1 is held low and Auto_Test_2 is allowed to float at 5 Vdc. This is the signal to start the auto test routines.

U3 and U4 are used to selectively enable various input and output ICs found on page 2 and 3 of the schematic.

U1 has two serial ports available. In this application, one port is used to communicate with transmitter system components where U1 is the master of a RS-485 serial bus. The other serial port is used to provide serial data I/O where U1 is not the master of the data port. A dual RS-232 port driver IC and a RS-485 port driver is also in the second serial data I/O system. The serial ports are wired such that serial data input can come through one of the three serial port channels. Data output is sent out through each of the three serial port channels.

Switch SW1 is used to select either transmitter operation or exciter driver operation. When the switches of SW1 are on, transmitter operation is selected and the power monitoring lines of the transmitter's power amplifier are routed to the system power monitoring lines.

PAGE 2:

Digital output latches are used to control system devices. Remote output circuits are implemented using open drain FETs with greater than 60 Volt drain to source voltage ratings.

Remote digital inputs are diode protected with a 1 Kohm pull-up resistor to 5Vdc. If the remote input voltage is greater than about 2 volts or floating, a FET is turned on and a logic low is applied to the digital input buffer. If the remote input voltage is less than the turn on threshold of the FET (about 2 Vdc), a logic high is applied to the digital input buffer.

Four of the circuits on page two are auxiliary I/O connections wired for future use. They are wired similar to the remote digital inputs but include a FET for digital output operation. To operate these signals as an input, the associated output FET must be turned off. These circuits are also connected to an analog input multiplexer IC.

PAGE 3:

Several ICs are used as input buffers to allow the microcontroller to monitor various digital input values. Most digital inputs use a 10 Kohm pull-up resistor. The buffer IC used for data transfer to the display is wired for read and write control.

PAGE 4:

Each analog input is expected to be between 0 and 5 Vdc. If a signal exceeds 5.1 Vdc, a 0.225 Watt zenor diode clamps the signals voltage. Most signals are calibrated at their source however two dual serial potentiometer ICs are used to calibrate four signals. For these four circuits, the input value is divided in half before it is applied to an op-amp. The serial potentiometer is used to adjust the input signal between 80 and 120% of the input signal. Serial data to the second serial potentiometer is transferred through the first IC. The wiper position of the digital potentiometer circuit is used to set the gain of the op-amp. Lower digital values for the wiper setting increases the gain of the op-amp. If N= 0, gain = 6.0. If N = 255, gain = 3.00. If Vin = 1.0 at spare_Ain_1 and N = 128, U21A out = 4.0V with gain = 4.

Two 20 position connectors are used to provide power to the backplane. J62 and J63 get power from the power supply after a nominal 3 amp resettable fuse. The Raychem polyswitch resettable fuses may open on a current as low as 2.43 amps at 50C. 3 amps at 25 C or 3.3 amps at 0C. They definately will open when the current is 4.86 amps at 50C, 6 amps at 25C, or 6.6 amps at 0C. Trace widths of these circuits are 0.140" (designed for maximum current).

PAGE 5:

Each of the four LED circuits drive a dual element common cathode LED. To make a good amber color, the current applied to the green element is slightly greater than the red element.

Several voltage regulators are used to power the board. Seven volts is typically applied to board LEDs and to the input of a precision 5.0 volt regulator. The 5.0 volt regulator is used for analog circuits and the microcontroller analog reference voltage. Another two 5 volt regulator circuits are used for most other board circuits.

Axcera		REV	ECO	DATE	APV
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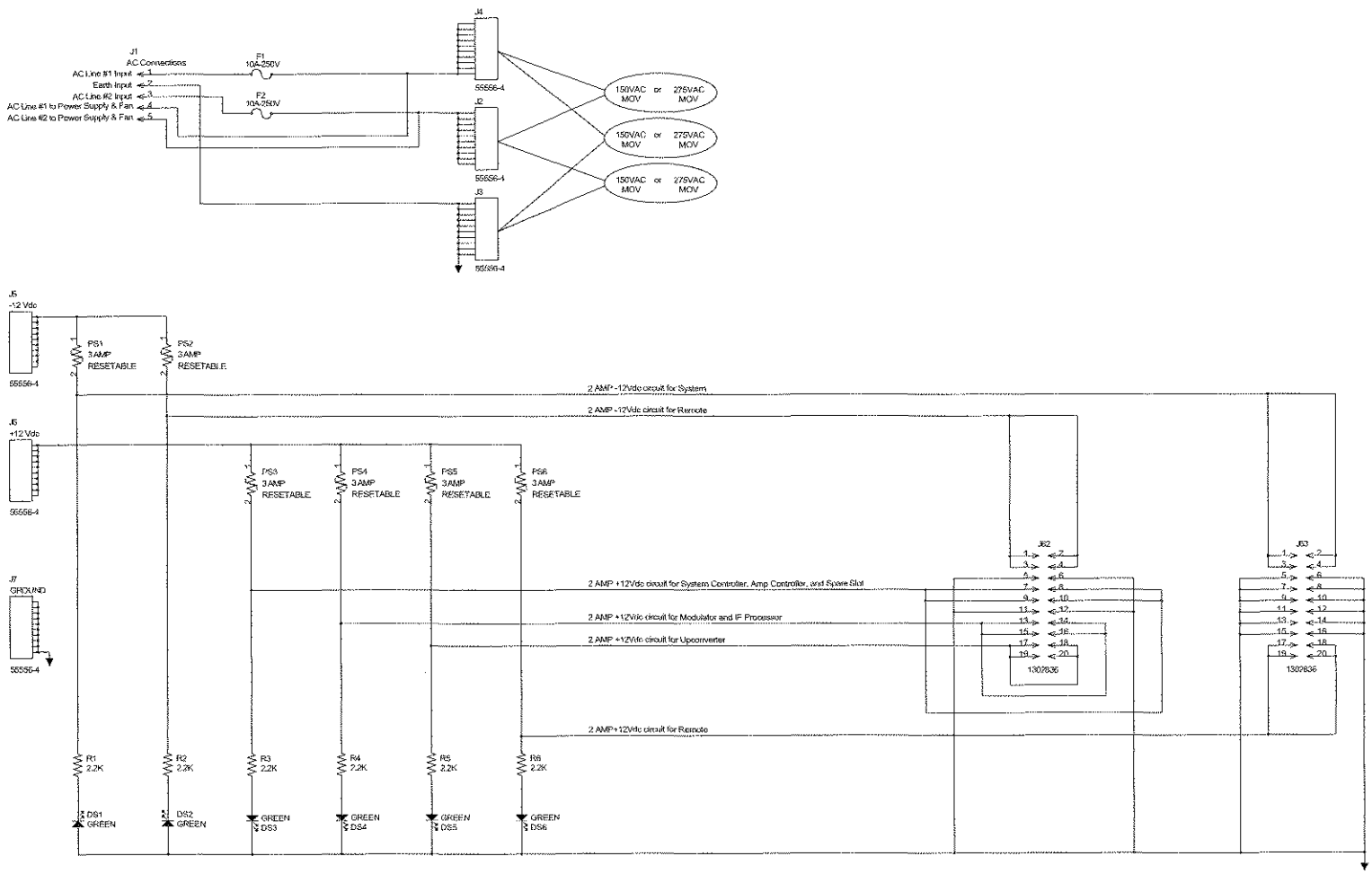
MATERIAL					
FINISH					

TITLE: SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)

DWN	RSH	3/28/03	DWG. NO.	REV
CHK	LRT	9/3/03	1302023	C0
APL	LRT	9/3/03	ID	SHEET 5 OF 5



Circuit Design Notes:

1. Track widths of 0.140 inch minimum top and bottom of board shall be used to connections to J1, J2, J3, J4.
2. Track widths of 0.140 inch minimum top of board shall be used to connections to J5 and J6.
3. Track widths of 0.065 inch minimum shall be used to connections to J62 and J63.
4. Track widths of 0.020 inch minimum shall be used to connections between LEDs and resistors.
5. Board BOM needs the following items added to those exported from Orcad:

Part Number	Qty	Description
102071	4	Fuse Clip, PC BD Mnt., 15 Amp

MATERIAL NUMBERS:
1302837 PIONEER, POWER PROTECTION
1302838 PCB, PIONEER, PWR PROTECT
1302839 SCH, PIONEER, PWR PROTECT
1302840 STENCIL FOR 1302838

Axcera		REV	ECO	DATE	APV
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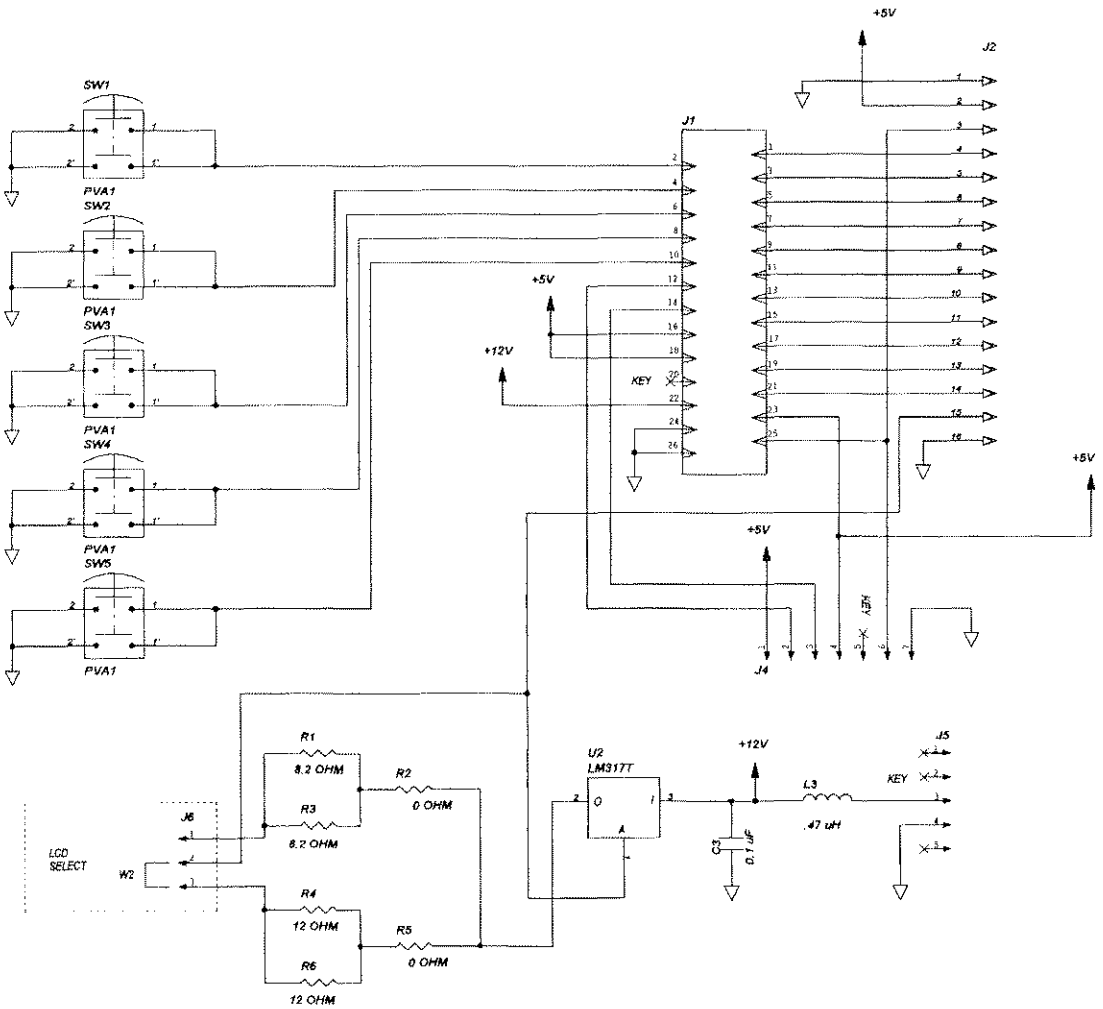
MATERIAL: -----					
FINISH: -----					

TITLE: SCH, PIONEER, PWR PROTECT (1302837)

DWN	REH	5/29/03	DWG. NO.	REV.
CHK	REH	5/29/03	1302839	AO
ENG.	REH	5/29/03	D SCALE: -----	SHEET 1 OF 1



REV	ECN	DATE	APV
	DELETED C1, C2, L1, L2, U1, J3, & W1. MOVED W2 FROM J6-1,-2 TO J6 -2,-3.		JKF
3	8603	11/7/96	
	AT J2 W2 WAS W1. (TMY)		
2	8424	9/29/96	JCM
	SWITCHED PINS 1 & 2 OF U2 (TMY)		
1	8368	8/27/96	RAS

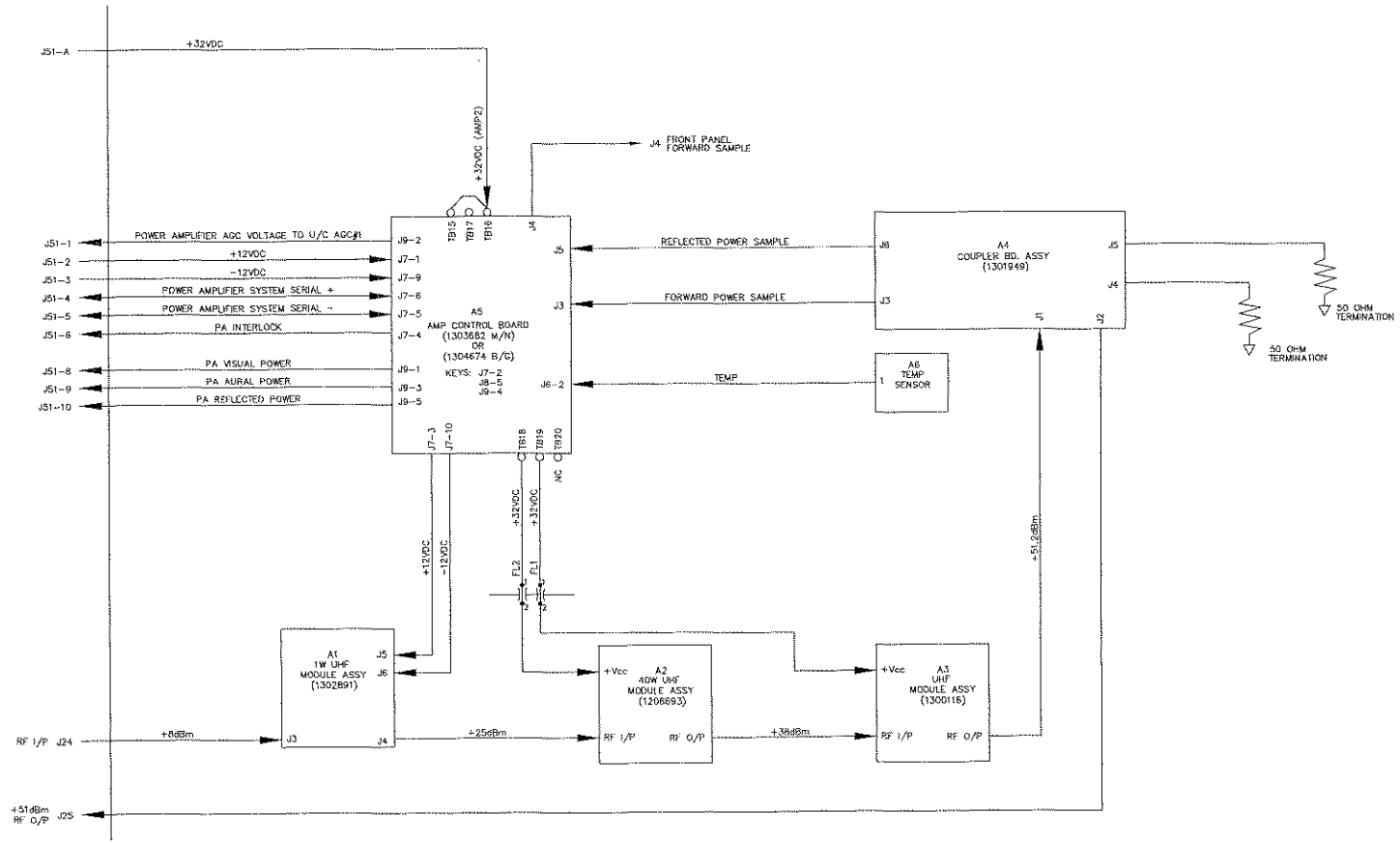
ITS CORPORATION

MATERIAL ---

FINISH ---

TITLE SCHEMATIC SWITCH BOARD (1527-1406)

			DWG. NO.	REV
DWN	DLM	6/3/96	1527-3406	3
CHK	RAS	6/14/96		
REL	RAS	6/14/96	B SCALE ---	SHEET 1 OF 1



NOTE:
1. ALL POWER LEVELS ARE PK-SYNC +10% AURAL. FOR DTV LEVELS, SUBTRACT 3dBm.

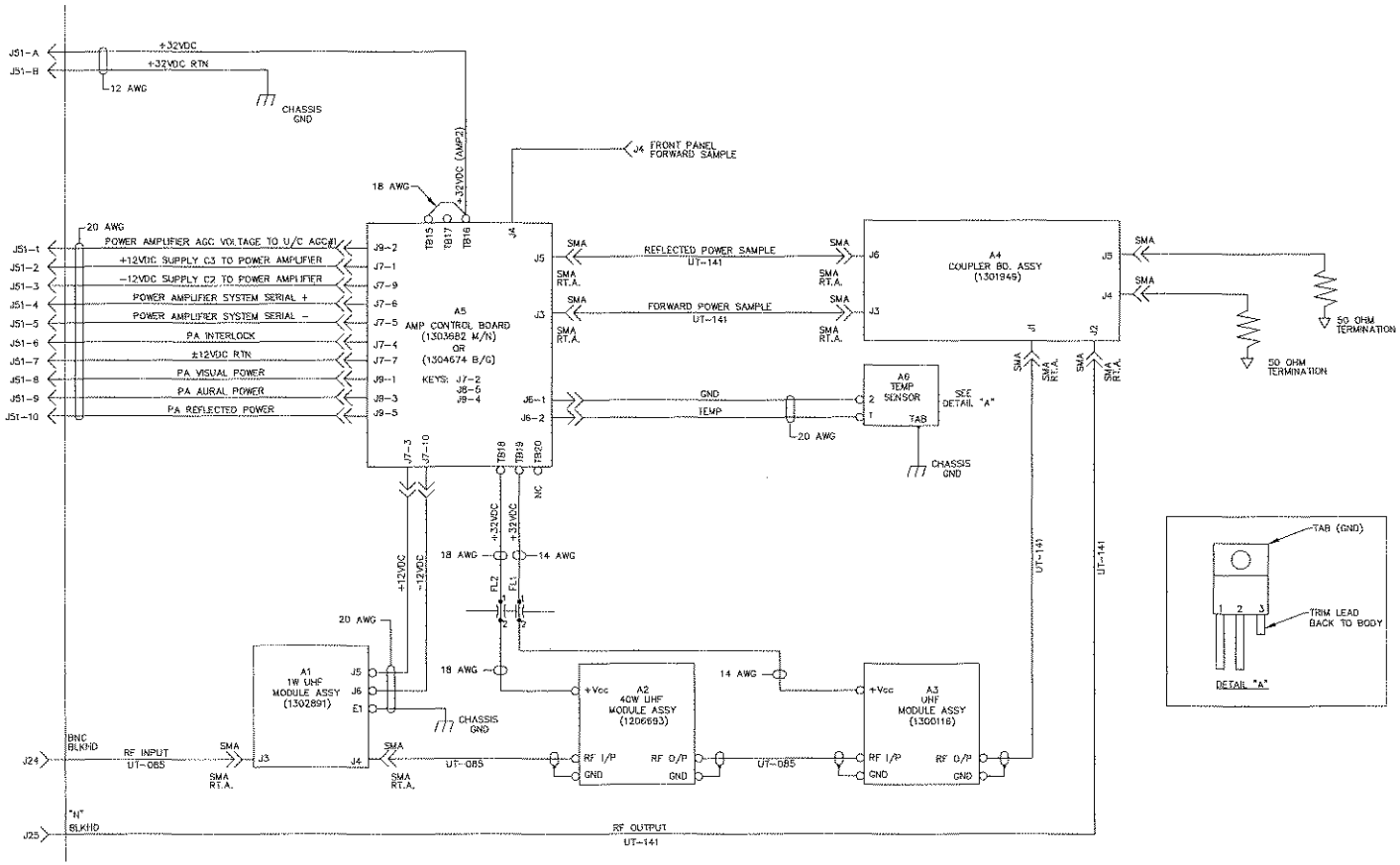
REV	ECO	DATE	APV
A5 WAS 1301982. (RGE)			
C0	20111306h	3/15/04	RCH
AT A4, REVERSED J3 AND J6. (RGE)			
B0	20111248	5/7/04	LRT

MATERIAL ----

FINISH ----

TITLE
B/D
PA ASSEMBLY, 100W
LX SERIES

DWN	RGE	01/16/04	DWG. NO. 1303850 REV C0
CHK	LRT	1/16/04	
REL	LRT	1/16/04	D SCALE ---- SHEET 1 OF 1



NOTE:
1. ALL WIRE IS 18AWG UNLESS OTHERWISE NOTED.

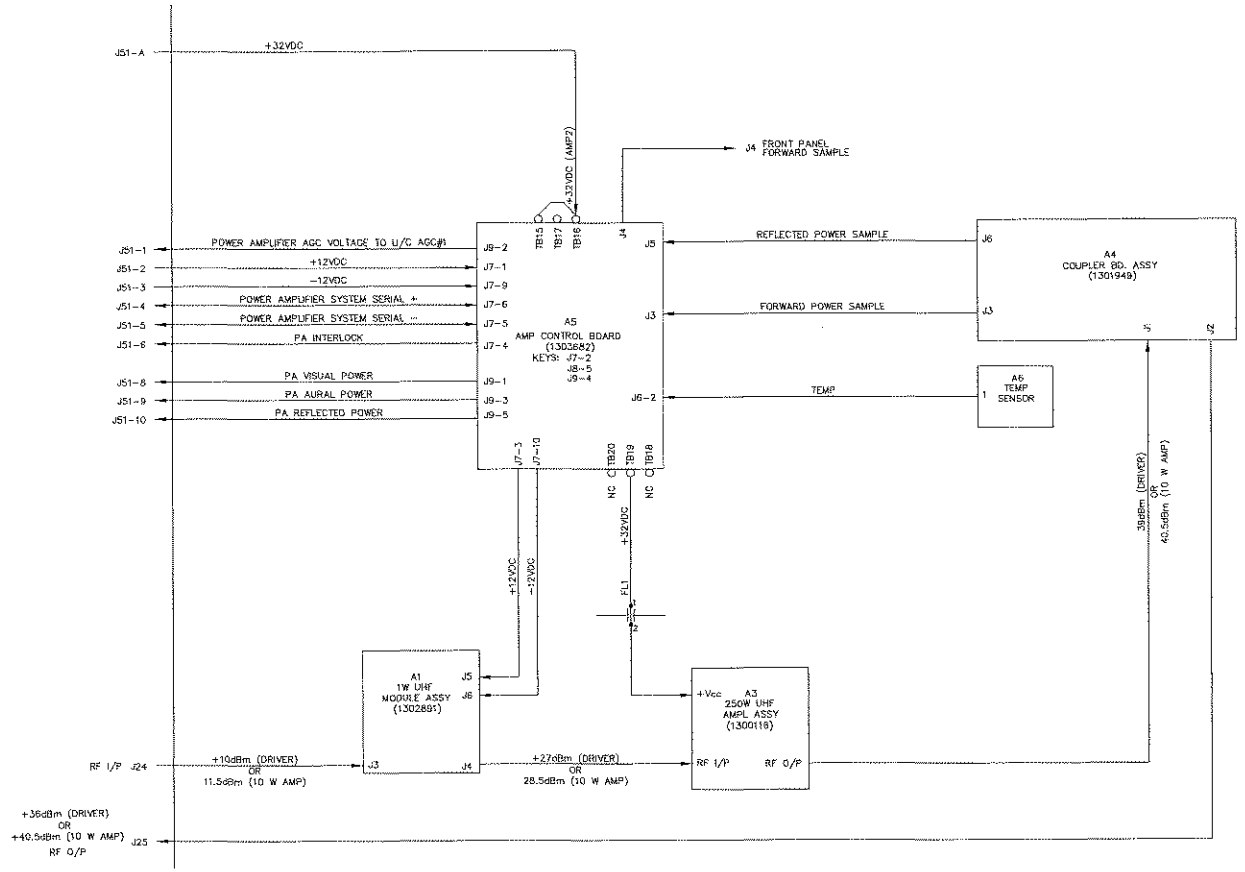
A5 WAS 1301902. (RGE)			
CO. 20111358	2/15/04	REH	
AT A4, REVERSED J5 AND J6. WIRE AT A5-J7-7 WAS 18 AWG. (RGE)			
B0 20111243	5/7/04	LRT	B
REV ECO	DATE	APV	

MATERIAL: ---

FINISH: ---

TITLE: I/C, PA ASSEMBLY, 100W LX SERIES

DWN	RGE	01/13/04	DWG. NO. 1303814 REV. C0
CHK	LRT	1/16/04	
REL	LRT	1/16/04	D SCALE --- SHEET 1 OF 1



NOTE:
1. ALL POWER LEVELS ARE PK-SYNC +10% AURAL FOR DTV LEVELS, SUBTRACT 3dBm.

REV	ECO	DATE	APV
B0	2201247	3/1/05	LRT

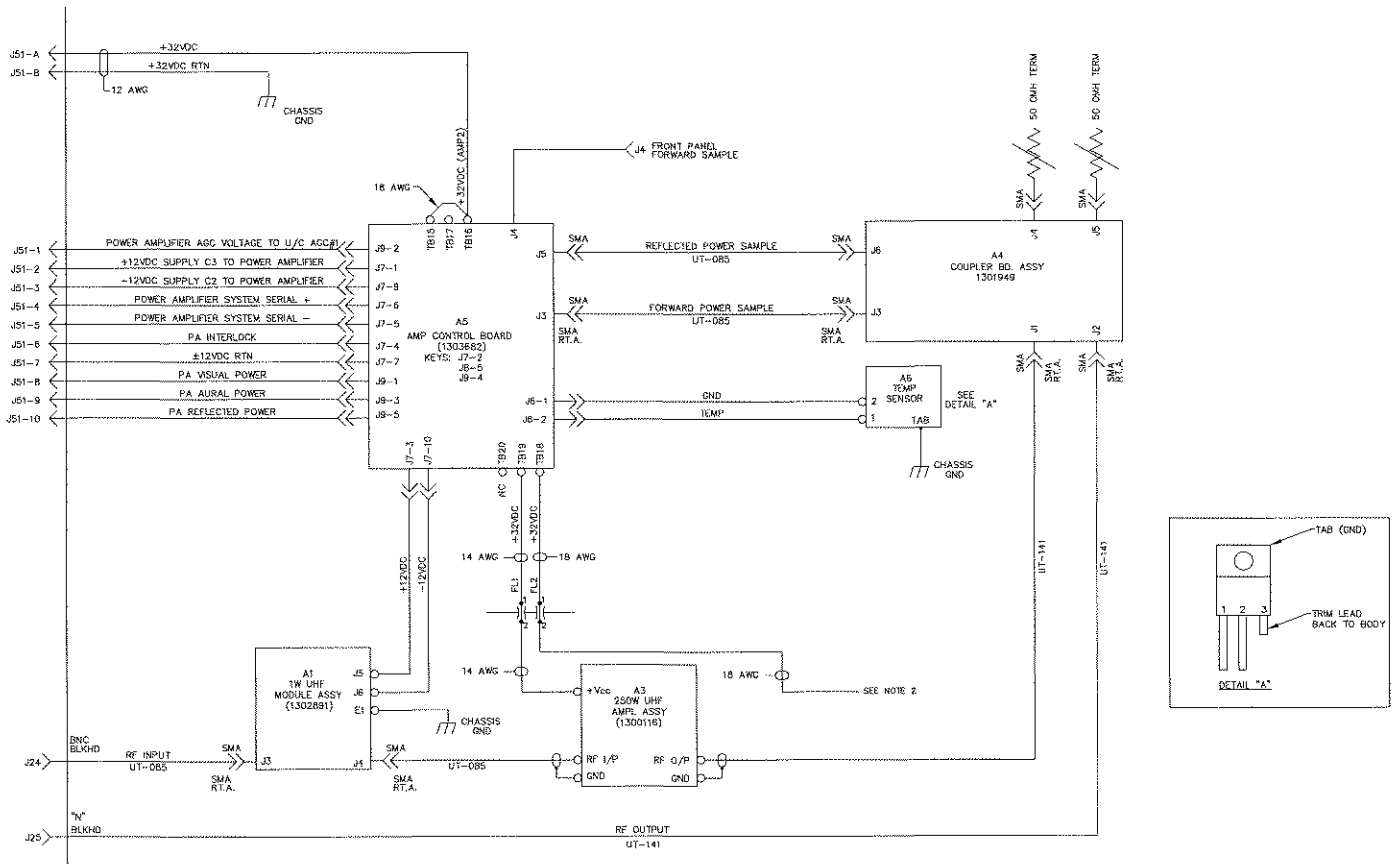
A4 WAS 1227-1316
ADDED REFLECTED SAMPLE FROM A4-J6 TO A5-J5.
ADDED AMPLIFIER POWER LEVELS. (SAK)

MATERIAL ——

FINISH ——

TITLE
B/D
PA ASSEMBLY, 2KW DRIVER/
10 W PA, LX SERIES

DWN	RCE	11/17/04	DWG. NO. 1305138 REV B0
CHK	LRT	11/18/04	
REL	LRT	11/18/04	D SCALE ---- SHEET 1 OF 1



NOTE:
1. ALL WIRE IS 20AWG UNLESS OTHERWISE NOTED.
2. THIS WIRE IS NOT USED ON THIS ASSEMBLY. COVER THE END WITH HEAT SHRINKABLE TUBING AND TIE BACK IN THE HARNESS.

REV	ECO	DATE	APV
A4 WAS 1227-1316. ADDED COAX FROM A4-J6 TO A5-J5. ADDED 50 OHM TERMINATIONS AT A4. (SAK)	C0	20111264	3/1/05	LRT
DELETED 50 OHM TERMINATION AT A5-J5. (RGE)	B0	20111266	05/05/03	LRT

MATERIAL ———

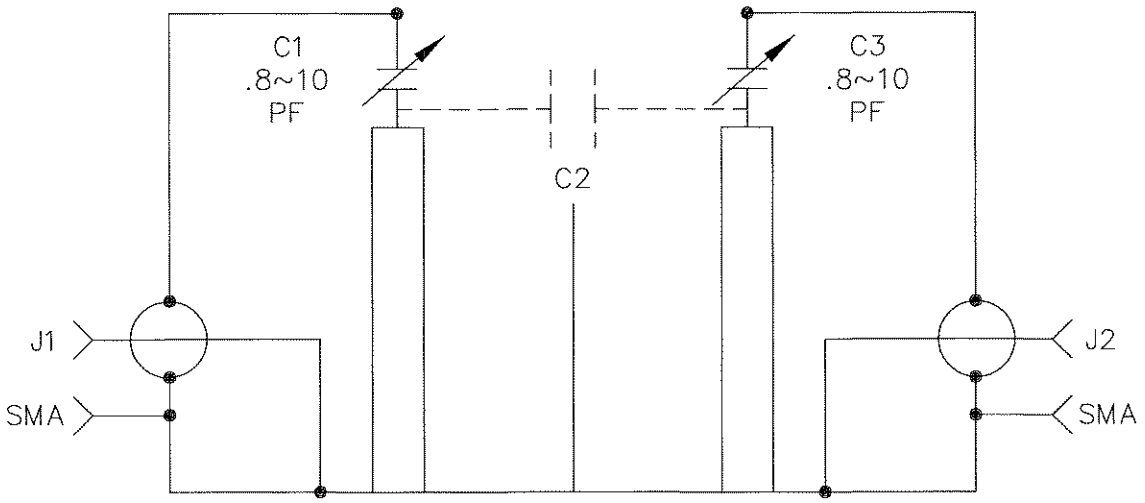
FINISH ———

TITLE: I/C, PA ASSEMBLY, 2KW DRIVER/ 10 W PA, LX SERIES

DWN	RGE	11/17/04
CHK	LRT	11/18/04
REL	LRT	11/18/04

DWG. NO. 1305137 REV C0

SCALE ——— SHEET 1 OF 1



NOTE: C2 IS STRAY CAPACITANCE BETWEEN LINE SECTIONS.

REV	ECO	DATE	APV

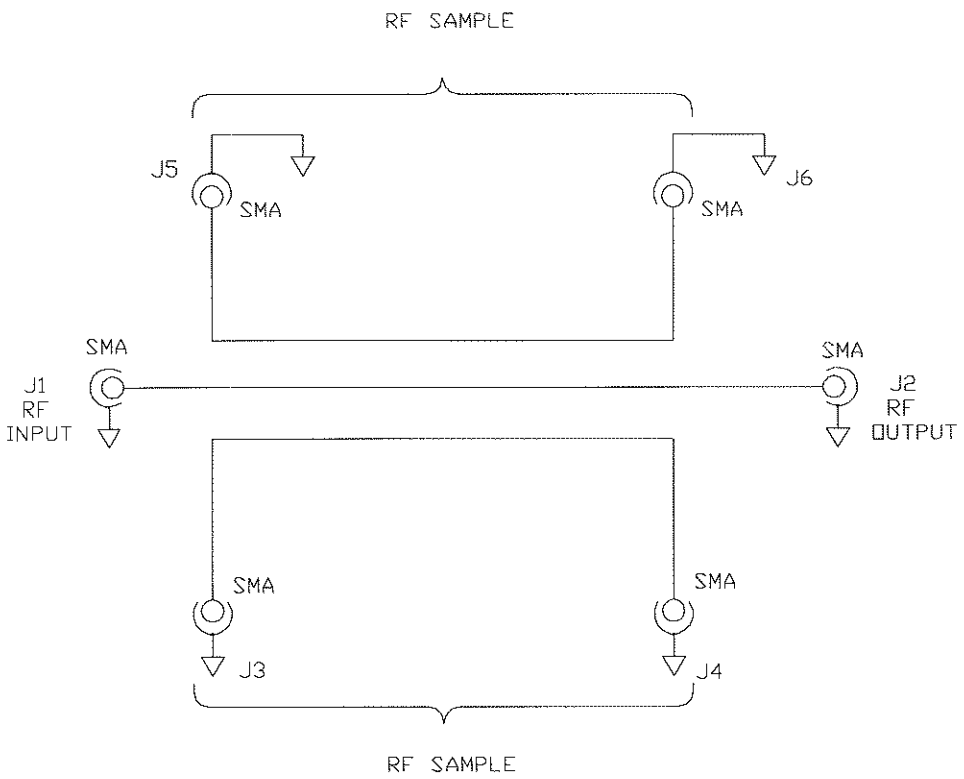
Axcera®

MATERIAL — — — —

FINISH — — — —

TITLE: SCHEMATIC — UHF FILTER

DWN	DD	9/13/83	DWG. NO. 1007-3101	REV 0
CHK	RWZ	9/13/83		
REL	RWZ	7/20/90	A SCALE — —	SHEET 1 OF 1



REV	ECO	DATE	APV

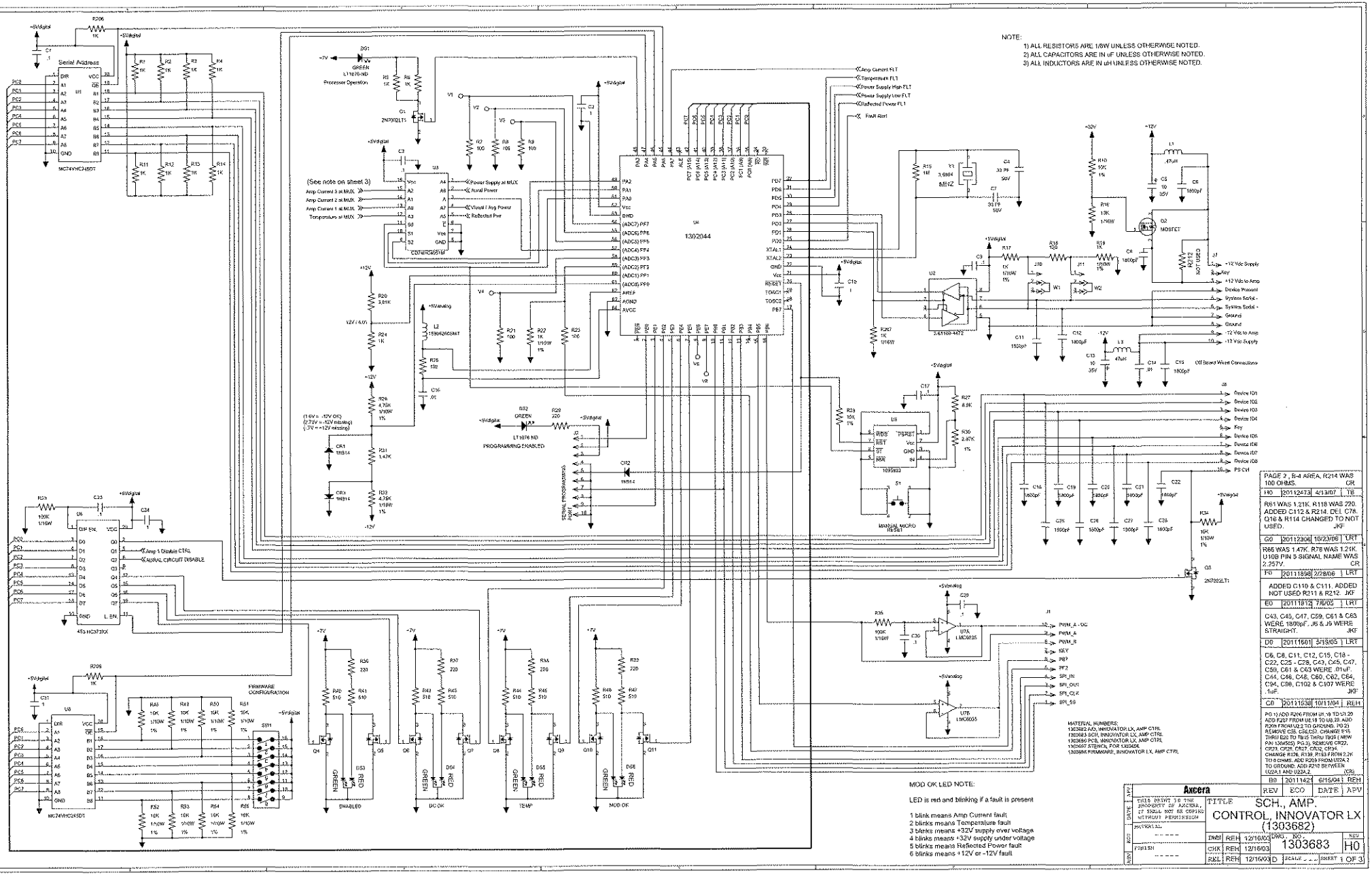
Axcera

MATERIAL — — — —

FINISH — — — —

TITLE: SCHEMATIC DIRECTIONAL COUPLER BOARD

DWN	MH	8/11/03	DWG. NO. 1303152	REV A0
CHK	JCM	8/25/03		
REL	JCM	8/25/03	B SCALE ---	SHEET 1OF1


NOTE:
1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.
Serial Address
MC74VHC245DT
(See note on sheet 3)
Power Supply at MUX
Aural Power
Visual / Avg Power
Reflected Pwr
Amp Current 3 at MUX
Amp Current 2 at MUX
Amp Current 1 at MUX
Temperature at MUX
1302044
Amp Current FLT
Temperature FLT
Power Supply High FLT
Power Supply Low FLT
Reflected Power FLT
Fault Alert
2.61152-4212
Device ID1
Device ID2
Device ID3
Device ID4
Key
Device ID5
Device ID6
Device ID7
Device ID8
PS CH
LT1076 ND
PROGRAMMING ENABLED
MANUAL MICRO RESET
453 HC373X
Amp 1 Disable CTRL
AURAL CIRCUIT DISABLE
FIRMWARE CONFIGURATION
ENABLED
DC OK
TEMP
MOD OK
MOD OK LED NOTE:
LED is red and blinking if a fault is present
1 blink means Amp Current fault
2 blinks means Temperature fault
3 blinks means +32V supply over voltage
4 blinks means +32V supply under voltage
5 blinks means Reflected Power fault
6 blinks means +12V or -12V fault
MATERIAL NUMBERS:
1303682 ASY, INNOVATOR LX, AMP CTRL
1303683 SCH, INNOVATOR LX, AMP CTRL
1303686 PCB, INNOVATOR LX, AMP CTRL
1303687 STENCIL FOR LASSER
1303686 FIRMWARE, INNOVATOR LX, AMP CTRL
PAGE 2 , B-4 AREA, R214 WAS 100 OHMS. CR
H0 20112473 4/13/07 TB
R61 WAS 1.21K, R118 WAS 220. ADDED C112 & R214. DEL C78, C116 & R114 CHANGED TO NOT USED. JKF
G0 20112306 10/23/06 LRT
R66 WAS 1.47K, R78 WAS 1.21K. U10B PIN 5 SIGNAL NAME WAS 2.257V. CR
F0 20111898 2/28/06 LRT
ADDED C110 & C111, ADDED NOT USED R211 & R212. JKF
E0 20111812 7/6/05 LRT
C43, C45, C47, C59, C61 & C63 WERE 1800pF, J6 & J9 WERE STRAIGHT. JKF
D0 20111501 5/19/05 LRT
C5, C8, C11, C12, C15, C18 - C22, C25 - C28, C43, C45, C47, C59, C61 & C63 WERE .01uF. C44, C46, C48, C60, C62, C64, C94, C96, C102 & C107 WERE .1uF. JKF
C0 20111638 10/11/04 REH
PG 1) ADD R206 FROM U1.19 TO U1.20 ADD R207 FROM U6.18 TO U6.20 ADD R208 FROM U12.2 TO GROUND. PG 2) REMOVE C55, C56,C57. CHANGE R15 THRU R20 TO R6-5 THRU R20 (NEW P/N 1304565) PG 3) REMOVE CR22, CR23, CR26, CR27, CR32, CR34. CHANGE R176, R139, R153 FROM 2.2K TO 8 OHMS. ADD R205 FROM U22A.2 TO GROUND. ADD R215 BETWEEN U22A.1 AND U22A.2. (CR)
B0 20111421 6/15/04 REH
Axcera
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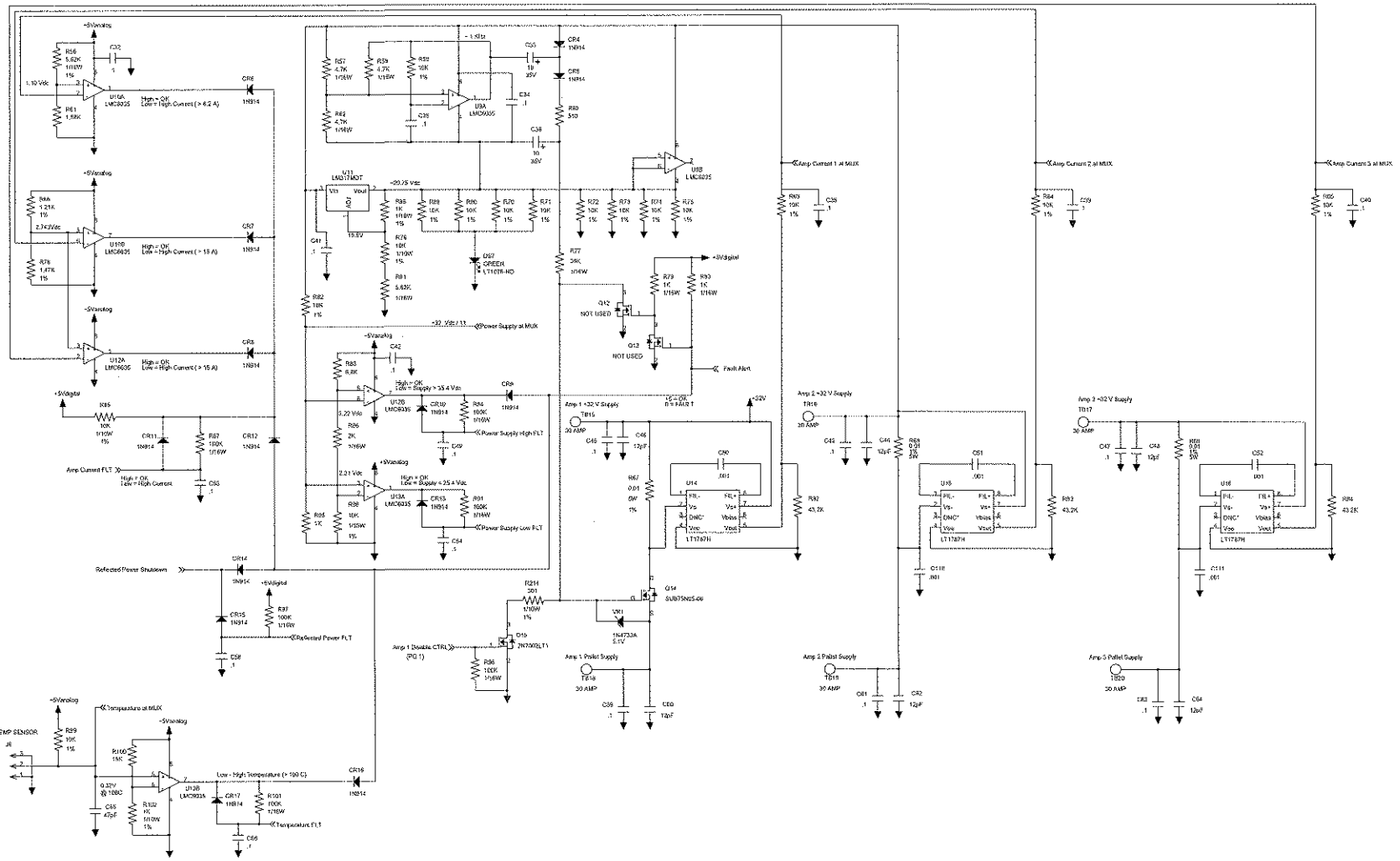
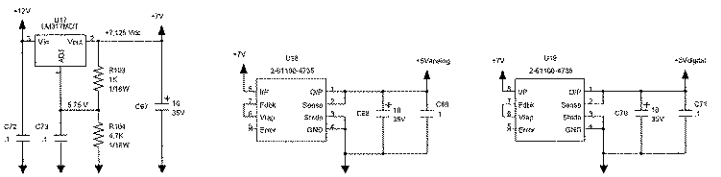
MATERIAL
FINISH
REV ECO DATE APV
TITLE SCH., AMP. CONTROL, INNOVATOR LX (1303682)
DWN REH 12/16/03
CHK REH 12/16/03
ENG REH 12/16/03
DWG. NO. 1303683
REV H0
SCALE
SHEET 1 OF 3

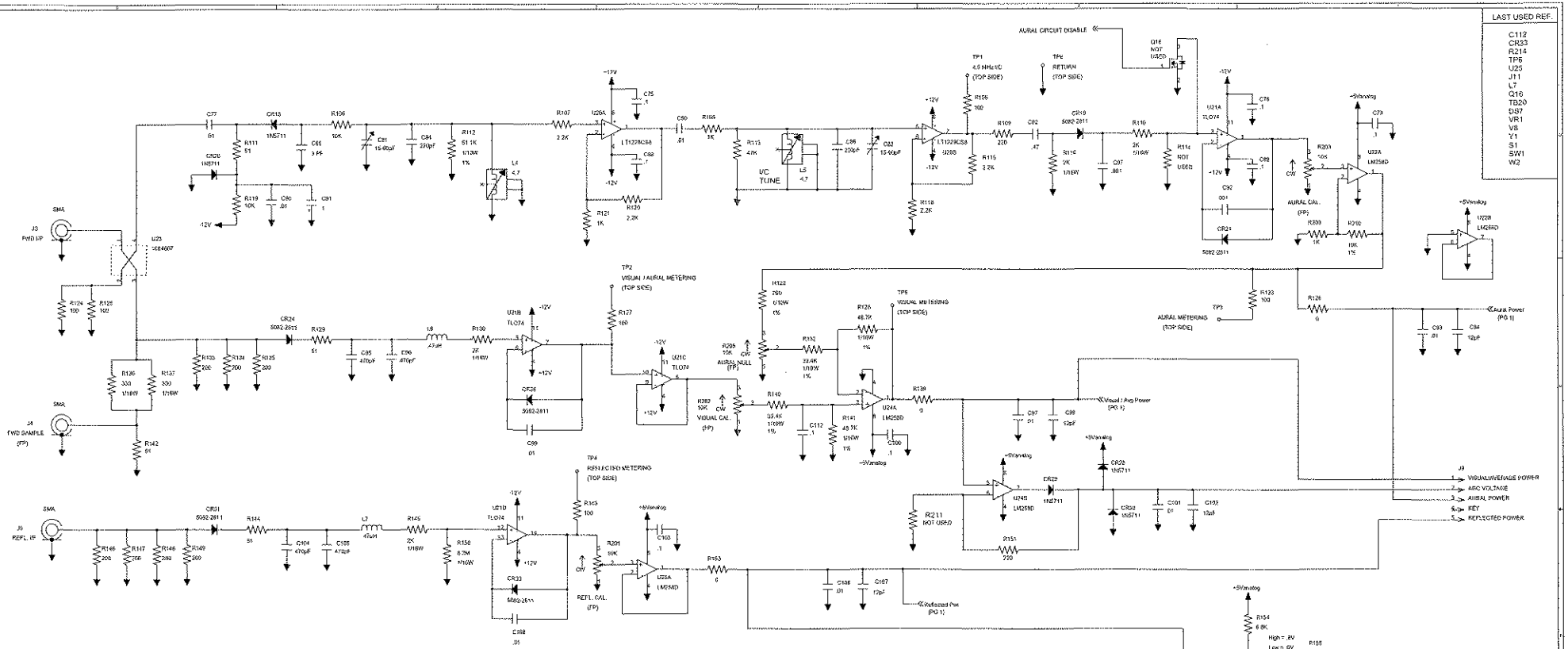


NOTE:

A track width of 0.3 inch is needed between power input vias and sense resistors R55,R56,R57. 0.3 inch track width is also needed between the output of the sense resistors and the output vias that provide power to the amplifier pallets.



Axcera		REV	ECO	DATE	APV
THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE	SCH., AMP. CONTROL, INNOVATOR LX (1303682)			
MATERIAL	DWN	REH	12/16/03	DWG. NO. 1303683	REV H0
FINISH	CHK	REH	12/16/03		
	SEQ.	REH	12/16/03	SCALE	SHEET 2 OF 3



Circuit Description

Page 1:

Upper center of page one is U4 which is the controller. This in-circuit Atmel microcontroller is operated at 3.6864 MHz. Programming of this device is performed through J2. U4 selects the desired analog channel of U3 through the settings of PA0 - PA2. PA3 of U4 is a processor operating LED that can be flashed to show continued operation. PF1 is used to monitor the +12 Vdc supply to the board. PF4 is the selected channel of analog switch U3. PF3 and other select microcontroller pins are connected to a via for future access.

J2 is our standard serial to RS-485 driver IC. U5 is a watchdog IC used to hold the microcontroller in reset if the supply voltage is less than 4.21 Vdc; (1.25 Vdc < Pin 4 (IN) < Pin 2 (Vcc)). U5 momentarily resets the microcontroller if Pin 6 (IST) is not clocked every second. A manual reset switch is provided but should not be needed.

Upper left corner U1 is used to determine where the amplifier control board is located. The eight inputs come from amp connector J8 and are used to set the SCADA address of the controller. Pull-up resistors set a default condition of logic high.

U6 below U1 is used to control two of the four board's status LEDs and three other circuits that are not allowed to change state during a microcontroller reset. A FET is turned on to shut current away from the LED to turn it off. U6 below U5 is used to enable different features within software. Actual use is TBD.

Page 2:

In the lower right corner are voltage regulator circuits. U17 should allow for 0.14 amps of power using its 92 C/W rating if Ta = 60C max and Tj = 125C max. 0.26 amps can be obtained from U17 if the mounting pad is 0.5 sqr. inches. The controller will not need this much current.

U18 and U19 are low drop-out voltage regulators with a tolerance greater than or equal to 1%. 100 mA is available from each device but again the controller will not need this much current.

In the upper left section are circuits with U9 and U11. U11 is used to generate a regulated voltage that is about 5 Volts less than the +32 Volt supply. When the +32 Volt supply is enabled, the circuitry around U9A is used to provide gate voltage to Q14 that is 5 volts greater than the source pin of this FET. The gate of Q14 can be turned off by any one of a few different circuits. These circuits are wired through Q12 and Q13. At this time these transistors are not installed but they may be installed to increase the shut-down time on a detected fault. Without Q12 and Q13 installed, Q14 is only turned off by the microcontroller through Q16.

U10A is used to detect high current in amplifier #1. At 1.10 Vdc, the current to amplifier #1 should be about 6.20 Amps. U10B and U12A are used to detect a high current condition in amplifier stages #2 or #3. With a 2.74 Vdc reference, high current shut down should be about 15 Amps.

U12B is used to detect high power supply voltage. U13A is used to indicate that the power supply voltage is less than 26 volts.

U25B on page 3 is used to detect high reflected power. U13B determines if the power supply temperature gets too hot.

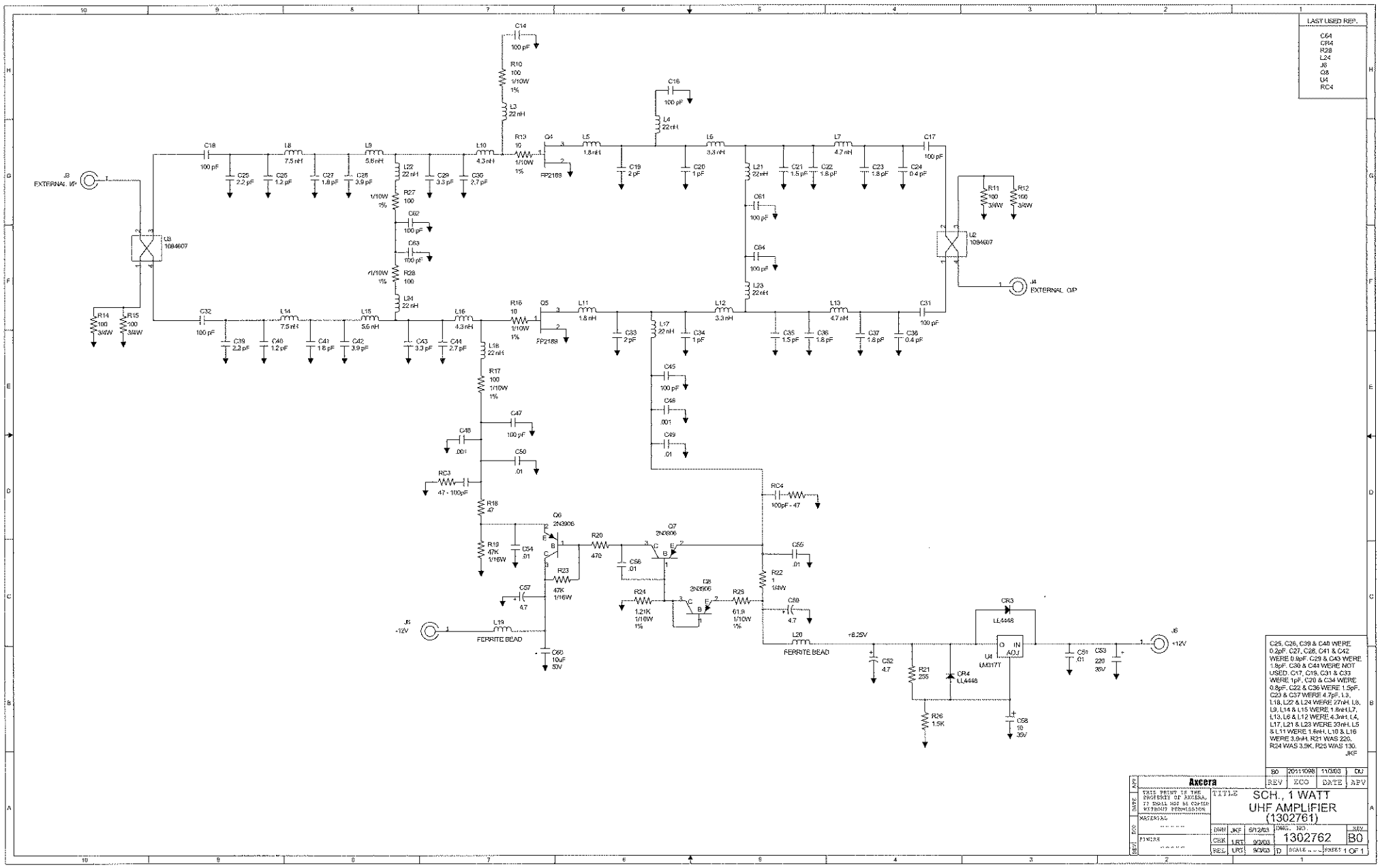
Current Monitoring Sections - A 0.01 ohm 1% 5 Watt thru-hole resistor is used for monitoring the current through several sections of the amplifier. The voltage developed across this resistor is amplified for current monitoring by U14, U15, or U16. The Linear Technology LT1787HVCS8 precision high side current sense amplifier accepts a maximum voltage of 60 Vdc. The 49.9 Kohm resistor from Pin 5 to ground sets the gain of the amplifier to about 17.26. This value is not set with much accuracy since the manufacture internal matches the resistors of this part but their actual resistance value is not closely defined. A trimming resistor is suggested to give a temperature stability of -200ppm/C but instead the microcontroller will determine the exact gain of the circuit and use a correction factor for measurements.

Page 3:

RF power detector circuits. Q16 is used by the microcontroller to disable the aural circuit of a digital transmitter or in external amplifiers where the amplifier is not to monitor visual power.

The Visual or Forward power circuit is calibrated and presented on the input of U24B pin 5. If this module has the highest detected forward power in a multi-amplifier system, it will have the highest forward power signal. This signal level into U24B pin 5 will be used to set the AGC output voltage of J9-2. If another amplifier has a higher forward power, the level into U24B pin 6 will be higher than pin5 and this amplifiers output signal will not be used to set the voltage level of J9-2.

Axcera		REV	ECO	DATE	APV
THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE	SCH., AMP. CONTROL, INNOVATOR LX (1303682)			
MATERIAL: - - - - -	DWN	REH	12/16/03	DWG. NO.	REV
FINISH: - - - - -	CHK	REH	12/16/03	1303683	H0
	ISS1	REH	12/16/03	D SCALE: - - -	SHEET 3 OF 3


LAST USED REF.
C64
CR4
R28
L24
J6
Q8
U4
RC4
C14
100 pF
R10
100
1/10W
1%
L3
22 nH
C16
100 pF
L4
22 nH
J3
EXTERNAL I/P
C18
100 pF
C25 2.2 pF
L8
7.5 nH
C26 1.2 pF
C27 1.8 pF
L9
5.6 nH
C28 3.9 pF
L22
22 nH
C29 3.3 pF
L10
4.3 nH
C30 2.7 pF
R13
10
1/10W
1%
Q4
FP2189
L5
1.8 nH
C19 2 pF
C20 1 pF
L6
3.3 nH
L21
22nH
C21 1.5 pF
L7
4.7 nH
C22 1.8 pF
C23 1.8 pF
C17
100 pF
C24 0.4 pF
C61
100 pF
C64
100 pF
L23
22 nH
R11
100
3/4W
R12
100
3/4W
U2
1084607
J4
EXTERNAL O/P
U3
1084607
R27
100
1/10W
1%
C62
100 pF
C63
100 pF
R28
100
1/10W
1%
L24
22 nH
R14
100
3/4W
R15
100
3/4W
C32
100 pF
C39 2.2 pF
L14
7.5 nH
C40 1.2 pF
L15
5.6 nH
C41 1.8 pF
C42 3.9 pF
L16
4.3 nH
C43 3.3 pF
C44 2.7 pF
R16
10
1/10W
1%
Q5
FP2189
L11
1.8 nH
C33 2 pF
L17
22 nH
C34 1 pF
L12
3.3 nH
C35 1.5 pF
C36 1.8 pF
L13
4.7 nH
C37 1.8 pF
C38 0.4 pF
C31
100 pF
L18
22 nH
R17
100
1/10W
1%
C45
100 pF
C46
.001
C49
.01
C47
100 pF
C48
.001
C50
.01
RC3
47 - 100pF
RC4
100pF - 47
R18
47
Q6
2N3906
R19
47K
1/16W
C54
.01
R20
470
Q7
2N3906
C56
.01
C55
.01
R22
1
1/4W
R23
47K
1/16W
C57
4.7
R24
1.21K
1/10W
1%
Q8
2N3906
R25
61.9
1/10W
1%
C59
4.7
J5
+12V
L19
FERRITE BEAD
C65
10µF
50V
L20
FERRITE BEAD
+8.25V
CR3
LL4448
U4
LM317T
O
IN
ADJ
CR4
LL4448
C52
4.7
R21
255
R26
1.5K
C58
10
35V
C51
.01
C53
220
35V
J6
+12V
C25, C26, C39 & C40 WERE 0.2pF. C27, C28, C41 & C42 WERE 0.9pF. C29 & C43 WERE 1.8pF. C30 & C44 WERE NOT USED. C17, C19, C31 & C33 WERE 1pF, C20 & C34 WERE 0.8pF. C22 & C36 WERE 1.5pF. C23 & C37 WERE 4.7pF. L3, L18, L22 & L24 WERE 27nH. L8, L9, L14 & L15 WERE 1.8nH. L7, L13, L6 & L12 WERE 4.3nH. L4, L17, L21 & L23 WERE 33nH. L5 & L11 WERE 1.6nH. L10 & L16 WERE 3.9nH. R21 WAS 220. R24 WAS 3.9K. R25 WAS 130.
JKF
B0 20111098 11/3/03 DJ
REV ECO DATE APV
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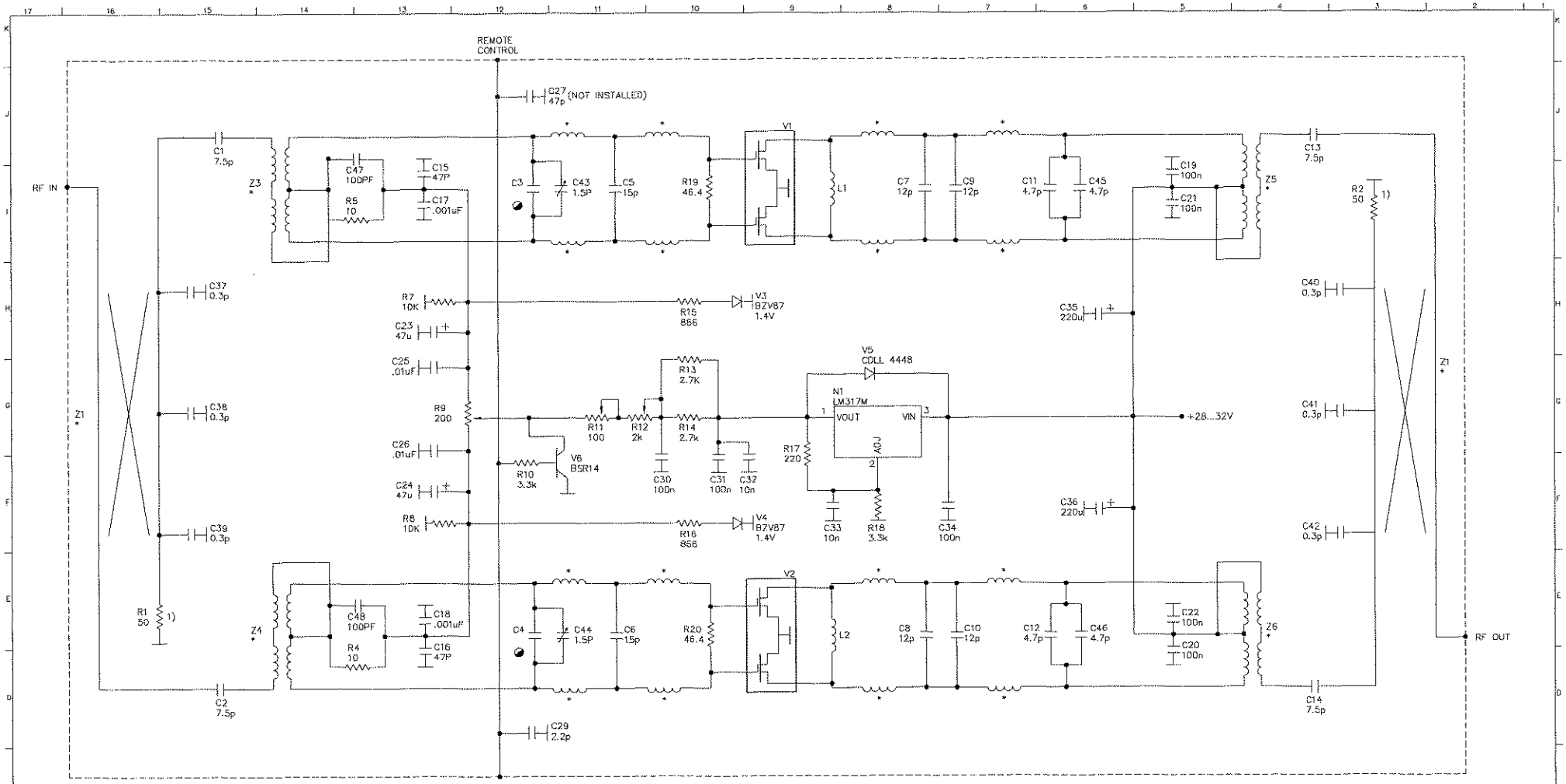
MATERIAL
FINISH
TITLE
SCH., 1 WATT
UHF AMPLIFIER
(1302761)
DWN JKF 9/12/03
CHK LRT 9/22/03
REL LRT 9/30/03
DWG. NO. 1302762
REV B0
SCALE
SHEET 1 OF 1



* PRINTED COMPONENT

FACTORY SET VALUE

PC BOARD LAYOUT SEE 51-5379-309-00 (2)

REV	ECO	DATE	APV
	DELETED PTF10159 P/N FROM LDMOS. ADDED C23,C24 & C27. CDD/CR		
CO	28019228	5/17/02	RE
	R15 AND R16 WERE 680 OHMS. PWN		
BO	28035824	4/02/02	LRT

10	R15 & R16 WERE 820 OHM.	PWN	04/01/02	
9	ADDED C23 & C24 PER CR 28018867 & 28019228	PWN	04/01/02	
8	ADDED C27 PER CR 28019228	PWN	04/01/02	
7	CHANGE R3 FROM A 2.2 OHM RESISTOR TO C47, 100PF, SM, CAP., 100WVDC. CHANGE R6 FROM A 2.2 OHM RESISTOR TO CAP, 100PF, 100WVDC. CHANGE R4 FROM A 2.2 OHM RESISTOR TO 1-596D000GSMT, SM., RES., 10 OHM 5%	PWN	04/01/02	
6	1/REW CHANGE R5 FROM A 2.2 OHM RESISTOR TO 1-596R000GSMT, SM., RES. 10 OHM 5%	PWN	04/01/02	
5	1/REW CHANGE C17 FROM A 47PF CAP, FIXED CERAMIC, 47 PF TO 1-596R561GSMT, SM., CAP., 001 UF, 50 WVDC	PWN	04/01/02	
4	CHANGE C18 FROM A 47PF CAP, FIXED CERAMIC, 47 PF TO 1-596R561GSMT, SM., CAP., 001 UF, 50 WVDC. CHANGE C23 (1-301148, SM. CAP, 47NF, 50V, LOW ESR, C25 (1-301148, SM. CAP, 47NF, 50V, LOW ESR, C26 1-596R181SMT, SM., CAP., 01 UF, 50 WVDC. ADDED C56 1-596R681SMT, SM., CAP., 01 UF, 50 WVDC. PWN	PWN	04/01/02	
3	DO NOT PRINT ON THIS REVISION	PWN	04/01/02	

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MATERIAL

FINISH

TITLE: AMPLIFIER MODULE

DWN	PWN	04/01/02	DWG. NO.
CHK	LRT	04/03/02	51-5379-309-00 WSH
REL	LRT	04/03/02	SCALE

REV: FO

SHEET 1 OF 1