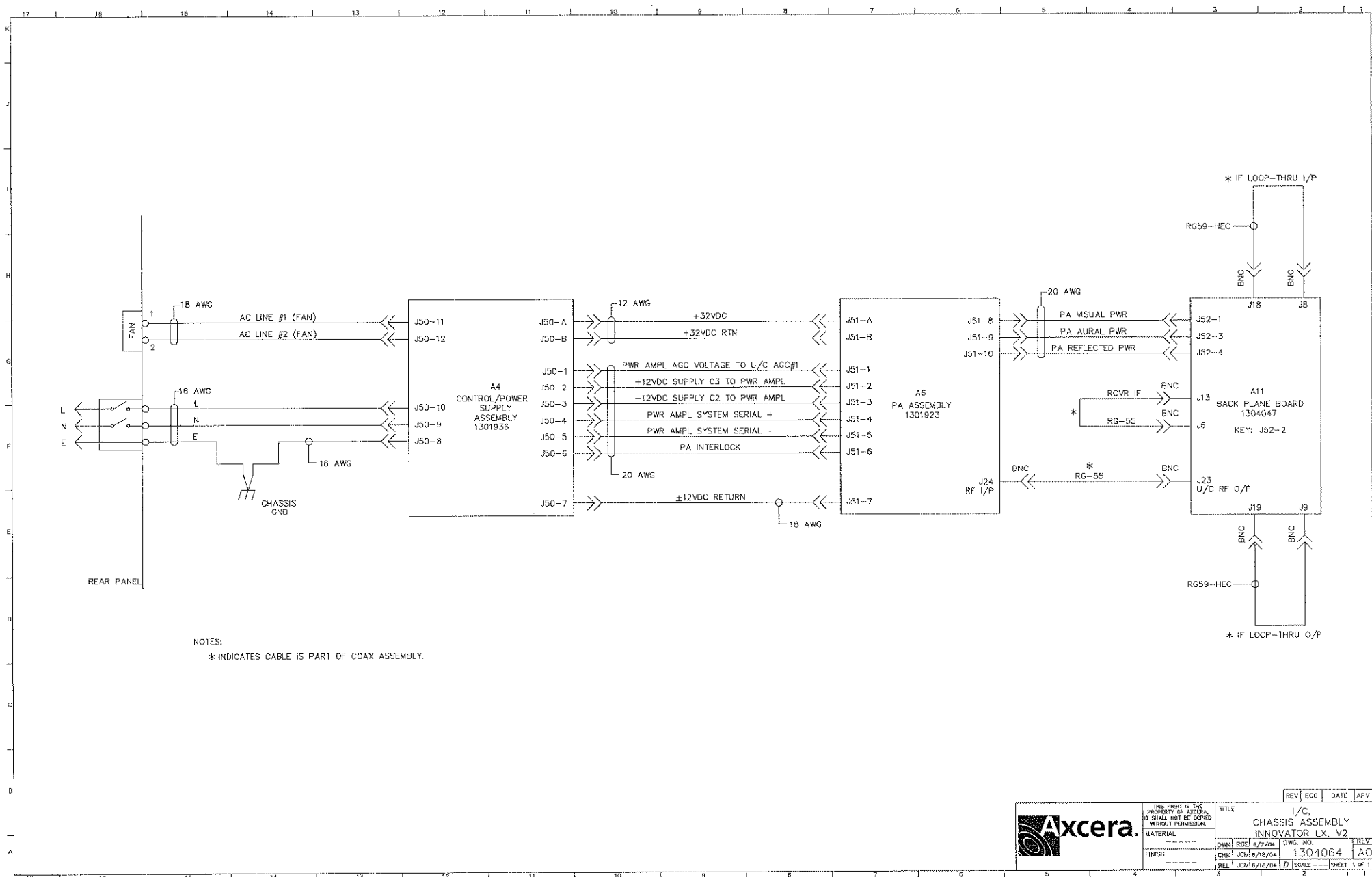
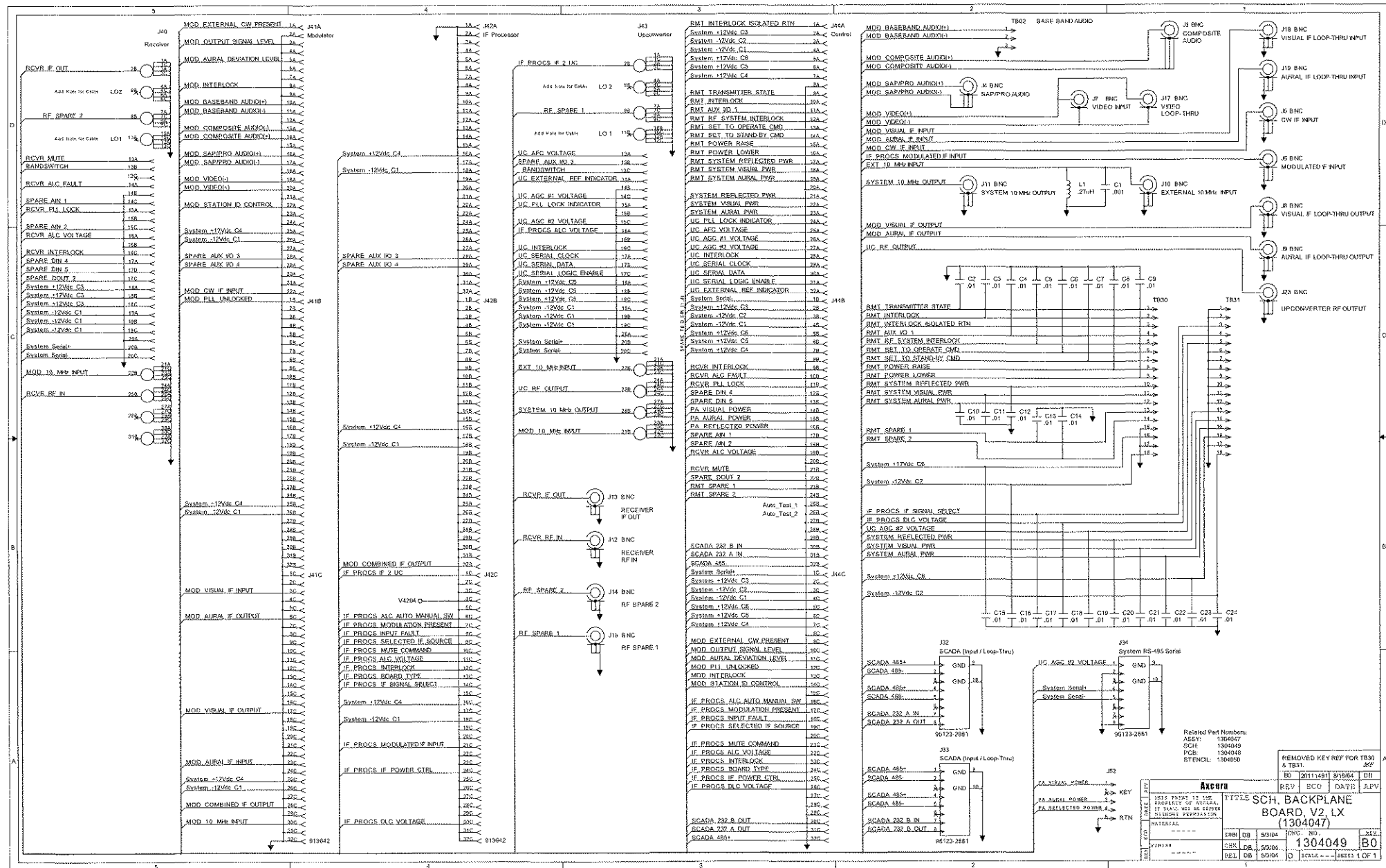
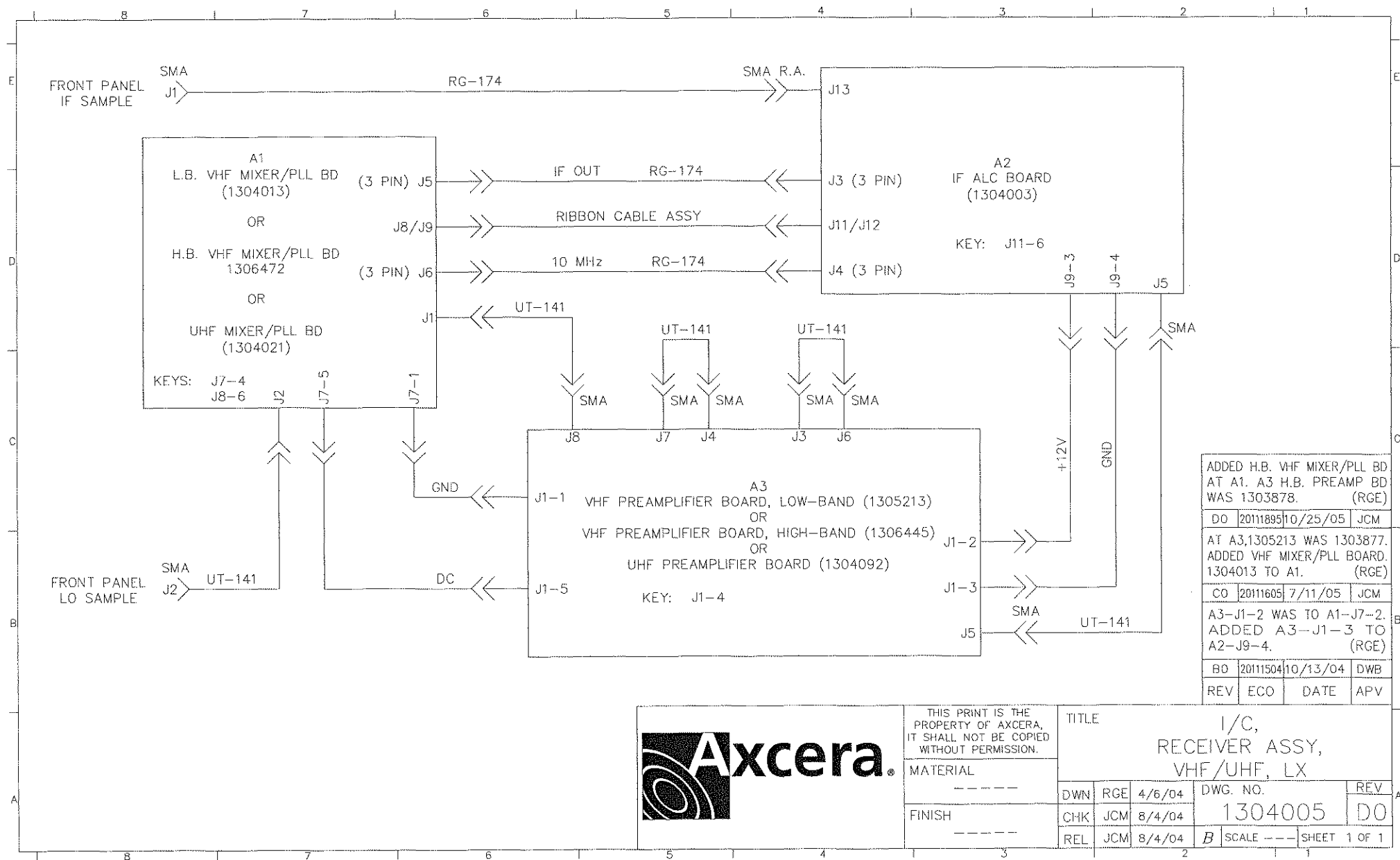




REV		ECO	DATE	APV
		TITLE I/C, CHASSIS ASSEMBLY INNOVATOR LX, V2		
MATERIAL		DRN	ROE	UWG
FINISH		CHK	JCM	6/18/04
		REL	JCM	6/18/04
		SCALE	1 OF 1	





ADDED H.B. VHF MIXER/PLL BD AT A1. A3 H.B. PREAMP BD WAS 1303878. (RGE)			
DO	20111895	10/25/05	JCM
AT A3,1305213 WAS 1303877. ADDED VHF MIXER/PLL BOARD. 1304013 TO A1. (RGE)			
CO	20111605	7/11/05	JCM
A3-J1-2 WAS TO A1-J7-2. ADDED A3-J1-3 TO A2-J9-4. (RGE)			
BO	20111504	10/13/04	DWB
REV	ECO	DATE	APV

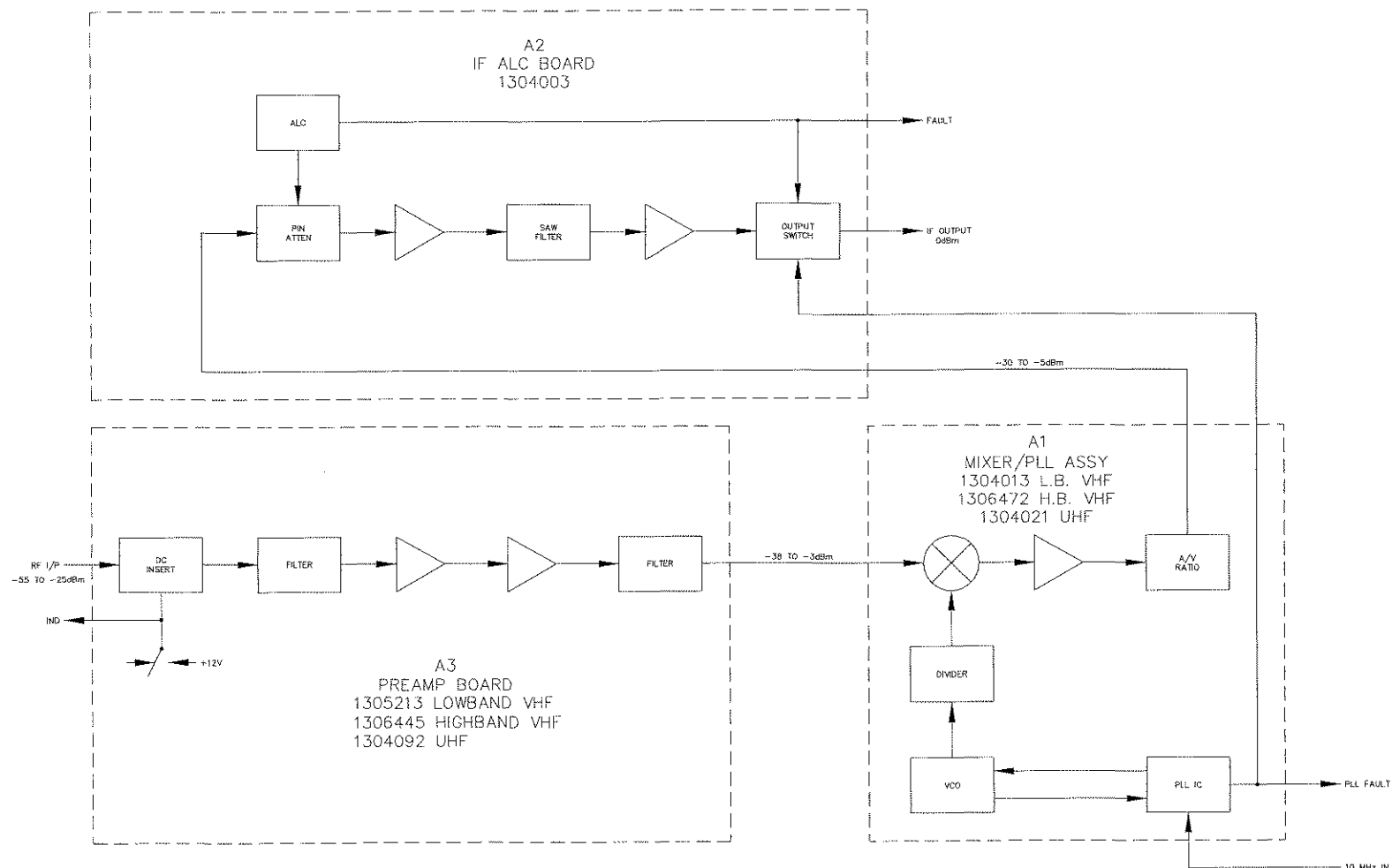
THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION.

MATERIAL: -----

FINISH: -----

TITLE: I/C, RECEIVER ASSY, VHF/UHF, LX

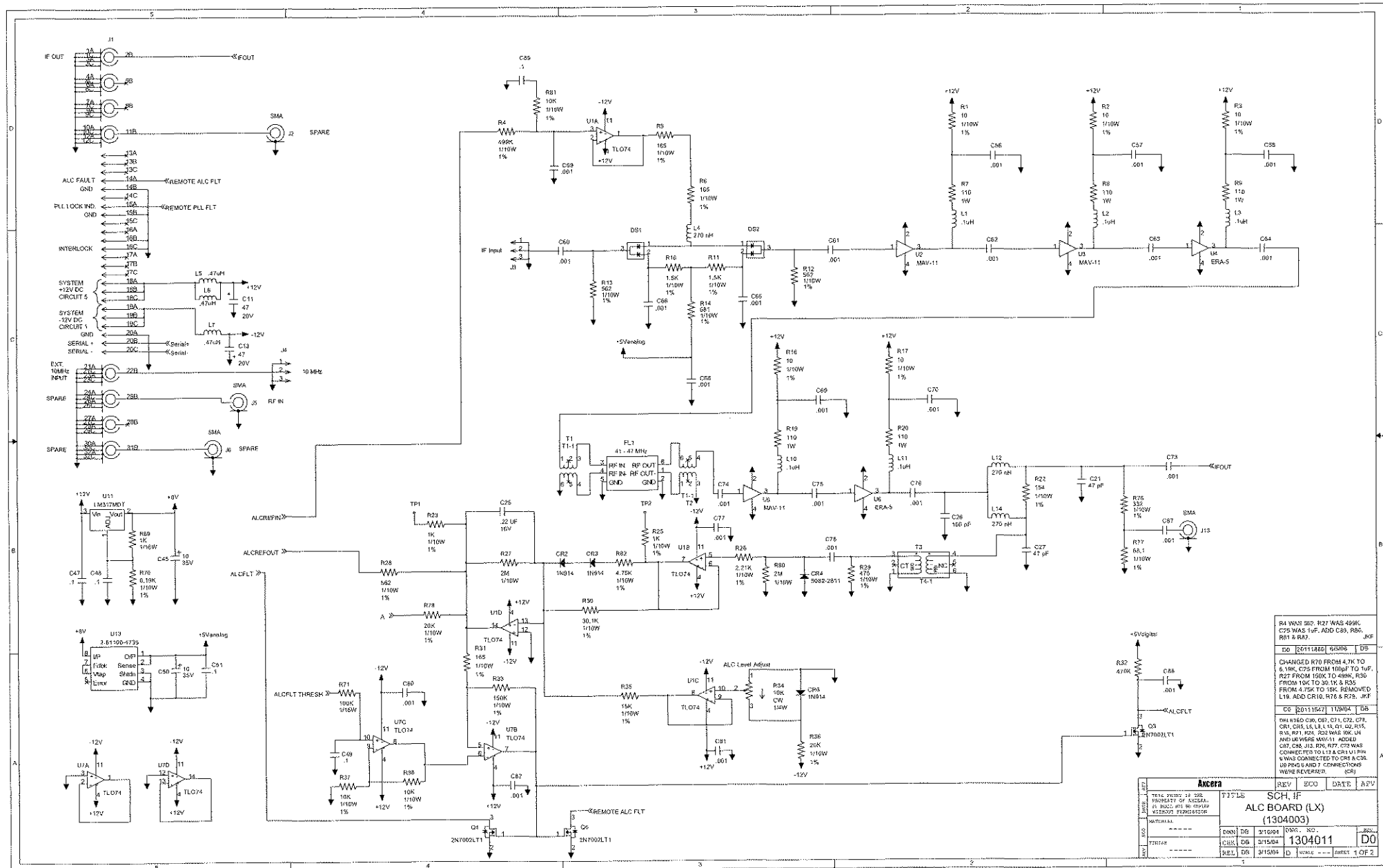
DWN	RGE	4/6/04	DWG. NO.	REV
CHK	JCM	8/4/04	1304005	DO
REL	JCM	8/4/04	B	SCALE --- SHEET 1 OF 1

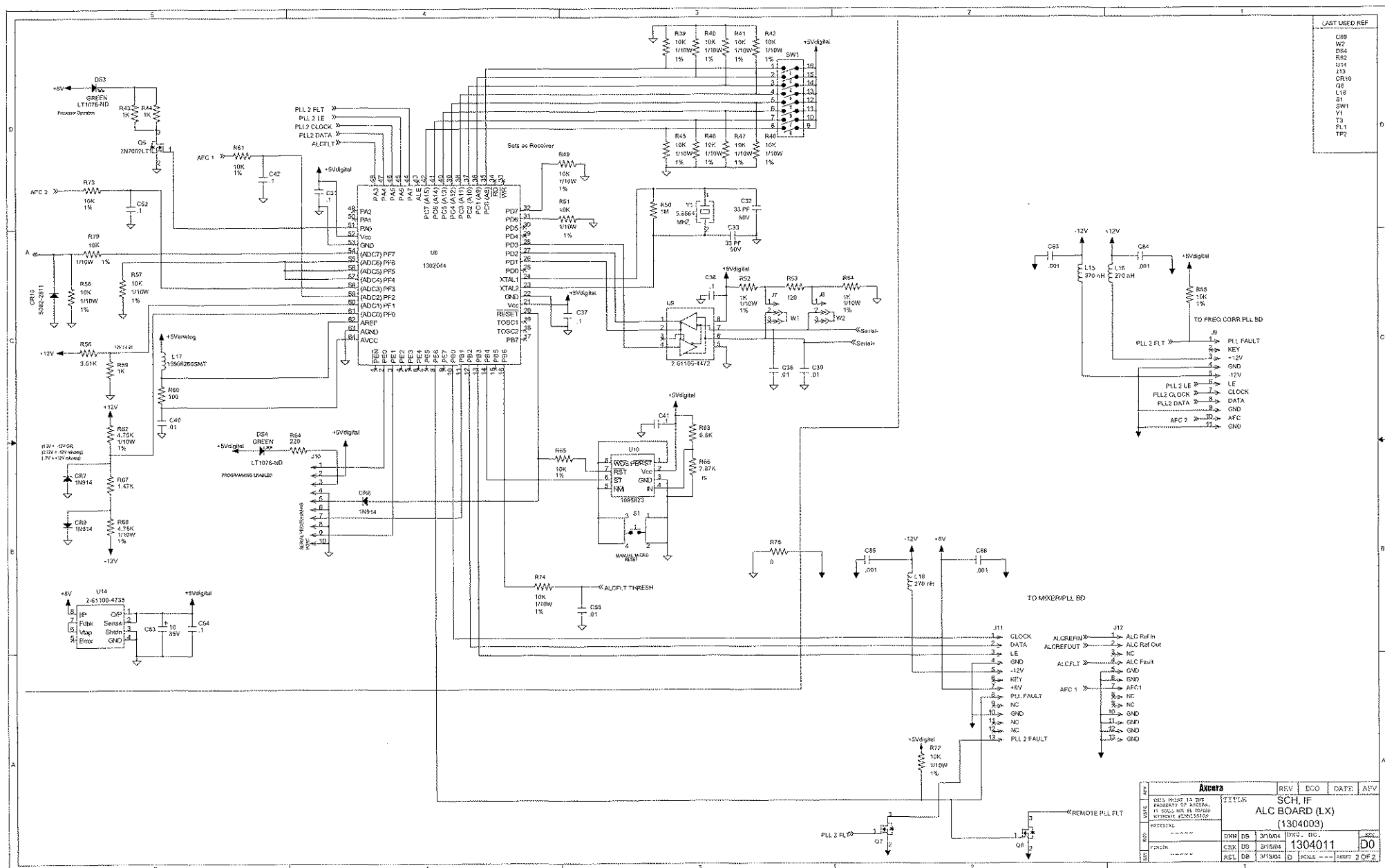


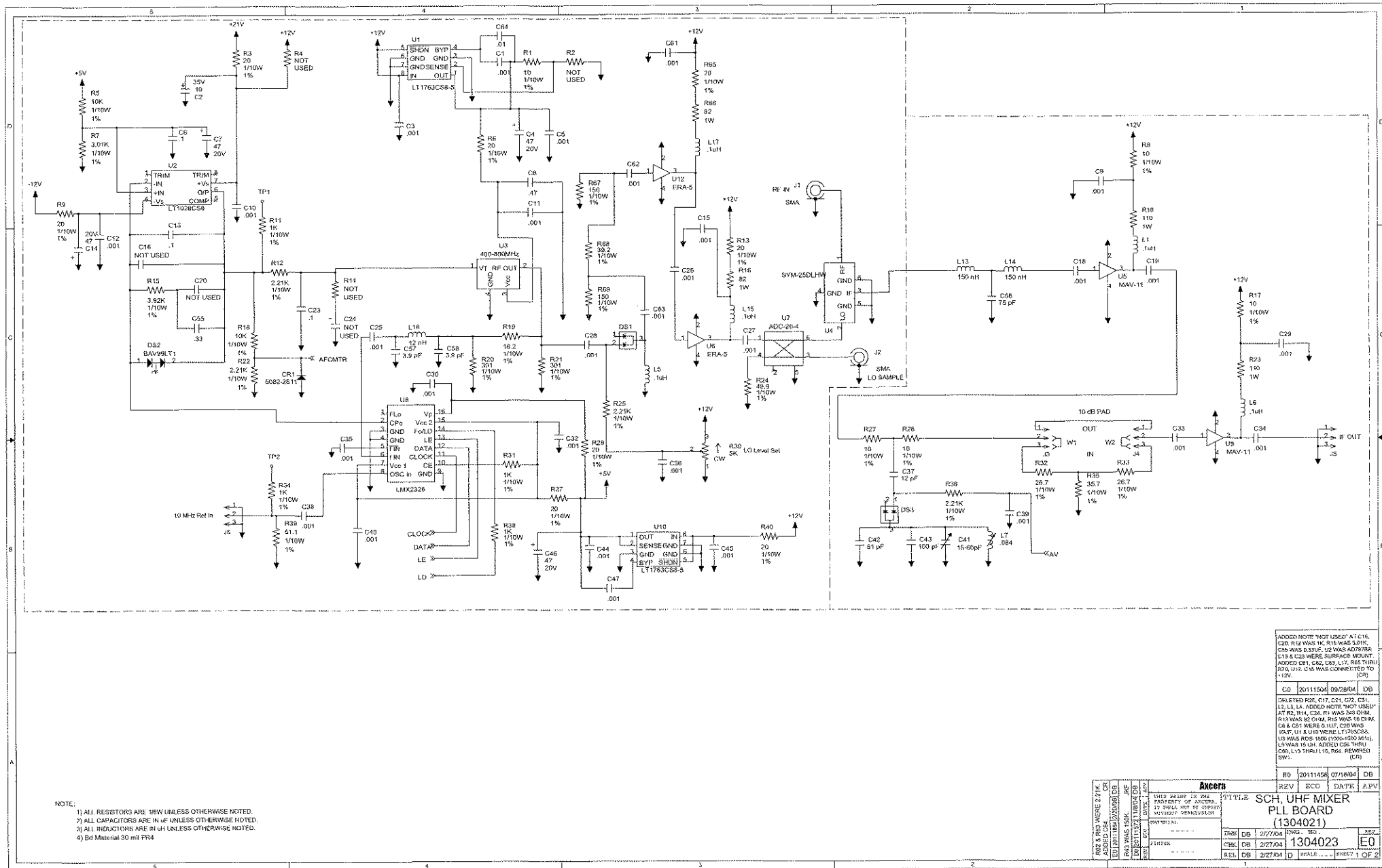
ADDED H.B. VHF MIXER/PLL BD
 AT A1, A3 H.B. PREAMP BD
 WAS 1303576 (RCS)
 CO 02/09/00/25/00 JCM
 A3 LOWBAND VHF PRE-
 AMP BD WAS 1303677.
 (RCS)
 DO 02/09/00 7/5/05 LRT
 REV COO DATE APV

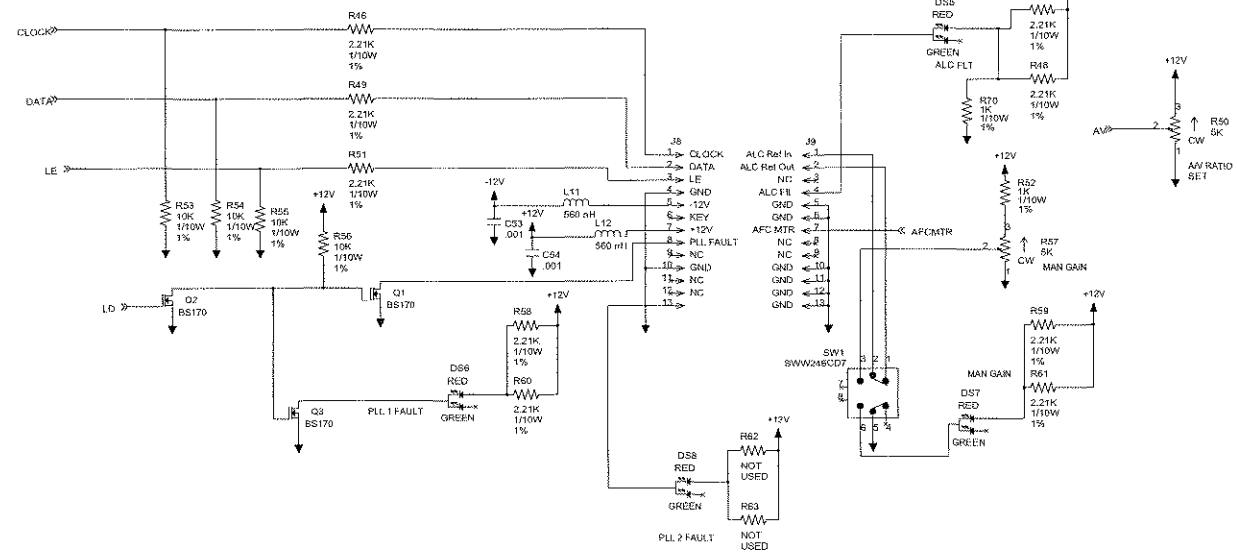
 Axcera.		THIS PRINT IS THE PROPERTY OF AXICERA. IT SHALL NOT BE COPIED WITHOUT PERMISSION.		TITLE		REV	DATE	APV
		MATERIAL		B/D, RECEIVER ASSEMBLY, VHF/UHF LX				
FINISH		DRAWN	RUE 5/4/04	DWG. NO.		REV		
		CHEK	DIMS 6/26/04	1304004		CO		
		REL	DIMS 6/26/04	D	SCALE	SHEET 1 OF 1		



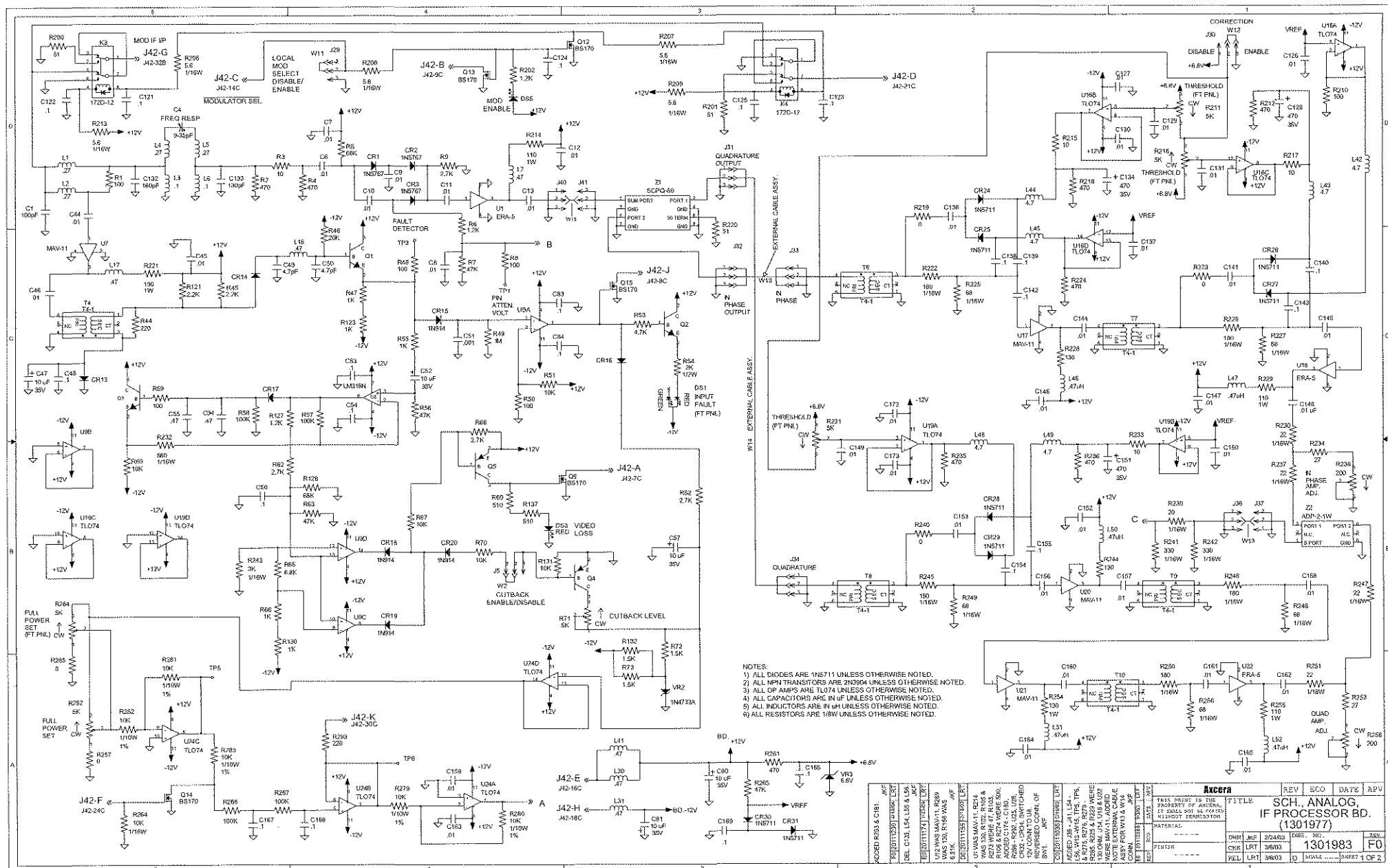


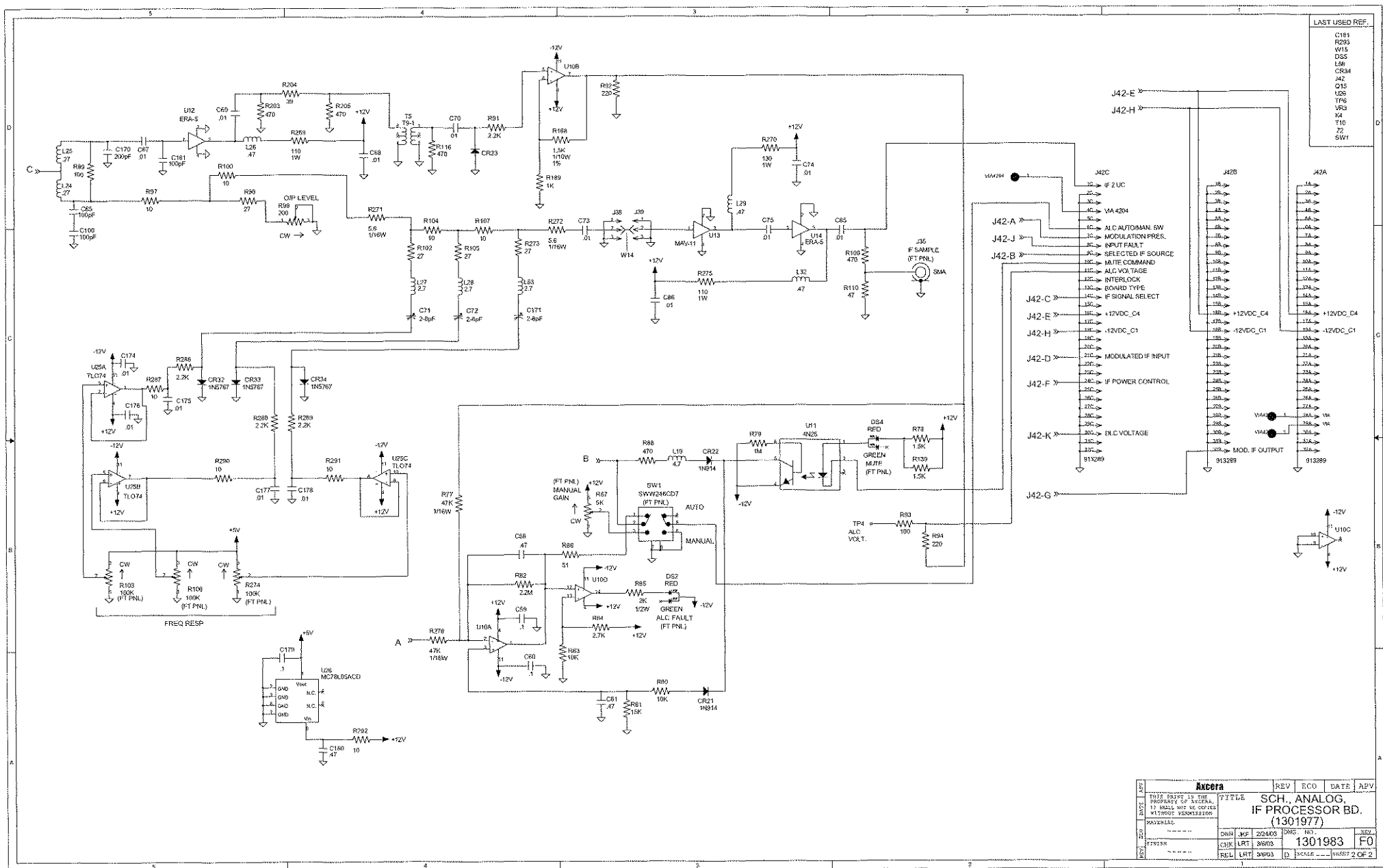


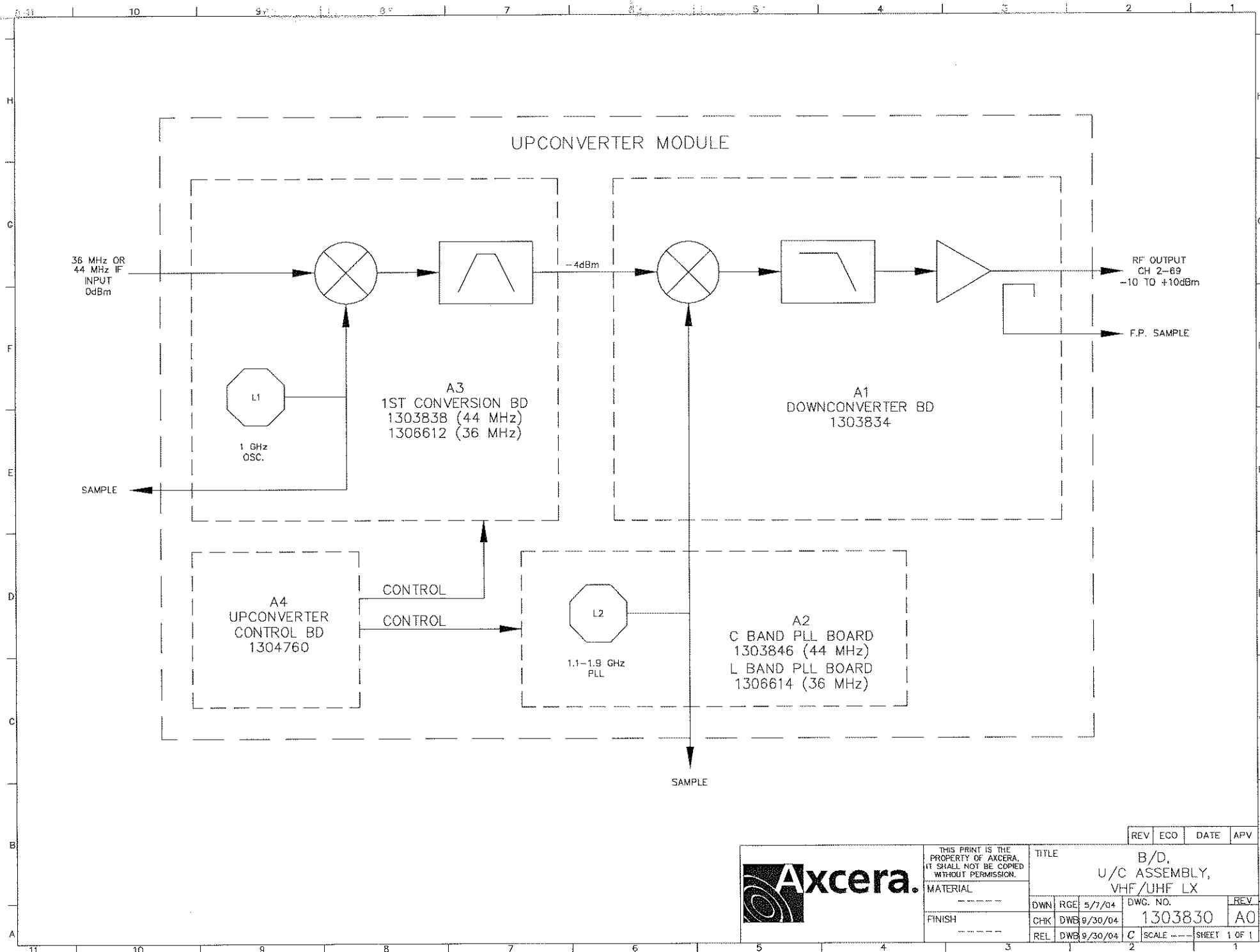




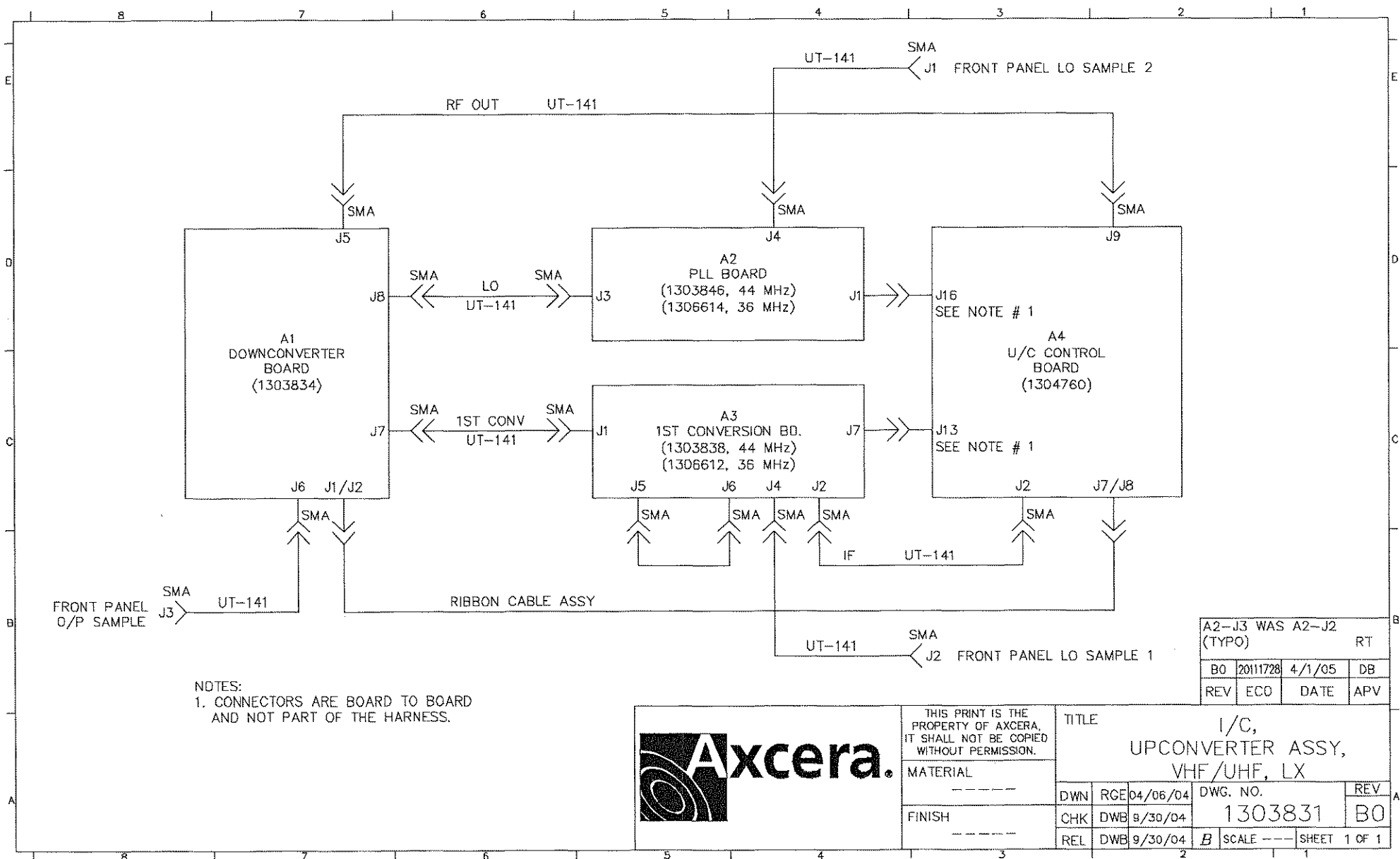
REV	ECO	DATE	APV
Ancera			
THIS DRAWING IS THE PROPERTY OF ANCERA. IT SHALL NOT BE COPIED WITHOUT PERMISSION			
TITLE SCH. UHF MIXER/ PLL BOARD (1304021)			
MATERIAL			
DATE	REV	ECO	APV
-----	-----	-----	-----
DATE	REV	ECO	APV
2/27/74	06	06	06
2/27/74	06	06	06
2/27/74	06	06	06
1304023	E0	2 OF 2	







REV ECO DATE APV				B/D.			
THIS PRINT IS THE PROPERTY OF AXCERA. IT SHALL NOT BE COPIED WITHOUT PERMISSION.				U/C ASSEMBLY, VHF/UHF LX			
MATERIAL				DWN	RGE	5/7/04	DWG. NO.
FINISH				CHK	DWG	9/30/04	1303830
REL				DWG	9/30/04	C	SCALE
				SHEET 1 OF 1			



A2-J3 WAS A2-J2 (TYPO)				RT
B0	20111728	4/1/05	DB	
REV	ECD	DATE	APV	

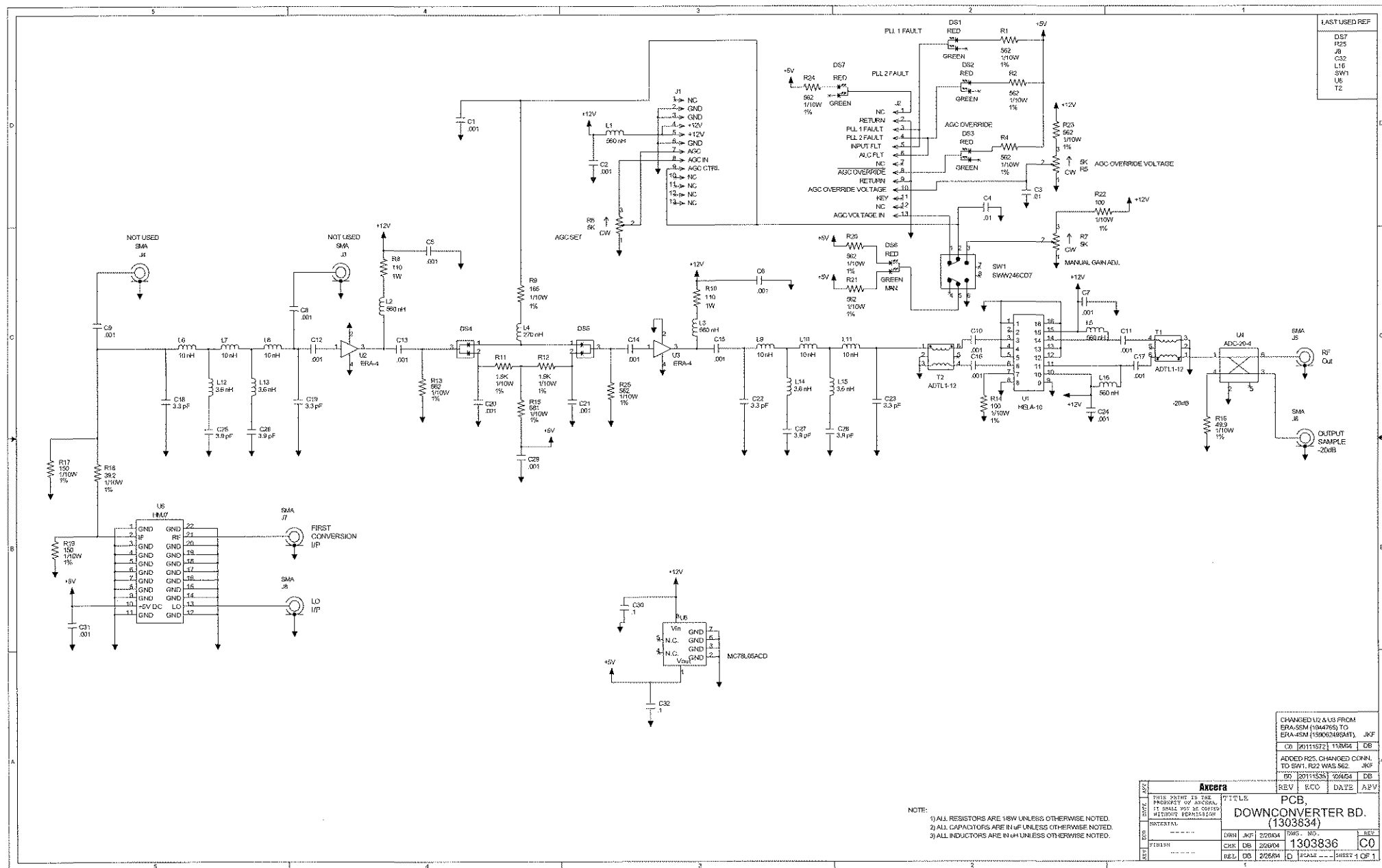


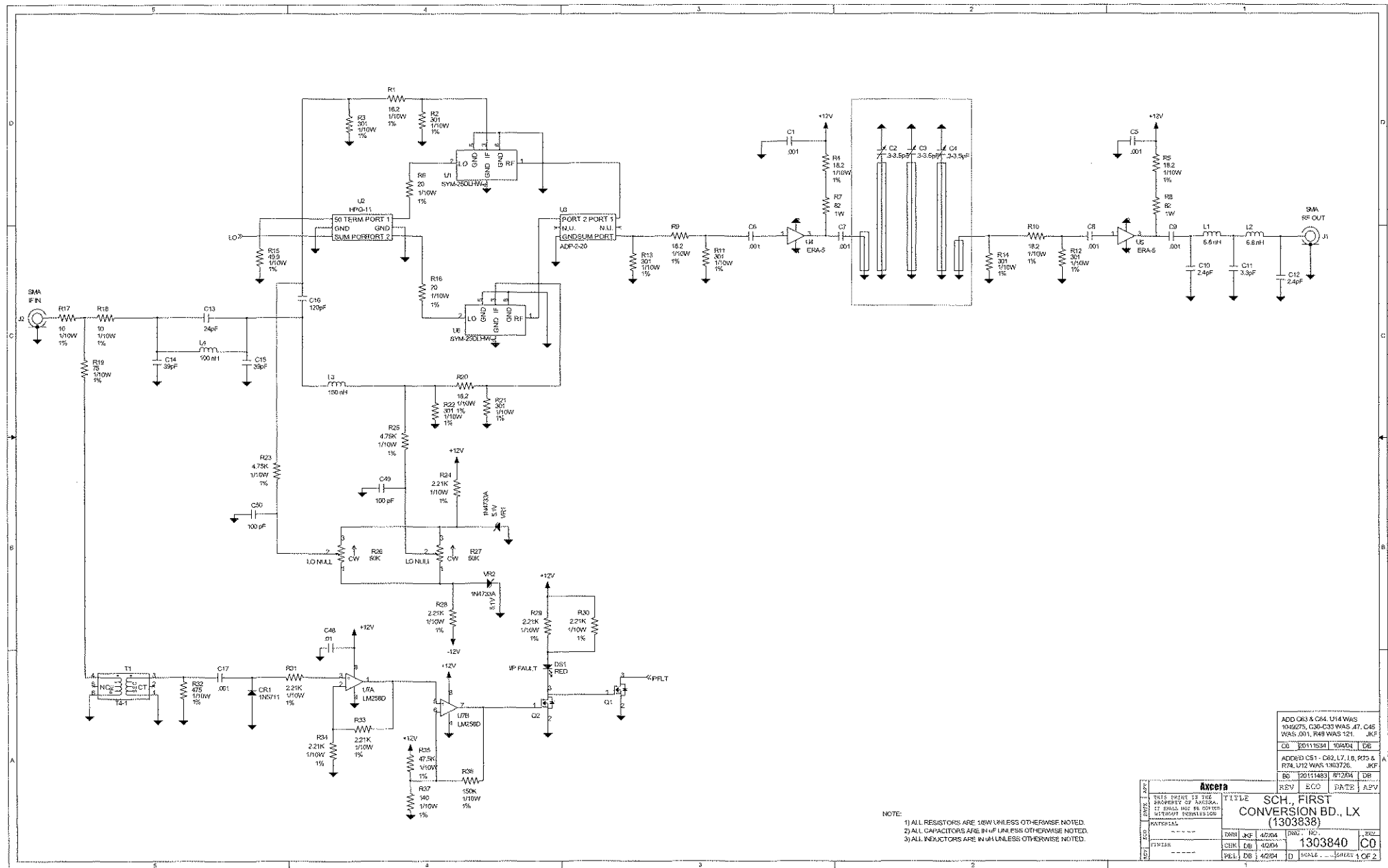
THIS PRINT IS THE PROPERTY OF AXCERA. IT SHALL NOT BE COPIED WITHOUT PERMISSION.

MATERIAL

FINISH

TITLE I/C, UPCONVERTER ASSY, VHF/UHF, LX				
DWN	RGE	04/06/04	DWG. NO.	REV
CHK	DWB	9/30/04	1303831	B0
REL	DWB	9/30/04	B	SCALE --- SHEET 1 OF 1





ADD Q3 & C4, U14 WAS
1049275, C30-C33 WAS 47, C45
WAS .001, R49 WAS 121. JCF

CO 20111534 104924 DB

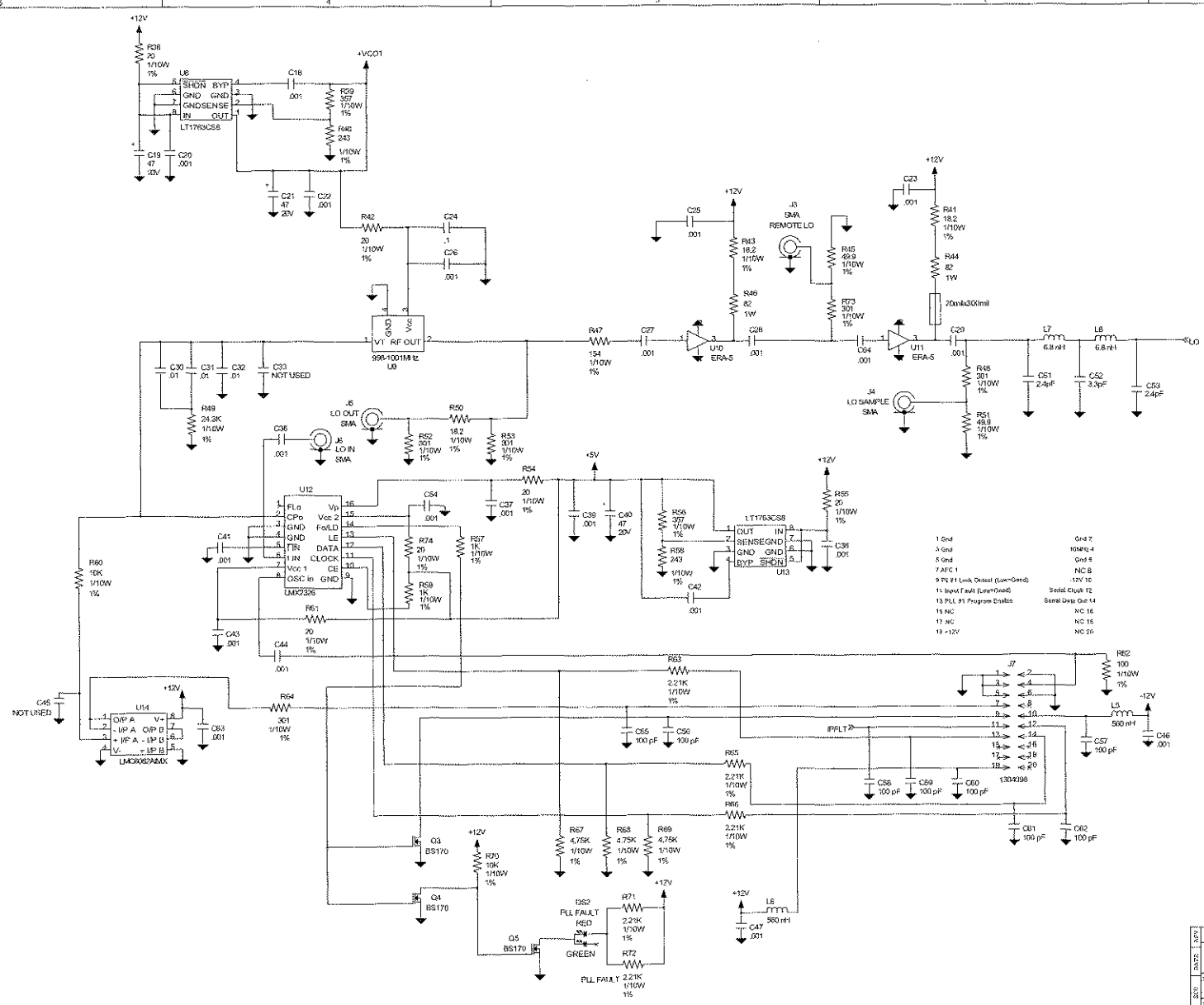
ADDED C61, C62, L7, L8, R75 &
R76, L12 WAS 1303720. JCF

EC 120111483 87224 DB

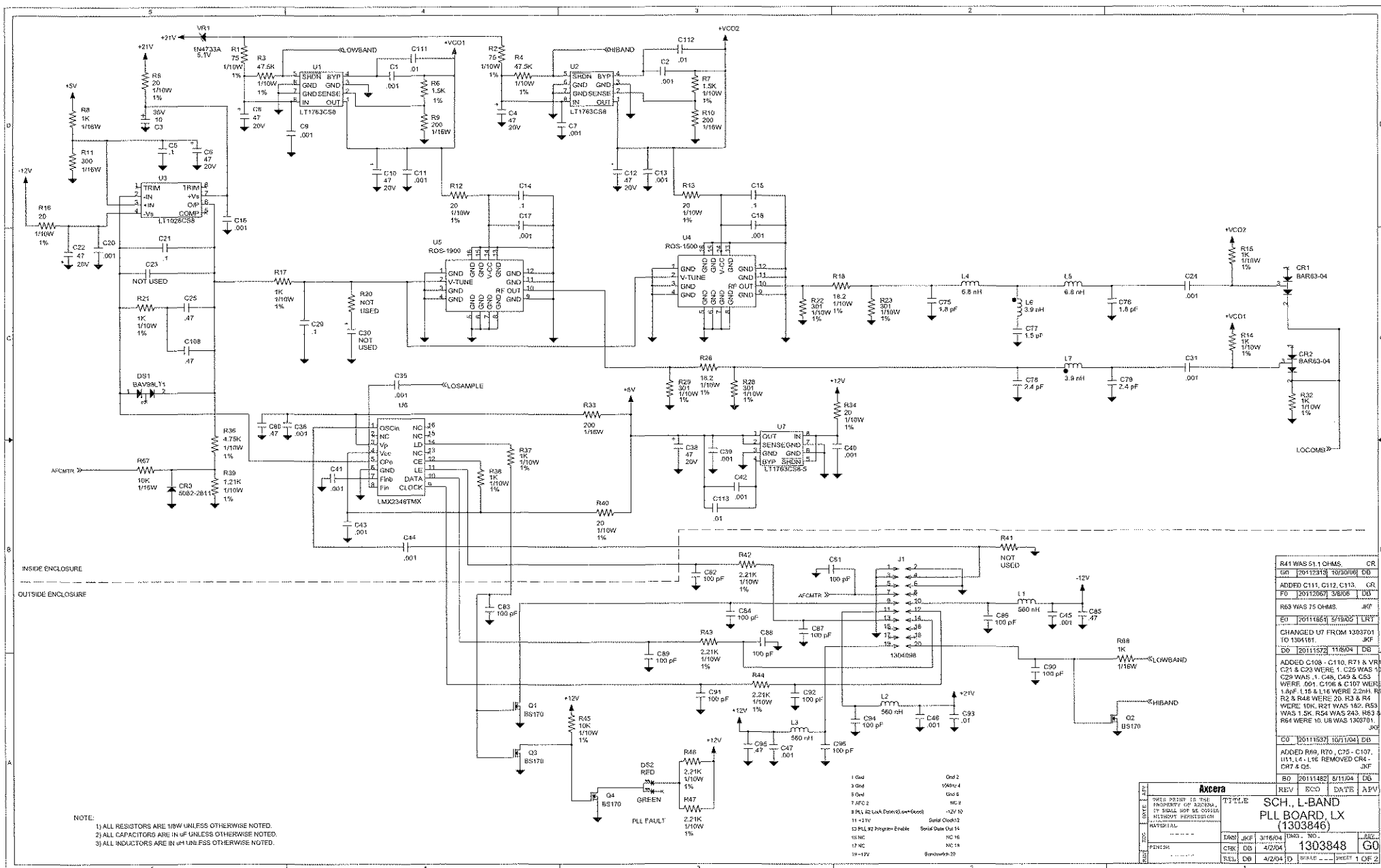
REV ECO DATE APV

Axceta				REV	ECO	DATE	APV
DATE PRINT IS THE PROPERTY OF AXICETA. IT SHALL NOT BE COPIED WITHOUT PERMISSION				TITLE SCH., FIRST CONVERSION BD., LX (1303838)			
MATERIAL	DRAW	QF	4/20/04	DWG	NO		
FIGURE	CHK	DB	4/20/04	1303840			
REL	DB	4/20/04	D	SCALE			1 OF 2

LAST USED REF
 L8
 J7
 R74
 Q5
 DS2
 VR2
 CR1
 T1

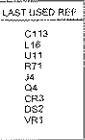


Axcera		REV	ECO	DATE	REV
TITLE		SCH. FIRST CONVERSION BD., LX (1303838)			
MATERIAL					
FINISH					
REL		OWN	WFO	1303840	C0
		CHK	DB	4/2/04	
		REL	DB	4/2/04	
		PAGE 2 OF 2			



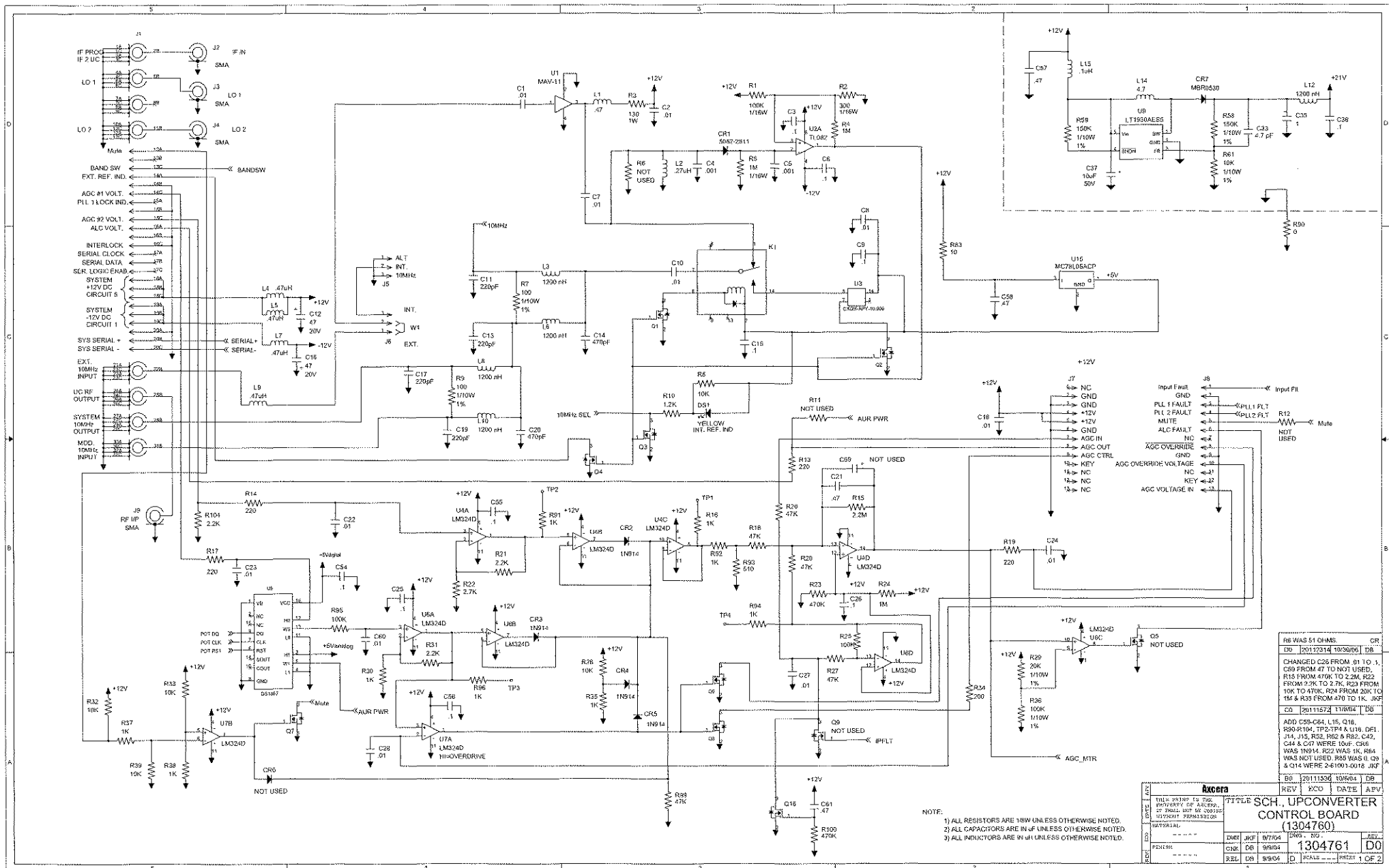
R41	WAS	51.1	OHMS.	CR
FO	2011/2313	7/30/01	DB	
ADDED	C111, C112, C113	CR		
FO	2011/2067	3/30/06	UD	
R63	WAS	75	OHMS.	ACF
EO	2011/1651	5/18/02	LRY	
CHANGED	UT FROM	1305/01		
TO	1341/01			
FO	2011/1572	11/06/04	DB	
ADDED	C108 - C110, R71 & VR			
C111	WERE. C125 WAS 1.2			
C28	WAS 1. C48, C49 & C53			
WERE.	001, C108, C107 WERE			
1.06F, 1.18, 1.16 WERE	2.25H, R8			
WERE. C107, C108, C109	WERE. C107, C108, C109			
WERE. C121, R21 WAS	1.62F, R21			
WAS 1.5K, R54 WAS	243.5, R83 & R54			
WERE	10. US WAS 100/01.			
FO	2011/1531	10/11/04	DB	
ADDED	R69, R70, C75 - C107			
R11, C111, C112 REMOVED	CR47 & C55			
CR7 & C55	INF			

					BO	2011482	6/11/04	DB
					REV	ECCO		
							DATE	APV
DATE	FY			TITLE	SCH., L-BAND			
					PLL BOARD, LX			
					(1303846)			
DESC				DWG. NO.				
					1303848			
PINSH				DRG.				
				REL	DB	4/2/04	DRG#	1 OF 2



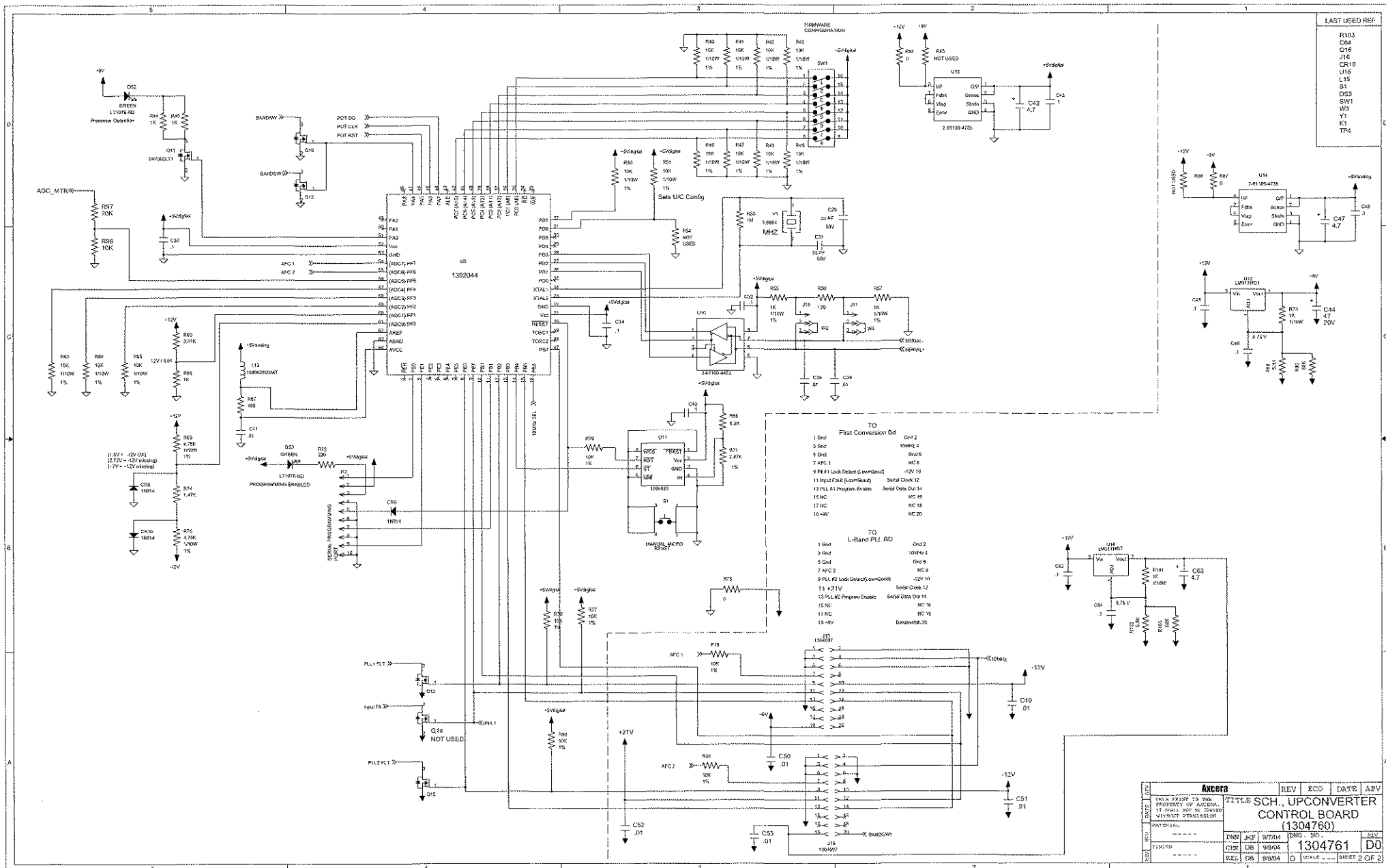
REV	ECO	DATE	APV
Axcera			
THIS PRINT IS THE PROPERTY OF AXCERA. IT SHALL NOT BE COPIED WITHOUT PERMISSION		TITLE SCH., L-BAND PLL BOARD, LX (1303846)	
AUTORIAL			

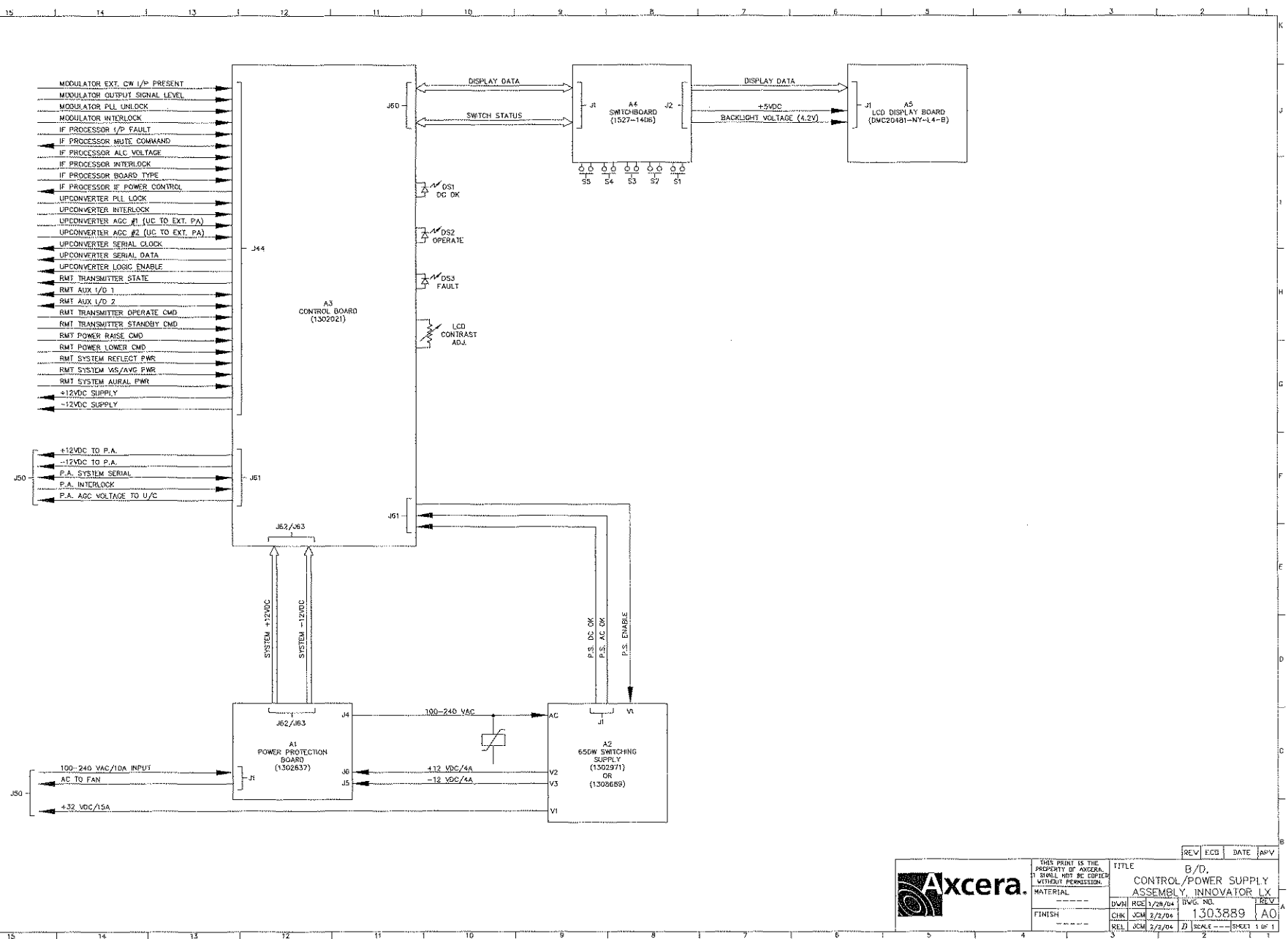
DATE	DWG. NO.	REV.	
FINISH	CHK DB 3/16/04	1303848	G0
	CRK DB 4/2/04		
	CRK DB 4/2/04		
	SCALE	SHEET 2 OF 2	



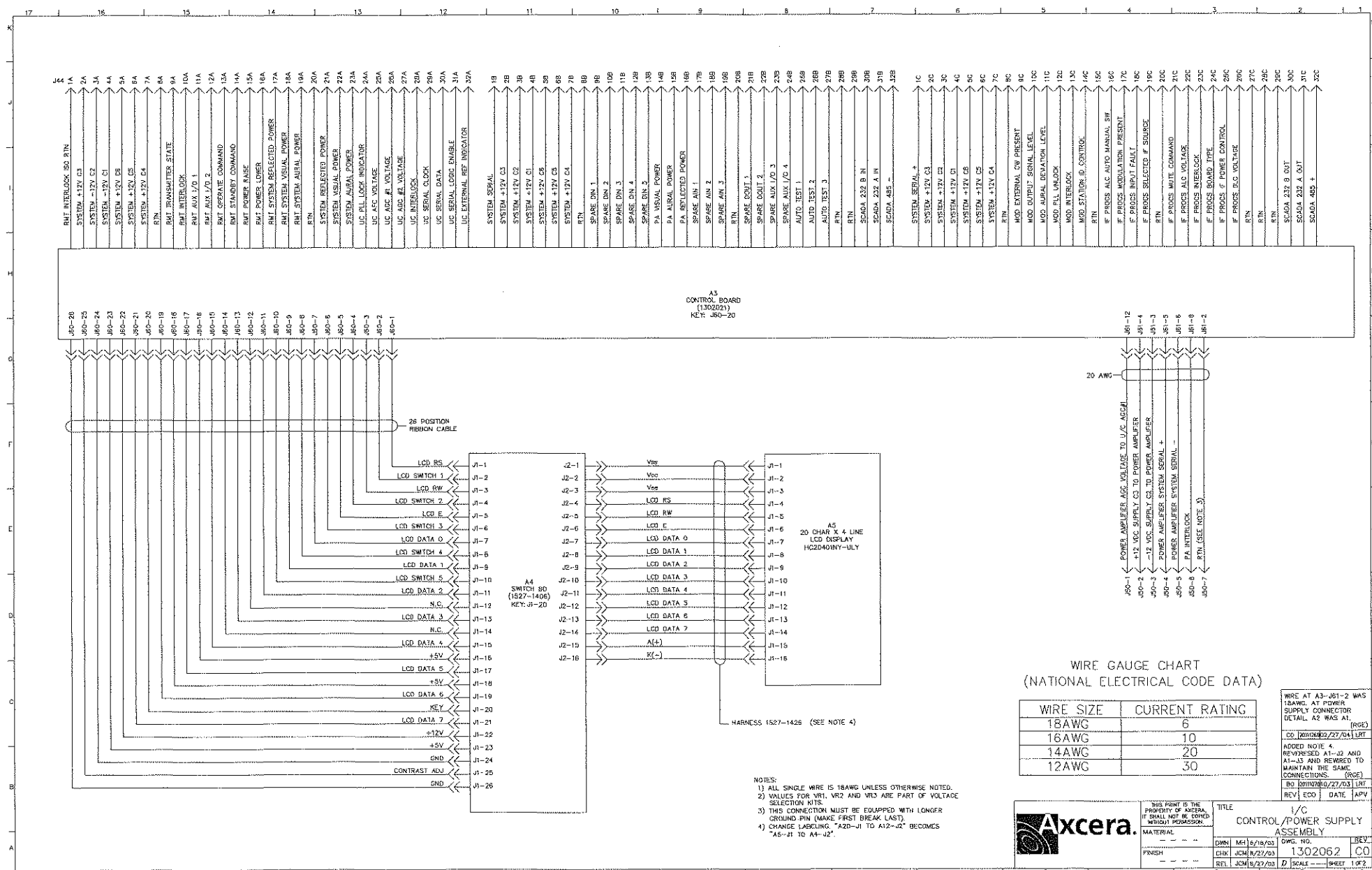
NOTE:
 1) ALL RESISTORS ARE 18W UNLESS OTHERWISE NOTED.
 2) ALL CAPACITORS ARE IN μ F UNLESS OTHERWISE NOTED.
 3) ALL INDUCTORS ARE IN μ H UNLESS OTHERWISE NOTED.

TITLE SCH., UPCONVERTER CONTROL BOARD (1304761)			
REV	DATE	DESCRIPTION	BY
1	20111524	10/30/06	APV
2	20111524	10/30/06	APV
3	20111524	10/30/06	APV
4	20111524	10/30/06	APV
5	20111524	10/30/06	APV
6	20111524	10/30/06	APV
7	20111524	10/30/06	APV
8	20111524	10/30/06	APV
9	20111524	10/30/06	APV
10	20111524	10/30/06	APV
11	20111524	10/30/06	APV
12	20111524	10/30/06	APV
13	20111524	10/30/06	APV
14	20111524	10/30/06	APV
15	20111524	10/30/06	APV
16	20111524	10/30/06	APV
17	20111524	10/30/06	APV
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19	20111524	10/30/06	APV
20	20111524	10/30/06	APV
21	20111524	10/30/06	APV
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23	20111524	10/30/06	APV
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39	20111524	10/30/06	APV
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41	20111524	10/30/06	APV
42	20111524	10/30/06	APV
43	20111524	10/30/06	APV
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95	20111524	10/30/06	APV
96	20111524	10/30/06	APV
97	20111524	10/30/06	APV
98	20111524	10/30/06	APV
99	20111524	10/30/06	APV
100	20111524	10/30/06	APV





REV	ECG	DATE	APV
1			
Axcera.			
THIS PRINT IS THE PROPERTY OF AXCIERA. IT SHALL NOT BE COPIED WITHOUT PERMISSION.			
TITLE B/D, CONTROL/POWER SUPPLY ASSEMBLY, INNOVATOR LX			
MATERIAL			
FINISH			
DRAWN	REV	DATE	BY
CHK	ECG	2/2/94	1303889
REL	ECG	2/2/94	2
SCALE 1:1			



WIRE GAUGE CHART
(NATIONAL ELECTRICAL CODE DATA)

WIRE SIZE	CURRENT RATING
18AWG	6
16AWG	10
14AWG	20
12AWG	30

WIRE AT A3-J61-2 WAS
18AWG. AT POWER
SUPPLY CONNECTOR
DETAIL A2 WAS A1.

[RG]	
...	...

CO 201202/27/04 ERI

ADDED NOTE 4.
REVERSED A1-J2 AND

A1-J3 AND REQUIRED TO
MAINTAIN THE SAME

MAINTAIN THE SAME
CONNECTIONS. (RGE)

BO	201107010/27/03	181
----	-----------------	-----

REV	ECO	DATE	AP
-----	-----	------	----

1/C

OL/POWER SUPPLY

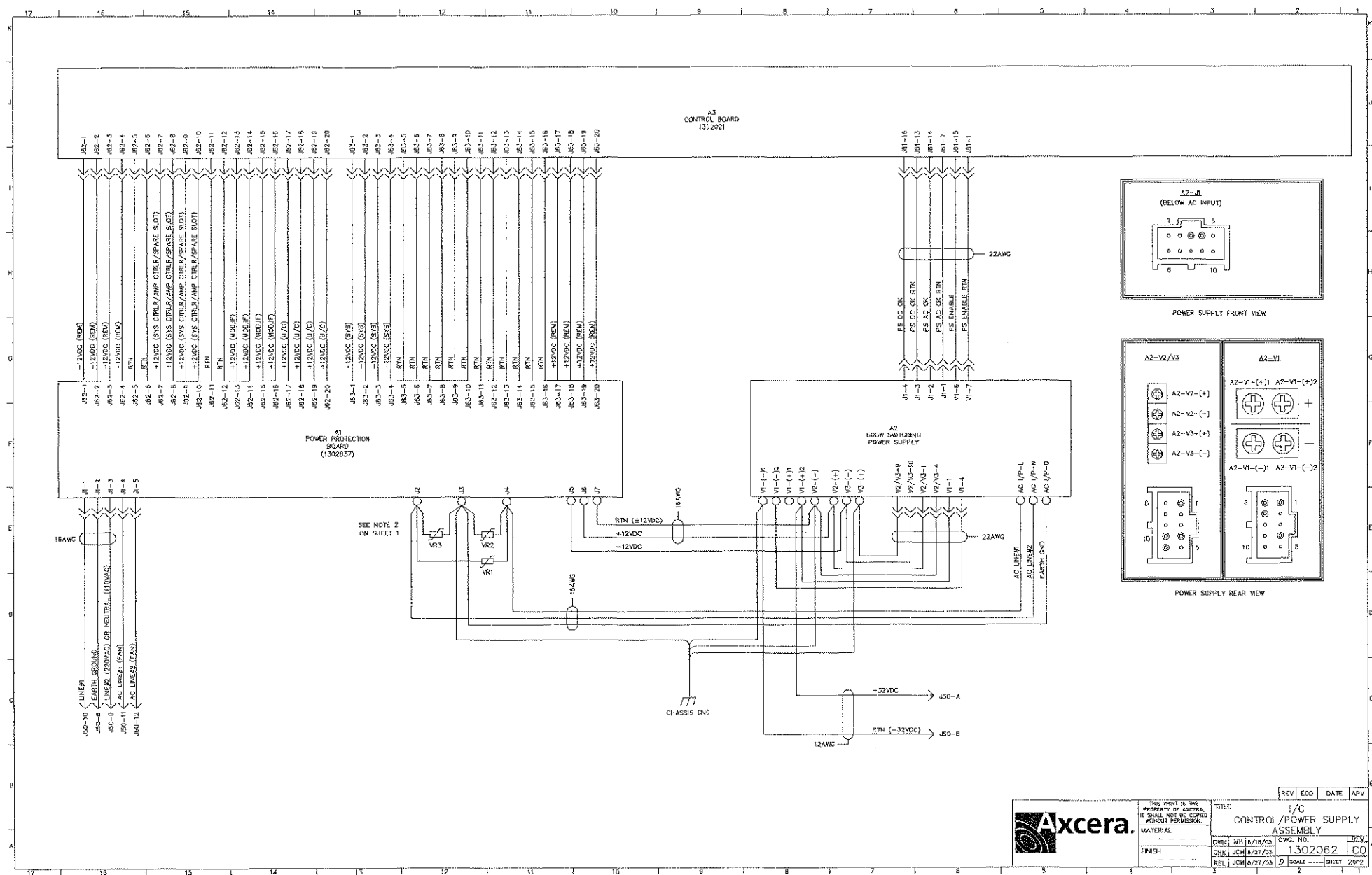
ASSEMBLY

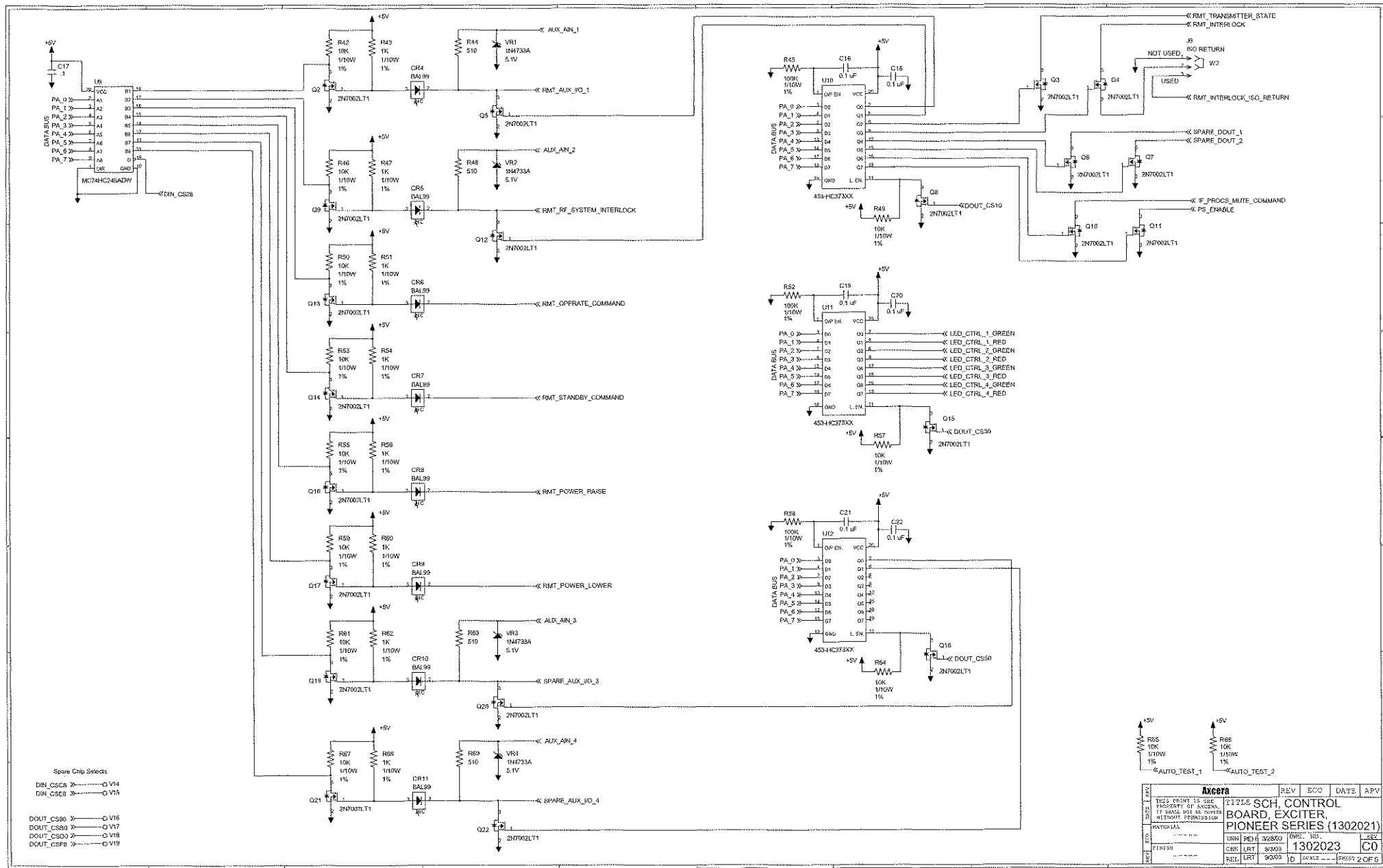
03	DWG. NO.	RE
----	----------	----

03	1302062	C
----	---------	---

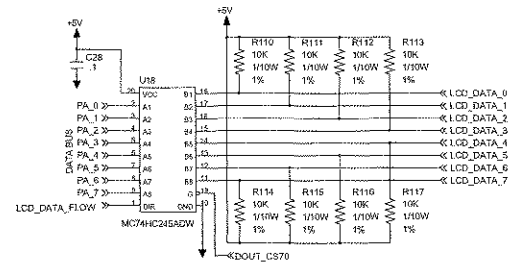
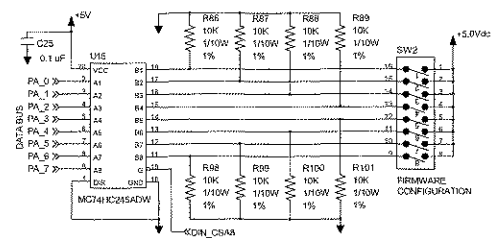
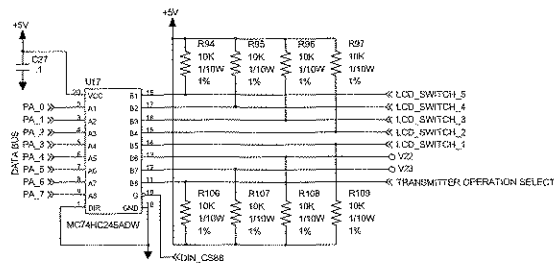
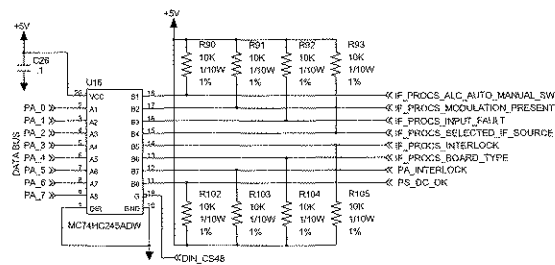
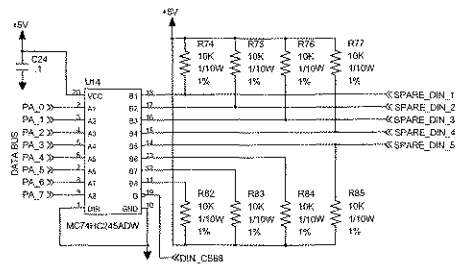
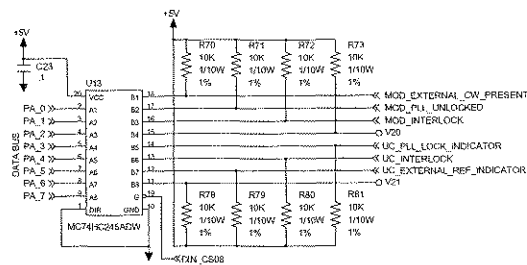
03 D SCALE ---- SHEET 1 OF 1

2 1 1

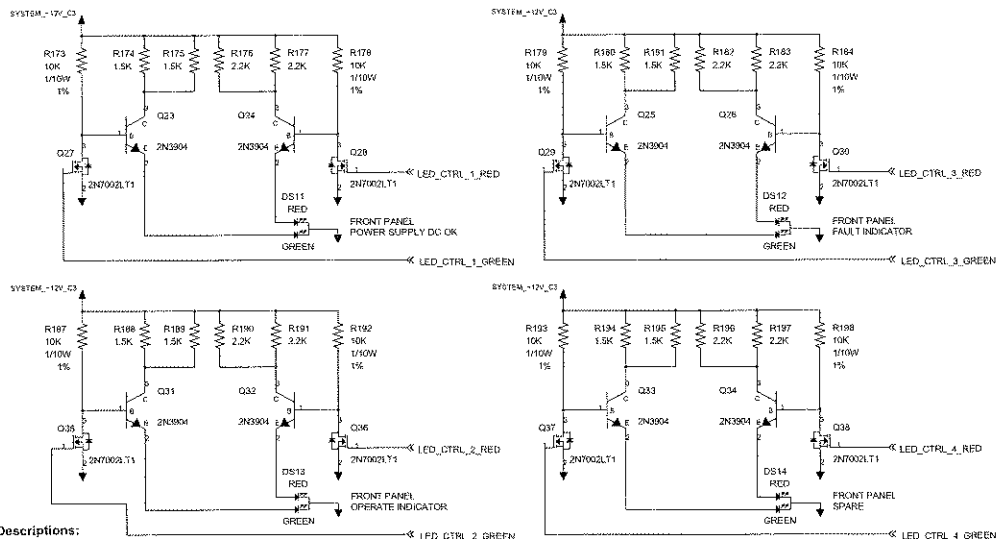




Axcera		REV	ECO	DATE	APV
THIS PRINT IS THE PROPERTY OF AXCERA. IT SHALL NOT BE REPRODUCED WITHOUT PERMISSION.		TITLE: SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)			
MATERIAL		DRN	REV	DATE	REV
FINISH		CRN	LRT	9/30/03	1302023 C0
		REL	LRT	9/30/03	1302023 C0



REV	ECO	DATE	APV
1			
Ancera THIS PRINT IS THE PROPERTY OF ANCERA. IT SHALL NOT BE COPIED WITHOUT PERMISSION.			
TITLE SCH. CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)			
ECO	DES	REV	DATE
FINISH	0801	3/28/03	0801
REV	0801	3/28/03	0801
1302023		C0	
9363		D SCALE 1:1 SHEET 3 OF 5	



Circuit Descriptions:

PAGE 1:

U1 is an Atmel Atmega128 microcontroller. This part is in-circuit programmed using the serial programming port. When the microcontroller is held in reset by either the programming port or the external watchdog IC, a transistor inverts the reset signal while serial programming lines are connected to U1 through analog switch U5.

U2 is a watchdog IC used to hold the microcontroller in reset if the supply voltage is less than 4.21 Vdc; (1.25 Vdc < Pin 4 (IN) < Pin 2 (Vcc)). The watchdog momentarily resets the microcontroller if Pin 6 (IST) is not clocked every second. A manual reset switch is provided but should not be needed.

Diodes DS1 through DS8 are used for display of auto test results. A test board is used to execute self test routines. When the test board is installed, Auto_Test_1 is held low and Auto_Test_2 is allowed to float at 5 Vdc. This is the signal to start the auto test routines.

U3 and U4 are used to selectively enable various input and output ICs found on page 2 and 3 of the schematic.

U1 has two serial ports available. In this application, one port is used to communicate with transmitter system components where U1 is the master of a RS-485 serial bus. The other serial port is used to provide serial data I/O where U1 is not the master of the data port. A dual RS-232 port driver IC and a RS-485 port driver is also in the second serial data I/O system. The serial ports are wired such that serial data input can come through one of the three serial port channels. Data output is sent out through each of the three serial port channels.

Switch SW1 is used to select either transmitter operation or exciter driver operation. When the switches of SW1 are on, transmitter operation is selected and the power monitoring lines of the transmitter's power amplifier are routed to the system power monitoring lines.

PAGE 2:

Digital output latches are used to control system devices. Remote output circuits are implemented using open drain FETs with greater than 60 Volt drain to source voltage ratings.

Remote digital inputs are diode protected with a 1 Kohm pull-up resistor to 5Vdc. If the remote input voltage is greater than about 2 volts or floating, a FET is turned on and a logic low is applied to the digital input buffer. If the remote input voltage is less than the turn on threshold of the FET (about 2 Vdc), a logic high is applied to the digital input buffer.

Four of the circuits on page two are auxiliary I/O connections wired for future use. They are wired similar to the remote digital inputs but include a FET for digital output operation. To operate these signals as an input, the associated output FET must be turned off. These circuits are also connected to an analog input multiplexer IC.

PAGE 3:

Several ICs are used as input buffers to allow the microcontroller to monitor various digital input values. Most digital inputs use a 10 Kohm pull-up resistor. The buffer IC used for data transfer to the display is wired for read and write control.

PAGE 4:

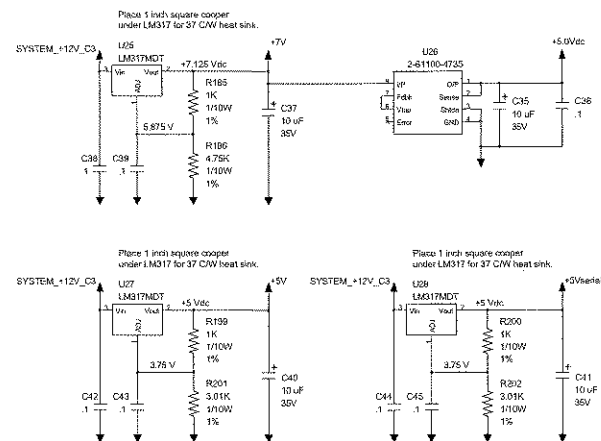
Each analog input is expected to be between 0 and 5 Vdc. If a signal exceeds 5.1 Vdc, a 0.225 Watt zener diode clamps the signals voltage. Most signals are calibrated at their source however two dual serial potentiometer ICs are used to calibrate four signals. For these four circuits, the input value is divided in half before it is applied to an op-amp. The serial potentiometer is used to adjust the input signal between 60 and 120% of the input signal. Serial data to the second serial potentiometer is transferred through the first IC. The wiper position of the digital potentiometer circuit is used to set the gain of the op-amp. Lower digital values for the wiper setting increases the gain of the op-amp. If N = 0, gain = 6.0. If N = 255, gain = 3.00. If Vin = 1.0 at spare_Ain_1 and N = 128, U21A out = 4.0V with gain = 4.

Two 20 position connectors are used to provide power to the backplane. J62 and J63 get power from the power supply after a nominal 3 amp resettable fuse. The Raychem polyswitch resettable fuses may open on a current as low as 2.43 amps at 50C, 3 amps at 25 C or 3.3 amps at 0C. They definitely will open when the current is 4.86 amps at 50C, 6 amps at 20C, or 6.6 amps at 0C. Trace widths of these circuits are 0.140" (designed for maximum current).

PAGE 5:

Each of the four LED circuits drive a dual element common cathode LED. To make a good amber color, the current applied to the green element is slightly greater than the red element.

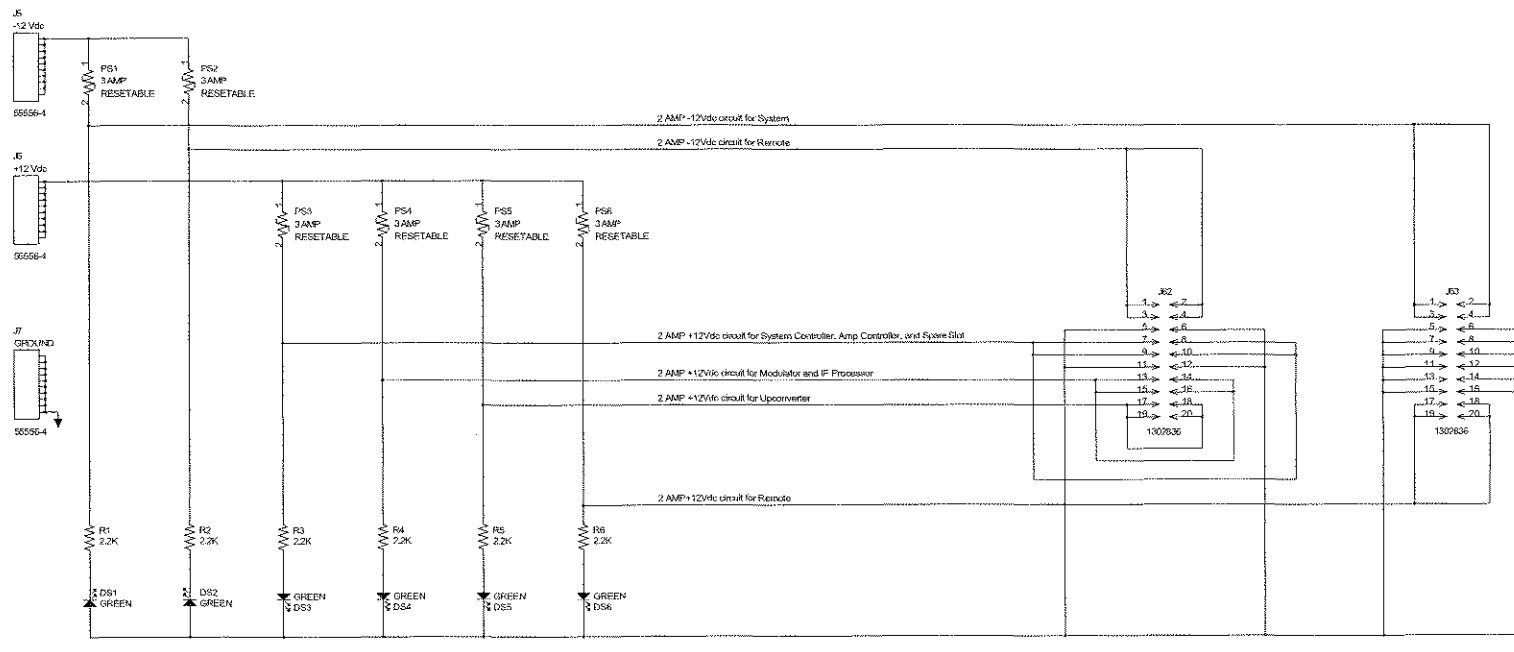
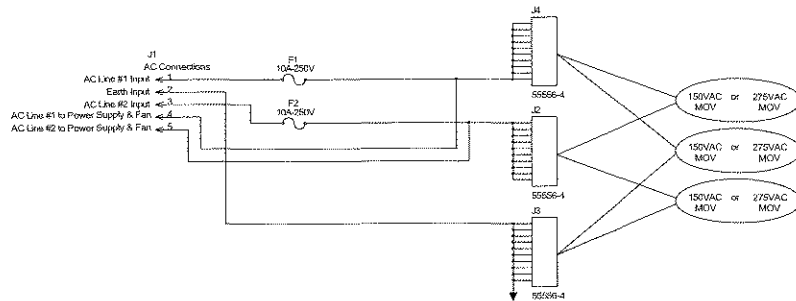
Several voltage regulators are used to power the board. Seven volts is typically applied to board LEDs and to the input of a precision 5.0 volt regulator. The 5.0 volt regulator is used for analog circuits and the microcontroller analog reference voltage. Another two 5 volt regulator circuits are used for most other board circuits.



LAST USED REF:

R202
C49
Q47
DS14
U28
VR22
J63
TP17
V72
SW2
CR11
W2
Y1
L2
S1

Axcera		REV	ECO	DATE	APV
THIS DRAWING IS THE PROPERTY OF AXCERA. IT SHALL NOT BE COPIED WITHOUT PERMISSION.		TITLE SCH. CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)			
MATERIAL		DRW	REV	3/28/03	DRG. NO.
FINISH		CHG	1RT	9/3/03	1302023
REF		LRT	9/3/03	10	SCALE 1:1 SHEET 5 OF 5



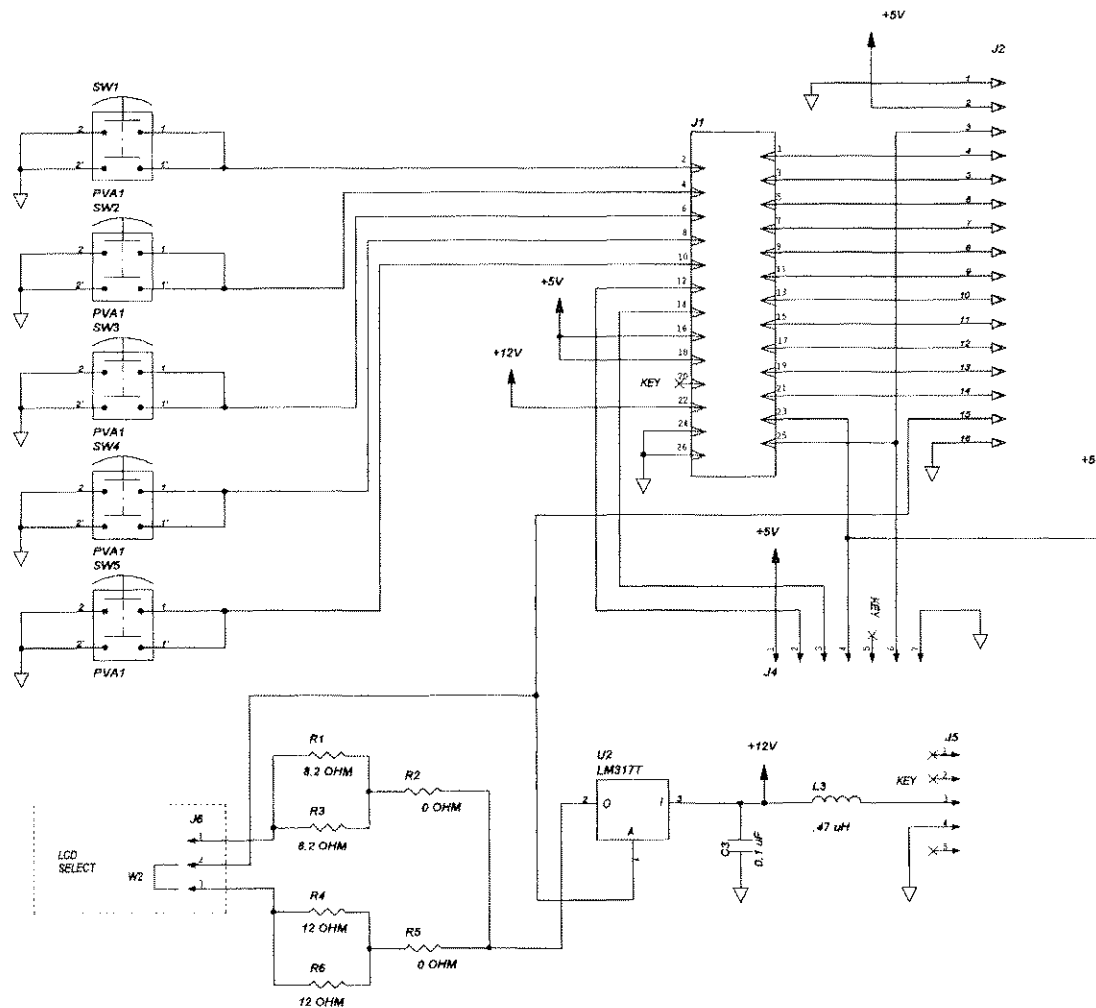
Circuit Design Notes:

1. Track widths of 0.140 inch minimum top and bottom of board shall be used to connections to J1, J2, J3, J4.
2. Track widths of 0.140 inch minimum top of board shall be used to connections to J5 and J6.
3. Track widths of 0.065 inch minimum shall be used to connections to J2 and J3.
4. Track widths of 0.020 inch minimum shall be used to connections between LEDs and resistors.
5. Board BOM needs the following items added to those exported from Orcad:

Part Number	Qty	Description
102071	4	Fuse Clip, PTC DO Mnt., 15 Amp

MATERIAL NUMBERS:
1302838 PCB, PIONEER, POWER PROTECT
1302839 SCH, PIONEER, PWR PROTECT
1302840 STENCIL FOR 1302839

Axcera		REV	ECO	DATE	APV
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DRAWN	REV	52003	DWG. NO.	REV.	
CHECK	REV	52003	1302839	AO	
REL	REV	52003	D	SCALE	SHEET 1 OF 1



DELETED C1, C2, L1, L2,
U1, J3, & W1. MOVED
W2 FROM J6-1,-2 TO J6
-2,-3. JKF

3 8603 11/7/96 8/18

AT J2 W2 WAS W1. (TMY)

2 8424 9/29/96 JCM

SWITCHED PINS 1 & 2 OF
U2 (TMY)

1 8368 8/27/96 RAS

REV ECN DATE APV

ITS CORPORATION

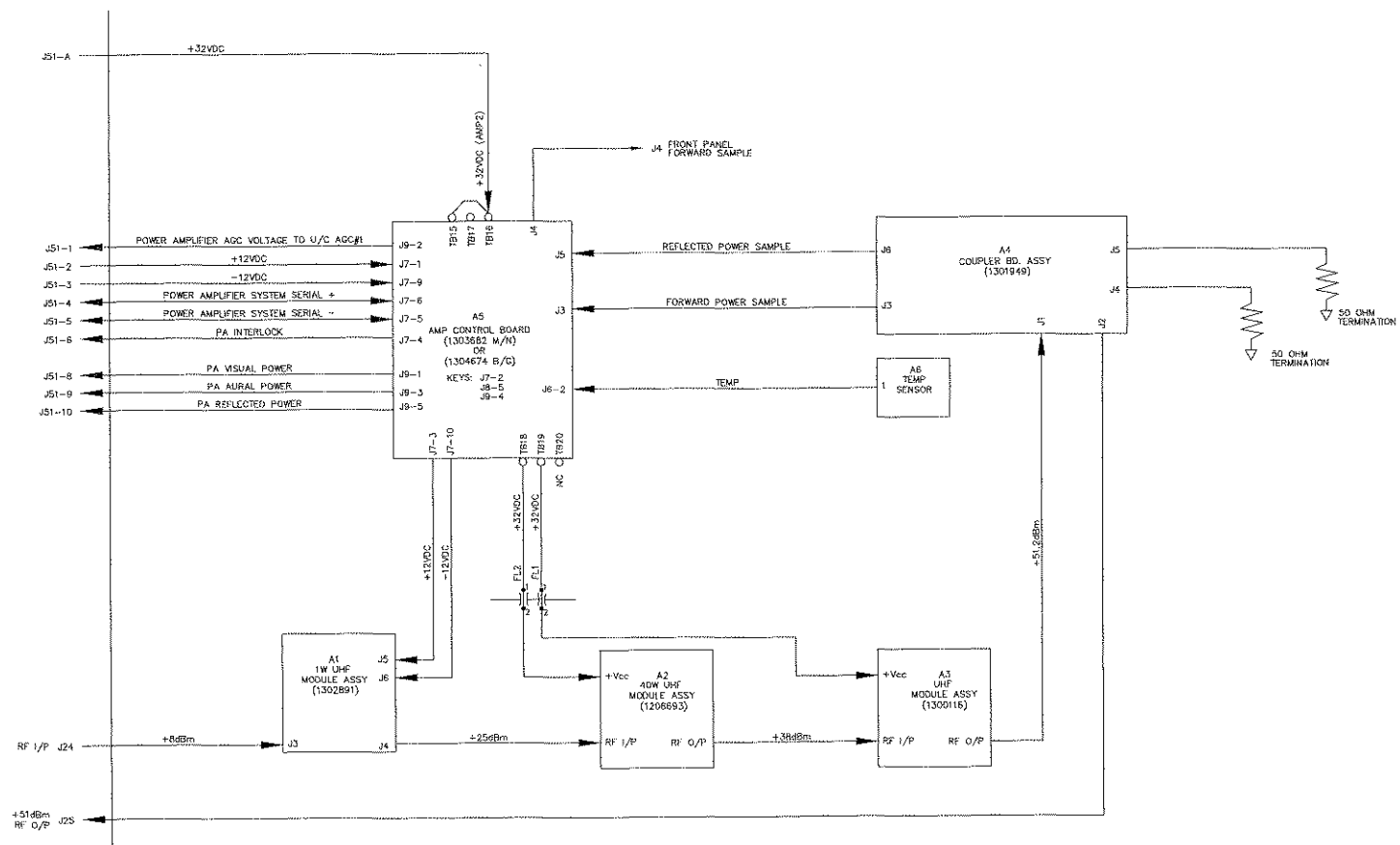
THIS PRINT IS THE
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WITHOUT PERMISSION

TITLE SCHEMATIC
SWITCH BOARD
(1527-1406)

MATERIAL
FINISH

DWN DLM 6/3/96
CHK RAS 6/14/96
REL RAS 6/14/96

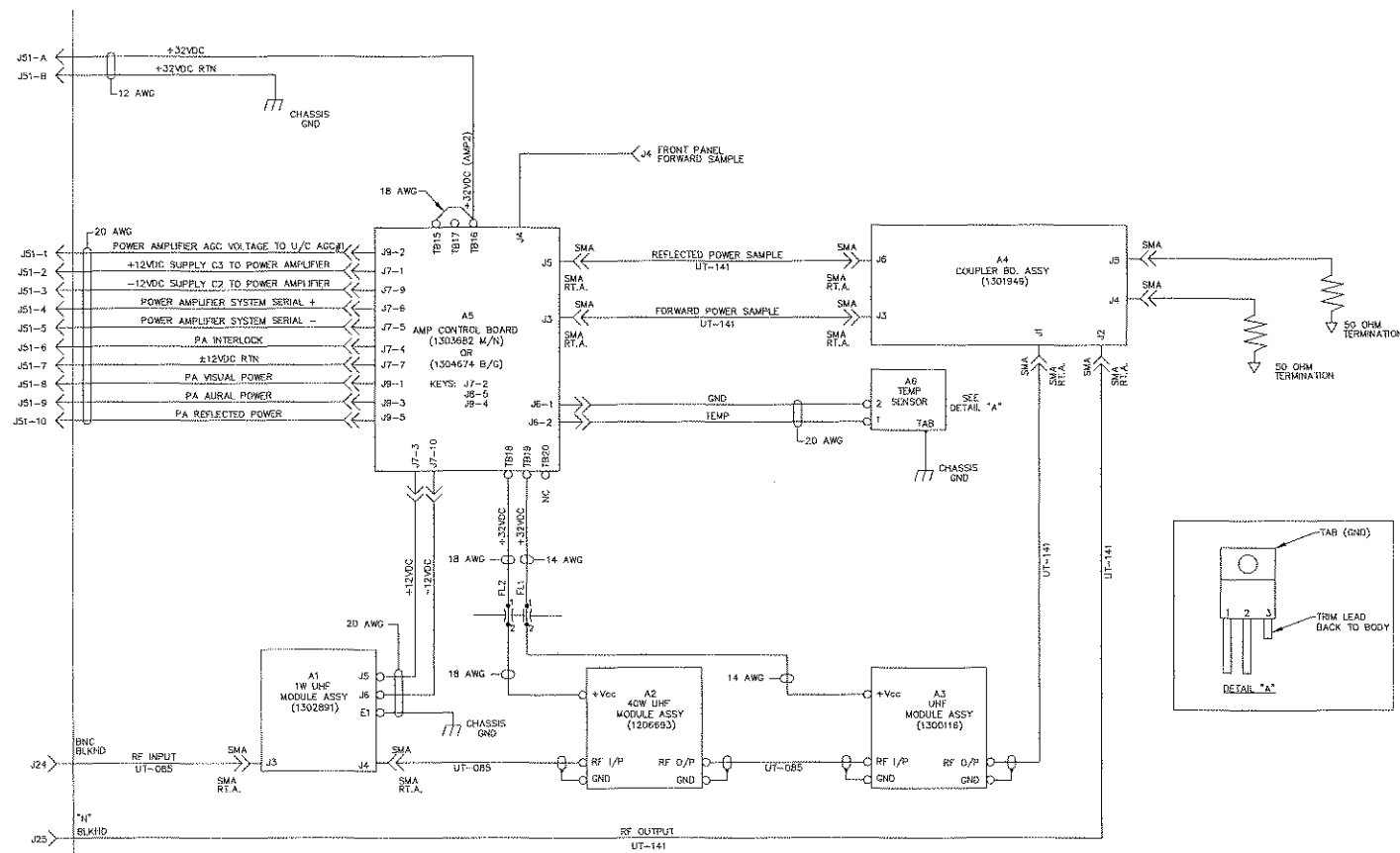
DWG. NO. 1527-3406
REV 3
SCALE SHEET 1 OF 1



NOTE:
1. ALL POWER LEVELS ARE PK-SYNC +10% AURAL FOR DTV LEVELS, SUBTRACT 3dBm.

AS WAS 1301982. (RGE)
CO 12/15/04 RCH
AT A4, REVERSED J3 AND J6. (RGE)
RG 12/15/04
REV ECO DATE LRT

		TITLE		B/D	
		PA ASSEMBLY, 100W LX SERIES		C0	
MATERIAL	---	DWG. NO.	1303850	REV	A
FINISH	---	SCALE	1/16/04	SHEET	1 OF 1

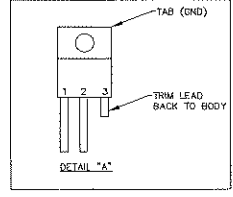
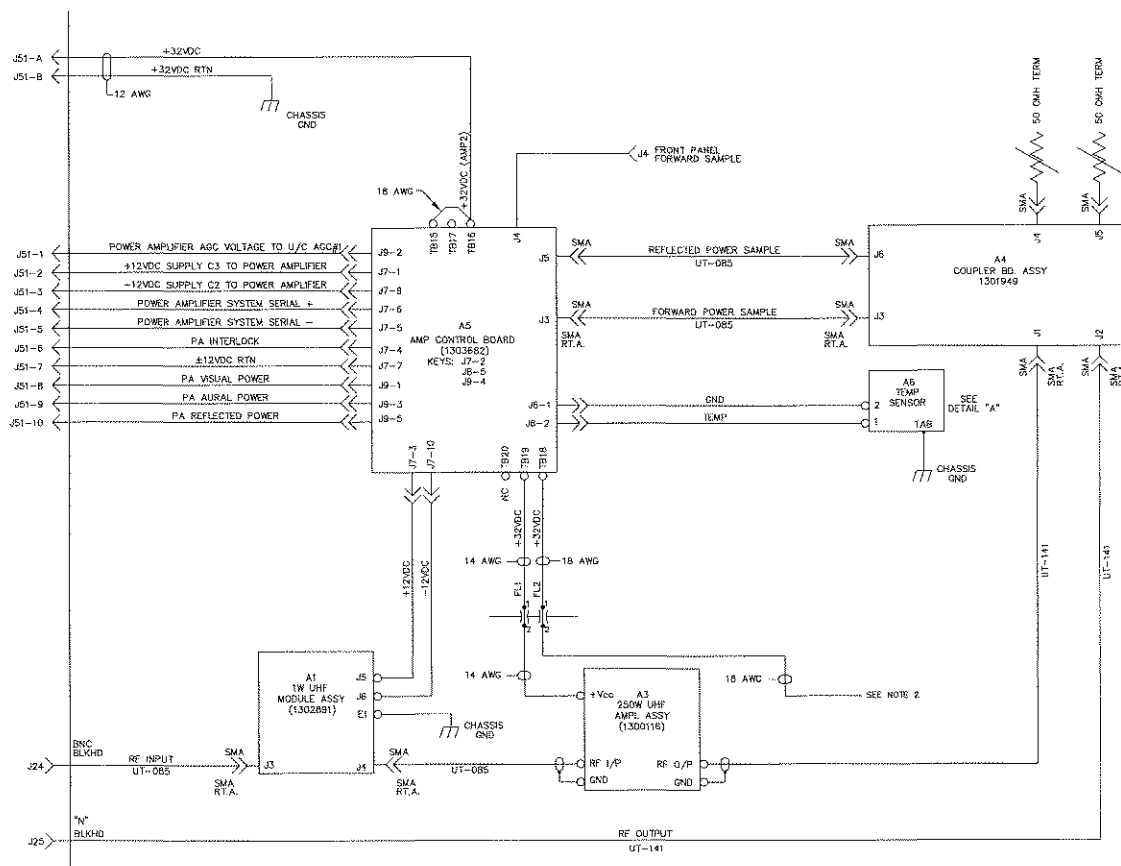


NOTE:
1. ALL WIRE IS 18AWG UNLESS OTHERWISE NOTED.

AS WAS 1301962. (RGE)
CD 2011280/2/15/04 18H
AT A4, REVERSED J3 AND
J6. WIRE AT A5-J7-7
WAS 18 AWG. (RGE)
BD 2011245 5/7/04 LRT
REV ECO DATE APV



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MATERIAL		1/C.	
FINISH		PA ASSEMBLY, 100W LX SERIES	
DWG. NO.	1303814	REV.	CO
CHK. LRT	1/16/04	SCALE	1 OF 1
REL. LRT	1/16/04	SCALE	1 OF 1

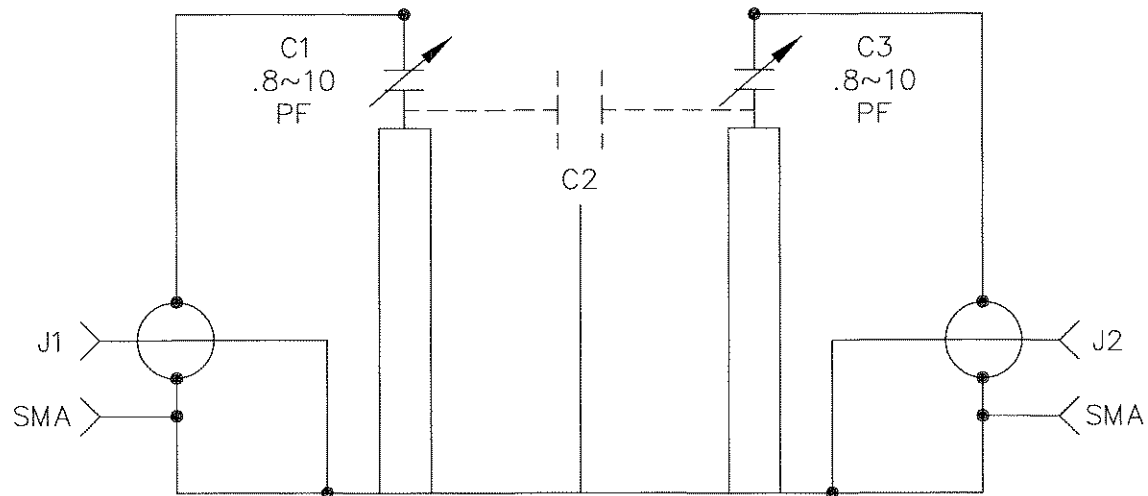


NOTE:
 1. ALL WIRE IS 20AWG UNLESS OTHERWISE NOTED.
 2. THIS WIRE IS NOT USED ON THIS ASSEMBLY. COVER THE END WITH HEAT SHRINKABLE TUBING AND 10" BACK IN THE HARNESS.

A4 WAS 1227-1316, ADDED COAX FROM A4-J6 TO A5-J5	REV	ECO	DATE	APV
ADDED 50 OHM TERMINATIONS AT A4.				
CS 1301949 12/05 1301				
DELETED 50 OHM TERMINATION AT A5-J5. (RSC)				
BD 1301949 05/05 1301				

	THIS PRINT IS THE PROPERTY OF AXCCERA. IT SHALL NOT BE COPIED WITHOUT PERMISSION.		TITLE	
	MATERIAL		PA ASSEMBLY, 2KW DRIVER/ 10 W PA, I.X. SERIES	
	FINISH		OWN: RCE/17/04 CNC: LRT/17/04 REL: LRT/17/04	
			ENG. NO. 1305137 CO	

REV	ECO	DATE	APV



NOTE: C2 IS STRAY CAPACITANCE
BETWEEN LINE SECTIONS.



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MATERIAL

— — — —

FINISH

— — — —

TITLE

SCHEMATIC —
UHF FILTER

DWN DD 9/13/83

CHK RWZ 9/13/83

REL RWZ 7/20/90

DWG. NO.

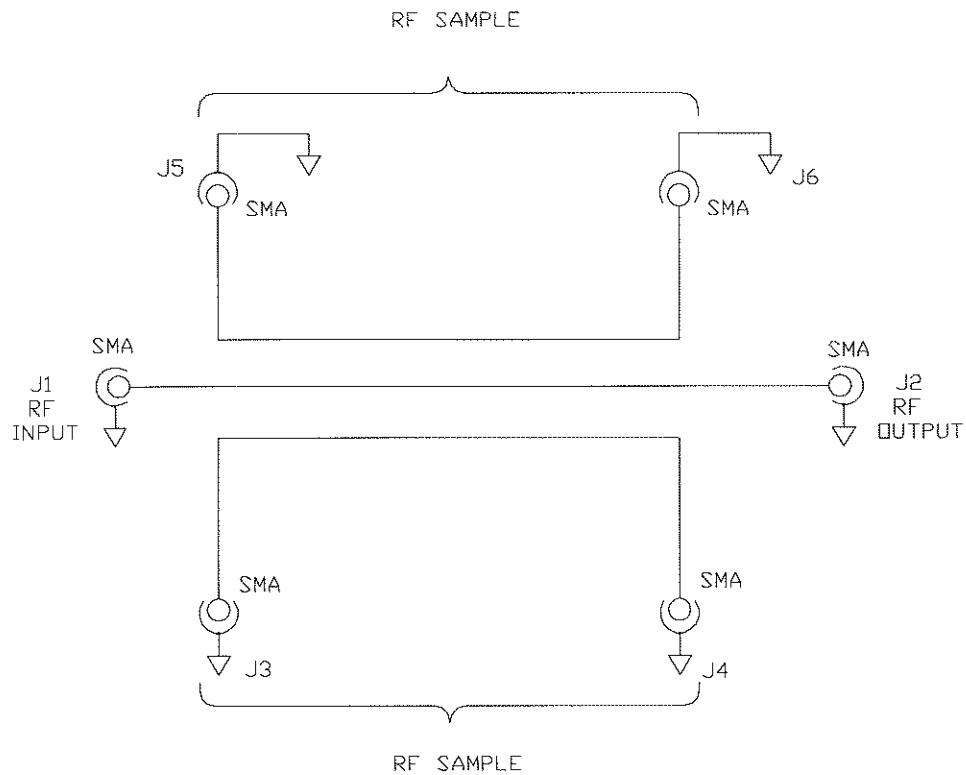
1007-3101

REV

0

SCALE — —

SHEET 1 OF 1



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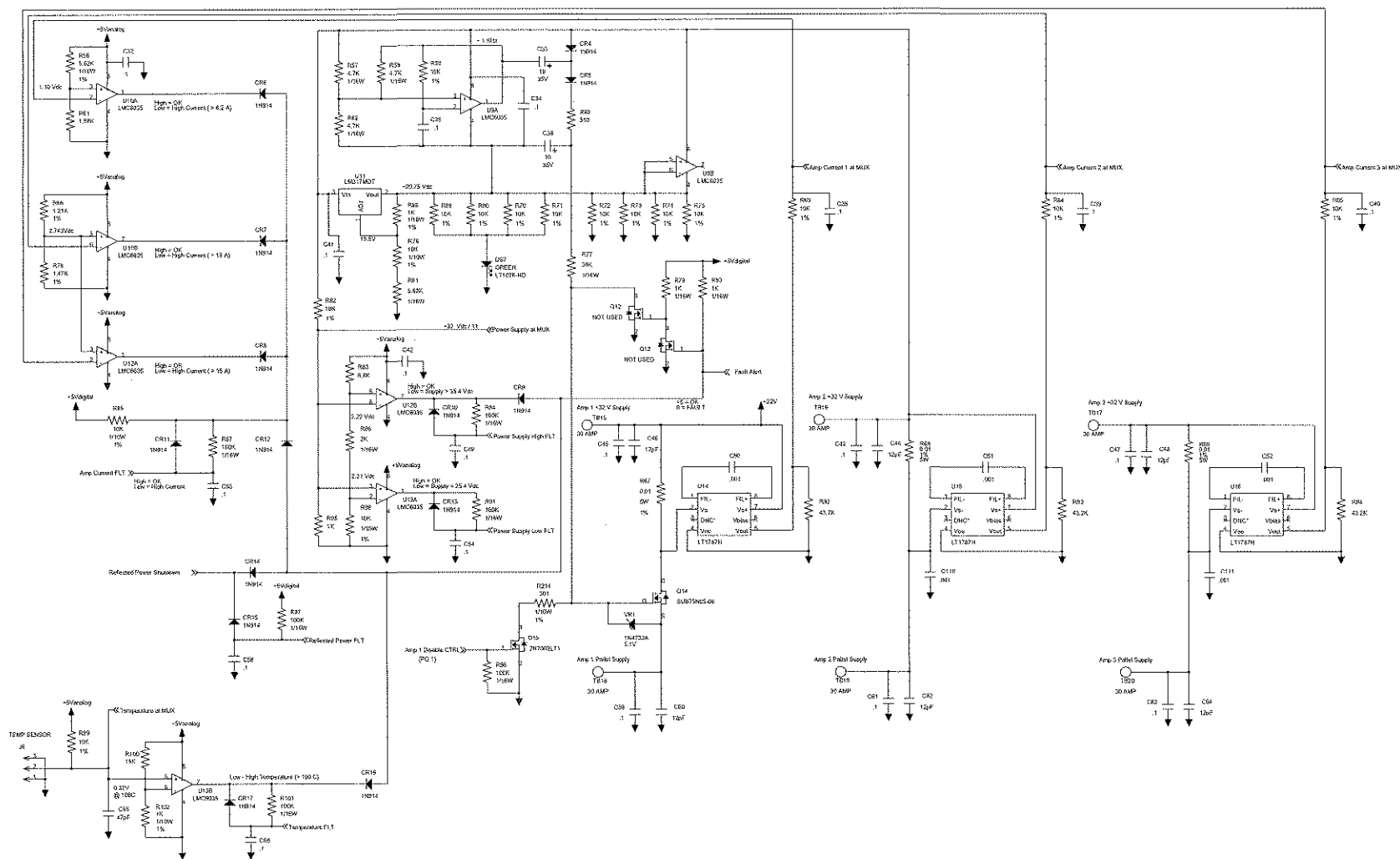
MATERIAL
- - - -

FINISH
- - - -

TITLE
SCHEMATIC
DIRECTIONAL COUPLER
BOARD

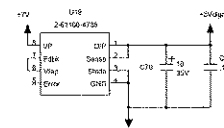
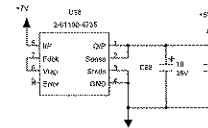
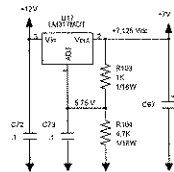
DWN	MH	8/11/03	DWG. NO.	REV
CHK	JCM	8/25/03	1303152	A0
REL	JCM	8/25/03	B SCALE ---	SHEET 10F1

REV	ECD	DATE	APV
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NOTE:

A track width of 0.3 inch is needed between power input vias and sense resistors R55, R56, R57. 0.3 inch track width is also needed between the output of the sense resistors and the output vias that provide power to the amplifier pallets.



Ancera		REV	ECO	DATE	APV
TITLE		SCH., AMP			
CONTROL, INNOVATOR LX		(1303682)			
MATERIAL					
DESIGN		DWG. NO.	12/16/03	1303683	H0
CHECK		REV.	12/16/03	3	2 OF 3

