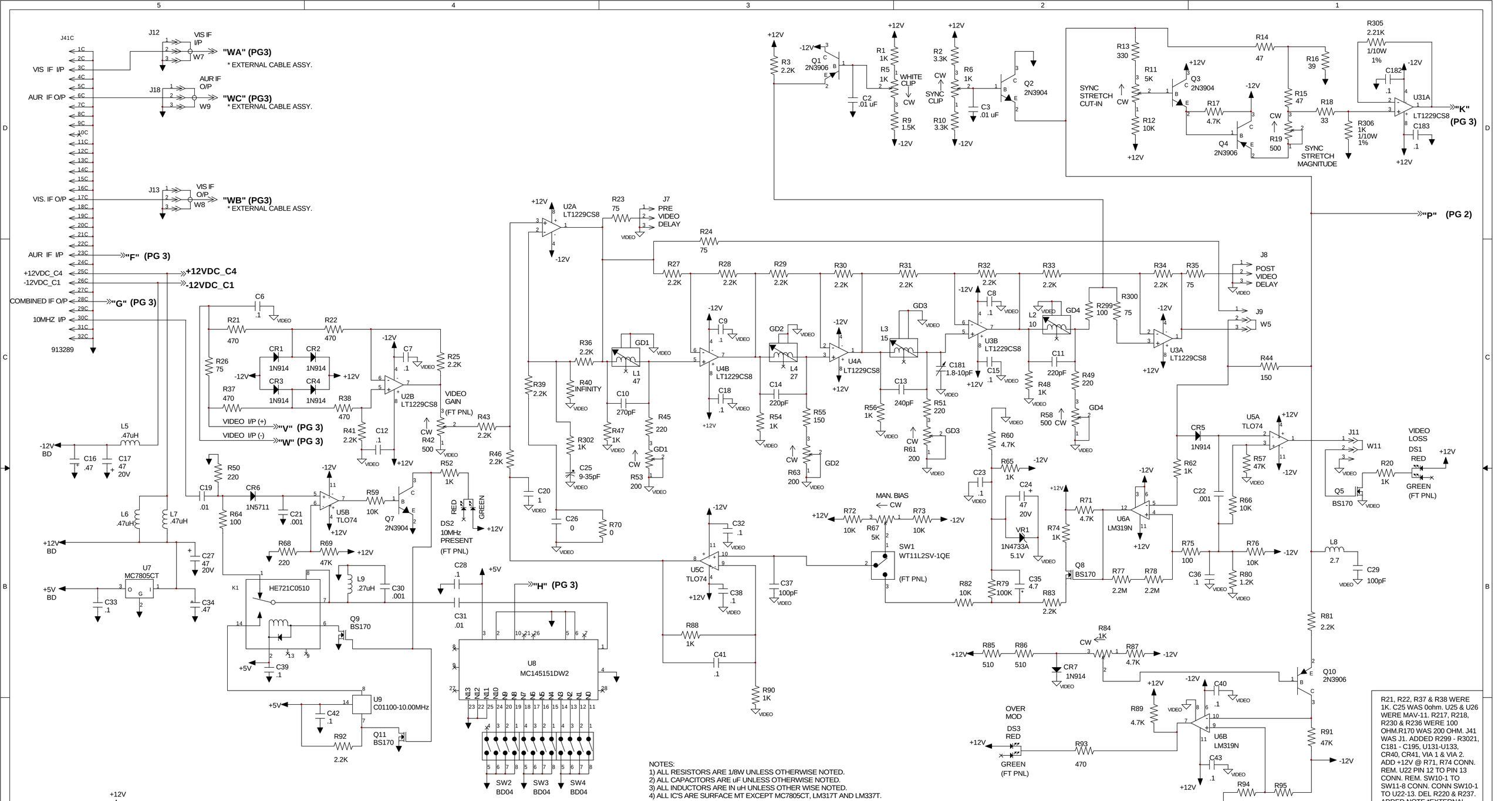

NOTES:
1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHER WISE NOTED.
4) ALL IC'S ARE SURFACE MT EXCEPT MC7805CT, LM317T AND LM337T.
5) ALL TRANSISTORS ARE SURFACE MT.
6) ALL PASSIVE COMPONENTS ARE SURFACE MOUNT EXCEPT: SWITCHES, VARIABLE CAPS, COILS, POTS, MV209 , MVAM108, DIPPED MICA CAPS, LEDS, CONNECTORS.
7) J1 IS A 96 PIN DIN.
8) VIA 3, 4, 5, & 6 CONNECTS IF GND TO MAIN GND.
9) VIA 1 & 2 CONNECTS VID GND TO MAIN GND.
10) VIA 7 & 8 CONNECTS AUDIO GND TO MAIN GND.
11) W7 CONNECTS J12-J14.
12) W8 CONNECTS J13-J17.
13) W9 CONNECTS J18-J21.
14) W10 CONNECTS J19-J20.

R21, R22, R37 & R38 WERE 1K. C25 WAS 0ohm. U25 & U26 WERE MAV-11. R217, R218, R230 & R236 WERE 100 OHM.R170 WAS 200 OHM. J41 WAS J1. ADDED R299 - R3021, C181 - C195, U131-U133, CR40, CR41, VIA 1 & VIA 2. ADD +12V @ R71, R74 CONN. REM. U22 PIN 12 TO PIN 13 CONN. REM. SW10-1 TO SW11-8 CONN. CONN SW10-1 TO U22-13. DEL R220 & R237. ADDED NOTE *EXTERNAL CABLE ASSY. FOR W7-W10 CONN. JKF

REV	ECO	DATE	APV
B0	20110968	9/3/03	LRT

Axcera

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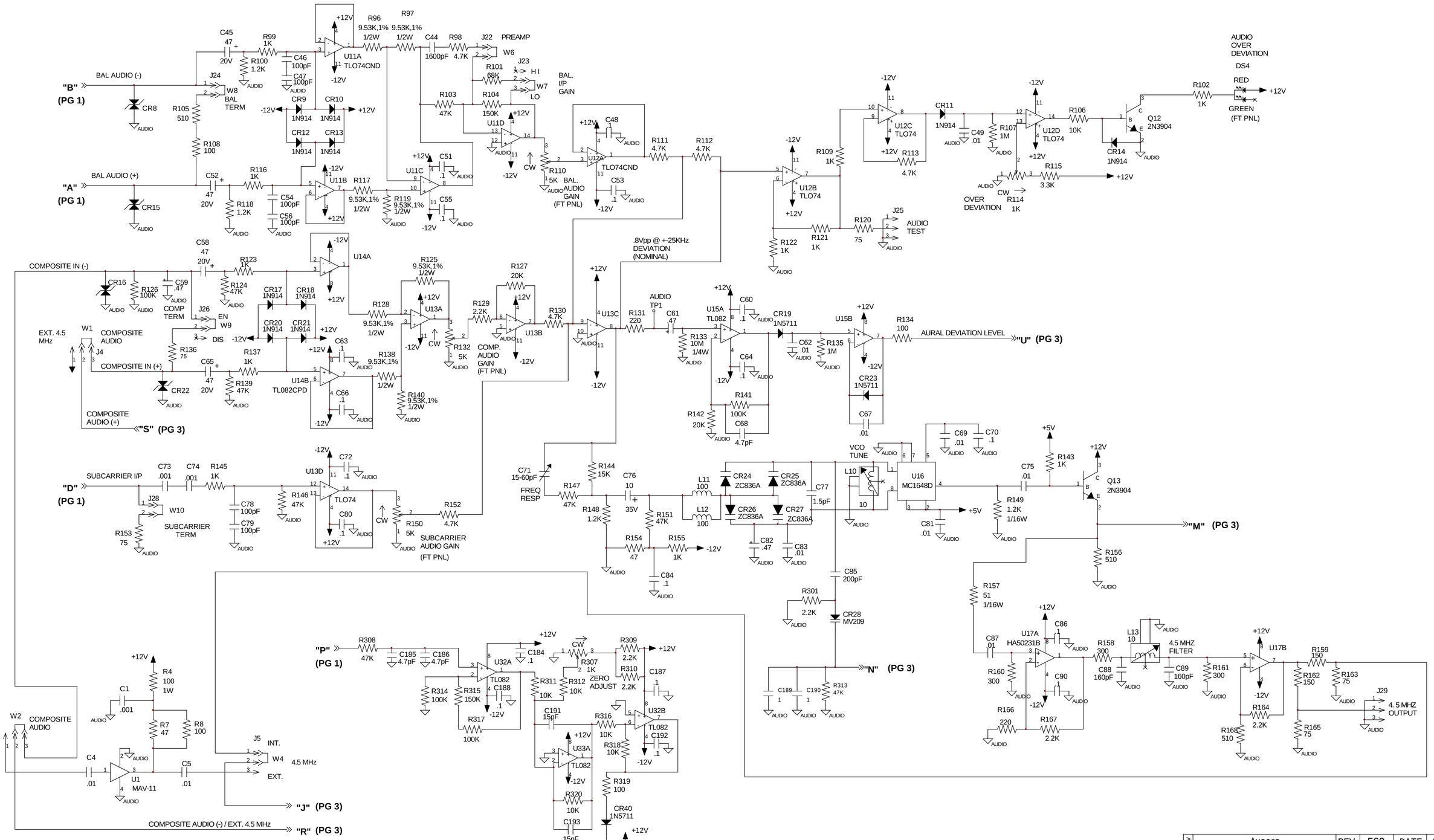
MATERIAL: - - - - -

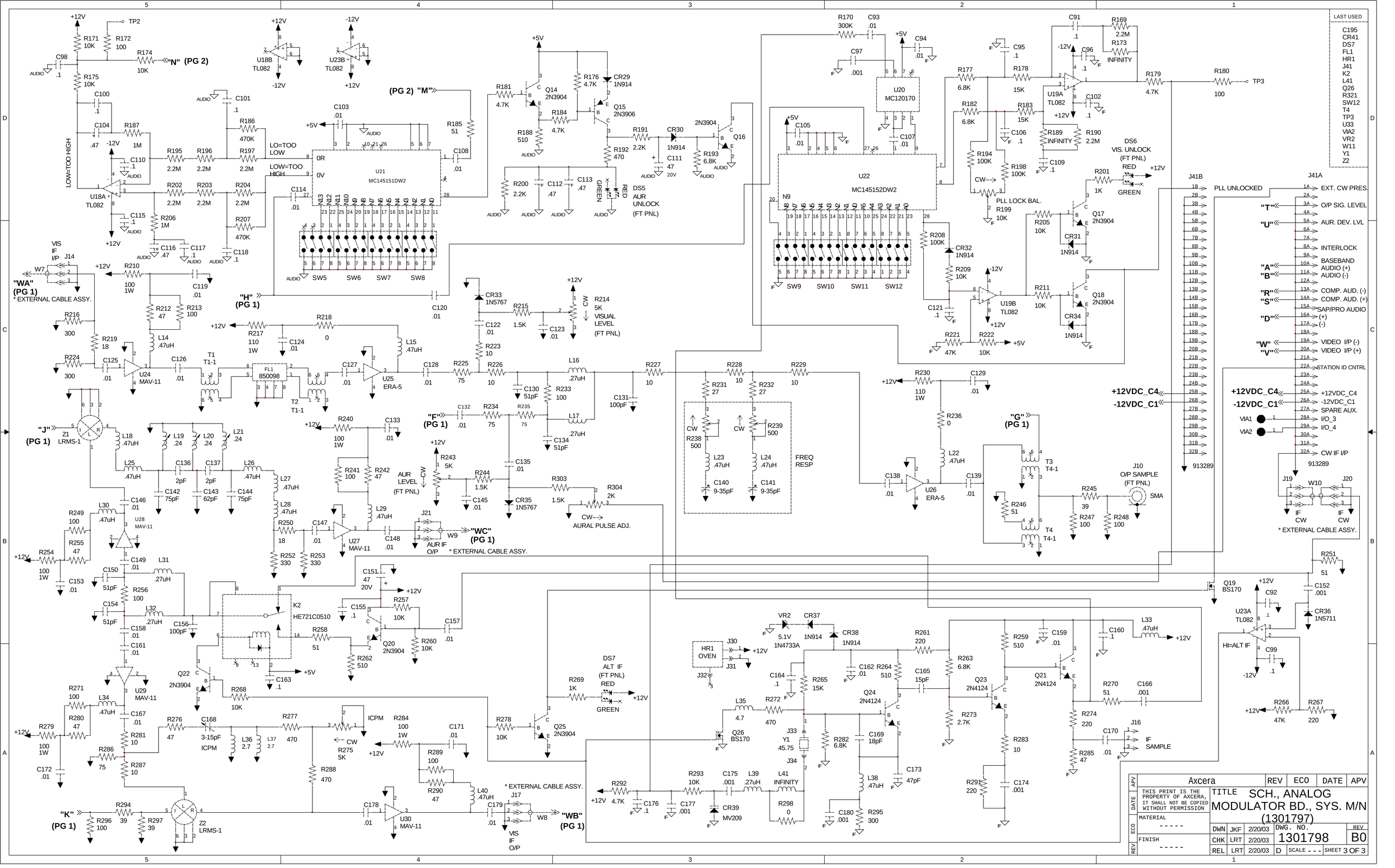
FINISH: - - - - -

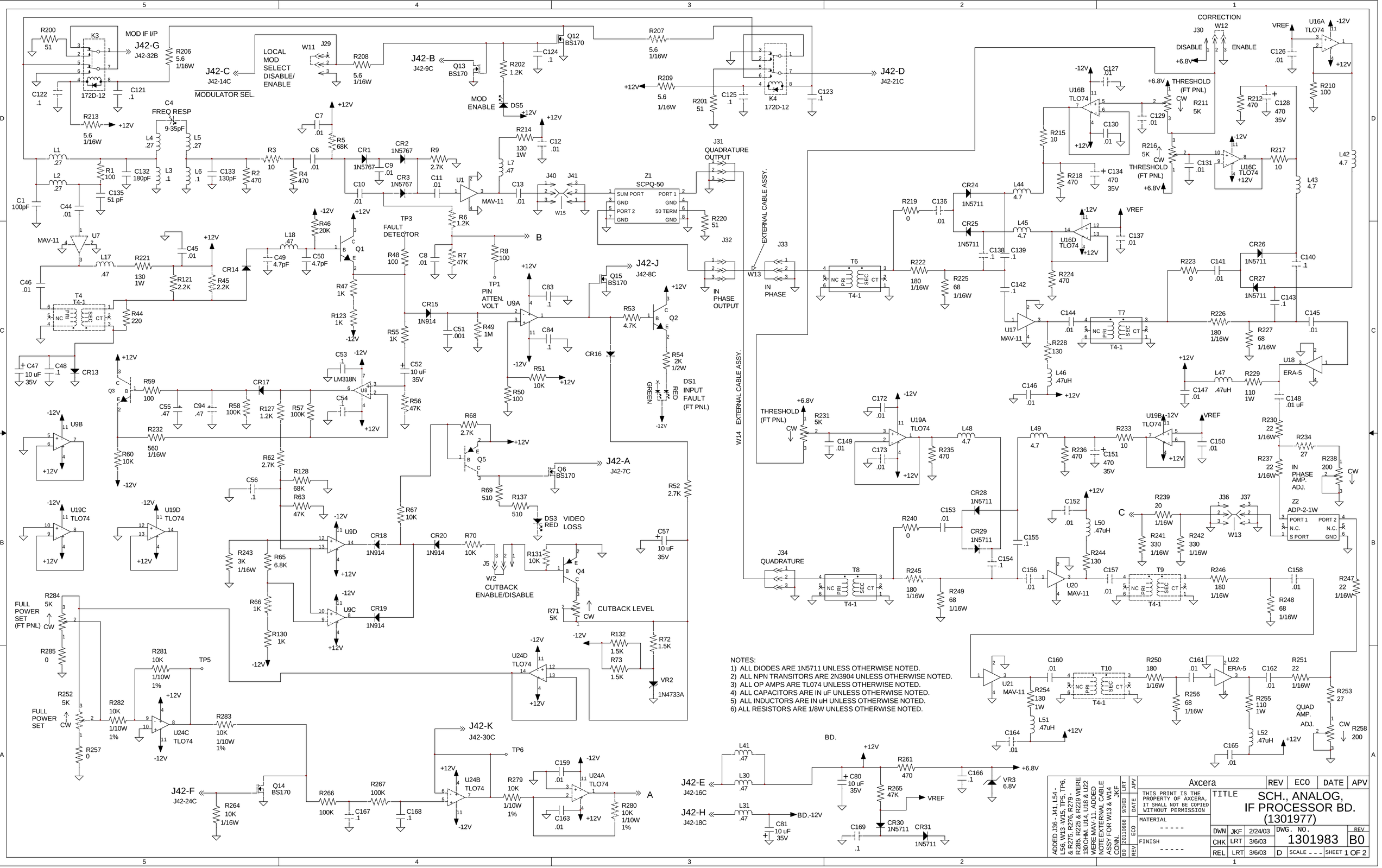
TITLE: SCH., ANALOG MODULATOR BD., SYS. M/N (1301797)

DWN	JKF	2/20/03	DWG. NO. 1301798
CHK	LRT	2/20/03	REV B0
REL	LRT	2/20/03	D SCALE - - - SHEET 1 OF 3



APV	Axcera	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH., ANALOG MODULATOR BD., SYS. M/N (1301797)			
ECO	MATERIAL -----	DWN JKF 2/20/03	DWG. NO. 1301798		REV B0
REV	FINISH -----	CHK LRT 2/20/03			
		REL LRT 2/20/03	D	SCALE - - -	SHEET 2 OF 3


LAST USED
C195
CR41
DS7
FL1
HR1
J41
K2
L41
Q26
R321
SW12
T4
TP3
U33
VIA2
VR2
W11
Y1
Z2
"N" (PG 2)
"M" (PG 2)
"H" (PG 1)
"WA" (PG 1)
* EXTERNAL CABLE ASSY.
"J" (PG 1)
"F" (PG 1)
"WC" (PG 1)
"K" (PG 1)
"WB" (PG 1)
"G" (PG 1)
LOW=TOO HIGH
LO=TOO LOW
LOW=TOO HIGH
U21
MC145151DW2
U22
MC145152DW2
U20
MC120170
DS5
AUR UNLOCK
(FT PNL)
DS6
VIS. UNLOCK
(FT PNL)
PLL LOCK BAL.
R199
10K
R214
5K
VISUAL
LEVEL
(FT PNL)
AUR
LEVEL
(FT PNL)
R243
5K
R275
5K
R303
1.5K
R304
2K
CW
AURAL PULSE ADJ.
AUR IF
O/P
VIS
IF
O/P
VIS
IF
I/P
ICPM
FREQ
RESP
J10
O/P SAMPLE
(FT PNL)
SMA
DS7
ALT IF
(FT PNL)
HR1
OVEN
HI=ALT IF
IF
SAMPLE
J41B
PLL UNLOCKED
J41A
EXT. CW PRES.
O/P SIG. LEVEL
AUR. DEV. LVL
INTERLOCK
BASEBAND
AUDIO (+)
AUDIO (-)
COMP. AUD. (-)
COMP. AUD. (+)
SAP/PRO AUDIO
(+)
(-)
VIDEO I/P (-)
VIDEO I/P (+)
STATION ID CNTRL
+12VDC_C4
-12VDC_C1
SPARE AUX.
I/O_3
I/O_4
CW IF I/P
913289
J19
W10
J20
IF
CW
* EXTERNAL CABLE ASSY.
Axcera
REV
ECO
DATE
APV
THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION
TITLE
SCH., ANALOG
MODULATOR BD., SYS. M/N
(1301797)
MATERIAL
FINISH
DWN JKF 2/20/03
CHK LRT 2/20/03
REL LRT 2/20/03
DWG. NO.
1301798
REV
B0
SCALE
SHEET 3 OF 3


MOD IF I/P
J42-G
J42-32B
J42-C
J42-14C
MODULATOR SEL.
LOCAL MOD SELECT DISABLE/ ENABLE
J42-B
J42-9C
J42-D
J42-21C
J42-J
J42-8C
J42-A
J42-7C
J42-K
J42-30C
J42-E
J42-16C
J42-H
J42-18C
J42-F
J42-24C
FREQ RESP
MODULATOR
MOD ENABLE
FAULT DETECTOR
PIN ATTEN. VOLT
QUADRATURE OUTPUT
IN PHASE OUTPUT
EXTERNAL CABLE ASSY.
W14 EXTERNAL CABLE ASSY.
INPUT FAULT (FT PNL)
VIDEO LOSS
CUTBACK ENABLE/DISABLE
CUTBACK LEVEL
FULL POWER SET (FT PNL)
FULL POWER SET
CORRECTION
DISABLE
ENABLE
THRESHOLD (FT PNL)
IN PHASE AMP. ADJ.
QUAD AMP. ADJ.
Z1 SCPQ-50
Z2 ADP-2-1W
Axcera
SCH., ANALOG, IF PROCESSOR BD. (1301977)
DWG. NO. 1301983
REV B0
SHEET 1 OF 2
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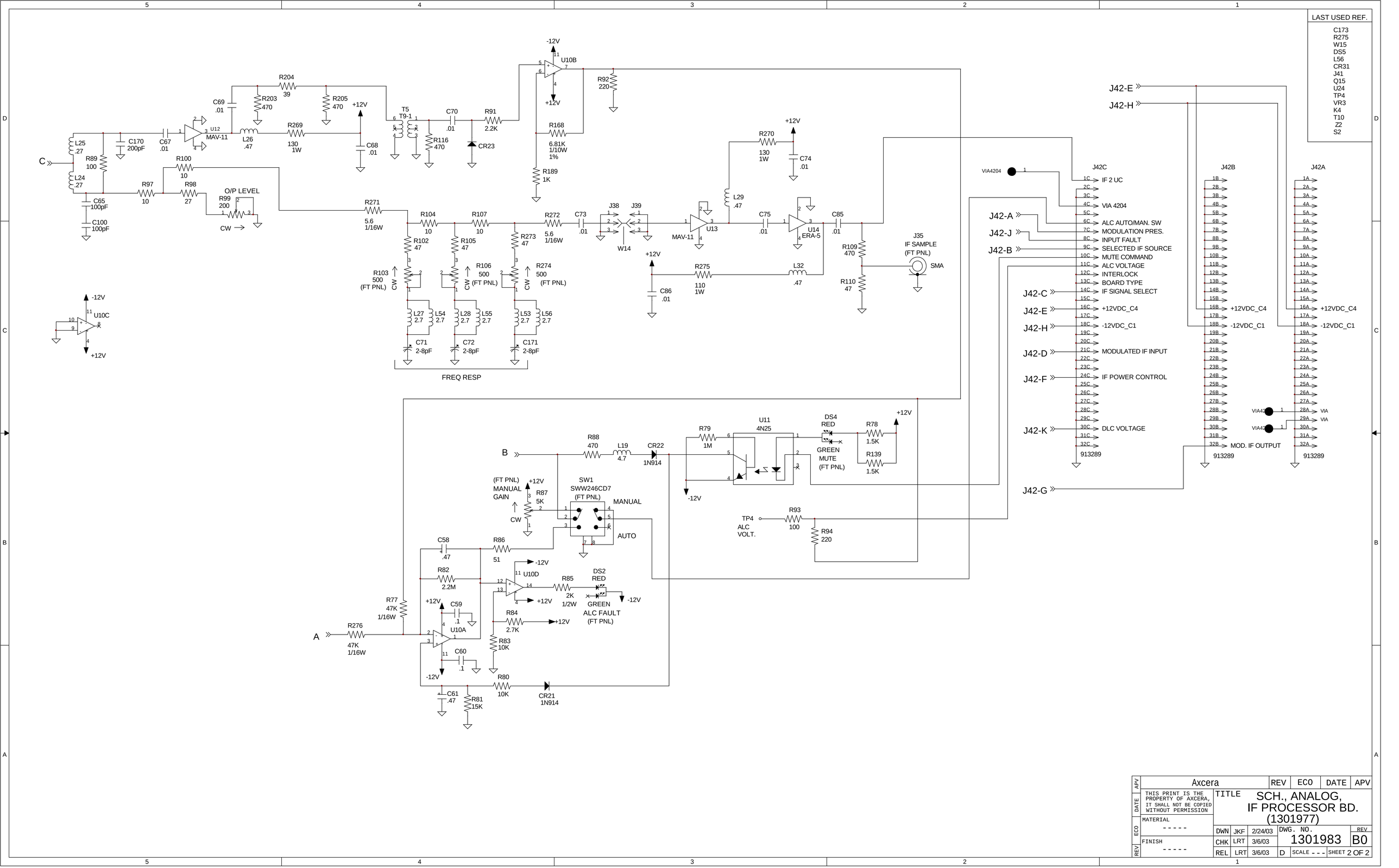
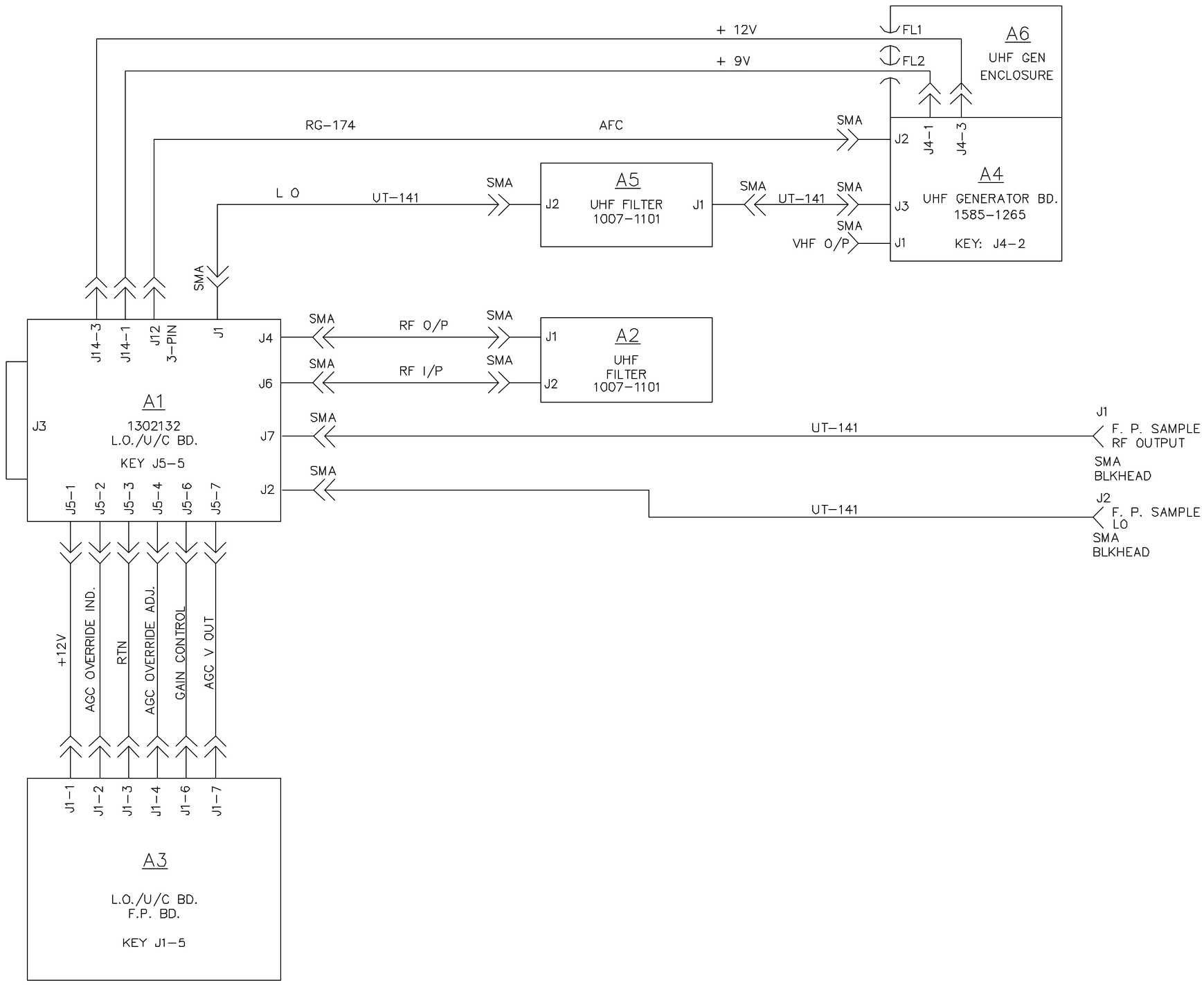
ADDED J36 - J41, L54 - L56, W13 -W15, TP5, TP6, & R275, R276, R279 - R285, R225 & R229 WERE 130OHM. U14, U18 & U22 WERE MAV-11. ADDED NOTE EXTERNAL CABLE ASSY FOR W13 & W14 CONN.
NOTES:
1) ALL DIODES ARE 1N5711 UNLESS OTHERWISE NOTED.
2) ALL NPN TRANSITORS ARE 2N3904 UNLESS OTHERWISE NOTED.
3) ALL OP AMPS ARE TL074 UNLESS OTHERWISE NOTED.
4) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
5) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.
6) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.



APV	Axcera	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE	SCH., ANALOG, IF PROCESSOR BD. (1301977)		
ECO	MATERIAL -----	DWN JKF 2/24/03	DWG. NO. 1301983	REV B0	
REV	FINISH -----	CHK LRT 3/6/03			
		REL LRT 3/6/03	D	SCALE - - -	SHEET 2 OF 2



NOTES:

1) ALL WIRES 22AWG UNLESS OTHERWISE NOTED.

REV	ECO	DATE	APV

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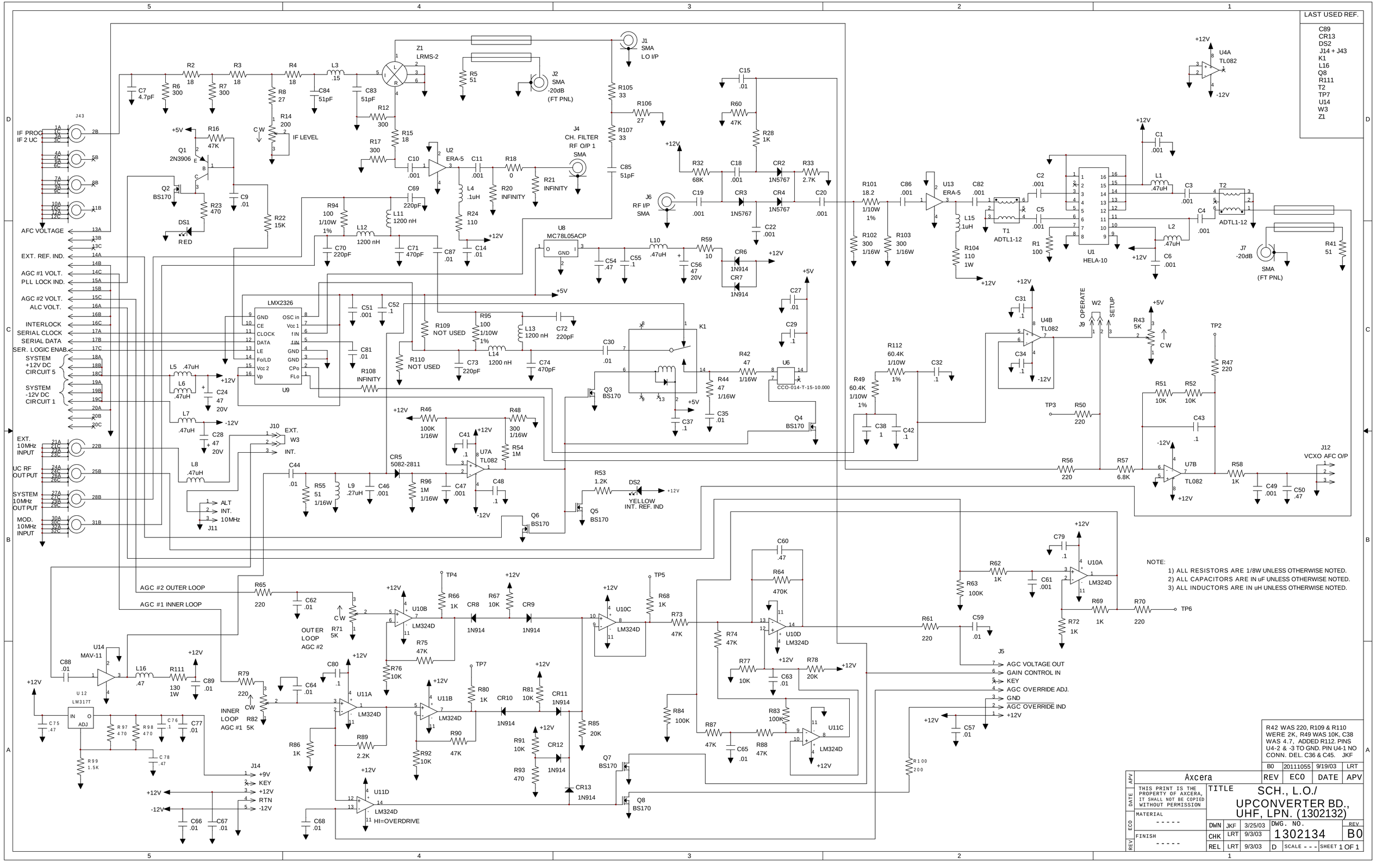
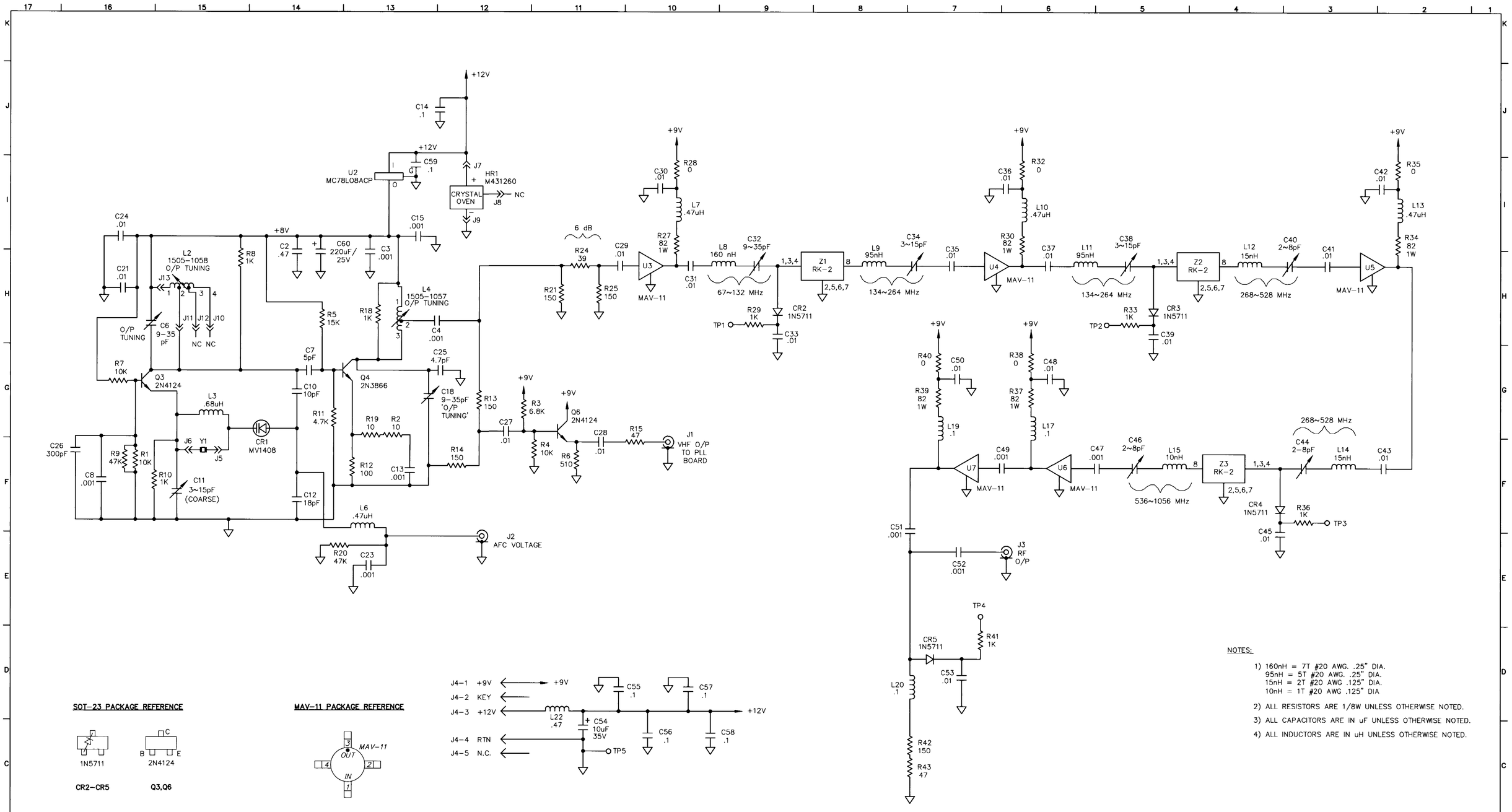
MATERIAL — — — —

FINISH — — — —

TITLE I/C, L.O./ U/C ASSY, UHF LOW PHASE NOISE

DWN	MH	6/11/03	DWG. NO. 1302060	REV A0
CHK	LRT	6/12/03		
REL	LRT	6/12/03	C SCALE ---	SHEET 1 OF 1


LAST USED REF.
C89
CR13
DS2
J14 + J43
K1
L16
Q8
R111
T2
TP7
U14
W3
Z1
J43
IF PROC
IF 2 UC
AFC VOLTAGE
EXT. REF. IND.
AGC #1 VOLT.
PLL LOCK IND.
AGC #2 VOLT.
ALC VOLT.
INTERLOCK
SERIAL CLOCK
SERIAL DATA
SER. LOGIC ENAB.
SYSTEM +12V DC CIRCUIT 5
SYSTEM -12V DC CIRCUIT 1
EXT. 10MHz INPUT
UC RF OUT PUT
SYSTEM 10MHz OUT PUT
MOD. 10MHz INPUT
Z1 LRMS-2
J1 SMA LO I/P
J2 SMA -20dB (FT PNL)
J4 CH. FILTER RF O/P 1 SMA
J6 RF I/P SMA
IF LEVEL
Q1 2N3906
Q2 BS170
DS1 RED
U2 ERA-5
U8 MC78L05ACP
LMX2326
U9
U13 ERA-5
T1 ADTL1-12
U1 HELA-10
T2 ADTL1-12
J7 -20dB SMA (FT PNL)
U4A TL082
U4B TL082
W2 OPERATE SETUP
TP2
TP3
J12 VCXO AFC O/P
U7B TL082
U7A TL082
CCO-014-T-15-10.000
U6
K1
Q3 BS170
Q4 BS170
Q5 BS170
Q6 BS170
Q7 BS170
Q8 BS170
DS2 YELLOW INT. REF. IND
CR5 5082-2811
J10 EXT. W3 INT.
J11 ALT INT. 10MHz
U12 LM317T
U14 MAV-11
U10A LM324D
U10B LM324D
U10C LM324D
U10D LM324D
U11A LM324D
U11B LM324D
U11C LM324D
U11D LM324D
HI=OVERDRIVE
AGC #2 OUTER LOOP
AGC #1 INNER LOOP
OUTER LOOP AGC #2
INNER LOOP AGC #1
J5
AGC VOLTAGE OUT
GAIN CONTROL IN
KEY
AGC OVERRIDE ADJ.
GND
AGC OVERRIDE IND
+12V
J14
+9V
KEY
+12V
RTN
-12V
NOTE:
1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.
R42 WAS 220, R109 & R110 WERE 2K, R49 WAS 10K, C38 WAS 4.7, ADDED R112. PINS U4-2 & -3 TO GND. PIN U4-1 NO CONN. DEL. C36 & C45. JKF
B0 20111055 9/19/03 LRT
REV ECO DATE APV
Axcera
THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION
MATERIAL -----
FINISH -----
TITLE SCH., L.O./ UPCONVERTER BD., UHF, LPN. (1302132)
DWN JKF 3/25/03
CHK LRT 9/3/03
REL LRT 9/3/03
DWG. NO. 1302134
REV B0
D SCALE --- SHEET 1 OF 1



NOTES:

1) 160nH = 7T #20 AWG. .25" DIA.
   95nH = 5T #20 AWG. .25" DIA.
   15nH = 2T #20 AWG .125" DIA.
   10nH = 1T #20 AWG .125" DIA
2) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
3) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
4) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.

REV	ECO	DATE	APV
2	k306	[illegible]	[illegible]	ADDED C60 & C54 WAS 47uF/20V. (RFB)
1	k312	1/30/98	DWB	R28,32,35,38, & 40 WAS 27ohm. R27, 30,34,37, & 39 WAS 100ohm 1W. ADDED +9V TO BD. AT J1-1 LOCATION. ALL +9V WAS +12V. JKF

ADC Telecommunications

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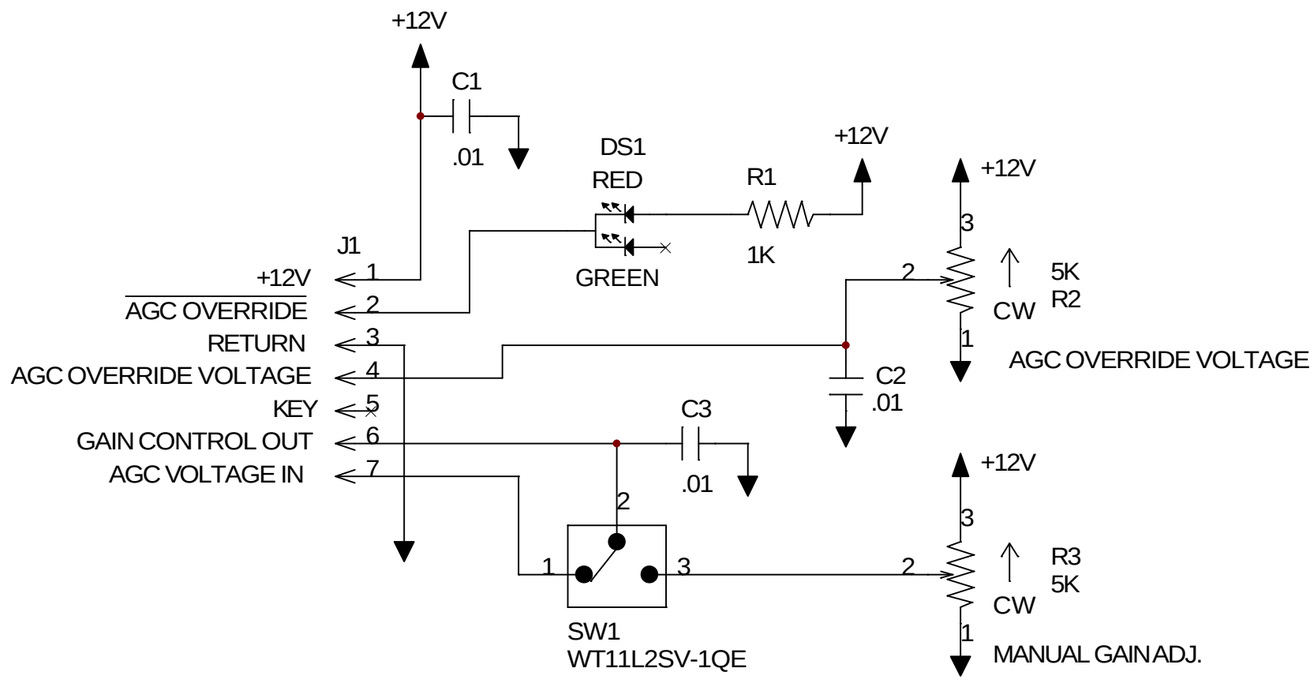
MATERIAL ---

FINISH ---

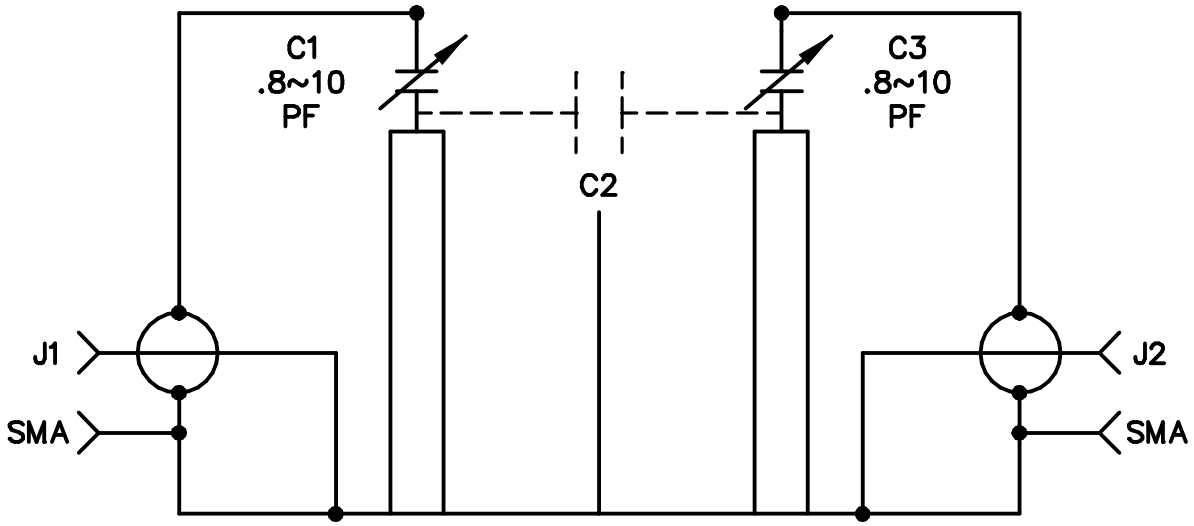
TITLE SCHEMATIC, UHF GENERATOR (1585-1265)

DWN	JKF	12/8/97	DWG. NO. 1585-3265
CHK	DWB	12/22/97	REV 2
REL	DWB	12/22/97	D SCALE 1=1 SHEET 1 OF 1



Axcera		REV	ECO	DATE	APV
THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH., FRONT PANEL LED DISPLAY BOARD (1303033)				
MATERIAL -----	DWN	JKF	7/24/03	DWG. NO. 1303035	REV A0
FINISH -----	CHK	LRT	7/25/03		
	REL	LRT	7/25/03	B	SCALE --- SHEET 1 OF 1

APV DATE ECO REV



NOTE: C2 IS STRAY CAPACITANCE BETWEEN LINE SECTIONS.

REV	ECO	DATE	APV

ADC

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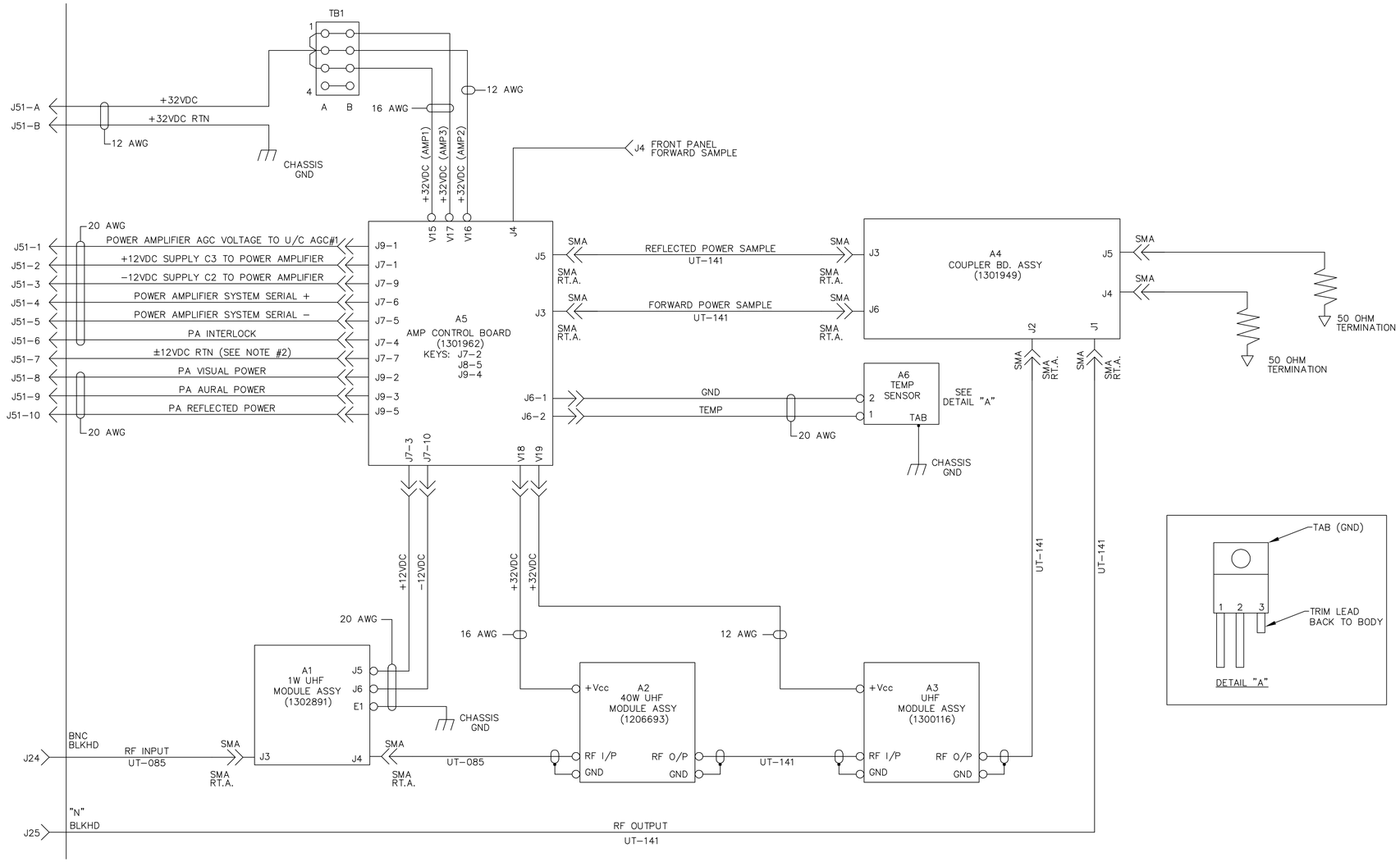
MATERIAL ------

FINISH ------

TITLE **91-00-00-50Z-61**
UHF FILTER

DWN	DD	9/13/83	DWG. NO. 1007-3101	REV 0
CHK	RWZ	9/13/83		
REL	RWZ	7/20/90	A SCALE ---	SHEET 1 OF 1



NOTE:
1. ALL WIRE IS 18AWG UNLESS OTHERWISE NOTED.
2. THIS CONNECTION MUST BE EQUIPPED WITH LONGER GROUND PIN. (MAKE FIRST BREAK LAST)

REV	ECO	DATE	APV
B0	20110990	9/11/03	JCM

DELETED .141 RIGID BETWEEN A5-J4 AND J1. (SAK)

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MATERIAL: -----

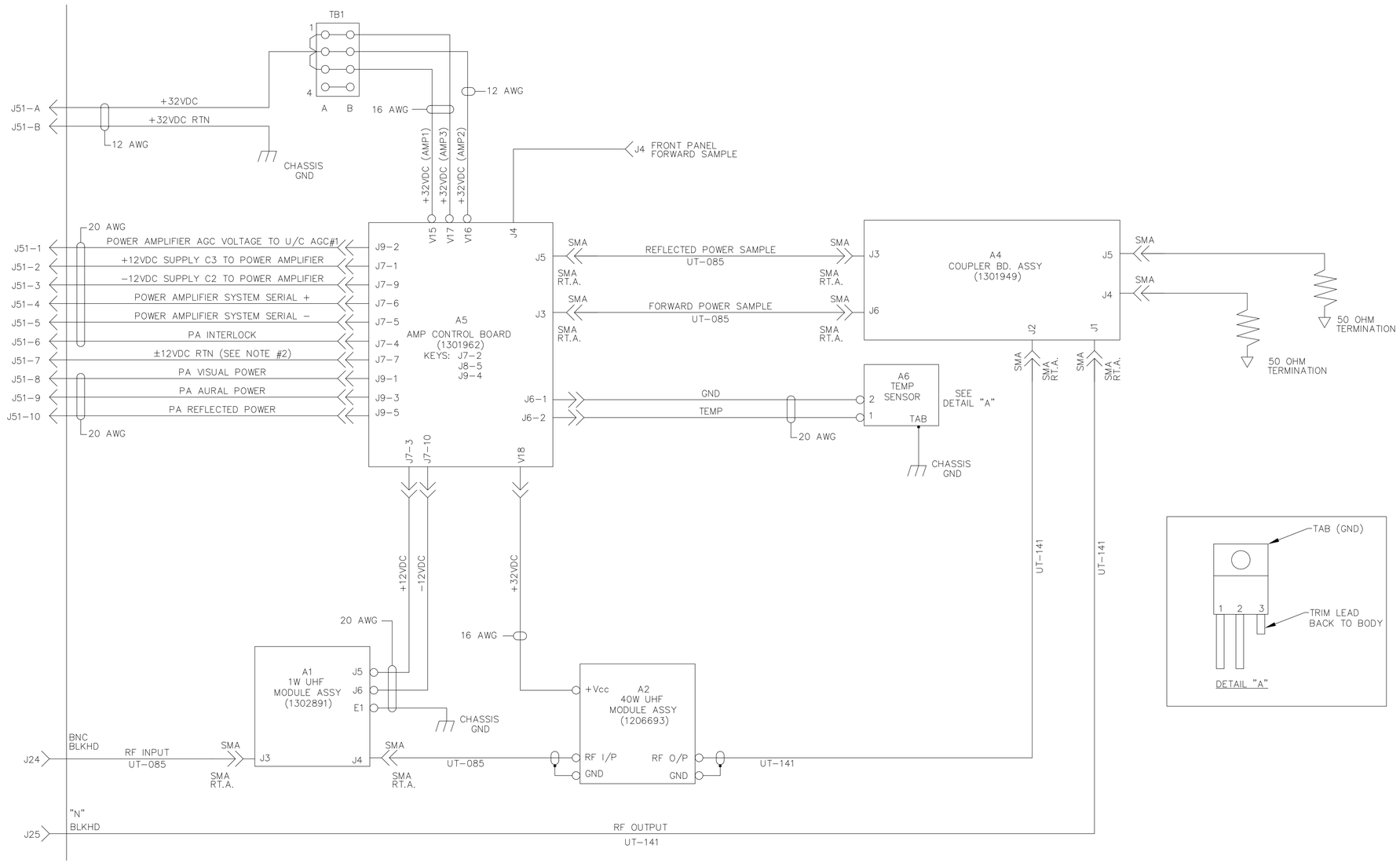
FINISH: -----

TITLE: I/C, PA ASSEMBLY, 100W PIONEER SERIES

DWN	MH	8/13/03	
CHK	JCM	8/27/03	
REL	JCM	8/27/03	

DWG. NO. 1302061 REV B0

D SCALE --- SHEET 1 OF 1



NOTE:
1. ALL WIRE IS 18AWG UNLESS OTHERWISE NOTED.
2. THIS CONNECTION MUST BE EQUIPPED WITH LONGER GROUND PIN. (MAKE FIRST BREAK LAST)

REV	ECO	DATE	APV
B0	20111102	11/6/03	JCM

A5-J9-2 WAS A5-J9-1.
A5-J9-1 WAS A5-J9-2.
REFLECTED AND FORWARD POWER SAMPLE CABLES WERE UT-141. (RGE)

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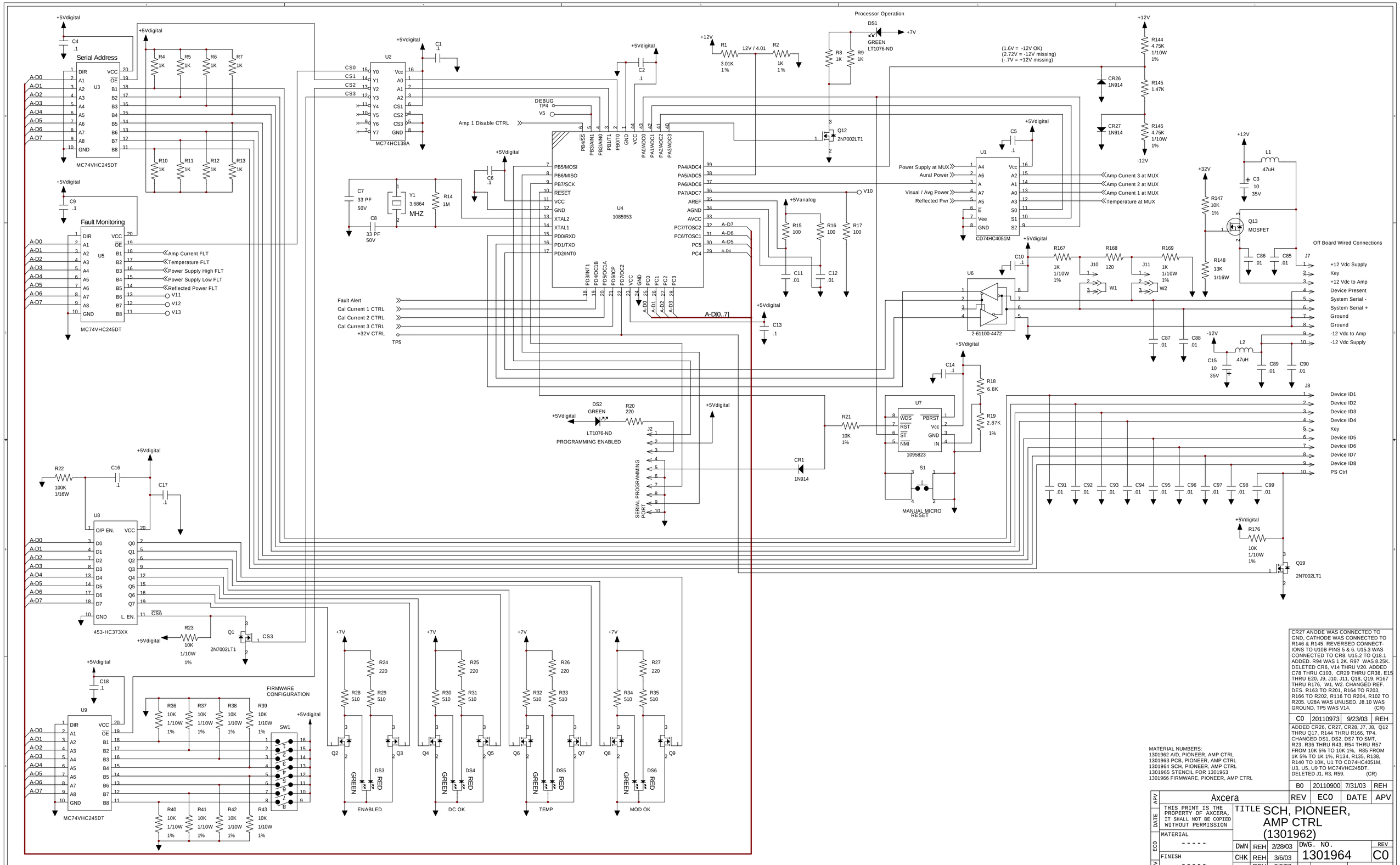
MATERIAL -----

FINISH -----

TITLE I/C, PA ASSEMBLY, 1KW, DRIVER LX SERIES

DWN	MH	10/21/03	DWG. NO. 1303452	REV. B0
CHK	RT	10/22/03		
REL	JCM	10/22/03	D SCALE ---	SHEET 1 OF 1



CR27 ANODE WAS CONNECTED TO GND, CATHODE WAS CONNECTED TO R146 & R145. REVERSED CONNECTIONS TO U10B PINS 5 & 6. U15.3 WAS CONNECTED TO CR8. U15.2 TO Q18.1 ADDED. R94 WAS 1.2K. R97 WAS 8.25K. DELETED CR6, V14 THRU V20. ADDED C78 THRU C103, CR29 THRU CR38, E15 THRU E20, J9, J10, J11, Q18, Q19, R167 THRU R176, W1, W2. CHANGED REF. DES. R163 TO R201, R164 TO R203, R166 TO R202, R116 TO R204, R102 TO R205. U28A WAS UNUSED. J8.10 WAS GROUND. TP5 WAS V14. (CR)

C0	20110973	9/23/03	REH

ADDED CR26, CR27, CR28, J7, J8, Q12 THRU Q17, R144 THRU R166, TP4, CHANGED DS1, DS2, DS7 TO SMT, R23, R36 THRU R43, R54 THRU R57 FROM 10K 5% TO 10K 1%, R85 FROM 1K 5% TO 1K 1%, R134, R135, R138, R140 TO 10K, U1 TO CD74HC4051M, U3, U5, U9 TO MC74VHC245DT. DELETED J1, R3, R59. (CR)

B0	20110900	7/31/03	REH

MATERIAL NUMBERS:
1301962 A/D, PIONEER, AMP CTRL
1301963 PCB, PIONEER, AMP CTRL
1301964 SCH, PIONEER, AMP CTRL
1301965 STENCIL FOR 1301963
1301966 FIRMWARE, PIONEER, AMP CTRL

Axcera		REV	ECO	DATE	APV

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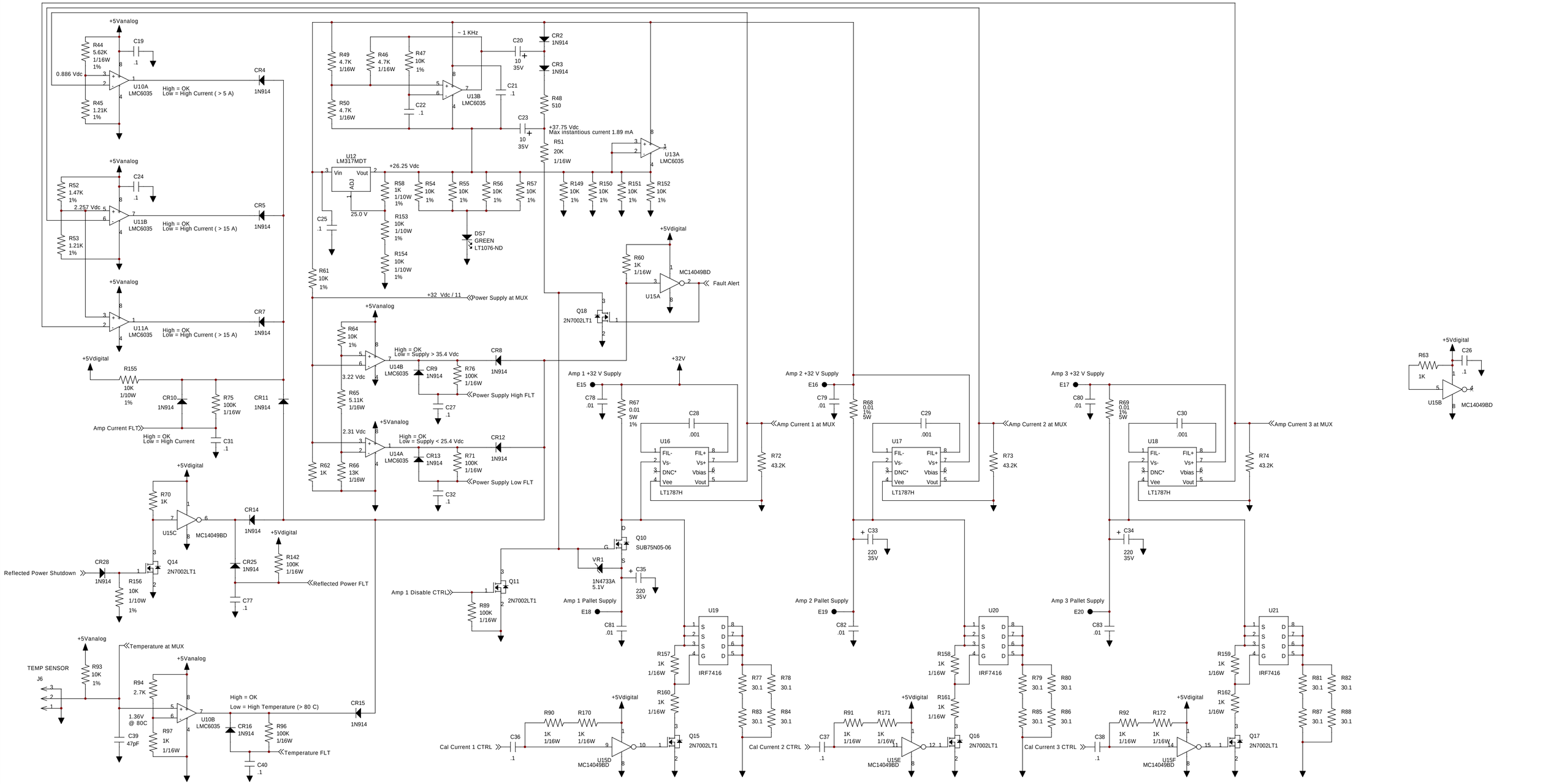
MATERIAL -----

FINISH -----

TITLE SCH, PIONEER, AMP CTRL (1301962)

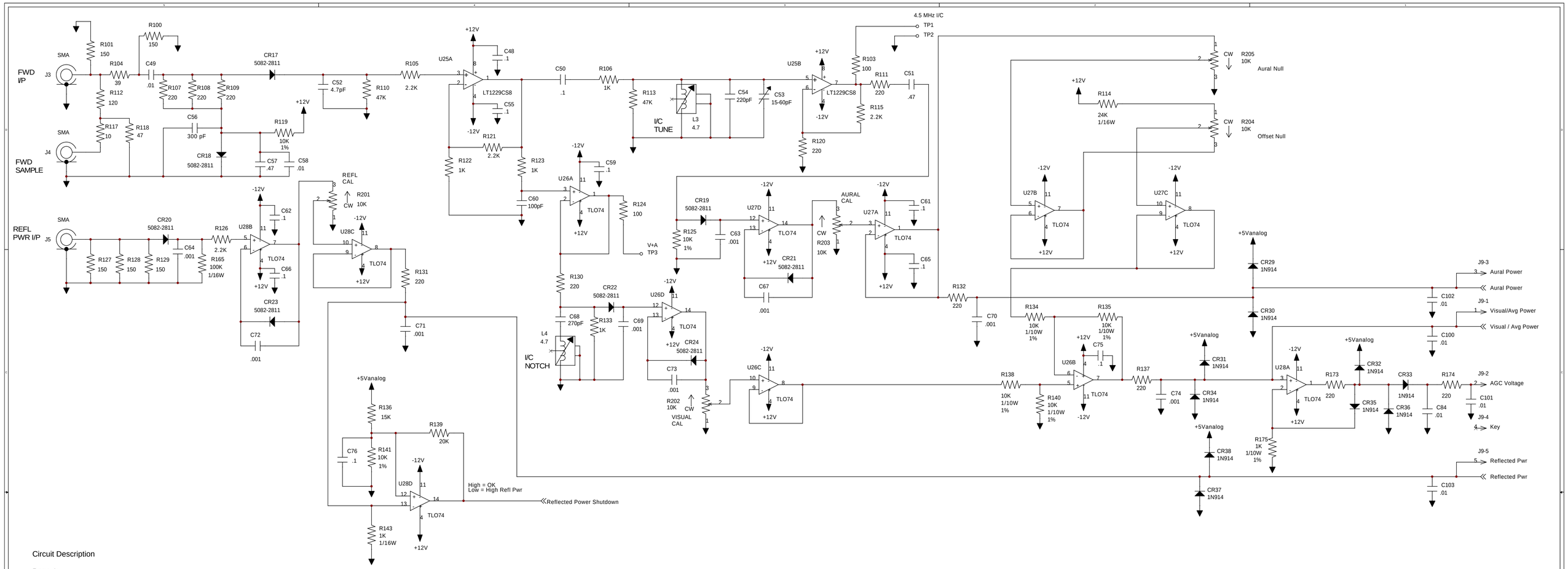
DWN	REH	2/28/03	DWG. NO. 1301964	REV C0
CHK	REH	3/6/03		
REL	REH	3/6/03	D SCALE ---	SHEET 1 OF 3



NOTE:

A track width of 0.3 inch is needed between power input vias and sense resistors R55,R56,R57. 0.3 inch track width is also needed between the output of the sense resistors and the output vias that provide power to the amplifier pallets.

Axcera		REV	ECO	DATE	APV
THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH, PIONEER, AMP CTRL (1301962)				
MATERIAL -----					
FINISH -----					
	DWN	REH	2/28/03	DWG. NO. 1301964	REV C0
	CHK	REH	3/6/03		
	REL	REH	3/6/03	D SCALE - - -	SHEET 2 OF 3



Circuit Description

Page 1:
Upper center of page one is U4 which is the controller. This in-circuit Atmel microcontroller is operated at 3.6864 MHz. Programming of this device is performed through J2. U4 selects the desired analog channel of U1 through the settings of PA0 - PA3. PA4 of U4 is a processor operating LED that can be flashed to show continued operation.
The outputs of Port A must be set and not changed during an analog input read of channels PA5 - PA7. PA5 is used to monitor the +12 Vdc supply to the board. PA6 is the selected channel of analog switch U1. PA7 is connected to a via for future access.

U6 is our standard serial to RS-485 driver IC. U7 is a watchdog IC used to hold the microcontroller in reset if the supply voltage is less than 4.21 Vdc; (1.25 Vdc < Pin 4 (IN) < Pin 2 (Vcc)). U7 momentarily resets the microcontroller if Pin 6 (!ST) is not clocked every second. A manual reset switch is provided but should not be needed.

Upper right corner U3 is used to determine where the amplifier control board is located. The eight inputs come from the main amp connector and are used to set the SCADA address of the controller. Pull-up resistors set a default condition of logic high.

U5 below U3 is used for getting digital input information of the board. Page two has several monitoring circuits that provide information on the amplifier's status. Many of these circuits automatically shut down the amplifier if a specific fault occurs.

U8 below U5 is used to control four board mounted status LEDs. A FET is turned on to shut current away from the LED to turn it off. U9 below U8 is used to enable different features within software. Actual use is TBD.

Page 2:

In the lower right corner are voltage regulator circuits. U22 should allow for 0.14 amps of power using its 92 C/W rating if Ta = 60C max and Tj = 125C max. 0.26 amps can be obtained from U22 if the mounting pad is 0.5 sqr. inches. The controller will not need this much current.

U23 and U24 are low drop-out voltage regulators with a tolerance greater than or equal to 1%. 100 mA is available from each device but again the controller will not need this much current.

In the upper left section are circuits with U12 and U13. U12 is used to generate a regulated voltage that is about 5 Volts less than the +32 Volt supply. When the +32 Volt supply is enabled, the circuitry around U13B is used to provide gate voltage to Q10 that is 5 volts greater than the source pin of this FET. The gate of Q10 can be turned off by any one of a few different circuits.

U10A is used to turn off the gate of Q10 in the event of high current in amplifier #1. At 0.886 Vdc, the current to amplifier #1 should be about 5.12 Amps. U11 is used to turn of the FET if high current is detected in amplifier #2 or #3. With 2.26 Vdc at pin 5 and pin 3 of U11, the voltage output of current sense amplifier U17 or U18 at high current shut down should be about 13.1 Amps.

U14B is used to turn off the gate of Q10 in the event of high power supply voltage. U14A is used to keep the FET disabled if the power supply voltage is less than 26 volts.

U28D on page 3 is used to turn off the gate of Q10 in the event of high reflected power. U10B turn off the gate of Q1 if the power supply temperature gets too hot.

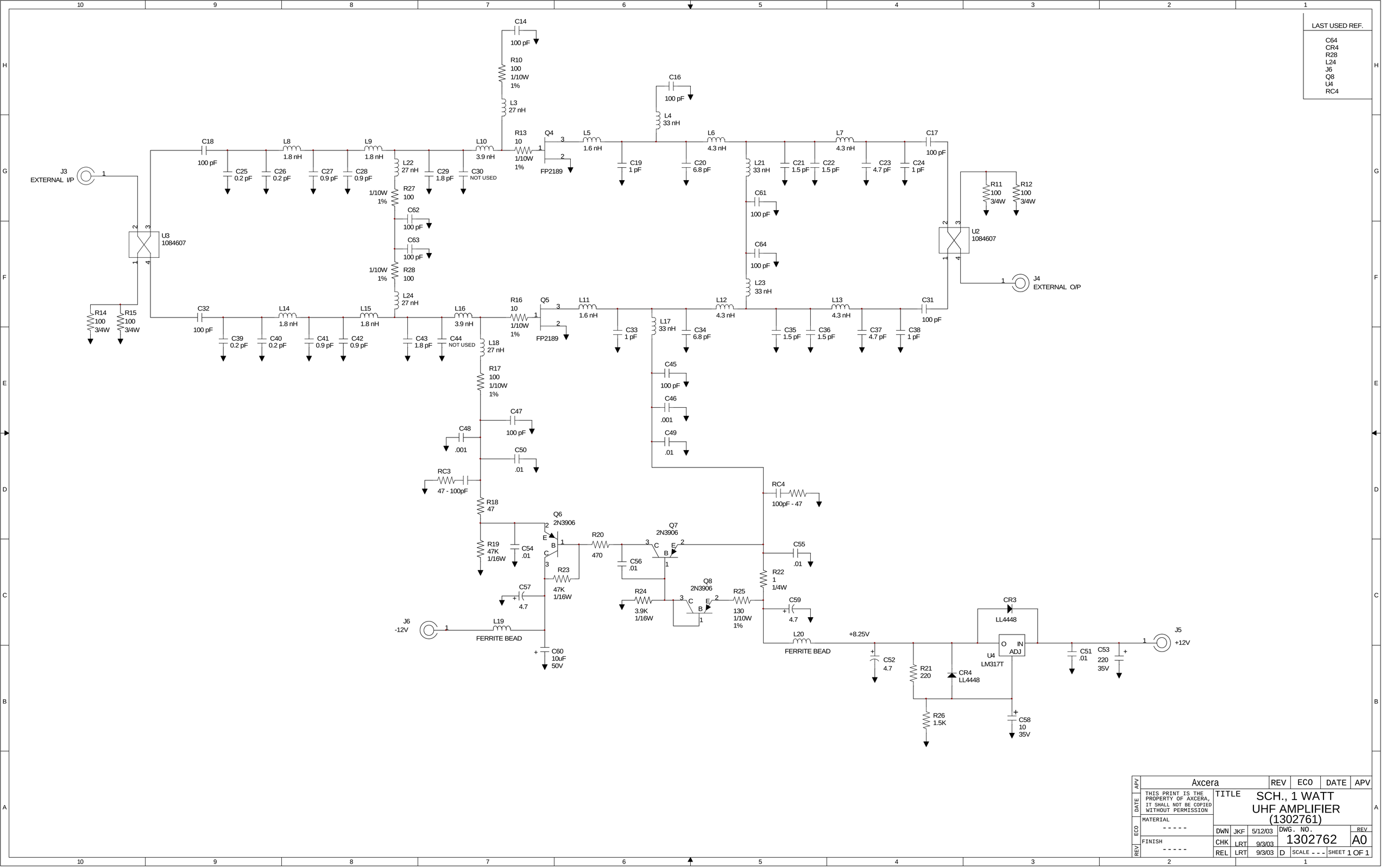
Current Monitoring Sections - A 0.01 ohm 1% 5 Watt thru-hole resistor is used for monitoring the current through several sections of the amplifier. The voltage developed across this resistor is amplified for current monitoring by U16, U17, or U18. The Linear Technology LT1787HVCS8 precision high side current sense amplifier accepts a maximum voltage of 60 Vdc.
The 43.2 Kohm resistor from Pin 5 to ground sets the gain of the amplifier to about 17.28. This value is not set with much accuracy since the manufacture internal matches the resistors of this part but their actual resistance value is not closely defined. A trimming resistor is suggested to give a temperature stability of -200ppm/C but instead the microcontroller will determine the exact gain of the circuit and use a correction factor for measurements. Circuit loading components are located in the lower portion of each current monitoring circuit. These components allow for short duration high current loading of the supply. By measuring the current through the sense resistor with and without the additional load, the microcontroller can determine the gain of each circuit. The input to each hex inverter protects the load resistors from prolonged power dissipation. The load resistors are four 30.1 ohm 1% 1206 resistors. For very short duration pulses, a 1206 resistor can handle up to 60 watts. The Atmel processor requires 226 uSec per conversion. A supply voltage of 32 volts will pass 1.06 amps + 1% through the load resistors.

Page 3:

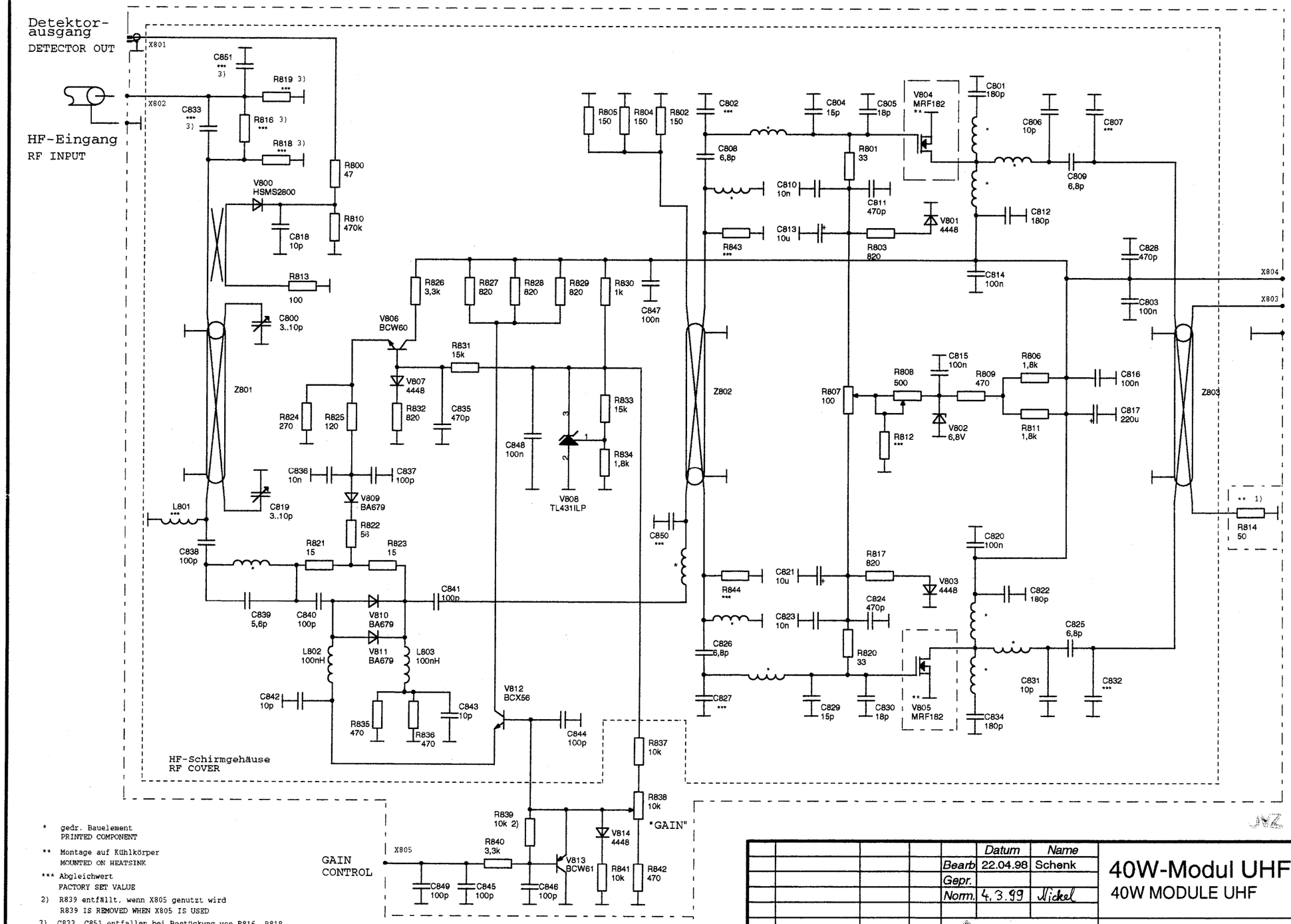
RF power detector circuits. Gain of power measurements will be done through software. Only the Aural Null and Offset Null need to be done through front panel pots.

NOTES:
1) ALL RESISTORS ARE 1/8 WATT UNLESS NOTED OTHERWISE.
2) ALL CAPACITORS ARE uF UNLESS NOTED OTHERWISE.
3) ALL INDUCTORS ARE uH UNLESS NOTED OTHERWISE.

APV	Axcera	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH, PIONEER, AMP CTRL (1301962)			
ECO	MATERIAL -----	DWN REH 2/28/03	DWG. NO. 1301964		REV C0
REV	FINISH -----	CHK REH 3/6/03	REL REH 3/6/03	D	SCALE --- SHEET 3 OF 3



APV	Axcera	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE	SCH., 1 WATT UHF AMPLIFIER (1302761)		
ECO	MATERIAL -----	DWN	JKF	5/12/03	DWG. NO. 1302762 REV A0
REV	FINISH -----	CHK	LRT	9/3/03	
		REL	LRT	9/3/03	D SCALE - - - SHEET 1 OF 1



* gedr. Bauelement
PRINTED COMPONENT

** Montage auf Kühlkörper
MOUNTED ON HEATSINK

*** Abgleichwert
FACTORY SET VALUE

2) R839 entfällt, wenn X805 genutzt wird
R839 IS REMOVED WHEN X805 IS USED

3) C833, C851 entfallen bei Bestückung von R816, R818 u. R819
C833, C851 ARE REMOVED WHEN R816, R818, R819 ARE INSTALLED

Leiterplattenbestückung siehe
PC BOARD LAYOUT SEE
51-5379-308-00 (1)

Maschinell erzeugt!
Nicht manuell ändern!

Schutzvermerk nach DIN 34 beachten!
NOTE: copyright protected as in DIN 34 !

OrCAD SCHEMATIC
SN79-308
SCHEMATIC1
G:\EPROI\ORCADWSP\5379\308-02\SN79-308.DSN

					Datum	Name
				Bearb	22.04.98	Schenk
				Gepr.		
				Norm.	4.3.99	Nickel

40W-Modul UHF
40W MODULE UHF

Zust.	Änderung	Datum	Name
02	E185	26.10.98	Sche
01		8.5.98	Sche

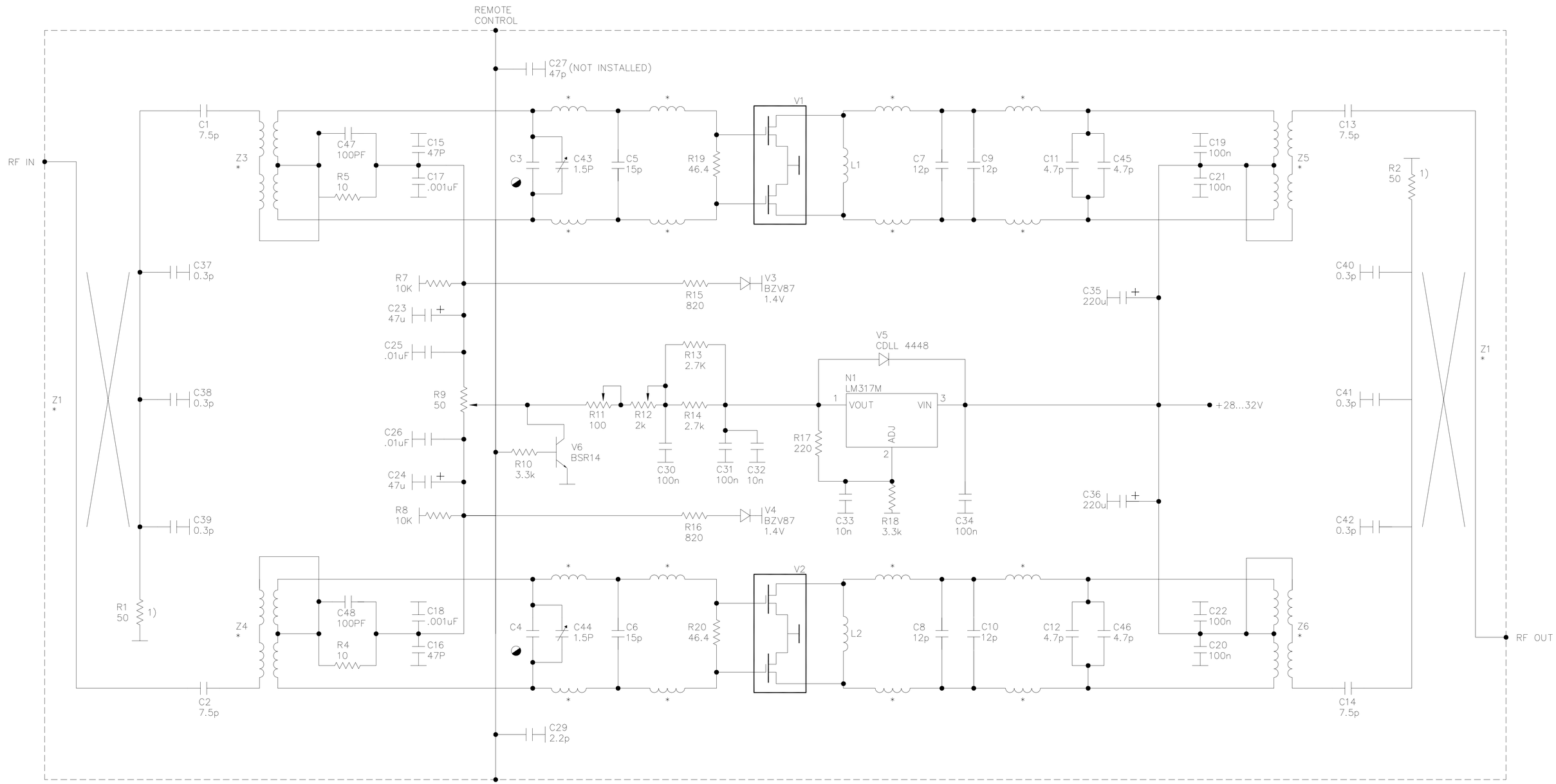
TELEFUNKEN Sendertechnik

51-5379-308-00 WSP XB

Blatt 1 / 1 Bl.

Urspr.: Ers. f.: Ers. d.:

A3L



* PRINTED COMPONENT

FACTORY SET VALUE

PC BOARD LAYOUT SEE
51-5379-309-00 (2)

REV	ECO	DATE	APV
CO	20110221	5/17/02	RE
BO	20100316	04/02/02	LRT

DELETED PTF10159 P/N FROM LDMOS. ADDED C23,C24 & C27. CDD/CR

R15 AND R16 WERE 680 OHMS. PWN

D0	CHANGE R3 FROM A 2.2 OHM RESISTOR TO C47, SM., CAP., 100PF, 500WDC.
	CHANGE R6 FROM A 2.2 OHM RESISTOR TO C48, SM., CAP., 100PF, 500WDC.
	CHANGE R4 FROM A 2.2 OHM RESISTOR TO 1590600SMT, SM., RES., 10 OHM 5% 1/8W.
	CHANGE R5 FROM A 2.2 OHM RESISTOR TO 1590600SMT, SM., RES., 10 OHM 5% 1/8W.
	CHANGE C17 FROM A 47PF CAP, FIXED CERAMIC, 47 PF TO 1590616OSMT, SM., CAP., .001 UF, 50 WVDC.
	CHANGE C18 FROM A 47PF CAP, FIXED CERAMIC, 47 PF TO 1590616OSMT, SM., CAP., .001 UF, 50 WVDC.
	ADD C23, 1301246, SM. CAP, 47MF, 50V, LOW ESR.
	ADD C24, 1301246, SM. CAP, 47MF, 50V, LOW ESR.
	ADD C25, 1590616ISMT, SM., CAP., .01 UF, 50 WVDC.
	ADD C26, 1590616ISMT, SM., CAP., .01 UF, 50 WVDC. PWN
D0	20110444 09-18-02 RJ

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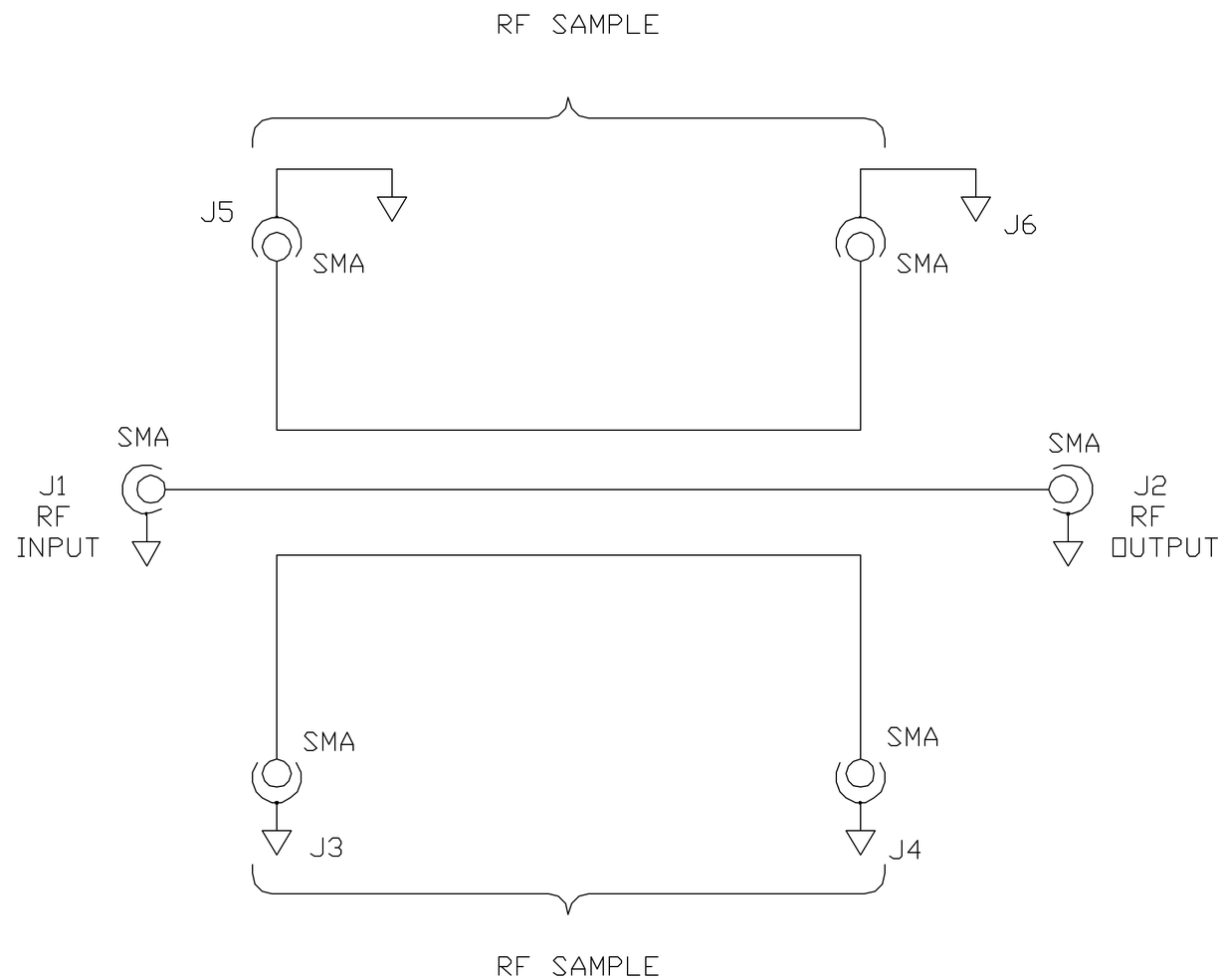
MATERIAL

FINISH

TITLE AMPLIFIER MODULE

DWN	PWN	04/01/02	DWG. NO.	REV
CHK	LRT	04/03/02	51-5379-309-00 WSP	D0
REL	LRT	04/03/02	D SCALE	SHEET 1 OF 1



REV	ECO	DATE	APV

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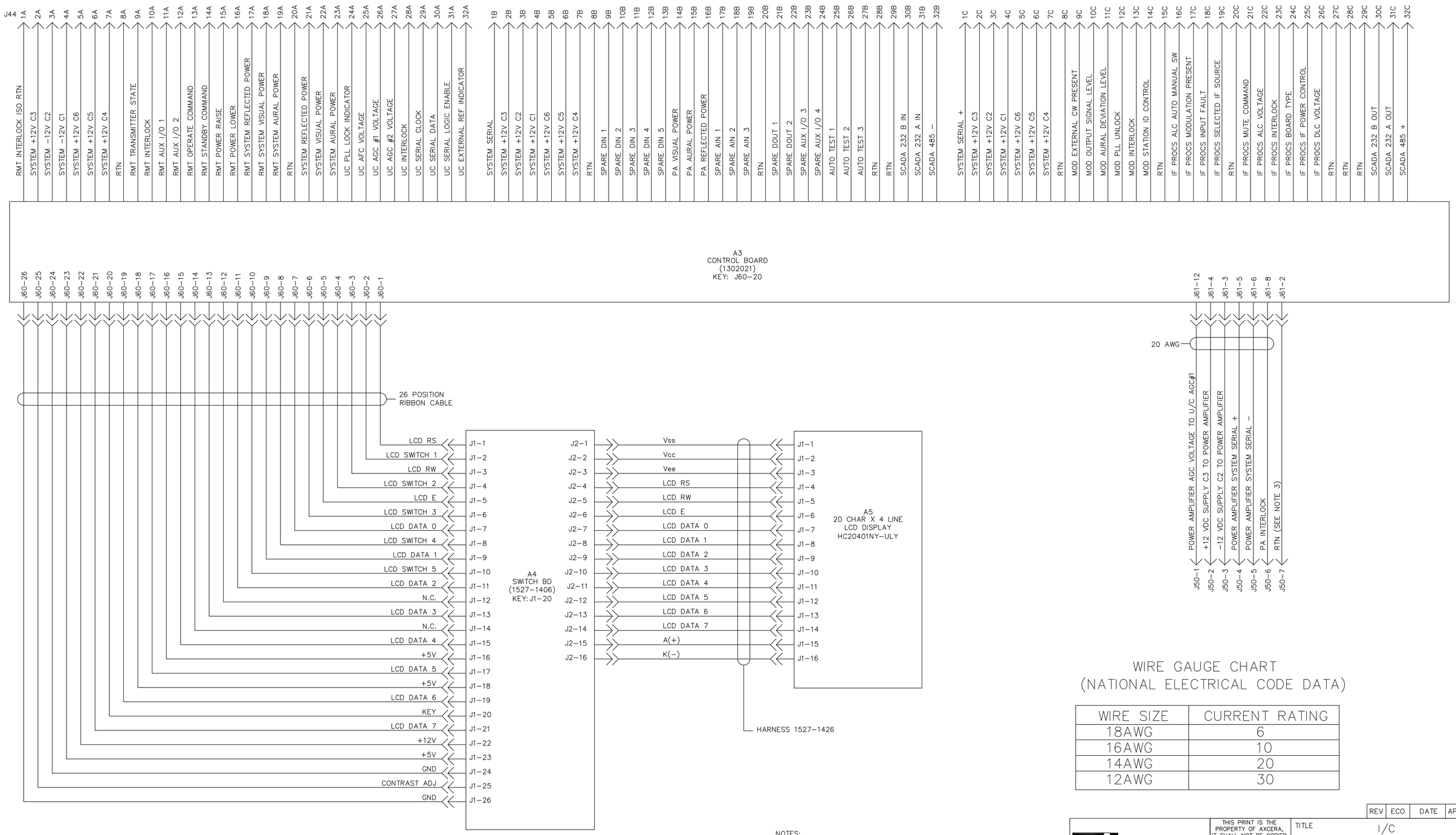
MATERIAL
— — — —

FINISH
— — — —

TITLE
SCHEMATIC
DIRECTIONAL COUPLER
BOARD

DWN	MH	8/11/03	DWG. NO. 1303152	REV A0
CHK	JCM	8/25/03		
REL	JCM	8/25/03	B SCALE — — —	SHEET 1 OF 1



WIRE GAUGE CHART
(NATIONAL ELECTRICAL CODE DATA)

WIRE SIZE	CURRENT RATING
18AWG	6
16AWG	10
14AWG	20
12AWG	30

NOTES:
1) ALL SINGLE WIRE IS 18AWG UNLESS OTHERWISE NOTED.
2) VALUES FOR VR1, VR2 AND VR3 ARE PART OF VOLTAGE SELECTION KITS.
3) THIS CONNECTION MUST BE EQUIPPED WITH LONGER GROUND PIN (MAKE FIRST BREAK LAST).

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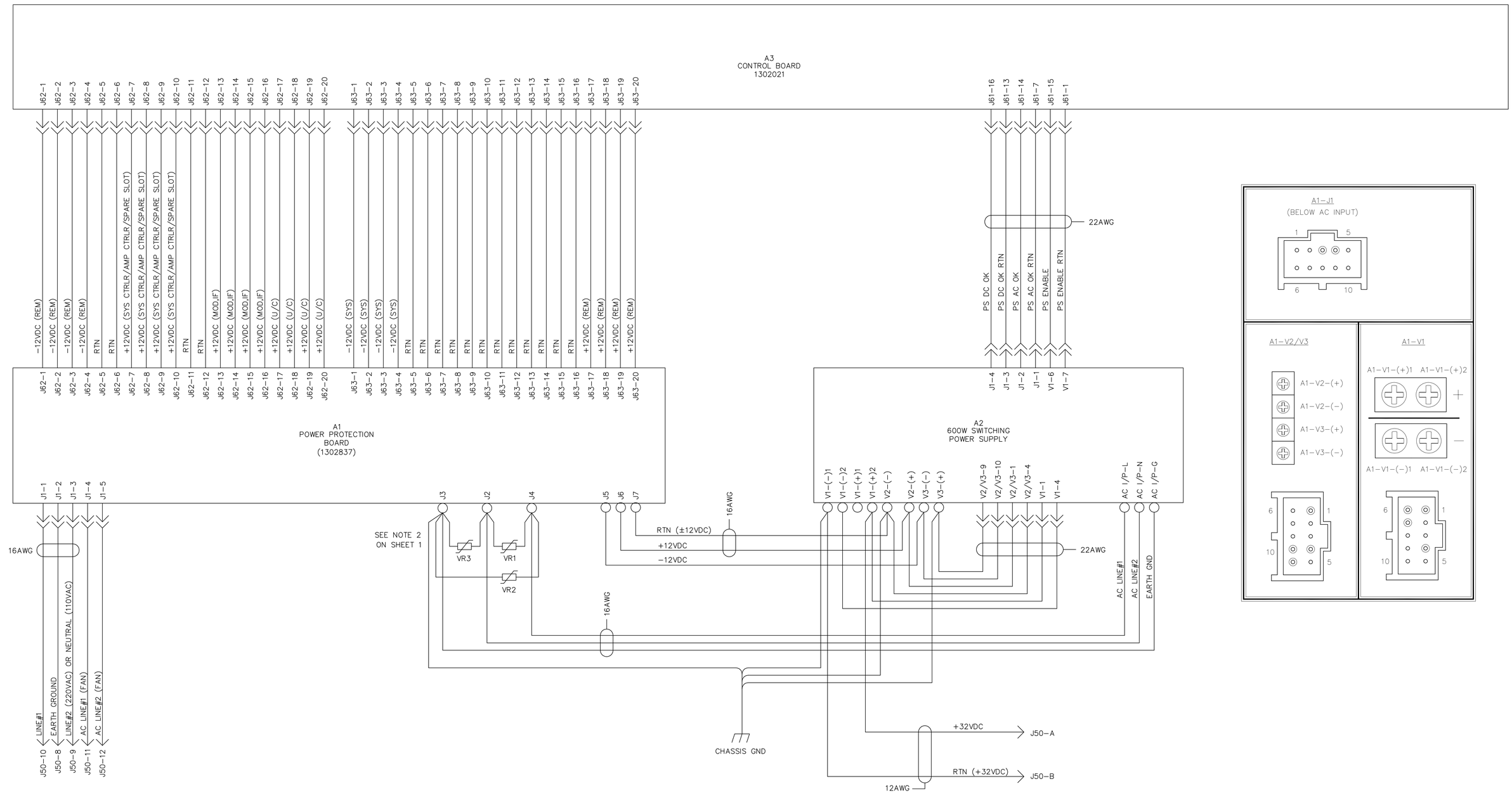
MATERIAL — — — —

FINISH — — — —

REV	ECO	DATE	APV

TITLE I/C CONTROL/POWER SUPPLY ASSEMBLY

DWN	MH	6/18/03	DWG. NO. 1302062	REV A0
CHK	JCM	8/27/03		
REL	JCM	8/27/03	D SCALE — — —	SHEET 1 OF 2



REV	ECO	DATE	APV

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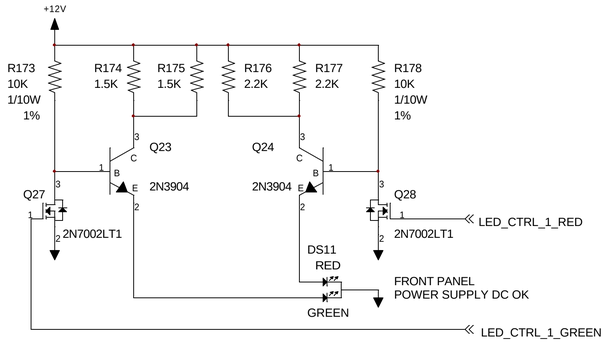
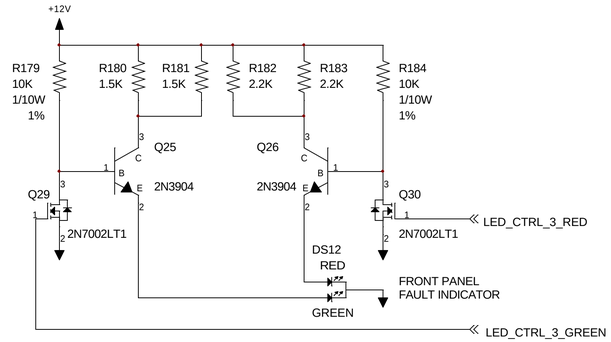
MATERIAL — — — —

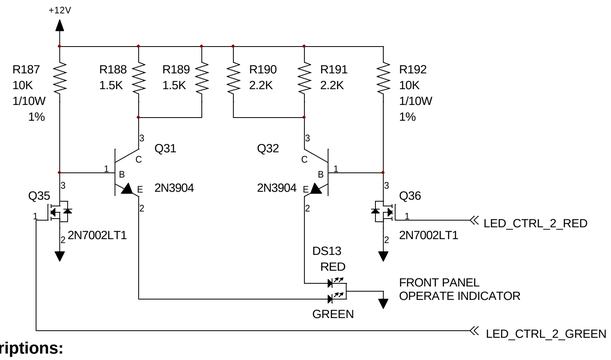
FINISH — — — —

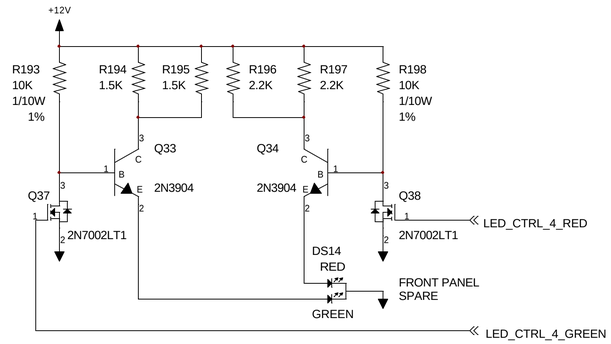
TITLE I/C CONTROL/POWER SUPPLY ASSEMBLY

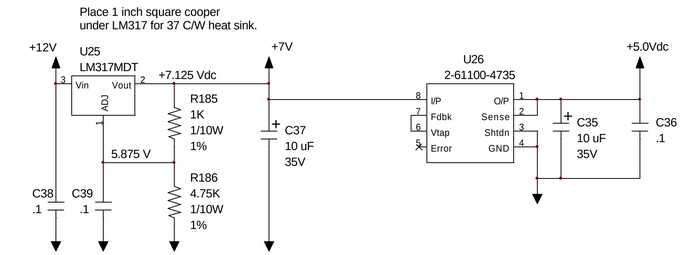
DWN	MH	6/18/03	DWG. NO. 1302062	REV A0
CHK	JCM	8/27/03		
REL	JCM	8/27/03	D SCALE — — —	SHEET 2 OF 2

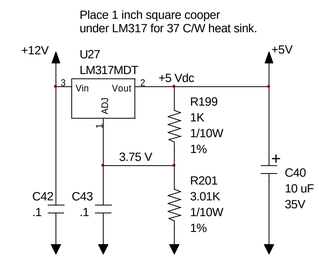


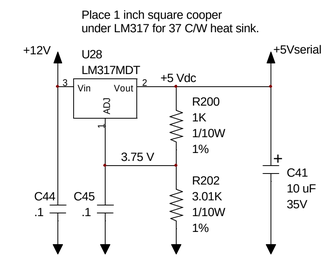












Circuit Descriptions:

PAGE 1:

U1 is an Atmel Atmega128 microcontroller. This part is in-circuit programmed using the serial programming port. When the microcontroller is held in reset by either the programming port or the external watchdog IC, a transistor inverts the reset signal while serial programming lines are connected to U1 through analog switch U5.

U2 is a watchdog IC used to hold the microcontroller in reset if the supply voltage is less than 4.21 Vdc; (1.25 Vdc < Pin 4 (IN) < Pin 2 (Vcc)). The watchdog momentarily resets the microcontroller if Pin 6 (!ST) is not clocked every second. A manual reset switch is provided but should not be needed.

Diodes DS1 through DS8 are used for display of auto test results. A test board is used to execute self test routines. When the test board is installed, Auto_Test_1 is held low and Auto_Test_2 is allowed to float at 5 Vdc. This is the signal to start the auto test routines.

U3 and U4 are used to selectively enable various input and output ICs found on page 2 and 3 of the schematic.

U1 has two serial ports available. In this application, one port is used to communicate with transmitter system components where U1 is the master of a RS-485 serial bus. The other serial port is used to provide serial data I/O where U1 is not the master of the data port. A dual RS-232 port driver IC and a RS-485 port driver is also in the second serial data I/O system. The serial ports are wired such that serial data input can come through one of the three serial port channels. Data output is sent out through each of the three serial port channels.

Switch SW1 is used to select either transmitter operation or exciter driver operation. When the switches of SW1 are on, transmitter operation is selected and the power monitoring lines of the transmitter's power amplifier are routed to the system power monitoring lines.

PAGE 2:

Digital output latches are used to control system devices. Remote output circuits are implemented using open drain FETs with greater than 60 Volt drain to source voltage ratings.

Remote digital inputs are diode protected with a 1 Kohm pull-up resistor to 5Vdc. If the remote input voltage is greater than about 2 volts or floating, a FET is turned on and a logic low is applied to the digital input buffer. If the remote input voltage is less than the turn on threshold of the FET (about 2 Vdc), a logic high is applied to the digital input buffer.

Four of the circuits on page two are auxiliary I/O connections wired for future use. They are wired similar to the remote digital inputs but include a FET for digital output operation. To operate these signals as an input, the associated output FET must be turned off. These circuits are also connected to an analog input multiplexer IC.

PAGE 3:

Several ICs are used as input buffers to allow the microcontroller to monitor various digital input values. Most digital inputs use a 10 Kohm pull-up resistor. The buffer IC used for data transfer to the display is wired for read and write control.

PAGE 4:

Each analog input is expected to be between 0 and 5 Vdc. If a signal exceeds 5.1 Vdc, a 0.225 Watt zenor diode clamps the signals voltage. Most signals are calibrated at their source however two dual serial potentiometer ICs are used to calibrate four signals. For these four circuits, the input value is divided in half before it is applied to an op-amp. The serial potentiometer is used to adjust the input signal between 80 and 120% of the input signal. Serial data to the second serial potentiometer is transferred through the first IC.

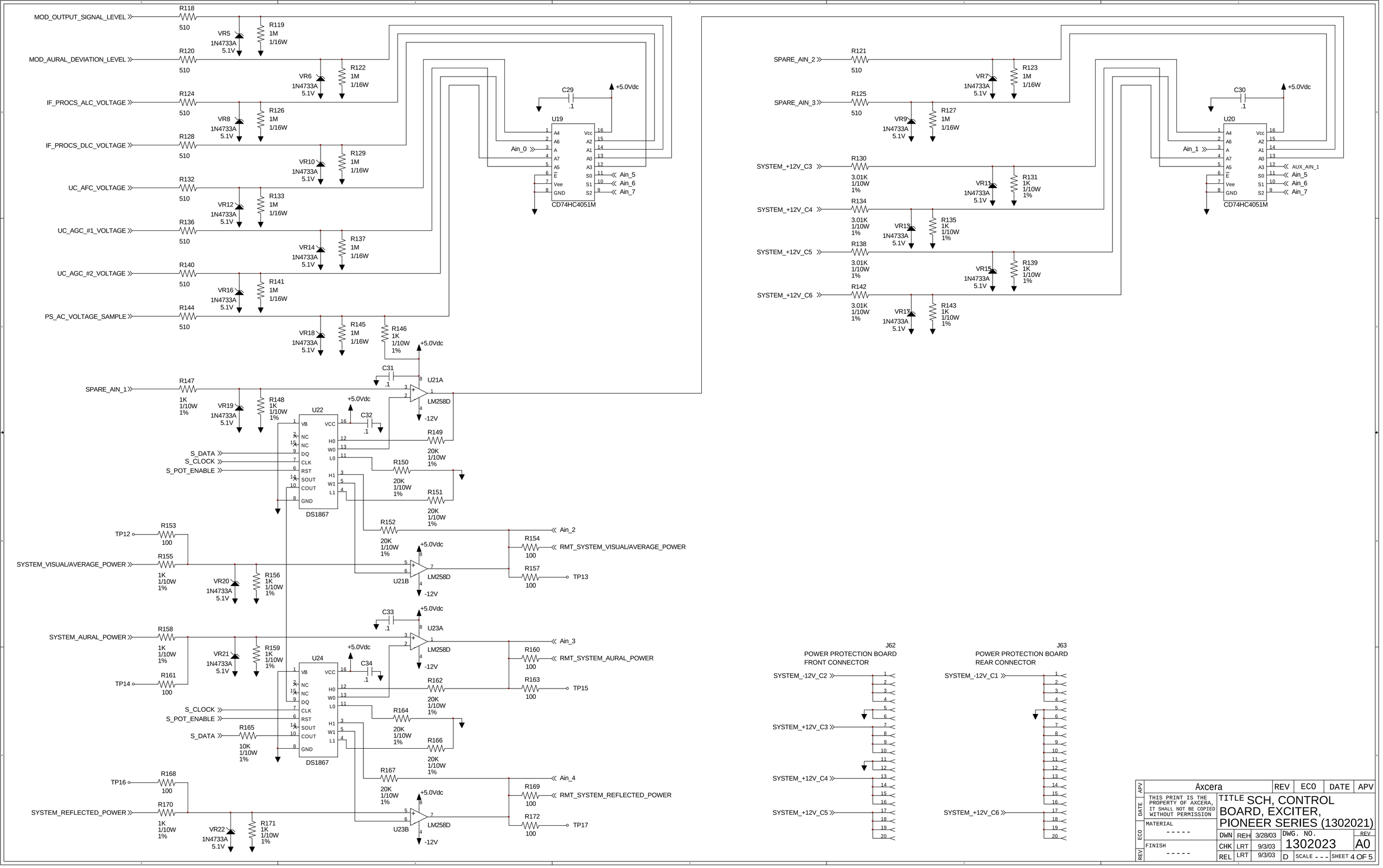
Two 20 position connectors are used to provide power to the backplane. J62 and J63 get power from the power supply after a nominal 3 amp resettable fuse. The Raychem polyswitch resettable fuses may open on a current as low as 2.43 amps at 50C, 3 amps at 25 C or 3.3 amps at 0C. They definately will open when the current is 4.86 amps at 50C, 6 amps at 20C, or 6.6 amps at 0C. Trace widths of these circuits are 0.140" (designed for maximum current).

PAGE 5:

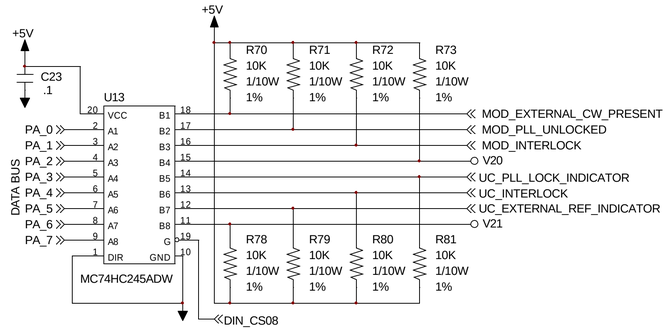
Each of the four LED circuits drive a dual element common cathode LED. To make a good amber color, the current applied to the green element is slightly greater than the red element.

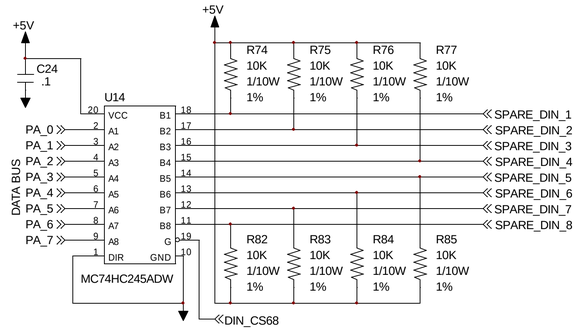
Several voltage regulators are used to power the board. Seven volts is typically applied to board LEDs and to the input of a precision 5.0 volt regulator. The 5.0 volt regulator is used for analog circuits and the microcontroller analog reference voltage. Another two 5 volt regulator circuits are used for most other board circuits.

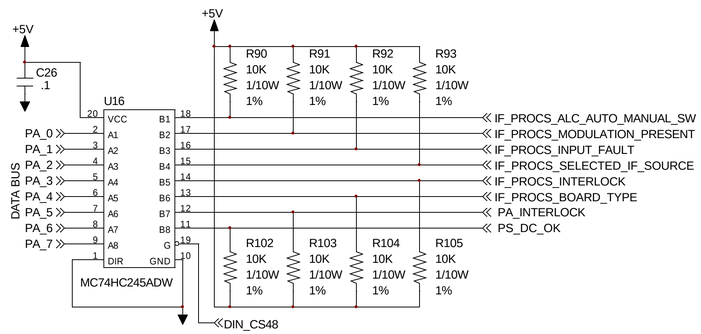
APV	Axcera	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)			
ECO	MATERIAL -----	DWN REH 3/28/03	DWG. NO. 1302023		REV A0
REV	FINISH -----	CHK LRT 9/3/03			
		REL LRT 9/3/03	D	SCALE - - -	SHEET 5 OF 5

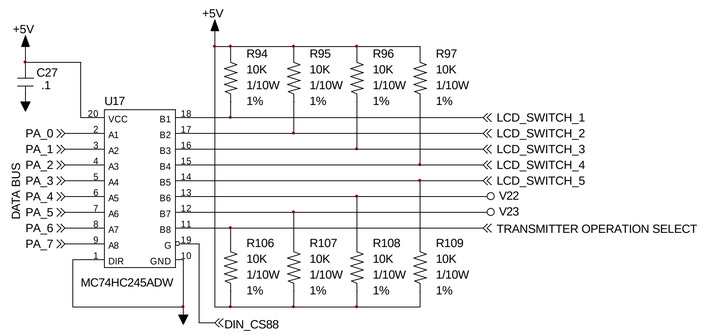


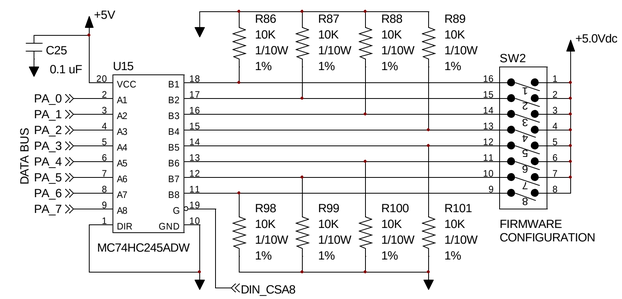
Axcera		REV	ECO	DATE	APV
THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)				
MATERIAL -----	DWN REH 3/28/03	DWG. NO. 1302023		REV A0	
FINISH -----	CHK LRT 9/3/03				
	REL LRT 9/3/03	D	SCALE - - -	SHEET 4 OF 5	

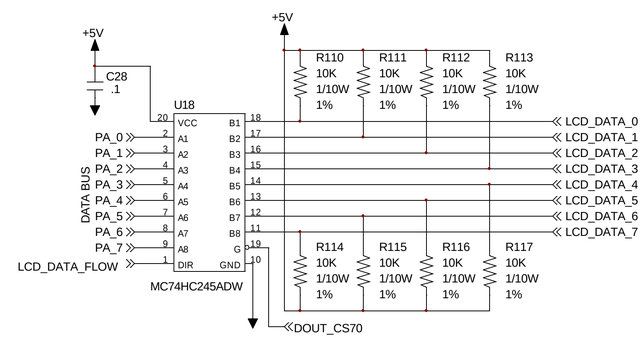












APV	Axcera	REV	ECO	DATE	APV
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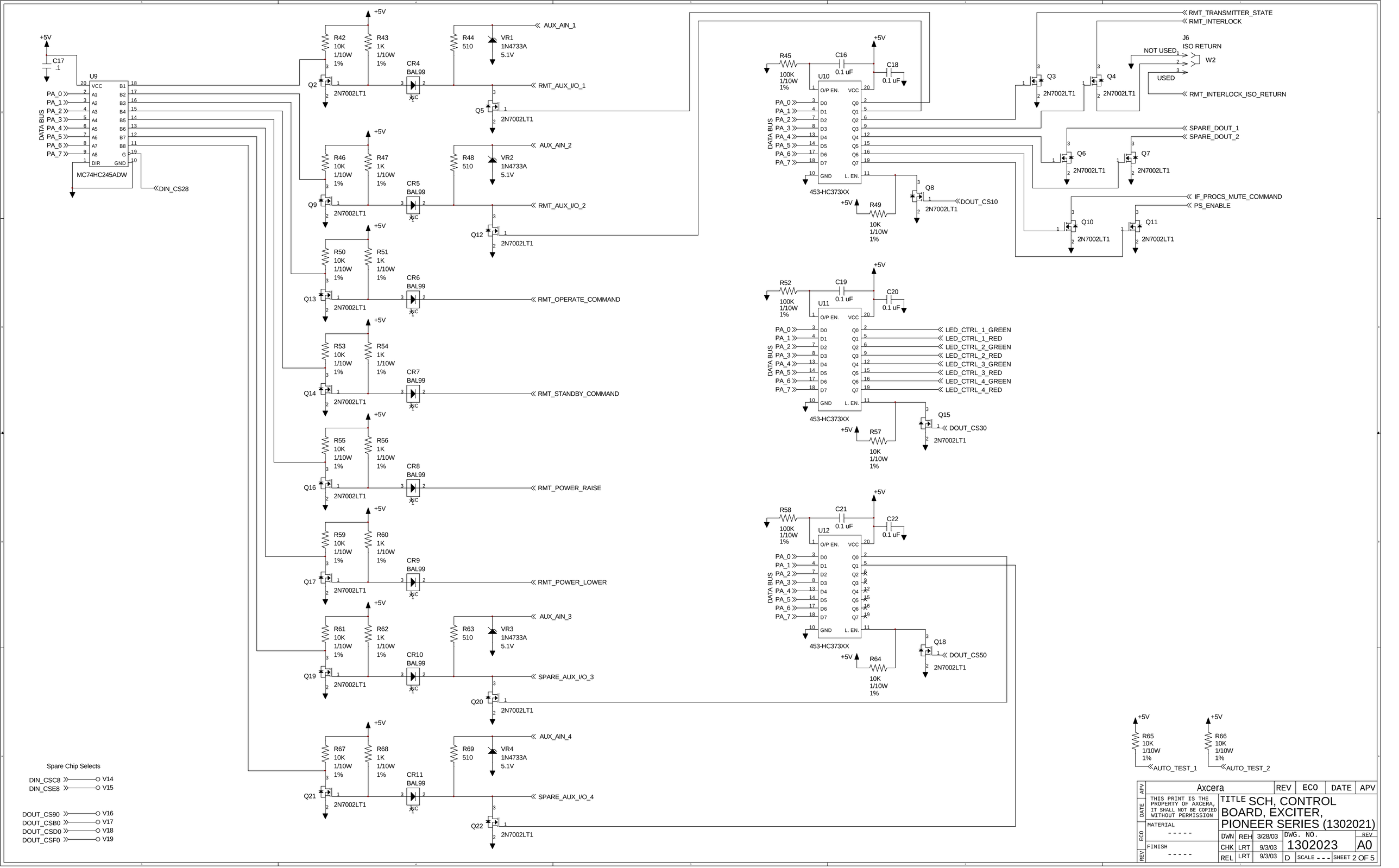
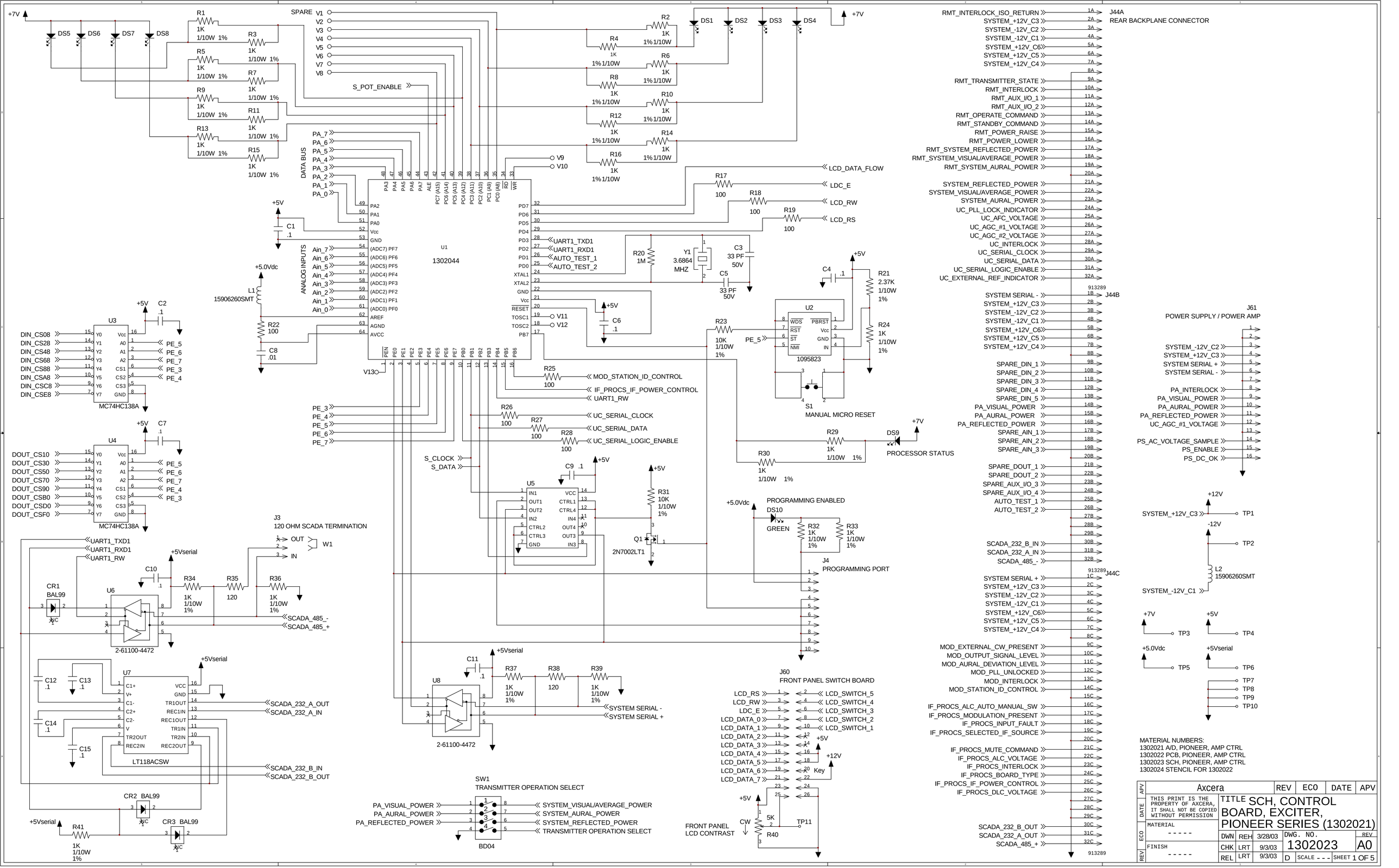
ECO	MATERIAL -----	DWN REH 3/28/03	DWG. NO. 1302023		REV A0
REV	FINISH -----	CHK LRT 9/3/03			
		REL LRT 9/3/03	D	SCALE - - -	SHEET 3 OF 5


+5V
C17
.1
U9
MC74HC245ADW
DATA BUS
PA_0
PA_1
PA_2
PA_3
PA_4
PA_5
PA_6
PA_7
VCC
A1
A2
A3
A4
A5
A6
A7
A8
DIR
GND
B1
B2
B3
B4
B5
B6
B7
B8
G
DIN_CS28
R42
10K
1/10W
1%
R43
1K
1/10W
1%
Q2
2N7002LT1
CR4
BAL99
NC
R44
510
VR1
1N4733A
5.1V
AUX_AIN_1
RMT_AUX_I/O_1
Q5
2N7002LT1
R46
10K
1/10W
1%
R47
1K
1/10W
1%
Q9
2N7002LT1
CR5
BAL99
R48
510
VR2
1N4733A
5.1V
AUX_AIN_2
RMT_AUX_I/O_2
Q12
2N7002LT1
R50
10K
1/10W
1%
R51
1K
1/10W
1%
Q13
2N7002LT1
CR6
BAL99
RMT_OPERATE_COMMAND
R53
10K
1/10W
1%
R54
1K
1/10W
1%
Q14
2N7002LT1
CR7
BAL99
RMT_STANDBY_COMMAND
R55
10K
1/10W
1%
R56
1K
1/10W
1%
Q16
2N7002LT1
CR8
BAL99
RMT_POWER_RAISE
R59
10K
1/10W
1%
R60
1K
1/10W
1%
Q17
2N7002LT1
CR9
BAL99
RMT_POWER_LOWER
R61
10K
1/10W
1%
R62
1K
1/10W
1%
Q19
2N7002LT1
CR10
BAL99
R63
510
VR3
1N4733A
5.1V
AUX_AIN_3
SPARE_AUX_I/O_3
Q20
2N7002LT1
R67
10K
1/10W
1%
R68
1K
1/10W
1%
Q21
2N7002LT1
CR11
BAL99
R69
510
VR4
1N4733A
5.1V
AUX_AIN_4
SPARE_AUX_I/O_4
Q22
2N7002LT1
Spare Chip Selects
DIN_CSC8
DIN_CSE8
V14
V15
DOUT_CS90
DOUT_CSB0
DOUT_CSD0
DOUT_CSF0
V16
V17
V18
V19
R45
100K
1/10W
1%
C16
0.1 uF
C18
0.1 uF
U10
453-HC373XX
O/P EN.
L. EN.
R49
10K
1/10W
1%
Q8
2N7002LT1
DOUT_CS10
RMT_TRANSMITTER_STATE
RMT_INTERLOCK
J6
ISO RETURN
NOT USED
USED
W2
RMT_INTERLOCK_ISO_RETURN
Q3
Q4
SPARE_DOUT_1
SPARE_DOUT_2
Q6
Q7
IF_PROCS_MUTE_COMMAND
PS_ENABLE
Q10
Q11
R52
100K
1/10W
1%
C19
0.1 uF
C20
0.1 uF
U11
453-HC373XX
LED_CTRL_1_GREEN
LED_CTRL_1_RED
LED_CTRL_2_GREEN
LED_CTRL_2_RED
LED_CTRL_3_GREEN
LED_CTRL_3_RED
LED_CTRL_4_GREEN
LED_CTRL_4_RED
R57
10K
1/10W
1%
Q15
DOUT_CS30
R58
100K
1/10W
1%
C21
0.1 uF
C22
0.1 uF
U12
453-HC373XX
R64
10K
1/10W
1%
Q18
DOUT_CS50
R65
10K
1/10W
1%
AUTO_TEST_1
R66
10K
1/10W
1%
AUTO_TEST_2
Axcera
REV
ECO
DATE
APV
THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION
MATERIAL
FINISH
TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)
DWN REH 3/28/03
CHK LRT 9/3/03
REL LRT 9/3/03
DWG. NO. 1302023
REV A0
D
SCALE - - -
SHEET 2 OF 5


U1
1302044
DATA BUS
ANALOG INPUTS
U2
1095823
S1
MANUAL MICRO RESET
U3
MC74HC138A
U4
MC74HC138A
U5
2N7002LT1
U6
2-61100-4472
U7
LT118ACSW
U8
2-61100-4472
J44A
REAR BACKPLANE CONNECTOR
J44B
J44C
J61
POWER SUPPLY / POWER AMP
J3
120 OHM SCADA TERMINATION
W1
J4
PROGRAMMING PORT
J60
FRONT PANEL SWITCH BOARD
SW1
TRANSMITTER OPERATION SELECT
BD04
PROGRAMMING ENABLED
PROCESSOR STATUS
FRONT PANEL
LCD CONTRAST
MOD_STATION_ID_CONTROL
IF_PROCS_IF_POWER_CONTROL
UC_SERIAL_CLOCK
UC_SERIAL_DATA
UC_SERIAL_LOGIC_ENABLE
SCADA_232_A_OUT
SCADA_232_A_IN
SCADA_232_B_IN
SCADA_232_B_OUT
SCADA_485_-
SCADA_485_+
SYSTEM SERIAL -
SYSTEM SERIAL +
LCD_DATA_FLOW
LDC_E
LCD_RW
LCD_RS
S_POT_ENABLE
S_CLOCK
S_DATA
UART1_TXD1
UART1_RXD1
UART1_RW
AUTO_TEST_1
AUTO_TEST_2
MATERIAL NUMBERS:
1302021 A/D, PIONEER, AMP CTRL
1302022 PCB, PIONEER, AMP CTRL
1302023 SCH, PIONEER, AMP CTRL
1302024 STENCIL FOR 1302022
Axcera
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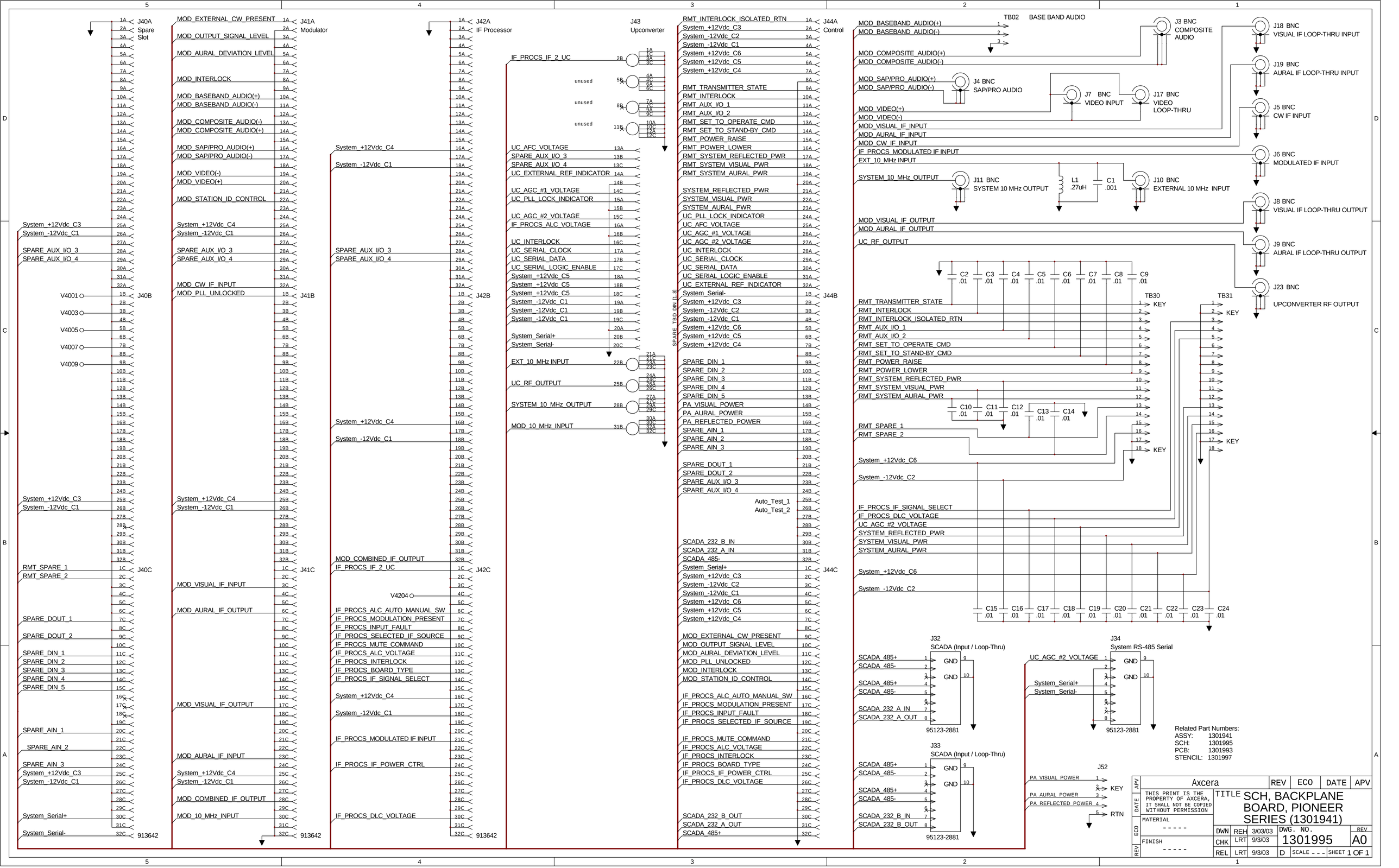
TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)
DWG. NO. 1302023
REV A0
SCALE - - -
SHEET 1 OF 5


J40A Spare Slot
J41A Modulator
J42A IF Processor
J43 Upconverter
J44A Control
J40B
J41B
J42B
J44B
J40C
J41C
J42C
J44C
913642
MOD_EXTERNAL_CW_PRESENT
MOD_OUTPUT_SIGNAL_LEVEL
MOD_AURAL_DEVIATION_LEVEL
MOD_INTERLOCK
MOD_BASEBAND_AUDIO(+)
MOD_BASEBAND_AUDIO(-)
MOD_COMPOSITE_AUDIO(-)
MOD_COMPOSITE_AUDIO(+)
MOD_SAP/PRO_AUDIO(+)
MOD_SAP/PRO_AUDIO(-)
MOD_VIDEO(-)
MOD_VIDEO(+)
MOD_STATION_ID_CONTROL
MOD_CW_IF_INPUT
MOD_PLL_UNLOCKED
MOD_VISUAL_IF_INPUT
MOD_AURAL_IF_OUTPUT
MOD_VISUAL_IF_OUTPUT
MOD_AURAL_IF_INPUT
MOD_COMBINED_IF_OUTPUT
MOD_10_MHz_INPUT
IF_PROCS_IF_2_UC
UC_AFC_VOLTAGE
SPARE_AUX_I/O_3
SPARE_AUX_I/O_4
UC_EXTERNAL_REF_INDICATOR
UC_AGC_#1_VOLTAGE
UC_PLL_LOCK_INDICATOR
UC_AGC_#2_VOLTAGE
IF_PROCS_ALC_VOLTAGE
UC_INTERLOCK
UC_SERIAL_CLOCK
UC_SERIAL_DATA
UC_SERIAL_LOGIC_ENABLE
System_+12Vdc_C5
System_+12Vdc_C4
System_-12Vdc_C1
System_Serial+
System_Serial-
EXT_10_MHz INPUT
UC_RF_OUTPUT
SYSTEM_10_MHz_OUTPUT
MOD_10_MHz_INPUT
IF_PROCS_ALC_AUTO_MANUAL_SW
IF_PROCS_MODULATION_PRESENT
IF_PROCS_INPUT_FAULT
IF_PROCS_SELECTED_IF_SOURCE
IF_PROCS_MUTE_COMMAND
IF_PROCS_ALC_VOLTAGE
IF_PROCS_INTERLOCK
IF_PROCS_BOARD_TYPE
IF_PROCS_IF_SIGNAL_SELECT
IF_PROCS_MODULATED IF INPUT
IF_PROCS_IF_POWER_CTRL
IF_PROCS_DLC_VOLTAGE
V4204
unused
RMT_INTERLOCK_ISOLATED_RTN
RMT_TRANSMITTER_STATE
RMT_INTERLOCK
RMT_AUX_I/O_1
RMT_AUX_I/O_2
RMT_SET_TO_OPERATE_CMD
RMT_SET_TO_STAND-BY_CMD
RMT_POWER_RAISE
RMT_POWER_LOWER
RMT_SYSTEM_REFLECTED_PWR
RMT_SYSTEM_VISUAL_PWR
RMT_SYSTEM_AURAL_PWR
SPARE_DIN_1
SPARE_DIN_2
SPARE_DIN_3
SPARE_DIN_4
SPARE_DIN_5
PA_VISUAL_POWER
PA_AURAL_POWER
PA_REFLECTED_POWER
SPARE_AIN_1
SPARE_AIN_2
SPARE_AIN_3
SPARE_DOUT_1
SPARE_DOUT_2
Auto_Test_1
Auto_Test_2
SCADA_232_B_IN
SCADA_232_A_IN
SCADA_485-
SCADA_232_B_OUT
SCADA_232_A_OUT
SCADA_485+
SPARE_TBD_DIN_[1..8]
TB02 BASE BAND AUDIO
J3 BNC COMPOSITE AUDIO
J18 BNC VISUAL IF LOOP-THRU INPUT
J19 BNC AURAL IF LOOP-THRU INPUT
J4 BNC SAP/PRO AUDIO
J7 BNC VIDEO INPUT
J17 BNC VIDEO LOOP-THRU
J5 BNC CW IF INPUT
J6 BNC MODULATED IF INPUT
J11 BNC SYSTEM 10 MHz OUTPUT
L1 .27uH
C1 .001
J10 BNC EXTERNAL 10 MHz INPUT
J8 BNC VISUAL IF LOOP-THRU OUTPUT
J9 BNC AURAL IF LOOP-THRU OUTPUT
J23 BNC UPCONVERTER RF OUTPUT
TB30
TB31
KEY
RTN
J32 SCADA (Input / Loop-Thru)
J33 SCADA (Input / Loop-Thru)
J34 System RS-485 Serial
GND
95123-2881
J52
PA_VISUAL_POWER
PA_AURAL_POWER
PA_REFLECTED_POWER
Related Part Numbers:
ASSY: 1301941
SCH: 1301995
PCB: 1301993
STENCIL: 1301997
Axcera
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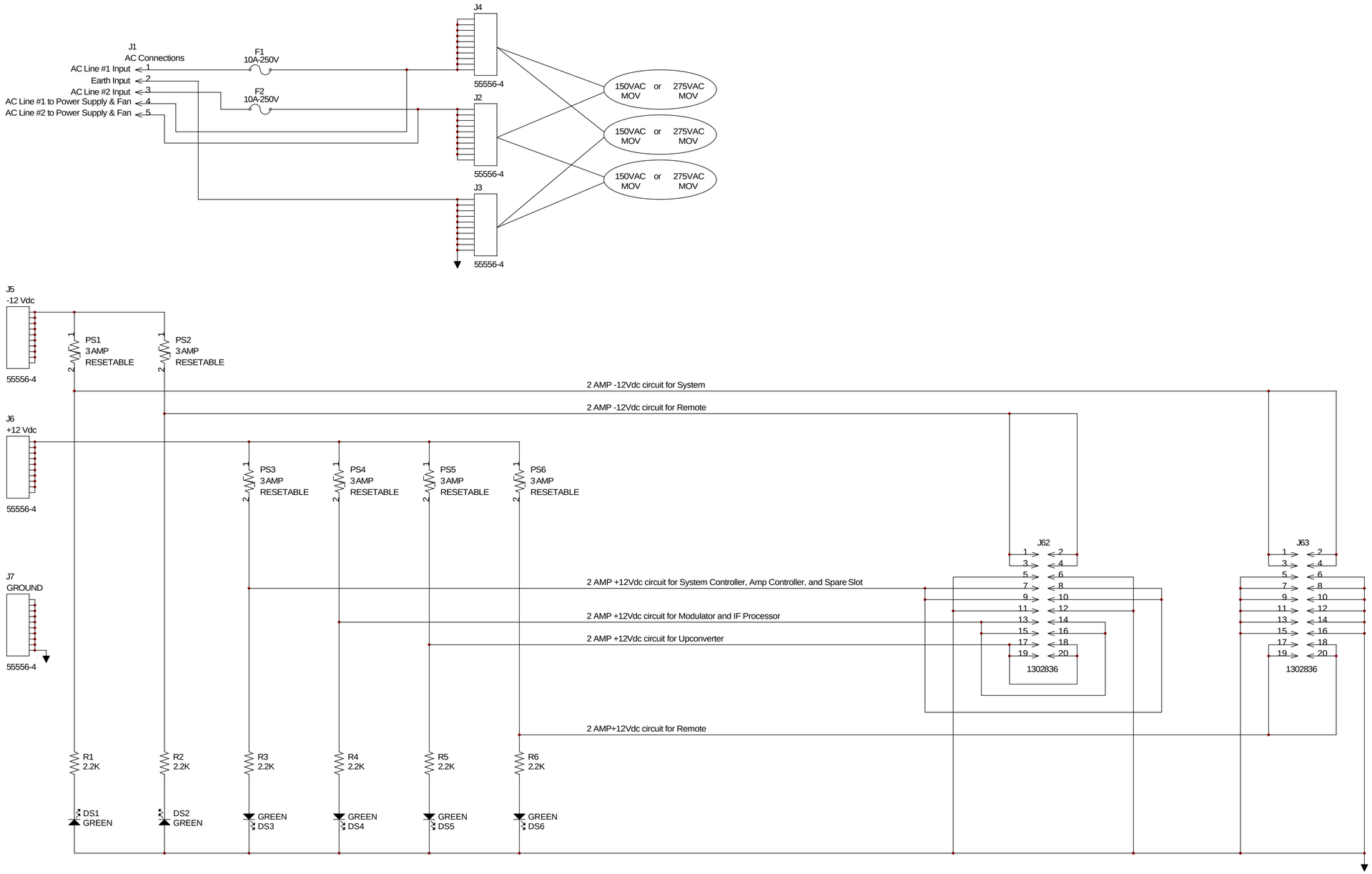
TITLE SCH, BACKPLANE BOARD, PIONEER SERIES (1301941)
MATERIAL -----
FINISH -----
DWN REH 3/03/03
CHK LRT 9/3/03
REL LRT 9/3/03
DWG. NO. 1301995
REV A0
SCALE ---
SHEET 1 OF 1



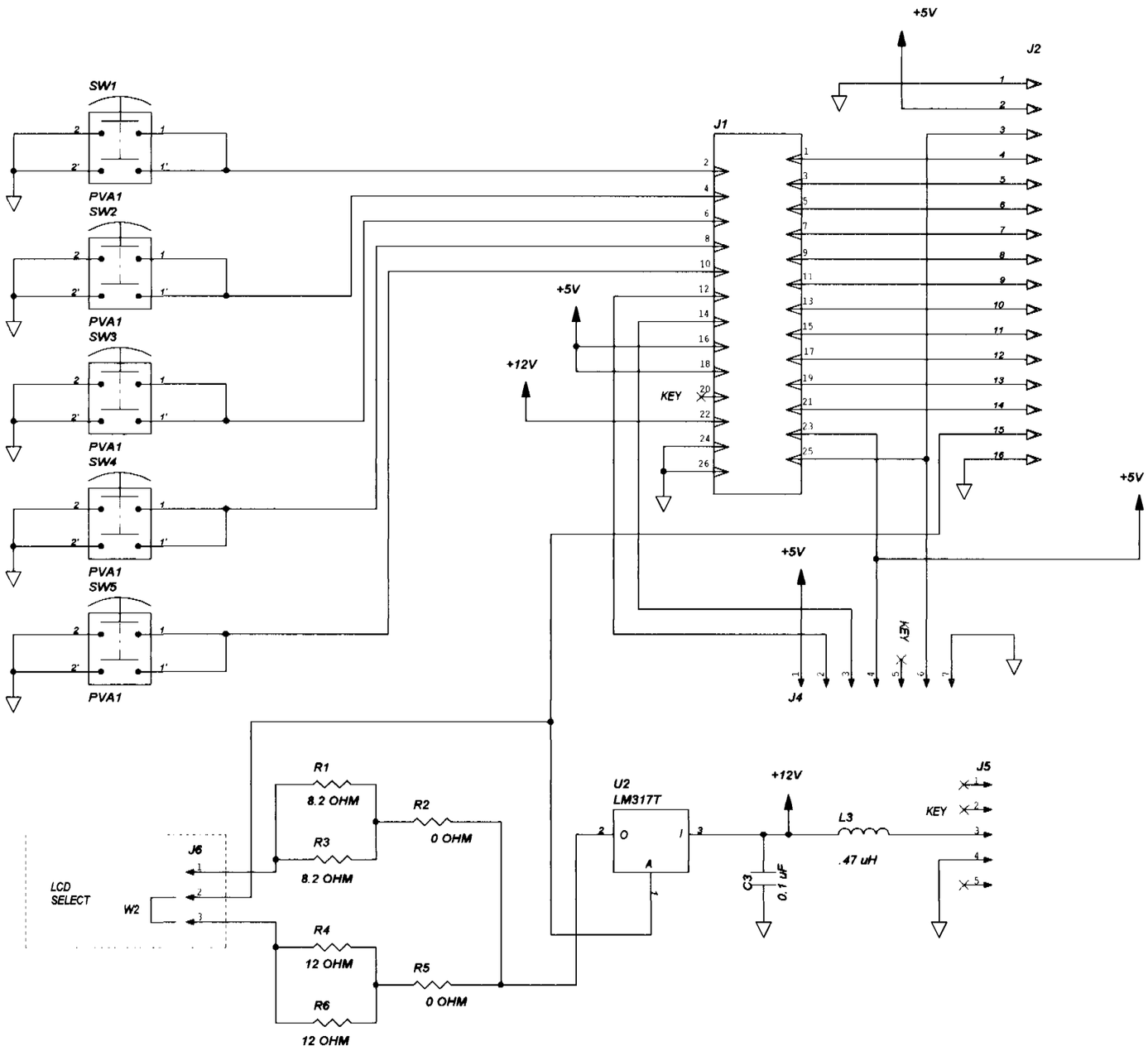
Circuit Design Notes:

1. Track widths of 0.140 inch minimum top and bottom of board shall be used to connections to J1, J2, J3, J4.
2. Track widths of 0.140 inch minimum top of board shall be used to connections to J5 and J6.
3. Track widths of 0.065 inch minimum shall be used to connections to J62 and J63.
4. Track widths of 0.020 inch minimum shall be used to connections between LEDs and resistors.
5. Board BOM needs the following items added to those exported from Orcad:

Part Number	Qty	Description
102071	4	Fuse Clip, PC BD Mnt., 15 Amp

MATERIAL NUMBERS:
1302837 PIONEER, POWER PROTECTION
1302838 PCB, PIONEER, PWR PROTECT
1302839 SCH, PIONEER, PWR PROTECT
1302840 STENCIL FOR 1302838

APV	Axcera	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH, PIONEER, PWR PROTECT (1302837)			
ECO	MATERIAL -----	DWN REH 5/29/03	DWG. NO. 1302839		REV AO
	FINISH -----	CHK REH 5/29/03			
REV		REL REH 5/29/03	D	SCALE - - -	SHEET 1 OF 1



REV	ECN	DATE	APV
3	8603	11/7/96	RAS
AT J2 W2 WAS W1. (TMY)			
2	8424	9/29/96	JCM
SWITCHED PINS 1 & 2 OF U2. (TMY)			
1	8368	8/27/96	RAS

DELETED C1, C2, L1, L2, U1, J3, & W1. MOVED W2 FROM J6-1,-2 TO J6 -2,-3. JKF

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MATERIAL ---

FINISH ---

TITLE SCHEMATIC SWITCH BOARD (1527-1406)

DWN	DLM	6/3/96
CHK	RAS	6/14/96
REL	RAS	6/14/96

DWG. NO. 1527-3406 REV 3

B SCALE --- SHEET 1 OF 1