# Chapter 4
# Circuit Descriptions

## 4.1 (A2) Modulator Module (1301929; Appendix B)

**NOTE:** Not used in a translator system.

### *4.1.1 Analog Modulator Board (1301797; Appendix B)*

The board takes the audio and video inputs and produces a modulated visual IF + aural IF output.

***Main Audio and Aural IF portion of the board***

The analog modulator board takes each of the three possible audio inputs and provides a single audio output.

*4.1.1.1 MONO, Balanced Audio Input*

The first of the three possible baseband inputs to the board is a 600-Ω, balanced-audio input (0 to +10 dBm) that enters through jack J41A, pins 10A (+), 12A (GND), and 11A (-), and is buffered by U11A and U11B. Diodes CR9, CR10, CR12 and CR13 protect the input to U11A and U11B if an excessive signal level is present on the input. The outputs of U11A and U1B are applied to differential amplifier U11C. U11C eliminates any common mode signals (hum) on its input leads. A pre-emphasis of 75 ms is provided by R97, C44, and R98 and can be eliminated by removing jumper W6 on J22. The signal is then applied to amplifier U11D whose gain is controlled by jumper W7 on J23. Jumper W7 on jack J23 is positioned according to the input level of the audio signal (0 or +10 dBm). If the input level is approximately 0 dBm, the mini-jumper should be in the high gain position between pins 1 and 2 of jack J23. If the input level is approximately +10 dBm, the mini-jumper should be in low gain position between pins 2 and 3 of jack J23. The balanced audio is then connected to buffer amplifier U12A whose input level is determined by the setting of the MONO, balanced audio gain pot R110, accessed through the front panel. The output of the amplifier stage is wired to the summing point at U13C, pin 9.

*4.1.1.2 STEREO, Composite Audio Input*

The second possible audio input to the board is the composite audio (stereo) input that connects to the board at J41A Pin 14A (+) and J41A Pin 13A (-).

**NOTE:** For the transmitter to operate using the composite audio input the Jumper W1 on J4 must be between Pins 2 and 3, the Jumper W2 on J6 must be between Pins 2 and 3 and the Jumper W4 on J5 must be between Pins 1 and 2. These jumpers connect the composite audio to the rest of the board.

Jumper W14 on jack J26 provides a 75Ω-input impedance when the jumper is between pins 1 and 2 and a high impedance when it is between pins 2 and 3. Diodes CR17, CR18, CR20 and CR21 protect the input stages of U14A and U14B if an excessive signal level is applied to the board. The outputs of U14A and U14B are applied to differential amplifier U13A, which eliminates common mode signals (hum) on its input leads. The composite input signal is then applied to amplifier U13B; whose gain is controlled by the STEREO, composite audio gain pot R132, accessed through the front panel. The composite audio signal is then connected to the summing point at U13C, pin 9.

*4.1.1.3 SAP/PRO, Subcarrier Audio Input*

The third possible input to the board is the SAP/PRO, SCA audio input at J41A pin 16A(+) and 17A(-). The SCA input has an input matching impedance of 75Ω that can be eliminated by removing jumper W15 from pins 1 and 2 of J28. The SCA input is bandpass filtered by C73, C74, R145, C78, C79, and R146 and is fed to buffer

amplifier U13D. The amplified signal is then applied though the SAP/PRO, SCA gain pot R150, accessed through the front panel, to the summing point at pin 9 of U13C.

*4.1.1.4 Audio Modulation of the 4.5 MHz VCO*

The Mono balanced audio, or the Stereo composite audio, or the SAP/PRO SCA buffered audio signal, is fed to the common junction of resistors R111, R130, and R152 that connect to pin 9 of amplifier U13C. The output audio signal at pin 8 of U13C is typically .8 Vpk-pk at a ±25-kHz deviation for Mono balanced audio or .8 Vpk-pk at ±75-kHz deviation for Stereo composite audio as measured at Test Point TP1. This audio deviation signal is applied to the circuits containing the 4.5 MHz aural VCO U16. A sample of the aural deviation level is amplified, detected by U15A and U15B, and connected to J41A pin 5A on the board. This audio-deviation level is connected to the front panel display on the Control/Power Supply Assembly.

The audio from U13C is connected thru C71, a frequency response adjustment, to varactor diodes, CR24 to CR27, that frequency modulates the audio signal onto the generated 4.5-MHz signal by U16. U16 is the 4.5-MHz VCO that generates the 4.5-MHz continuous wave (CW) signal. The output frequency of the 4.5 MHz signal is maintained and controlled by the correction voltage output of the U21 PLL integrated circuit (IC), at "N", that connects to the varactor diodes. The audio-modulated, 4.5-MHz signal is fed through the emitter follower Q13 to the amplifiers U17A and U17B. The amplified output of U17A is connected to a 4.5-MHz filter and then to U17B. The output of U17B is connected to the 4.5-MHz output sample jack at J29 and through the Jumper W4 on J5 pins 1 & 2, "J", to the I input of the mixer Z1.

*4.1.1.5 Phase Lock Loop (PLL) Circuit*

A sample of the signal from the 4.5-MHz aural VCO at the output of Q13, "M", is applied to PLL IC U21 at pin 1 the $F_{in}$ connection. In U21, the signal is divided down to 50 kHz and is compared to a 50-kHz reference signal. The reference signal is a divided-down sample of the 45.75-MHz visual IF signal that is applied to the oscillator-in connection at Pin 27 on the PLL chip. These two 50-kHz signals are compared in the IC and the fV, and fR is applied to the differential amplifier U18A. The output of U18A, "N", is fed back through CR28 and C85 to the 4.5-MHz VCO IC U16; this sets up a PLL circuit. The 4.5-MHz VCO will maintain the extremely accurate 4.5-MHz separation between the visual and aural IF signals; any change in frequency will be corrected by the AFC error voltage.

PLL chip U21 also contains an internal lock detector that indicates the status of the PLL circuit. When U21 is in a "locked" state, pin 28 is high. If the 4.5-MHz VCO and the 45.75-MHz oscillator become "unlocked," out of the capture range of the PLL circuit, pin 28 of U21 will go to a logic low and cause the LED DS5 to light red. The Aural Unlock LED is viewed through the front panel of the Assembly. An Aural unlock, PLL Unlocked, output signal from Q16 is also applied to jack J41B pin 1B.

***Sync tip clamp and the visual and aural modulator portions of the board***

The sync tip clamp and modulator portion of the board is made up of four circuits: the main video circuit, the sync tip clamp circuit, the visual modulator circuit and the aural modulator circuit.

The clamp portion of the board maintains a constant peak of sync level over varying average picture levels (APL). The modulator portion of the board contains the circuitry that generates an amplitude-modulated vestigial sideband visual IF signal output that is made up of the baseband video input signal (.5 to 1 Vpk-pk) modulated onto a 45.75-MHz IF carrier

frequency. The visual IF signal and the aural IF signal are then combined in the diplexer circuit to produce the visual IF + aural IF output, "G", that is connected to J41C pin 28C the Combined IF output of the board.

*4.1.1.6 Main Video Signal Path (Part 1 of 2)*

The baseband video input connects to the board at J41A pins 19A (-), "W", and 20A (+), "V". The +, "V" and -, "W", video inputs are fed to Diodes CR1 to CR4 that form a voltage-limiter network in which, if the input voltages exceed the supply voltages for U2B, the diodes conduct, preventing damage to U2B. CR1 and CR3 conduct if the input voltage exceeds the negative supply and CR2 and CR4 conduct if the input voltage exceeds the positive supply voltage. The baseband video input connects to the non-inverting and inverting inputs of U2B, a differential amplifier that minimizes any common-mode problems that may be present on the incoming signal

The video output of U2B is connected through the Video Gain pot R42, accessed through the front panel, to the amplifier U2A. The output of U2A connects to the delay equalizer circuits

*4.1.1.7 Delay Equalizer Circuits*

The delay equalizer circuits provide a delay to the video signal, correction to the frequency response, and amplification of the video signal.

The video output of U2A is wired to the first of four delay-equalizing circuits that shape the video signal to the FCC specification for delay equalization or to the shape needed for the system. The board has been factory-adjusted to this FCC specification and should not be readjusted without the proper equipment.

Resistors R53, R63, R61, and R58 adjust the sharpness of the response curve while inductors GD1, GD2, GD3, and GD4 adjust the position of the curve. The group delayed video signal at the output of U3A is split with a sample connected to J8 on the board that can be used for testing purposes of the Post Video Delay signal. The other portion of the video signal connects through the Jumper W5 on J9 pins 2 and 3. The video is slit with one part connecting to a sync tip clamp circuit and the other part to the main video output path through R44. A sample of the video at "P" connects to U32 and U33 that provide a zero adjust and a 1 Volt output level, which connects at "T" to J41A pin 3A. This video level is wired to the Control/Power Supply assembly.

*4.1.1.8 Sync Tip Clamp Circuit*

The automatic sync tip clamp circuit is made up of U6A, Q8, U5C, and associated components. The circuit begins with a sample of the clamped video that buffered by U3A, which is split off from the main video path that connects to U6A. The level at which the tip of sync is clamped, to -1.04 VDC as set by the voltage-divider network, R77, R78, R75, R76 and R80 connected to U6A. If the video level changes, the sample applied to U6A changes. The voltage from the clamp circuit that is applied to the summing circuit at the base of Q8 will change; this will bring the sync tip level back to -1.04 VDC. Q8 will be turned off and on according to the peak of sync voltage level that is applied to U6A. The capacitors C35 and C24, in the output circuit of Q8, will charge or discharge to the new voltage level. This will bias U5C more or less, through the front panel MANUAL/AUTO CLAMP switch, SW1, when it is in the Auto Clamp-On position, between pins 2 and 3. In AUTO CLAMP, U5C will increase or decrease its output, as needed, to bring the peak of sync back to the correct level. The voltage level is applied through U5C to U2A. In the Manual CLAMP position, SW1 in manual position, between pins 1 and 2, the adjustable resistor R67 provides the manual clamp bias adjustment for the video that connects to U5C. This level is set at the factory and is not adjustable by the customer. In Manual clamp the peak

of sync auto clamp circuit will not automatically be clamped to the pre set level.

*4.1.1.9 Main Video Signal Path (Part 2 of 2)*

A sample of the clamped video output from the group delay circuitry at the junction of R44, R62 and R300 is connected to a white clipper circuit consisting of Q1 and associated circuitry. The base voltage of Q1 is set by the voltage divider network consisting of R1, R9 and R5. R5 is variable and sets the level of the white clipper circuit to prevent video transients from over modulating the video carrier.

The clamped video output of amplifier U3A is split with one part connected through R35 to J8 that provides a sample of the Post Video Delay Signal.

The other clamped video path from U3A is through jumper W5 on J9 pins 2 & 3 through R44 to a sync-stretch circuit that consists of Q3 and Q4. The sync-stretch circuit contains R19, which adjusts the Sync Stretch Magnitude (amount), R11, which adjusts the Sync Stretch Cut-In and R6, which adjusts the Sync Clipping point. This sync-stretch adjustment should not be used to correct for output sync problems, but it can be used for video input sync problems. The output of the sync-stretch circuit is amplified by U31A and connected, "K", to pin 5, the I input of Mixer Z2, the Visual IF Mixer.

*4.1.1 10 45.75 MHz Oven Oscillator Circuit*

The oven oscillator portion of the board generates the visual IF CW signal at 45.75 MHz for NTSC system "M" usage.

The +12 VDC needed to operate the oven is applied through jack J30 pin 1 on the crystal oven HR1. The oven is preset to operate at 60° C. The oven encloses the 45.75 MHz crystal Y1 and stabilizes the crystal temperature. The crystal is the principal device that determines the operating frequency and is the most sensitive in terms of temperature stability.

Crystal Y1 operates in an oscillator circuit consisting of transistor Q24 and its associated components. Feedback that is provided by a voltage divider, consisting of C173, L38 and R295, is fed to the base of Q24 through C169. This circuitry operates the crystal in a common-base amplifier configuration using Q24. The operating frequency of the oscillator is maintained by a PLL circuit, which consists of ICs U20 and U22 and associated components, whose PLL output connects to R293 in the crystal circuit.

The oscillator circuit around Q24 has a regulated voltage, +6.8 VDC, which is produced from the +12 VDC by a combination of dropping resistor R261, diodes CR37 and CR38 and Zener diode VR2. The output of the oscillator at the collector of Q24 is capacitively coupled through C165 to the base of Q23. The small value of C165, 15 pF, keeps the oscillator from being loaded down by Q23. Q23 is operated as a common-emitter amplifier stage whose bias is provided through R259 from the +12 VDC line. The output of Q23, at its collector, is connected to an emitter-follower transistor stage, Q21. The output of Q21 at its emitter is split. One path connects to the input of the IC U20 in the PLL circuit. The other path is through R270 to establish an approximate 50-ohm source impedance through C166 to the Pin 1 contact of the relay K2. The 45.75 MHz connects through the closed contacts 0of K2 to a splitter network consisting of L31 and L32.

**NOTE:** The relay contacts for the internally generated 45.75 MHz signal will be closed unless an external IF signal, such as the IF for offset and precise frequency 45.74 or 45.76 MHz, connects to the board. The external IF CW Input connects at J41A pin 32A and is connected to J19 and through the external cable assembly W10 back to the board at J20. The external IF CW input is split on the board. One branch connects through C157 to a buffer amplifier Q20 to the K2 relay at pin 14. The other path is

through C152 to the amplifier U23A. The output of U23A is split with one part connecting to Q26 that shuts down the 45.75 MHz oscillator. Another path connects to Q25 the conducts and lights the LED DS7, Alternate IF, viewed on the front panel. The final path connects through R268 to Q22 that is biased on and energizes the relay, K2. The external IF CW Input at contact 14 now connects through the closed contact to the splitter network consisting of L31 and L32.

Either the internal or external CW IF from the K2 relay is split with one path through L31 to the amplifier U28 to the L input of Z1 the Aural IF Mixer. The other path is through L32 to the amplifier U29 to the L input of Z2 the Visual IF Mixer.

*4.1.1.11 Visual Modulator Circuit*

The video signal is heterodyned in mixer Z2 with the visual IF CW signal (45.75 MHz). The visual IF CW signal from L32 of the splitter connects to U29, where it is amplified and wired to pin 1, the L input of mixer Z2. Adjustable capacitor C168 and resistor R275 are set up to add a small amount of incidental carrier phase modulation (ICPM) correction to the output of the mixer stage to compensate for any non-linearities generated by the mixer.

The modulated 45.75-MHz RF output of mixer Z2, at pin 4 the R output, is amplified by U30 and is fed to J17 through W8, the external cable assembly, "WB", to J13 on the board. J17 is the visual IF loop-through output jack that is normally jumpered to J13 on the board. The modulated visual IF through J13 connects to J41C pin 17C the Visual IF Output of the board.

*4.1.1.12 Aural Modulator Circuit*

The 4.5 MHz aural modulated signal is heterodyned in mixer Z1 with the 45.75 MHz IF CW signal. The mixer Z1 heterodynes the aural-modulated, 4.5-MHz signal with the 45.75-MHz CW signal to produce the modulated 41.25-MHz aural IF signal. The audio modulated 4.5 MHz from 4.5 MHz VCO IC U16 connects, "J", to the I input at pin 5 of Z1. The visual IF CW signal from L31 of the splitter connects to U28, where it is amplified and wired to pin 1, the L input of mixer Z1. The R output of the mixer at pin 4 is fed to a bandpass filter, consisting of L18-L21, L25-L28 and C136, C137 and C142-144, that is tuned to pass only the modulated 41.25-MHz aural IF signal. The filtered 41.25 MHz is fed to the amplifier U27. The amplified 41.25-MHz signal is connected by a coaxial cable, W9, from J21, "WC", to J18 on the board. The modulated 41.25-MHz aural IF signal from J18 is connected to J41C pin 6C the Aural IF Output of the board.

*4.1.1.13 Combining the 45.75 MHz Visual IF and 41.25 MHz Aural IF Signals*

The Visual IF connects back to the board at J41C pin 3C, through a Visual IF jumper cable connected to the rear chassis of the exciter/driver. IF processing equipment can be connected in place of the jumper if needed. The visual IF is connected to J12, through jumper W7, "WA", to J14. The visual IF is amplified by U24 and filtered by FL1 with T1 and T2 providing isolation. The filtered IF is amplified by U25 and adjusted in level by R214 before it is connected to a summing circuit at the common connection of L16 and L17.

The Aural IF connects back to the board at J41C pin 23C, through an Aural IF jumper cable connected to the rear chassis of the exciter/driver. IF processing equipment can be connected in place of the jumper if needed. The aural IF, "F", is connected through C132, R234, R235 and adjusted in level by R243 before it is connected to a summing circuit at the common connection of L17 and L16.

The Aural IF and Visual IF signals are combined through L16 and L17. The frequency response of the combined 41.25 MHz + 45.75 MHz signal is set by R238 and R239 and associated components. The corrected combined IF signal is amplified by U25 and connected to a splitter

matching network consisting of T3 and T4. One part of signal connects to J10, the 41.25 MHz + 45.75 MHz sample output jack, located on the front panel. The other part, "G", connects to J41C pin 28C the Combined IF Output of the board.

*4.1.1.14 Voltage Requirements*

The ±12 VDC needed for the operation of the board enters through jack J41A pins 25A (+12 VDC) and 26A (-12 VDC). The +12 VDC is filtered by L6, L7, and C27 before it is connected to the rest of the board. The +12 VDC also connects to U7, a 5-volt regulator IC, that provides +5 VDC to the rest of the board.

The -12 VDC is filtered by L5, C16, and C17 before it is connected to the rest of the board.

## 4.2 (A3) IF Processor Module Assembly (1301938; Appendix B)

The IF from the 8 VSB modulator enters the module and the signal is pre-corrected as needed for amplitude linearity correction, Incidental Carrier Phase Modulation (ICPM) correction and frequency response correction.

The Module contains the following board.

### *4.2.1 IF Processor Board (1301977; Appendix B)*

The automatic level control (ALC) portion of the board provides the ALC and amplitude linearity correction of the IF signal. The ALC adjusts the level of the IF signal that controls the output power of the transmitter.

The IF from the 8 VSB modulator enters the board at J1B pin 32B. If the (optional) receiver tray is present, the IF input (-6 dBm) from the 8 VSB modulator tray connects to the modulated IF input jack J1C Pin 21C. The modulated IF input connects to relay K3 and the receiver IF input connects to relay K4. The two relays are controlled by the Modulator Select command that is connected to J1C Pin 14C on the board. Modulator select enable/disable jumper W11 on J29 controls whether the Modulator Select command at J1C Pin 14C controls the operation of the relays. With jumper W11 on J29 between pins 1 and 2, the Modulator Select command at J1C Pin 14C controls the operation of the relays; with jumper W11 on J29, pins 2 and 3, the modulator is selected all of the time.

*4.2.1.1 Modulator Selected*

With the modulator selected, J1C-14C low, this shuts off Q12 and causes Pin 8 on the relays to go high that causes relays K3 and K4 to de-energize. When K4 is de-energized, it connects the receiver IF input at J1C-21C, if present, to a 50Ω load. When K3 is de-energized, it connects the modulator IF input at J1B-32B to the rest of the board; Modulator Enable LED DS5 will be illuminated.

*4.2.1.2 External Modulated IF Selected*

With the External Modulated IF selected, J1C-14C high, this turns on Q12 and makes pin 8 on the relays low that causes the relays K3 and K4 to energized. When K4 is energized, it connects the receiver IF input at J at J1C-21C, if present, to the rest of the board. When K3 is energized, it connects to the modulator IF input at J1B-32B to a 50Ω load. The Modulator Enable LED DS5 will not be illuminated.

*4.2.1.3 Main IF Signal Path (Part 1 of 3)*

The selected IF input (-6 dBm average) signal is split, with one half of the signal entering a bandpass filter that consists of L3, L4, C4, L5, and L6. This bandpass filter can be tuned with C4 and is substantially broader than the IF signal bandwidth. It is used to slightly steer the frequency response of the IF to make up for any small discrepancies in the frequency response in the stages that precede this point. The filter also serves the additional function of rejecting unwanted frequencies that may occur if the tray cover is off and

the tray is in a high RF environment. (If this is the case, the transmitter will have to be serviced with the tray cover off in spite of the presence of other RF signals). The filtered IF signal is fed through a pi-type matching pad consisting of R2, R3, and R4 to the pin-diode attenuator circuit consisting of CR1, CR2, and CR3.

*4.2.1.4 Input Level Detector Circuit*

The other part of the split IF input is connected through L2 and C44 to U7. U7 is an IC amplifier that is the input to the input level detector circuit. The amplified IF is fed to T4, which is a step-up transformer that feeds diode detector CR14. The positive-going detected signal is then low-pass filtered by C49, L18, and C50. This allows only the positive digital peaks to be applied through emitter follower Q1. The signal is then connected to detector CR15 to produce a peak digital voltage that is applied to op-amp U9A. There is a test point at TP3 that provides a voltage-reference check of the input level. The detector serves the dual function of providing a reference that determines the input IF signal level to the board and also serves as an input threshold detector.

The input threshold detector prevents the automatic level control from reducing the attenuation of the pin-diode attenuator to minimum, the maximum signal output, if the IF input to the board is removed. The ALC, input loss cutback, and the threshold detector circuits will only operate when jumper W2 on jack J5 is in the Enabled position, between pins 2 and 3. Without the threshold detector, and with the pin-diode attenuator at minimum, the signal will overdrive the stages following this board when the input is restored.

As part of the threshold detector operation, the minimum IF input level at TP3 is fed through detector CR15 to op-amp IC U9A, pin 2. The reference voltage for the op-amp is determined by the voltage divider that consists of R50 and R51, off the +12 VDC line. When the detected input signal level at U9A, pin 2, falls below this reference threshold, approximately 10 dB below the normal input level, the output of U9A at pin 1 goes high, toward the +12 VDC rail. This high is connected to the base of Q2 that is forward biased and creates a current path. This path runs from the -12 VDC line and through red LED DS1, the input level fault indicator, which lights, resistor R54, and transistor Q2 to +12 VDC. The high from U9A also connects through diode CR16 and R52, to U24D pin 12, whose output at pin 14 goes high. The high connects through the front panel accessible ALC Gain pot R284 and the full power set pot R252 to U24C Pin 9. This high causes U24C pin 8 to go low. A power raise/lower input from the Control/Monitoring Module connects to J42C pin 24C and is wired to Q14. This input will increase or decrease the value of the low applied to U24B and therefore increase or decrease the power output of the transmitter.

The low connects to U24B pin 5 whose output goes low. The low is wired to U24A pin2 whose output goes high. The high is applied to U10A, pin 2, whose output goes low. The low connects through the switch SW1, if it is in the auto gain position, to the pin-diode attenuator circuit, CR1, CR2 & CR3. The low reverse biases them and cuts back the IF level, therefore the output level, to 0. When the input signal level increases above the threshold level, the output power will increase, as the input level increases, until normal output power is reached.

The digital input level at TP3 is also fed to a pulse detector circuit, consisting of IC U8, CR17, Q3, and associated components, and then to a comparator circuit made up of U9C and U9D. The reference voltage for the comparators is determined by a voltage divider consisting of R243, R65, R66, and R130, off the -12 VDC line. When the input signal level to the detector at TP3 falls below this reference threshold, which acts as a loss-of-digital peak detector circuit, the output of U9C and U9D goes towards the -12 VDC rail and is split, with one part biasing on transistor Q5. A current

path is then established from the +12 VDC line through Q5, the resistors R69 and R137, and the red LED DS3, input loss indicator, which is illuminated. When Q5 is on, it applies a high to the gate of Q6. This causes it to conduct and apply a modulation loss pull-down output to J42C, pin 7C, which is applied to the front panel display on the Control/Monitor module.

The other low output of U9C and U9D is connected through CR18, CR19 & CR20 to jack J5. Jumper W2 on J5, in the Cutback Enable position, which is between pins 2 and 3, connects the low to the base of Q4 that is now forward-biased. **NOTE:** If jumper W2 is in the Disable position, between pins 1 and 2, the auto cutback will not operate. With Q4 biased on, a negative level determined by the setting of cutback level pot R71 is applied to U24D, pin 12. The level is set at the factory to cut back the output to approximately 25%. The output of U24D at pin 14 goes low and is applied through the power adjust pot to U24C, pin 9, whose output goes low.

The low connects to U24B, pin 5, whose output goes low. The low then connects to U24A, pin 2, whose output goes high. The high is applied to U10A, pin 2, whose output goes low. The low connects through the switch SW1, if it is in the auto gain position, to the to the pin-diode attenuator circuit, CR1, CR2 & CR3. The low reverse biases them and cuts back the level of the output to approximately 25%.

*4.2.1.5 Pin-Diode Attenuator Circuit*

The input IF signal is fed to a pin-diode attenuator circuit that consists of CR1, CR2 & CR3. Each of the pin diodes contains a wide intrinsic region; this makes the diodes function as voltage-variable resistors at this intermediate frequency. The value of the resistance is controlled by the DC bias supplied to the diode. The pin diodes are configured in a pi-type attenuator configuration where CR1 is the first shunt element, CR3 is the series element, and CR2 is the second shunt element. The control voltage, which can be measured at TP1, originates either from the ALC circuit when the switch SW1 is in the ALC Auto position, between pins 2 and 3, or from pot R87 when SW1 is in the Manual Gain position, between pins 1 and 2.

In the pin diode attenuator circuit, changing the amount of current through the diodes by forward biasing them changes the IF output level of the board. There are two extremes of attenuation ranges for the pin-diode attenuators. In the minimum attenuation case, the voltage, measured at TP1, approaches the +12 VDC line. There is a current path created through R6, through series diode CR3, and finally through R9 to ground. This path forward biases CR3 and causes it to act as a relatively low-value resistor. In addition, the larger current flow increases the voltage drop across R9 that tends to turn off diodes CR1 and CR2 and causes them to act as high-value resistors. In this case, the shunt elements act as a high resistance and the series element acts as a low resistance to represent the minimum loss condition of the attenuator (maximum signal output). The other extreme case occurs as the voltage at TP1 is reduced and goes towards ground or even slightly negative. This tends to turn off (reverse bias) diode CR3, the series element, causing it to act as a high-value resistor. An existing fixed current path from the +12 VDC line, and through R5, CR1, CR2, and R9, biases series element CR3 off and shunt elements, diodes CR1 and CR2, on, causing them to act as relatively low-value resistors. This represents the maximum attenuation case of the pin attenuator (minimum signal output). By controlling the value of the voltage applied to the pin diodes, the IF signal level is maintained at the set level.

*4.2.1.6 Main IF Signal Path (Part 2 of 3)*

When the IF signal passes out of the pin-diode attenuator through C11, it is applied to modular amplifier U1. This device contains the biasing and impedance-

matching circuits that makes it operate as a wide-band IF amplifier. The output of U1 connects to J40 that is jumpered to J41. The J40 jack is available, as a sample of the pre-correction IF for troubleshooting purposes and system setup. The IF signal is connector to a splitter Z1 that has an in phase output and a 90° Quadrature output, which are then connected to the linearity corrector portion of the board.

*4.2.1.7 Amplitude and Phase Pre-Correction Circuits*

The linearity corrector circuits use three stages of correction, two adjust for any amplitude non-linearities and one for phase non-linearities of the output signal. Two of the stages are in the in phase amplitude pre-correction path and one stage is in the quadrature phase pre-correction path. Each stage has a variable threshold control adjustment, R211 and R216, in the in phase path, and R231, in the quadrature path, that determines the point at which the gain is changed for that stage.

Two reference voltages are needed for the operation of the corrector circuits. The Zener diode VR3, through R261, provides the +6.8 VDC reference. The VREF is produced using the path through R265 and the diodes CR30 and CR31. They provide a .9 VDC reference, which temperature compensates for the two diodes in each corrector stage.

The first corrector stage in the in phase path operates as follows. The in phase IF signal is applied to transformer T6, which doubles the voltage swing by means of a 1:4 impedance transformation. Resistors R222 and R225 form an L-pad that lowers the level of the signal. The input signal level when it reaches a certain level causes the diodes CR24 and CR25 to turn on, generating current flow that puts them in parallel with the L-pad. When the diodes are put in parallel with the resistors, the attenuation through the L-pad is lowered, causing signal stretch.

The signal is next applied to amplifier U17 to compensate for the loss through the L-pad. The breakpoint, or cut-in point, for the first corrector is set by controlling where CR24 and CR25 turn on. This is accomplished by adjusting the threshold cut-in resistor R211. R211 forms a voltage-divider network from +6.8 VDC to ground. The voltage at the wiper arm of R211 is buffered by the unity-gain amplifier U16B. This reference voltage is then applied to R215, R216, and C134 through L44 to the CR24 diode. C134 keeps the reference from sagging during the vertical interval. The .9 VDC reference voltage is applied to the unity-gain amplifier U16D. The reference voltage is then connected to diode CR25 through choke L45. The two chokes L44 and L45 form a high impedance for RF that serves to isolate the op-amp ICs from the IF.

After the signal is amplified by U17, it is applied to the second corrector stage in the in phase path through T7. These two correctors and the third corrector stage in the quadrature path operate in the same fashion as the first. All three corrector stages are independent and do not interact with each other.

The correctors can be disabled by moving jumper W12 on J30 to the Disable position, between pins 1 and 2, this moves all of the breakpoints past the greatest peaks of digital so that they will have no affect.

The pre-distorted IF signal in the in phase path, connects to an op amp U18 whose output level is controlled by R238. R238 provides a means of balancing the level of the amplitude pre-distorted IF signal that then connects to the combiner Z2.

The pre-distorted IF signal in the quadrature path connects to op amp U20 and then step up transformer T9, next op amp U21 and step up transformer T10 and finally op amp U22 whose output level is controlled by R258. R258 provides a means of balancing the level of the Phase pre-distorted IF signal that then connects to the combiner Z2.

The amplitude and phase pre-distorted IF signals are combined by Z2 and connected to J37 that is jumpered to J36 on the board. J37 can be used for testing or monitoring purposes of the IF signal after amplitude and phase pre-distortion. The pre-distorted IF signal connects through a resistor buffer network that prevents loading of the combiner before it is wired to the frequency response circuitry.

*4.2.1.8 Main IF Signal Path (Part 3 of 3)*

The IF signal, at the input to the frequency-response corrector circuit, is split using L24, L25 and R89. One path is through L24, which is the main IF path through the board. The main IF is fed through a resistor network that controls the level of the IF by adjusting the resistance of R99, the output level adjust. The IF signal is then applied to a three-stage, frequency-response corrector circuit that is adjusted as needed.

The frequency-response corrector circuit operates as follows. Variable resistors R103, R106 and R274 are used to adjust the depth and gain of the notches and variable caps C71, C72 and C171 are used to adjust the frequency position of the notches. These are adjusted as needed to compensate for frequency response problems.

The frequency-response corrected IF is connected to J38 that is jumpered to J39 on the board. J38 can be used for testing or monitoring purposes of the IF signal after frequency response pre-correction.

The IF is next amplified by U13 and U14. After amplification, the IF is split with one path connected to J42C pin 1C the IF output to the LO/Upconverter Module. The other path is fed through a divider network to J35 a SMA IF Sample Jack, located on the front panel, which provides a sample of the corrected IF for test purposes.

*4.2.1.9 ALC Circuit*

The other path of the corrected IF signal at the input to the frequency response corrector circuit is used in the ALC circuit. The IF flows through L25, of the L24 L25 splitter, and connects to the op-amp U12. The IF signal is applied through a resistor divider network to transformer T5. T5 doubles the voltage swing by means of a 1:4 impedance transformation before it is connected to the ALC detector circuit, consisting of C70, CR23 and R91. The detected ALC level output is amplified by U10B and wired to U10A, pin 2, where it is summed with the power control setting, which is the output power setting that is maintained by the ALC. The output of U10A connects through SW1, if it is in the auto gain position, to the pin-diode attenuator circuit, CR1, CR2 & CR3. The high forward biases them more or less, that increases or decreases the IF level, therefore the output level, opposite the input level. When the input signal level increases, the forward bias on the pin attenuator decreases, therefore the output power will decrease, which keeps the output power the same as set by the customer.

An external power raise/lower switch can be used by connecting it to TB30, at TB30-8 power raise and TB30-9 power lower, on the rear of the exciter/amplifier chassis. The ALC voltage is set for .8 VDC at TP4 with a 0-dBm output at J42C pin 1C of the module. A sample of the ALC at J42C pin 11C, is wired to the Control Monitoring/Power Supply module where it is used on the front panel display and in the AGC circuits.

The ALC voltage, and the DC level corresponding to the IF level after signal correction, are fed to U10A, pin 2, whose output at pin 1 connects to the ALC pin-diode attenuator circuit. If there is a loss of gain somewhere in an IF circuit, the output power of the transmitter will drop. The ALC circuit senses this drop at U10A and automatically decreases the loss through the pin-diode attenuator circuit therefore

increasing its gain maintaining the same output power level.

The ALC action starts with the ALC detector level monitored at TP4. The detector output at TP4 is nominally +.8 VDC and is applied through resistor R77 to a summing point at op-amp U10A, pin 2. The current available from the ALC detector is offset, or complemented, by current taken away from the summing junction. In normal operation, U10A, pin 2, is at 0 VDC when the loop is satisfied. If the recovered or peak-detected IF signal level at IF input to this board should drop, which normally means that the output power will decrease, the null condition would no longer occur at U10A, pin 2. When the level drops, the output of U10A, pin 1, will go more positive. If SW1 is in the Automatic position, it will cause the ALC pin-diode attenuators CR1, CR2, and CR3 to have less attenuation and increase the IF level; this will compensate for the decrease in the level. If the ALC cannot increase the input level enough to satisfy the ALC loop, due to there not being enough range, an ALC fault will occur. The fault is generated because U10D, pin 12, increases above the trip point set by R84 and R83 until it conducts. This makes U10D, pin 14, high and causes the red ALC Fault LED DS2 to light.

*4.2.1.10 Fault Command*

The board also has circuitry for an external mute fault input at J42 pin 10C. This is a Mute command that protects the circuits of high-gain output amplifier devices against VSWR faults. This action needs to occur faster than just pulling the ALC reference down. Two different mechanisms are employed: one is a very fast-acting circuit to increase the attenuation of the pin-diode attenuator, CR1, CR2, and CR3, and the second is the reference voltage being pulled away from the ALC amplifier device. An external Mute is a pull-down applied to J42 pin 10C, which completes a current path from the +12 VDC line through R78 and R139, the LED DS4 (Mute indicator), and the LED section of opto-isolator U11. These actions turn on the transistor section of U11 that applies -12 VDC through CR21 to U10A pin 3, and pulls down the reference voltage. This is a fairly slow action controlled by the low-pass filter function of R81 and C61. When the transistor section of U11 is on, -12 VDC is also connected through CR22 directly to the pin-diode attenuator circuit. This establishes a very fast muting action, by reverse biasing CR3. This action occurs in the event of an external VSWR fault.

*4.2.1.11 ±12 VDC Needed to Operate the Board*

The ±12 VDC connects to the board at J42C. The +12 VDC connects to J42C pin 16C and is filtered by L30, L41, and C80 before it is applied to the rest of the board. The -12 VDC connects to J42C pin 18C and is filtered by L31 and C81 before it is applied to the rest of the board.

The +12 VDC also connects through R261 to the zener diode VR3 that connects to ground, which generates the +6.8 VDC output to the rest of the board.

The +12 VDC also connects through R265 to the diodes CR30 and CR31 provide a .9 VDC reference output voltage VREF that temperature compensates for the two diodes in each corrector stage.

## 4.3 (A5) LO/Upconverter Module (1301930; Appendix B)

This module contains the LO/Upconverter board, the UHF Generator Board, LED Display Board and channel filters. This module takes an external IF and converts it to the final RF output frequency using an internally generated local oscillator.

The local oscillator consists of a VCXO that is phase locked to an external 10 MHz reference. The 10 MHz reference and the VCO are both divided down to 5 kHz and compared by the phase lock loop circuit. Any error from this comparison is generated in the form of an error current

that is converted to a bias voltage that connects to the VCO. This voltage adjusts the output frequency of the VCO until it is on the desired frequency.

The Phase lock loop is programmed by loading in data generated by the control module. This data sets the dividers so that the 10MHz and the VCXO frequency are divided to 5kHz. These divide numbers are loaded into U6 using the clock, data and LE lines. This data is sent whenever the module is first plugged into the backplane board or when power is applied to the transmitter. This is necessary because the divide numbers are lost when power is removed from the module.

There is an alarm generated if the phase locked loop is unlocked. This alarm is displayed locally and is also sent to the control module in the transmitter to be displayed as a fault. The bias voltage to the VCO is also available to be monitored at TP1 and also can be viewed on the front panel display of the Transmitter. Typical values for this voltage are 0.1 to 0.5V. The 10 MHz reference is normally an external reference. There is also a high stability internal reference option that is available if there is a desire to operate the transmitter without an external reference. Jumper W1 determines whether an external or internal high stability reference is to be used.

The IF signal is applied at a level of −15 dBm average and is converted to the final RF channel frequency. The RF signal is applied to a filter that selects the right conversion product. Next, the signal is amplified to -7 dBm by A3 and exits the front of the module at J2. There are also a front panel samples of the RF output at J3 and the LO at J1. The RF sample level is approximately -20 dB below the RF output. The LO sample level is -7 dBm.

### *4.3.1 (A4) UHF Generator Board (1585-1265; Appendix B)*

The UHF generator board is mounted in the UHF Generator Enclosure for EMI and RFI protection. The board contains a VCXO circuit and additional circuitry to multiply the VCXO frequency by eight.

The VCXO circuit uses the crystal Y1, mounted in a crystal oven for stability, to produce an output of ≈ 67 MHz to 132 MHz, depending on the desired channel frequency. Course adjustment to the frequency of the crystal is made by C11, while fine adjustments are accomplished by the AFC voltage at J2 from (A1) the LO/Upconverter board (1302132). The VCXO output level is adjusted by C6, L2, L4 and C18. The output is split and provides an input to the x8 multiplier circuitry as well as a VHF Output sample at J1.

The x8 circuitry consists of three identical x2 broadband frequency doublers. The input signal at the fundamental frequency is fed through a 6-dB pad consisting of R21, R24, and R25 through C29 to amplifier U3. The output of the amplifier stage is directed through a bandpass filter consisting of L8 and C32, which is tuned to the fundamental frequency (67 MHz to 132 MHz). The voltage measured at TP1 is typically +.6 VDC. The first doubler stage consists of Z1 with bandpass filter L9 and C34 tuned to the second harmonic (134 MHz to 264 MHz). The harmonic is amplified by U4 and again bandpass filtered at the second harmonic by C38 and L11 (134 MHz to 264 MHz). The voltage measured at TP2 is typically +1.2 VDC. The next doubler stage consists of Z2 with bandpass filter C40 and L12 tuned to the fourth harmonic of the fundamental frequency (268 MHz to 528 MHz). The fourth harmonic is then amplified by U5 and fed through another bandpass filter tuned to the fourth harmonic consisting of L14 and C44 (268 MHz to 528 MHz). The voltage measured at TP3 is typically +2.0 VDC. The final doubler stage consists of Z3 with bandpass filter C46 and L15 tuned to the eighth harmonic of the fundamental frequency (536 MHz to 1056 MHz). The signal is amplified by U6 and U7 to a typical value of from +2 to +4 VDC as measured at TP4. The amplified eighth harmonic is

then fed to the SMA RF output jack of the board at J3. Typical output level of the signal is +16 dBm nominal. This output connects through A5 a channel filter to the LO/Upconverter Board.

The DC voltages needed to operate the UHF generator board are supplied by the LO/Upconverter Board. The +12 VDC for the board enters through jack J4-3 and is filtered by L22 and C54-C58 before being distributed to the circuits on the board.

The +9 VDC for the board enters through jack J4-1 and is distributed to the rest of the board.

### *4.3.2 (A2 and A5) UHF Filters (1007-1101; Appendix B)*

Both UHF filters are tunable two-section cavity filters that are typically tuned for a bandwidth of 6 MHz and have a loss of -1 dB through the filter.

### *4.3.3 (A1) LO/Upconverter Board (1302132; Appendix B)*

*The upconverter portion of the board*

The LO/Upconverter board provides upconversion processing by mixing the IF and LO signals in mixer Z1 to produce the desired RF frequency output. The RF output is connected through J4 to A5, an external channel filter, and applied back to the board at J6. The RF is amplified and connected to the RF output jack of the board at J43-25B.

The IF signal (-6 dBm average) enters the board at J43-2B and is applied through a matching pad and filter circuit to the mixer. The pad consists of R6, R2 and R7, which presents a relatively good source impedance. The IF is then connected through a voltage divider network consisting of R3, R4, R8 and R14. R14 is variable and adjusted to set the 0 dBm IF input level to the mixer. The IF in next filtered by L3, C84 and C83 and connected to pin 5, the I input of the mixer Z1.

The local oscillator signal (+13 dBm) from UHF Generator Board, through (A5) a UHF channel filter, connects to the board at jack J1, an SMA connector. THE LO is connected directly to pin 1, the L input of the mixer Z1.

The frequency of the LO is the sum of the IF frequency above the required digital carrier. For instance, in system M, for digital applications, the LO is the center frequency of the digital channel added to the 44-MHz IF frequency. By picking the local oscillator to be 44 MHz above the digital carrier, a conversion in frequency occurs by selecting the difference product. The difference product, the local oscillator minus the IF, will be at the desired digital carrier frequency output. There will also be other signals present at the RF output connector J3 at a lower level. These are the sum conversion product: the LO and the IF frequencies. Usually, the output product that is selected by the tuning of the external filter is the difference product: the LO minus the 44-MHz IF.

If a bad reactive load is connected to the mixer, the LO signal that is fed through it can be increased because the mixer no longer serves as a double-balanced mixer. The mixer has the inherent property of suppressing signals that may leak from one input port to any of the other ports. This property is enhanced by having inputs and outputs of the mixer at 50Ω impedance. The RF output of the mixer connects through a pad made up of R12, R15, and R17 before it is wired to the amplifier U2. The RF signal is amplified by U2, a modular amplifier, and includes within it biasing and impedance matching networks that makes U2 act as a wideband-RF amplifier device. This amplifier, in a 50Ω system, has approximately 12 dB of gain. U2 is powered from the +12 VDC line through RF decoupling components R24, C14, and L4. Inductor L4 is a broadband-RF choke and is resonance free through the UHF band. The amplified RF connects through a pad to the SMA RF output jack J4 and is cabled to (A2) an external channel filter. The reactive channel filter that is externally connected to J4 of the board does not

appear as a good 50-Ω load at all frequencies. The pad, in the output line of the board, consisting of R20, R18, and R21 buffers the bad effects of the reactive filter load and makes it appear as a 50Ω impedance.

The RF input signal from the external filter re-enters the board at J6 (-11 to -17 dBm) and is capacitively coupled to the pin-diode attenuator circuit consisting of CR2, CR3, and CR4. The pin-diode attenuator acts as a voltage-variable attenuator in which each pin diode functions as a voltage-variable resistor that is controlled by the DC bias connected to the diodes. The pin diodes, because of a large, intrinsic region, cannot rectify signals at this RF frequency; therefore, they only act as a linear voltage-variable resistor. These diodes are part of the AGC for the transmitter.

*The automatic gain control (AGC) portion of the board*

The automatic gain control (AGC) provides automatic gain control for the power amplifier module(s).

The AGC circuitry attempts to maintain the ratio between an input reference proportional to the input power and the output power of either the exciter/amplifier PA output, AGC #1, Inner Loop, or the output of external power amplifiers, AGC #2, Outer Loop, farther downstream. **NOTE:** The AGC #2 Outer Loop is not used in 5W-50W digital transmitters.

An ALC reference input is applied to the board at J43-16A, amplified by U10A, and sent to the front panel board through J5-7 where it is connected to a AGC Manual Gain pot, accessed through the front panel. A switch AUTO/MAN AGC is also located on the front panel. When switched in MAN the MAN GAIN Pot adjusts the output power level. The Gain Control voltage is reapplied to the board at J5-6. The gain control voltage is summed to the added together inner and outer loop AGC reference voltage at U10D.

The AGC output reference from the exciter/amplifier PA module, AGC #1 INNER LOOP, is applied at J43-14C and from the external PA module, AGC #2 OUTER LOOP, is applied at J43-15C.

The larger voltage of either the inner or the outer loop is used to control the AGC loop. Since the outer loop is not used in this system, the inner loop controls the AGC. R82 is adjusted so that the inner loop voltage at TP7 is larger than the voltage at TP4 by approximately .1 VDC. This ensures that the output of the exciter/amplifier is the reference used for AGC. In systems that use the outer loop, that level is adjusted to .1 VDC above the inner loops reference. This ensures that the output of the system is the reference used for AGC. If that reference drops to the point where it is smaller than the inner loop reference, the system switches over to using the inner loop reference.

The AGC reference that is being used is buffered by U10C and connected to U10D. U10D generates an output voltage that is used to bias the pin attenuators, CR2, CR3 and CR4, which sets the gain of the exciter/amplifier.

This Auto AGC circuit can be disabled by the AGC Auto/Man switch, located on the front panel, which switches the pin-attenuator bias to a variable voltage that is set by the Manual Gain Adjust.

The level-controlled RF signal, from the pin-diode attenuator circuit, is amplified by the wideband-hybrid amplifier IC U13 that is configured in the same way as U2. The RF signal is converted by T1 to a balanced, dual feed output that is applied to the push-pull Class A amplifier IC U1. Capacitors C2 and C5 provide DC blocking for the input signal to the IC. The RF outputs of the IC are applied through C3 and C4, which provide DC blocking for the output signals. The RF signals connect to combiner T2 that combines the RF back to a single-RF output at a 50Ω impedance.

The RF then enters a coupler stage, which provides a sample of the RF at J7 (–20dB), the front panel RF sample jack. The main path through coupler is to J43 pin 25B, the Upconverter RF output jack of the module (+0 to +10 dBm).

*The PLL and 10-MHz Reference section of the Board*

The PLL and 10-MHz reference portion of the board utilizes either an external 10 MHz reference or an internally generated 10 MHz as the reference for the PLL circuit that generates the AFC voltage, which controls the frequency of the VCXO on the UHF Generator Board.

The (PLL) phase lock loop circuit, provides the automatic frequency control (AFC) voltage, that connects to the VCXO, located on the UHF generator board, and maintains the accurate output frequency of the VCXO. The AFC is generated by comparing a sample of the 10-MHz reference to a sample of the VCXO frequency. The PLL uses an external 10-MHz signal as the reference, unless it is missing, then an internally generated 10-MHz signal is used. The two 10-MHz reference signals are connected to the K1 relay and the selected reference connects to the comparator synthesizer IC U9. The switching between the two references is accomplished by the K1 relay. When the relay is de-energized, it applies the external 10-MHz reference to U9. The relay will remain de-energized as long as an externally generated 10-MHz reference signal is present and the Jumper W3 on J10 is placed in the external position, between Pins 1 & 2. An alternate 10 MHz reference can be connected to J11 on the board. The jumper W3 on J10 must then be moved to pins 2 & 3, internal, to connect the alternate 10 MHz to K1. The alternate 10 MHz will then act in the circuit like the external 10 MHz.

If the external 10-MHz reference is lost, the relay will energized and the internally generated 10-MHz reference is then applied through the K1 relay pin 14 to pin 1 to the IC U9.

With the relay de-energized, the externally generated 10-MHz from jack J43 pin 22B connects through the normally closed contacts of the relay from pin 1 to pin 7 to the IC U9.

*External 10-MHz Reference Present Circuitry*

The external 10-MHz reference signal enters the board at J43 pin 22B and is isolated by L8 and connected to the External/Internal Jack J10. W3 on J10 is a manual jumper that must be connected between pins 1 & 2, External, for the external 10 MHz to connect to the rest of the circuit. The external 10 MHz is filtered by C44, R55, L9 and C46 before it split with one path connected to the K1 relay at pin 1 of the normally closed contacts. The other path takes the 10 MHz and rectifies it by CR5 and filters it before it is connected to U7A pin 2. If the sample level of the external 10 MHz is above the reference set by R46 and R48, which is connected to pin 3 of U7A, the output of U7A stays low. The low connects to the gates of Q3, Q5 and Q6, which are biased off and cause their drains to go high. The high from the drain of Q6 is wired to J43, pin 14A, for connection to a remote external 10-MHz present indicator. The high from the drain of Q5 connects to the yellow LED DS2, internal reference indictor, which will not light. This indicates that an external 10-MHz reference is present. The low from U7A also connects to the gate of Q3, biasing it off and causing its drain to go high. This high de-energizes the K1 relay and applies the external 10-MHz reference signal to pin 6 on U9 for use as the reference in the PLL circuits.

*Internal 10-MHz Reference Circuitry*

The internally generated 10-MHz reference signal connects from U6, the 10-MHz oscillator IC, to pin 14, the Normally Open contacts of relay K1.

With no external 10-MHz reference input, the level connected to U7A Pin 2 will be low. This will be less than the reference set by R46 and R48, which is connected to pin 3 of U7A, that causes the output of U7A to go high. The high connects to the gates of Q3, Q5 and Q6, which are biased on and causes their drains to go low. The low from the drain of Q6 is wired to J43, pin 14A, for connection to a remote external 10-MHz present indicator. The low from the drain of Q5 connects to the yellow LED DS2, internal reference indictor, which will light. This indicates that an external 10-MHz reference is not present and that the internal 10-MHz is being used as the reference. The high from U7A also connects to the gate of Q3, biasing it on and causing its drain to go low. This low energizes the K1 relay and applies the internal 10-MHz reference signal through K1 pin 14 to pin 7 to pin 6 on U9 for use as the reference in the PLL circuits.

*Selected 10-MHz Reference Samples*

A sample of the selected 10-MHz is split off the main path through L13 and R95 using L14 and C74 and C73. The sample path connects to another splitter circuit consisting of L2, R94, L11, C71 and C70. One output of the splitter connects to J43 pin 28B that is used by the external digital modulator tray. The other output of the splitter connects to J43 pin 31B that is used by the external analog modulator tray.

*Comparator Phase Lock Loop Circuit*

The selected 10-MHz reference connects to pin 6, Oscillator In, of the IC U9. The LO generated by the VCXO located on the UHF Generator Board connects to J1 on the LO/Upconverter Board. A sample of the LO is divided off the main line by R105, R106 and R107. The LO sample connects to pin 4, F In, of U9.

The U9 IC takes the 10 MHz reference and divides it down to 5 kHz. It also takes the LO sample input and divides it down to 50 kHz. The two 5 kHz divided down signals are compared inside of U9 and any differences are connected to U9 pin 16. The output of U9 at pin 16 are 5 kHz pulses whose pulse width varies as any differences between the 10-MHz and VCXO frequencies are detected. These pulses are changed to a DC voltage level by the capacitor-resistor filter network, C32, C36, C42, C38 and R49. The AFC voltage is then connected to the + input of U4B that amplifies it and connects it to jack J9. W2 on J9 must be in the operate position, between pins 1 and 2, for the PLL circuit to operate. With jumper W2 between pins 2 and 3 on J6, set up, the AFC bias is set by R43. **NOTE:** With the VCXO, located on the UHF Generator Board, set on frequency, the voltage as measured at TP2 should be –2 VDC.

The AFC output of J9 is split with one path connected to J43 pin 13A. The other path is amplified by U7B and connected to J12, VCXO AFC Output, on the board that connects to the VCXO on the UHF generator board. The PLL circuit, when locked, will maintain the very accurate VCXO output frequency because any change in frequency will be corrected by the AFC error voltage.

*Lock Detector Circuit*

IC chip U9 contains an internal lock detector that indicates the status of the PLL circuit. When U9 is in a locked state, pin 12 goes high; the high is applied to Q1, which is biased off. With Q1 off, pin 3 goes low and is connected to DS1, the Red Unlock LED, which does not lit. Q1 pin 3 low also connects to Q2 that is biased off. The drain of Q2, a high, is wired to J43 pin 15A, the PLL Lock Indicator output of the board.

If the 5-kHz from the 10-MHz reference and the 5-kHz from the VCXO become unlocked, out of the capture range of the PLL, pin 12 of U9 goes to a logic low that connects to the base of Q1. This biases On Q1 causing pin 3 to go high. The high connects to DS1, the red Unlock LED, which lights, and to Q2, which is biased on. When Q2 is biased on, it connects a low to

jack J43 pin 15A, the PLL Lock Indicator output of the board.

*Voltage Requirements*

The board is powered by ±12 VDC that is produced by an external power supply. +12 VDC enters the board through J43 pins 18A, B & C, and is filtered and isolated by L5, L6 and the shunt capacitor C24. The +12 VDC is then applied to the rest of the board and to J14 pin 3 for use by the UHF Generator Board.

One connection of the +12 VDC is to IC U12. U12 and associated circuitry produce a +9 VDC that connects to J14 pin 1 for use by the UHF Generator Board.

Another connection of the +12 VDC is to a +5 VDC regulator. The +12 VDC connects to diodes CR6 and CR7 that along with the pi type filter consisting of C56, L10, C54 and C55 removes any noise from the +12 VDC before it connects to the +5 VDC regulator IC U8. The output of the IC U8, +5 VDC, connects to the rest of the board.

The -12 VDC enters the board through J43 pins 19A, B & C and is filtered and isolated by L7 and the shunt capacitor C28. The -12 VDC is then applied to the rest of the board and to J14 pin 5 for use by the UHF Generator Board.

## 4.4 (A4) Control Monitoring/Power Supply Module (110 VAC, 1301936 OR 220 VAC, 1303229;Appendix B)

The Control Monitoring/Power Supply Module Assembly contains (A1) a Power Protection Board (1302837), (A2) a 600 Watt Switching Power Supply, (A3) a Control Board (1302021), (A4) a Switch Board (1527-1406) and (A5) a LCD Display.

*AC Input to Pioneer Exciter/Amplifier Chassis Assembly*

The AC input to the Pioneer Exciter/Amplifier Chassis Assembly is connected from J1, part of a fused entry module, located on the rear of the chassis assembly to J50 on the Control Monitoring/Power Supply Module. There are two possible modules that can be part of your system, 1301936 for 110 VAC or 1303229 for 220 VAC operation. J50-10 is line #1 input, J50-8 is earth ground and J50-9 is line #2 input. The input AC connects to J1 on the Power Protection Board where it is fuse protected and connected back to J50, at J50-11 AC Line #1 and J50-12 AC Line #2, for distribution to the cooling Fan.

### *4.4.1 (A1) Power Protection Board (1302837; Appendix B)*

The input AC connects through J1 to two 10 Amp AC fuses F1 and F2. The AC line #1 input connects from J1-1 to the F1 fuse. The AC line #1 input after the F1 fuse is split with one line connected back to Jack J1 Pin 4, which becomes the AC Line #1 to the Fan. The other line of the split connects to J4. The AC line #2 input connects from J1-3 to the F2 fuse. The AC line #2 input after the F2 fuse is split with one line connected back to Jack J1 at Pin 5, which becomes the AC Line #2 to the Fan. The other line of the split connects to J2. J1-2 is the earth ground input for the AC and connects to J3.

Three 150-VAC, for 115 VAC input, or three 275-VAC, for 230 VAC input, MOVs are connected to the input AC for protection. One connects from each AC line to ground and one connects across the two lines. VR1 connects from J4 to J2, VR2 connects from J4 to J3 and VR3 connects from J2 to J3.

*+12 VDC Circuits*

+12 VDC from the Switching Power Supply Assembly connects to J6 on the board. The +12 VDC is divided into four separate circuits each with a 3 amp self resetting fuse, PS3, PS4, PS5 and PS6.

The polyswitch resettable fuses may open on a current as low as 2.43 Amps at 50°C, 3 Amps at 25°C or 3.3 Amps at 0°C. They definitely will open when the current is 4.86 Amps at 50°C, 6 Amps at 25°C or 6.6 Amps at 0°C.

PS3 protects the +12 VDC 2 Amp circuits for the System Controller, the Amplifier Controller and the Spare Slot through J62 pins 7, 8, 9 and 10. If this circuit is operational, the Green LED DS3, mounted on the board, will be lit.

PS4 protects the +12 VDC 2 Amp circuits for the Modulator and the IF Processor through J62 pins 13, 14, 15 and 16. If this circuit is operational, the Green LED DS4, mounted on the board, will be lit

PS5 protects the +12 VDC 2 Amp circuits for the Upconverter through J62 pins 17, 18, 19 and 20. If this circuit is operational, the Green LED DS5, mounted on the board, will be lit

PS6 protects the +12 VDC 2 Amp circuits for the Remote through J63 pins 17, 18, 19 and 20. If this circuit is operational, the Green LED DS6, mounted on the board, will be lit

*-12 VDC Circuits*

-12 VDC from the Switching Power Supply Assembly connects to J5 on the board. The -12 VDC is divided into two separate circuits each with a 3 amp self resetting fuse, PS1 and PS2.

PS1 protects the -12 VDC 2 Amp circuits for the System through J63 pins 1, 2, 3 and 4. If this circuit is operational, the Green LED DS1, mounted on the board, will be lit

PS2 protects the -12 VDC 2 Amp circuits for the Remote through J62 pins 1, 2, 3 and 4. If this circuit is operational, the Green LED DS2, mounted on the board, will be lit

The connections from J62 and J63 of the Power Protection Board are wired to J62 and J63 on the Control Board.

### *4.4.2 (A3) Control Board (1302021; Appendix B)*

In this transmitter, control monitoring functions and front panel operator interfaces are found on the Control Board. Front panel operator interfaces are brought to the control board using a 26 position conductor ribbon cable that plugs into J60. The control board controls and monitors the Power Supply and Power Amplifier module through a 16 position connector J61 and two 20 position connectors J62 & J63.

*Schematic Page 1*

U1 is an 8 bit RISC microcontroller that is in circuit programmed or programmed using the serial programming port J4 on the board. When the microcontroller, U1, is held in reset, low on pin 20, by either the programming port or the external watchdog IC (U2), a FET Q1 inverts the reset signal to a high that connects to the control lines of U5, an analog switch. The closed contacts of U5 connects the serial programming lines from J4 to U1. LED DS10 will be lit when programming port J4 is used.

U2 is a watchdog IC used to hold the microcontroller in reset, if the supply voltage is less the 4.21 VDC; (1.25 VDC < Pin 4 (IN) < Pin 2 (Vcc). The watchdog momentarily resets the microcontroller, if Pin 6 (ST) is not clocked every second. A manual reset switch S1 is provided but should not be needed.

Diodes DS1 through DS8 are used for display of auto test results. A test board is used to execute self test routines. When the test board is installed, Auto_Test_1 is held low and Auto_Test_2 is allowed to float at 5 VDC. This is the signal to start the auto test routines.

U3 and U4 are used to selectively enable various input and output ICs found on pages 2 & 3 of the schematic.

U1 has two serial ports available. In this application, one port is used to communicate with transmitter system components where U1 is the master of a RS-485 serial bus. The other serial port is used to provide serial data I/O where U1 is not the master of the data port. A dual RS-232 port driver IC and a RS-485 Port driver is also in the second serial data I/O system. The serial ports are wired such that serial data input can come through one of the three serial port channels. Data output is sent out through each of the three serial port channels.

Switch SW1, transmitter operation select, is used to select either transmitter operation or exciter/driver operation. When the contacts of SW1 are closed, transmitter operation is selected and the power monitoring lines of the transmitter's power amplifier are routed to the system power monitoring lines.

*Schematic Page 2*

U9 is a non-inverting transceiver IC that provides 2 way asynchronous communication between data busses. . The IC is used as an input buffer to allow the microcontroller to monitor various digital input values.

Digital output latch circuits are used to control system devices. Remote output circuits are implemented using open drain FETs, Q13, Q14, Q16, and Q17, with greater than 60 Volt drain to source voltage ratings.

Remote digital inputs are diode protected, using CR6, CR7, CR8 and CR9 with a 1 kΩ pull-up resistor, to +5 VDC. If the remote input voltage is greater than about 2 Volts or floating, the FET is turned on and a logic low is applied to the digital input buffer, U9. If the remote input voltage is less than the turn on threshold of the FET (about 2 VDC), a logic high is applied to the digital input buffer, U9.

Four of the circuits on page two of the schematic, which include Q2, Q9, Q19 and Q21, are auxiliary I/O connections wired for future use. They are wired similar to the remote digital inputs but include a FET, Q5, Q12, Q20 and Q22, for digital output operations. To operate these signals as inputs, the associated output FET must be turned off. The FETs are controlled by U10 and U12, analog input multiplexer ICs.

*Schematic Page 3*

U13, U14, U15, U16, U17 and U18 are 3 state non-inverting transceiver ICs that provide 2 way asynchronous communication between data busses. The ICs are used as input buffers to allow the microcontroller to monitor various digital input values. The digital inputs to the ICs utilize a 10 kΩ pull-up resistor. The buffer IC, U18, used for data transfer to the display is wired for read and write control.

*Schematic Page 4*

U19 and U20 are digitally controlled analog switches that provide samples back to the microprocessor. Each analog input is expected to be between 0 and 5 VDC. If a signal exceeds 5.1 VDC, a 5.1 Volt zener diode clamps the signals voltage, to prevent damage to the IC. Most signals are calibrated at their source, however two dual serial potentiometers ICs are used to calibrate four signals, System Visual/Average Power, System Aural Power, System Reflected Power and the Spare AIN 1. For these four circuits, the input value is divided in half before it is applied to an op-amp. The serial potentiometer is used to adjust the output signal level to between 80 and 120% of the input signal level. Serial data, serial clock and serial pot enables are supplied by the microprocessor to the dual serial potentiometer ICs. J62 and J63 are two 20 position connectors that provide the +12 VDC and –12 VDC power through the

Power Protection Board. The ±12 VDC generated by the switching power supply connects to J62 and J63 after being fuse protected on the Power Protection Board.

*Schematic Page 5*

There are three dual element, red/green, common cathode LED indicators mounted on the front panel of the sled assembly; DC OK, Operate and Fault.

There are three, the fourth is a spare, identical circuits that drive the front panel mounted LED indicators. The levels on the 1, 2, 3 and 4 LED Control Lines, for both the red and green LEDs, are generated by the IC U11 as controlled by the DATABUS from the microprocessor U1.

Each LED controller circuit consists of an N-Channel MOSFET w/internal diode that controls the base of an N-P-N transistor in an emitter follower configuration. The emitter of the transistor connects the LED.

With the LED control line LOW, the MOSFET is Off, which causes the base of the transistor to increase towards +12 VDC, forward biasing the transistor. With the transistor forward biased, current will flow from ground through the LED, the transistor and the current limiting resistors in the collector to the +12 VDC source. The effected LED will light.

With the LED control line HIGH, the MOSFET is On, which causes the base of the transistor go toward ground potential, reverse biasing the transistor. With the transistor reverse biased, no current through the transistor and LED, therefore the effected LED will not light.

A third color, amber, can also be generated by having both transistors conducting, both control lines LOW. The amber color is produced because the current applied to the green element is slightly greater than the red element. This occurs because the current limiting resistors have a smaller ohm value in the green circuit.

There are four voltage regulators, three for +5 VDC and one for +7 VDC, which are used to power the Control Board. +12 VDC is applied to U25 the +7 VDC regulator that produces the +7V, which is applied to the LEDs mounted on the board. The +7V is also connected to the input of U26 a precision +5.0 Volt regulator. The +5.0Vdc regulator output is used to power the analog circuits and as the microcontroller analog reference voltage. Another two +5 Volt regulator circuits U27, +5V, and U8, +5 Vserial, are used for most other board circuits.

### *4.4.3 (A4) Switch Board (1527-1406; Appendix B)*

The switch board provides five front-panel momentary contact switches for user control and interface with the front-panel LCD menu selections. The switches, SW1 to SW5, complete the circuit through connector J1 to connector J2 that connects to J1 on (A5) the 20 Character by 4 line LCD Display. J1 on the switch board is also cabled to the Control Board. When a switch is closed, it connects a logic low to the control board that supplies the information from the selected source to the display. By pushing the button again, a different source is selected. This occurs for each push button. Refer to Chapter 3 Section 3.5.4, for more information on the Display Menu Screens.

### *4.4.4 (A2) Switching Power Supply Assembly*

The power supply module contains a switching power supply, an eight position terminal block for distributing the DC voltages, a three position terminal block to which the AC Input connects, Jacks J1, V1 and V2. Jack J1 connects to the Control Board and supplies DC OK, at J1-4 & 3, and AC OK, at J1-2 & 1, status to the control board. A Power Supply enable connects from the control board to the

power supply at V1-6 & 7. The power supply is configured for three output voltages +12V, -12V, at the 8 position terminal block, and a main output power of +32 VDC at J50 pin A (+) and J50 pin B (Rtn). The power supply is power factor corrected to .98 for optimum efficiency and decrease in energy consumption. For safety purposes all outputs are over voltage and over current protected. This supply accepts input voltages from 85 to 264 volts AC, but the power entry module, for the exciter/amplifier chassis, must be switched to the proper input voltage setting, for the transmitter to operate.

### 4.5 (A4) Power Amplifier Module Assembly (1301923; Appendix B)

**NOTE:** Used in 10W-100W Transmitters.

The Power Amplifier Module Assembly contains (A1) a 1 Watt UHF Amplifier Module Assembly (1302891), (A2) a 40 Watt UHF Module Assembly (1206693), (A3) UHF RF Module Pallet Assembly (1300116), (A4) a Coupler Board Assembly (11301949), (A5) an Amplifier Control Board (1301962) and (A6) a Temperature Sensor IC.

The RF from the Upconverter Module Assembly connects from the Upconverter RF Output BNC Jack J23, through a cable, to the PA RF Input BNC Jack J24, located on the rear of the exciter/amplifier chassis assembly.

#### *4.5.1 (A1) 1-Watt UHF Module Assembly (1302891; Appendix B)*

The 1-watt UHF module assembly provides radio frequency interference (RFI) and electromagnetic interference (EMI) protection, as well as the heatsink, for the 1-watt UHF amplifier board (1302762) that is mounted inside the assembly. The assembly has approximately 17 dB of gain.

The RF input to the assembly connects to SMA Jack J3. The amplified RF output of the assembly is at the SMA Jack J4. Typically, with an input signal of +4 dBm at J1 of the assembly, an output of +21 dBm can be expected at J2.

The +12-VDC bias voltage connects through J5, a RF-bypassed, feed-through capacitor, to the amplifier board. The -12-VDC bias voltage connects through J6, a RF-bypassed, feed-through capacitor, to the amplifier board. E1 on the assembly connects to Chassis ground.

#### *4.5.2 (A1-A1) 1-Watt UHF Amplifier Board (1302761; Appendix B)*

The 1-watt UHF amplifier board is mounted in the 1-watt UHF amplifier assembly (1302891) and provides approximately +17 dB of gain.

The UHF signal enters the board at J3, a SMA connector, and is applied to U3 an IC hybrid coupler assembly that splits the input signal into two equal parts. The two amplifier paths are identical using Q4 and Q5, 1-Watt HFETs as the amplifier devices. Each HFET has approximately 14 dB of gain.

The drain voltage needed to operate each HFET is obtained from the +12 VDC line that connects to the board at J5 and is regulated down to +8.25 volts by U4. The gate negative bias voltage is obtained from the -12 VDC line that connects to the board at J6.

The amplified outputs of the HFETs are applied to U2 an IC hybrid coupler assembly that combines the amplified signals into a single output that connects to J4 of the board.

#### *4.5.3 (A4-A1) 40 Watt UHF Amplifier Assembly (1206693; Appendix B)*

The output of the UHF filter is connected to the input J1 of (A2) the 40 Watt UHF amplifier assembly (Figure 4-1). The assembly is made up of a (51-5378-308-00) module, which operates class AB and is a highly linear broadband amplifier for the frequency range of 470 to 860 MHz. It can

deliver an output power of 40 watts (CW) with approximately 14 dB of gain.

The amplification circuit consists of LDMOS transistors V804 and V805 connected in parallel and operating in class AB. The paralleling network is achieved with the aid of 3 dB couplers Z802 and Z803. A further 3 dB coupler Z801, in conjunction with capacitors C800 and C819, serves as a phase shifter. Phase alignment (for the complete amplifier), as well as quiescent current settings are achieved by means of potentiometers R807 and R808. The settings are factory implemented and should not be altered.

PIN diodes V810 & V811 form a variable-damping circuit that is used to adjust the amplification of the 40-watt module. The adjustment is performed with the Gain potentiometer R838. A readjustment of the amplification may be required, after repair work, to ensure that the PAs in multiple PA transmitters deliver the same output power

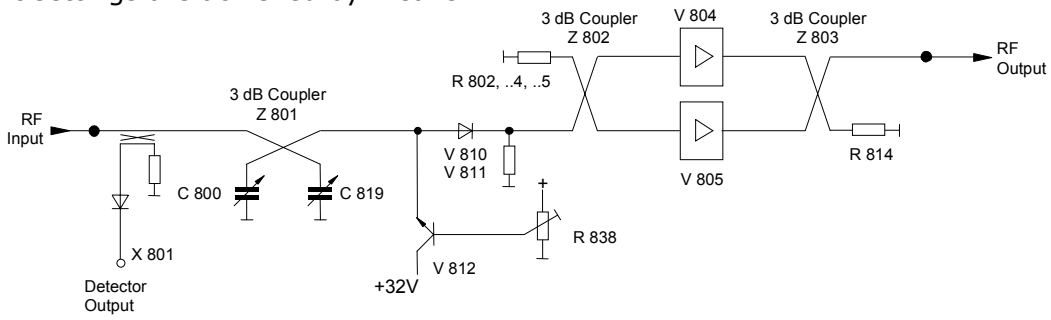


*Figure 4-1: 40 Watt UHF Amplifier Module*

### *4.5.4 (A3) UHF Module Assembly, RF Module Pallet, Philips (1300116; Appendix B)*

The UHF Module Assembly, 250-watt module (Figure 4-2) is a broadband amplifier for the frequency range 470 to 860 MHz. The amplifier is capable of delivering an output power of 70 $W_{rms}$. The amplification is approximately 13 dB.

The amplification circuit consists of the parallel connected push-pull amplifier blocks V1 and V2 operating in class AB. In order to match the transistor impedance to the characteristic impedance of the input and output sides, matching networks are placed ahead and behind the amplifier blocks. Transformers Z3 to Z6 serve to balance the input and output signals. The paralleling circuit is achieved with the aid of 3-dB couplers Z1 and Z2.

The working point setting is factory implemented by means of potentiometers R9, R11, and R12 and should not be altered.

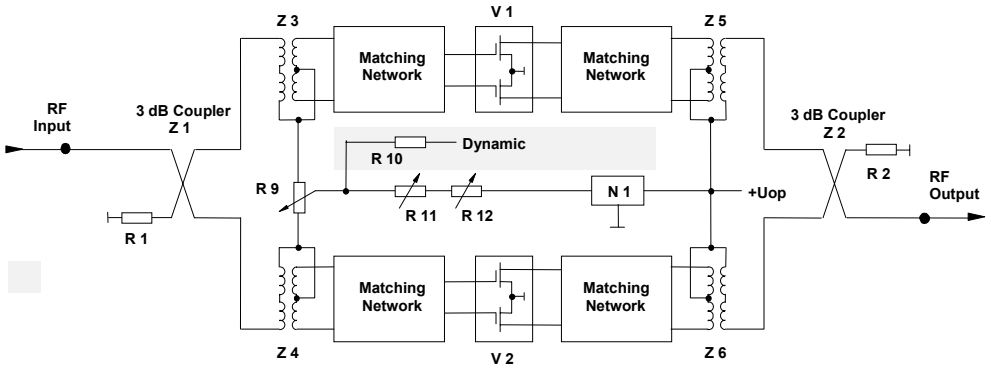


*Figure 4-2. UHF Amplifier Module, 250 Watts*

### *4.5.5 (A4) Coupler Board Assembly (1301949; Appendix B)*

The UHF coupler board assembly provides a forward and reflected power samples of the output to (A5) the amplifier control board where it connects to the input of the overdrive-protection circuit.

The RF input to the UHF coupler assembly, from the 250 Watt UHF amplifier module, connects to SMA jack J1. The RF is connected by a stripline track to the SMA type connector RF Output jack J2. A hybrid-coupler circuit picks off a power sample that is connected to SMA type connector jack J3 as the forward power sample. Another power sample is taken from the coupler circuit that is connected to SMA type connector jack J6 as the reflected power sample. Two 50Ω terminations, used as dissipation loads, connect to the reject and reflected ports, J5 and J4, of the coupler.

### *4.5.6 (A5) Amplifier Control Board (1301962; Appendix B)*

The amplifier control board provides LED fault and enable indications on the front panel of the module and also performs the following functions: overdrive cutback, when the drive level reaches the amount needed to attain 110% output power; and overtemperature, VSWR, and overdrive faults. The board also provides connections to the LCD Display for monitoring the % Reflected Power, % Output Power, and the power supply voltage.

Page 1

U4, located upper center of page, is an in circuit microcontroller. The controller is operated at the frequency of 3.6864 MHz using crystal Y1. Programming of this device is performed through the serial programming port J2. U4 selects the desired analog channel of U1 through the settings of PA0-PA3. The outputs of Port A must be set and not changed during an analog input read of channels PA5-PA7. PA4 of U4 is a processor operating LED that monitors the +/-12 VDC. PA5 is used to monitor the +12VDC supply to the board. PA6 is the selected channel of analog switch U1. PA7 is connected to a via, V10, for future access.

U6 is a serial to RS-485 driver IC. U7 is a watchdog IC used to hold the microprocessor in reset, if the supply voltage is less than 4.21 VDC. U7 momentarily resets the microcontroller if Pin 6 (!ST) is not clocked every second. A manual reset switch is provided but should not be needed.

Upper left corner U3 is used to determine where the amplifier control board is located. The eight inputs come from the main amp connector and are used to set the SCADA address of the controller. Pull-up resistors set a default condition of logic high.

U5 below U3 is used for getting digital input information of the board. Page two has several monitoring circuits that provide information on the amplifier's status. Many of these circuits automatically shut down the amplifier if a specific fault occurs.

U8 below U5 is used to control four board mounted status LEDs. A FET is turned On to shunt current away from the LED to turn it Off. U9 below U8 is used to enable different features within the software. Actual use is to be determined.

Page 2

In the lower right corner are voltage regulator circuits. U22 should allow for 0.14 amps of power using its 92 C/W rating if Ta = 60°C max and Tj = 125°C max 0.26 amps can be obtained from U22 if the mounting pad is 0.5 square inches. The controller will not need this much current.

U23 and U24 are low drop out +5 VDC, voltage regulators with a tolerance greater

than or equal to 1%. 100mA of current is available from each device but again the controller will not need this much current.

In the upper left section are circuits with U12 and U13. U12 is used to generate a regulated voltage that is about 5 volts less than the +32 VDC supply, approximately +26.25 VDC. When the +32 VDC supply is enabled, the circuitry around U13B is used to provide gate voltage to Q10 that is 5 volts greater than the source pin of this FET. The gate of Q10 can be turned Off by any one of a few different circuits.

U10A is used to turn Off the gate of Q10 in the event of high current in amplifier #1. At 0.886 VDC the current to amplifier #1 should be greater than 5 Amps. U11B is used to turn off the Q10 FET, if high current is detected in amplifier #2. U11A is used to turn off the Q10 FET, if high current is detected in amplifier #3. With 2.257 VDC at Pin 5 of U11B or Pin 3 of U11A, the voltage output of current sense amplifier U17 or U18 at high current shut down should be greater than 15 Amps.

U14B is used to turn Off the gate of Q10 in the event of high power supply voltage, approximately +35.4 VDC. U14A is used to keep the FET disabled in the event of low power supply voltage, approximately +25.4 VDC.

*Current monitoring sections of the board.*

The ICs U16, U17 and U18 along with associated components set up the current monitoring sections of the board. R67, R68 and R69 are 0.01Ω/5W 1% through hole resistor is used for monitoring the current through several sections of the amplifier. The voltage developed across these resistors are amplified for current monitoring by U16, U17 or U18. The LT1787HVCS8 precision high side current sense IC amplifier accepts a maximum voltage of 60 VDC. The 43.2 kΩ resistor from pin 5 to ground sets the gain of the amplifier to about 17.28. This value is not set with much accuracy since the manufacturer internally matches the resistors of this part but their actual resistance value is not closely defined. A trimming resistor is suggested to give a temperature stability of –200 ppm/C, but instead the microcontroller will determine the exact gain of the circuit and use a correction factor for measurements. Circuit loading components are located in the lower portion of each current monitoring circuit. These components allow for short duration high current loading of the supply. By measuring the current through the sense resistor with and without the additional four 30.1 Ω 1% resistors. For very short duration pulses, a 1206 resistor can handle up to 60 watts. The processor requires 226 uSec per conversion. A supply voltage of +32 VDC will pass 1.06 amps + 1% through the load resistors.

A6 is a temperature sensor thermistor that is used to monitor the temperature of the module's heat sink. It connects to J6 pins 1 & 2 on the board wand is wired to the comparator IC U10B. If the temperature increases above 75°C the output will go Low that is used as a temperature fault output, which generates a Fault alert at U15A and disables Amplifier #1.

*Aural, Visual/Average and Reflected power detector sections of the board.*

Page 3

A Forward Power Sample enters the board at SMA Jack J3 and is split. One part connects to J4 on the board that is cabled to J1, the SMA Forward Power Sample Jack, located on the front panel of the assembly. The other part of the split forward power sample is detected by CR17 and the DC level amplified by U25A. The output of U25A at pin 1 is split with one part connected to the Aural Power sample, which is not used in this digital transmitter. The other split output connects to U265A that is part of the Forward Average Power

circuit. The detected level is connected to L4 that is part of an intercarrier notch filter circuit that is tuned to eliminate the 4.5 MHz aural intercarrier, if present. The Average power sample is amplified by U26D and connected through the average calibration pot R166 to U26C. The output of U26C is connected to the comparator IC U26B that has Aural Null and Offset Null, if present in the system, connected to the other input. The output Average Forward power level connects to J9 pin 2 of the board.

A Reflected Power Sample enters the board at SMA Jack J5 and is detected by CR20 and the DC level amplified by U28B. The output of U28B at pin 7 is connected through the reflected calibration pot R163 to U28C. The output is split with one part connected to J9 pin 5, the Reflected Power Output level of the board. The other part of the split from U28C connects to the comparator IC U28D that has a reference level connected to the other input. If the reflected level increases above the reference level a low output is produced and connected to the Reflected Power Shutdown circuit at CR28. The low shuts off Q14 causing pin 3 to go high that is connected to the inverter U15C. The output of U15C goes low producing a Reflected Power Fault that is connected to an output of the board, the Fault Alert circuit and also shuts down Amplifier #1.

Gain of the power measurements is completed through software. Only the Aural Null and Offset Null need to be done through front panel pots.

This completes the description of the Power Amplifier Module Assembly that is used with 10W to 100 W transmitters.

### *4.5.7 (A9) Bandpass and (A10) Trap Filter*

The RF Output of the Tray is connected to (A9) the Bandpass Filter and then to (A10) the UHF Trap Filter Assembly. Both filters are tuned to provide high out of band rejection of unwanted products. The filtered RF Output at the "N" connector jack (J2) of the Trap Filter is cabled to the Antenna for your System.

## 4.6 (A4) Driver Amplifier Module Assembly (1302846; Appendix B)

**NOTE:** Used with high power transmitters with external PA assemblies.

The Power Amplifier Module Assembly contains (A1) a 1 Watt UHF Amplifier Module Assembly (1302891), (A2) a 40 Watt UHF Module Assembly (1206693), (A4) a Coupler Board Assembly (11301949), (A5) an Amplifier Control Board (1301962) and (A6) a Temperature Sensor IC.

The RF from the Upconverter Module Assembly connects from the Upconverter RF Output BNC Jack J23, through a cable, to the PA RF Input BNC Jack J24, located on the rear of the exciter/amplifier chassis assembly.

### *4.6.1 (A1) 1-Watt UHF Module Assembly (1302891; Appendix B)*

The 1-watt UHF module assembly provides radio frequency interference (RFI) and electromagnetic interference (EMI) protection, as well as the heatsink, for the 1-watt UHF amplifier board (1302762) that is mounted inside the assembly. The assembly has approximately 17 dB of gain.

The RF input to the assembly connects to SMA Jack J3. The amplified RF output of the assembly is at the SMA Jack J4. Typically, with an input signal of +4 dBm at J1 of the assembly, an output of +21 dBm can be expected at J2.

The +12-VDC bias voltage connects through J5, a RF-bypassed, feed-through capacitor, to the amplifier board. The -12-VDC bias voltage connects through J6, a RF-bypassed, feed-through capacitor, to the amplifier board. E1 on the assembly connects to Chassis ground.

### *4.6.2 (A1-A1) 1-Watt UHF Amplifier Board (1302761; Appendix B)*

The 1-watt UHF amplifier board is mounted in the 1-watt UHF amplifier assembly (1302891) and provides approximately +17 dB of gain.

The UHF signal enters the board at J3, a SMA connector, and is applied to U3 an IC hybrid coupler assembly that splits the input signal into two equal parts. The two amplifier paths are identical using Q4 and Q5, 1-Watt HFETs as the amplifier devices. Each HFET has approximately 14 dB of gain.

The drain voltage needed to operate each HFET is obtained from the +12 VDC line that connects to the board at J5 and is regulated down to +8.25 volts by U4. The gate negative bias voltage is obtained from the -12 VDC line that connects to the board at J6.

The amplified outputs of the HFETs are applied to U2 an IC hybrid coupler assembly that combines the amplified signals into a single output that connects to J4 of the board.

### *4.6.3 (A4-A1) 40 Watt UHF Amplifier Assembly (1206693; Appendix B)*

The output of the UHF filter is connected to the input J1 of (A2) the 40 Watt UHF amplifier assembly (Figure 4-1). The assembly is made up of a (51-5378-308-00) module, which operates class AB and is a highly linear broadband amplifier for the frequency range of 470 to 860 MHz. It can deliver an output power of 40 watts (CW) with approximately 14 dB of gain. It is set as needed to provide the drive level to the external PA Assemblies.

The amplification circuit consists of LDMOS transistors V804 and V805 connected in parallel and operating in class AB. The paralleling network is achieved with the aid of 3 dB couplers Z802 and Z803. A further 3 dB coupler Z801, in conjunction with capacitors C800 and C819, serves as a phase shifter. Phase alignment (for the complete amplifier), as well as quiescent current settings are achieved by means of potentiometers R807 and R808. The settings are factory implemented and should not be altered.

PIN diodes V810 & V811 form a variable-damping circuit that is used to adjust the amplification of the 40-watt module. The adjustment is performed with the Gain potentiometer R838. A readjustment of the amplification may be required, after repair work, to ensure that the PAs in multiple PA transmitters deliver the same output power.

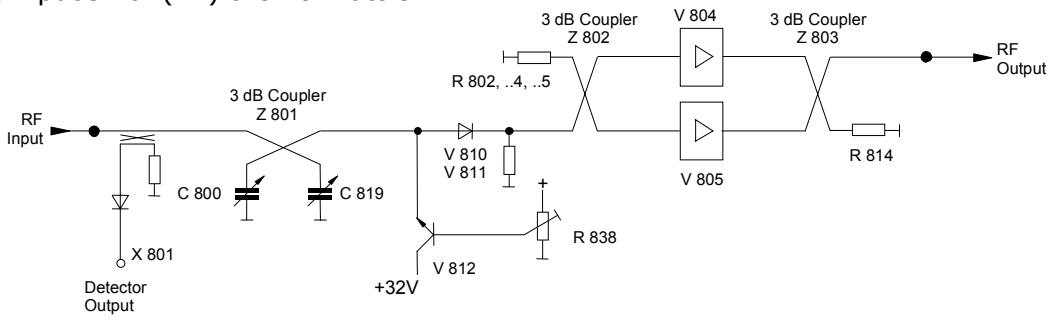


*Figure 4-3: 40 Watt UHF Amplifier Module*

### *4.6.4 (A4) Coupler Board Assembly (1301949; Appendix B)*

The UHF coupler board assembly provides a forward and reflected power samples of the output to (A5) the amplifier control

board where it connects to the input of the overdrive-protection circuit.

The RF input to the UHF coupler assembly, from the 40 Watt UHF amplifier module, connects to SMA jack J1. The RF is connected by a stripline track to the SMA type connector RF Output jack J2. A hybrid-coupler circuit picks off a power sample that is connected to SMA type connector jack J3 as the forward power sample. Another power sample is taken from the coupler circuit that is connected to SMA type connector jack J6 as the reflected power sample. Two 50Ω terminations, used as dissipation loads, connect to the reject and reflected ports, J5 and J4, of the coupler.

### *4.6.5 (A5) Amplifier Control Board (1301962; Appendix B)*

The amplifier control board provides LED fault and enable indications on the front panel of the module and also performs the following functions: overdrive cutback, when the drive level reaches the amount needed to attain 110% output power; and overtemperature, VSWR, and overdrive faults. The board also provides connections to the LCD Display for monitoring the % Reflected Power, % Output Power, and the power supply voltage.

Page 1

U4, located upper center of page, is an in circuit microcontroller. The controller is operated at the frequency of 3.6864 MHz using crystal Y1. Programming of this device is performed through the serial programming port J2. U4 selects the desired analog channel of U1 through the settings of PA0-PA3. The outputs of Port A must be set and not changed during an analog input read of channels PA5-PA7. PA4 of U4 is a processor operating LED that monitors the +/-12 VDC. PA5 is used to monitor the +12VDC supply to the board. PA6 is the selected channel of analog switch U1. PA7 is connected to a via, V10, for future access.

U6 is a serial to RS-485 driver IC. U7 is a watchdog IC used to hold the microprocessor in reset, if the supply voltage is less than 4.21 VDC. U7 momentarily resets the microcontroller if Pin 6 (!ST) is not clocked every second. A manual reset switch is provided but should not be needed.

Upper left corner U3 is used to determine where the amplifier control board is located. The eight inputs come from the main amp connector and are used to set the SCADA address of the controller. Pull-up resistors set a default condition of logic high.

U5 below U3 is used for getting digital input information of the board. Page two has several monitoring circuits that provide information on the amplifier's status. Many of these circuits automatically shut down the amplifier if a specific fault occurs.

U8 below U5 is used to control four board mounted status LEDs. A FET is turned On to shunt current away from the LED to turn it Off. U9 below U8 is used to enable different features within the software. Actual use is to be determined.

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In the lower right corner are voltage regulator circuits. U22 should allow for 0.14 amps of power using its 92 C/W rating if Ta = 60°C max and Tj = 125°C max 0.26 amps can be obtained from U22 if the mounting pad is 0.5 square inches. The controller will not need this much current.

U23 and U24 are low drop out +5 VDC, voltage regulators with a tolerance greater than or equal to 1%. 100mA of current is available from each device but again the controller will not need this much current.

In the upper left section are circuits with U12 and U13. U12 is used to generate a

regulated voltage that is about 5 volts less than the +32 VDC supply, approximately +26.25 VDC. When the +32 VDC supply is enabled, the circuitry around U13B is used to provide gate voltage to Q10 that is 5 volts greater than the source pin of this FET. The gate of Q10 can be turned Off by any one of a few different circuits.

U10A is used to turn Off the gate of Q10 in the event of high current in amplifier #1. At 0.886 VDC the current to amplifier #1 should be greater than 5 Amps. U11B is used to turn off the Q10 FET, if high current is detected in amplifier #2. U11A is used to turn off the Q10 FET, if high current is detected in amplifier #3. With 2.257 VDC at Pin 5 of U11B or Pin 3 of U11A, the voltage output of current sense amplifier U17 or U18 at high current shut down should be greater than 15 Amps.

U14B is used to turn Off the gate of Q10 in the event of high power supply voltage, approximately +35.4 VDC. U14A is used to keep the FET disabled in the event of low power supply voltage, approximately +25.4 VDC.

*Current monitoring sections of the board.*

The ICs U16, U17 and U18 along with associated components set up the current monitoring sections of the board. R67, R68 and R69 are 0.01Ω/5W 1% through hole resistor is used for monitoring the current through several sections of the amplifier. The voltage developed across these resistors are amplified for current monitoring by U16, U17 or U18. The LT1787HVCS8 precision high side current sense IC amplifier accepts a maximum voltage of 60 VDC. The 43.2 kΩ resistor from pin 5 to ground sets the gain of the amplifier to about 17.28. This value is not set with much accuracy since the manufacturer internally matches the resistors of this part but their actual resistance value is not closely defined. A trimming resistor is suggested to give a temperature stability of –200 ppm/C, but instead the microcontroller will determine the exact gain of the circuit and use a correction factor for measurements. Circuit loading components are located in the lower portion of each current monitoring circuit. These components allow for short duration high current loading of the supply. By measuring the current through the sense resistor with and without the additional four 30.1 Ω 1% resistors. For very short duration pulses, a 1206 resistor can handle up to 60 watts. The processor requires 226 uSec per conversion. A supply voltage of +32 VDC will pass 1.06 amps + 1% through the load resistors.

A6 is a temperature sensor thermistor that is used to monitor the temperature of the module's heat sink. It connects to J6 pins 1 & 2 on the board wand is wired to the comparator IC U10B. If the temperature increases above 75°C the output will go Low that is used as a temperature fault output, which generates a Fault alert at U15A and disables Amplifier #1.

*Aural, Visual/Average and Reflected power detector sections of the board.*

Page 3

A Forward Power Sample enters the board at SMA Jack J3 and is split. One part connects to J4 on the board that is cabled to J1, the SMA Forward Power Sample Jack, located on the front panel of the assembly. The other part of the split forward power sample is detected by CR17 and the DC level amplified by U25A. The output of U25A at pin 1 is split with one part connected to the Aural Power sample, which is not used in this digital transmitter. The other split output connects to U265A that is part of the Forward Average Power circuit. The detected level is connected to L4 that is part of an intercarrier notch filter circuit that is tuned to eliminate the 4.5 MHz aural intercarrier, if present. The Average power sample is amplified by U26D and connected through the average calibration pot R166 to U26C. The output

of U26C is connected to the comparator IC U26B that has Aural Null and Offset Null, if present in the system, connected to the other input. The output Average Forward power level connects to J9 pin 2 of the board.

A Reflected Power Sample enters the board at SMA Jack J5 and is detected by CR20 and the DC level amplified by U28B. The output of U28B at pin 7 is connected through the reflected calibration pot R163 to U28C. The output is split with one part connected to J9 pin 5, the Reflected Power Output level of the board. The other part of the split from U28C connects to the comparator IC U28D that has a reference level connected to the other input. If the reflected level increases above the reference level a low output is produced and connected to the Reflected Power Shutdown circuit at CR28. The low shuts off Q14 causing pin 3 to go high that is connected to the inverter U15C. The output of U15C goes low producing a Reflected Power Fault that is connected to an output of the board, the Fault Alert circuit and also shuts down Amplifier #1.

Gain of the power measurements is completed through software. Only the Aural Null and Offset Null need to be done through front panel pots.

This completes the description of the Driver Amplifier Module Assembly, which is used in high power transmitters with external PA assemblies.

The output of the driver amplifier module assembly connects to the output of the Exciter/Amplifier chassis assembly at the "N" type connector Jack J25. The RF output at J25 connects to J200 the RF input to the external Power Amplifier Assembly.

This also completes the description for the entire Exciter/Amplifier chassis assembly.