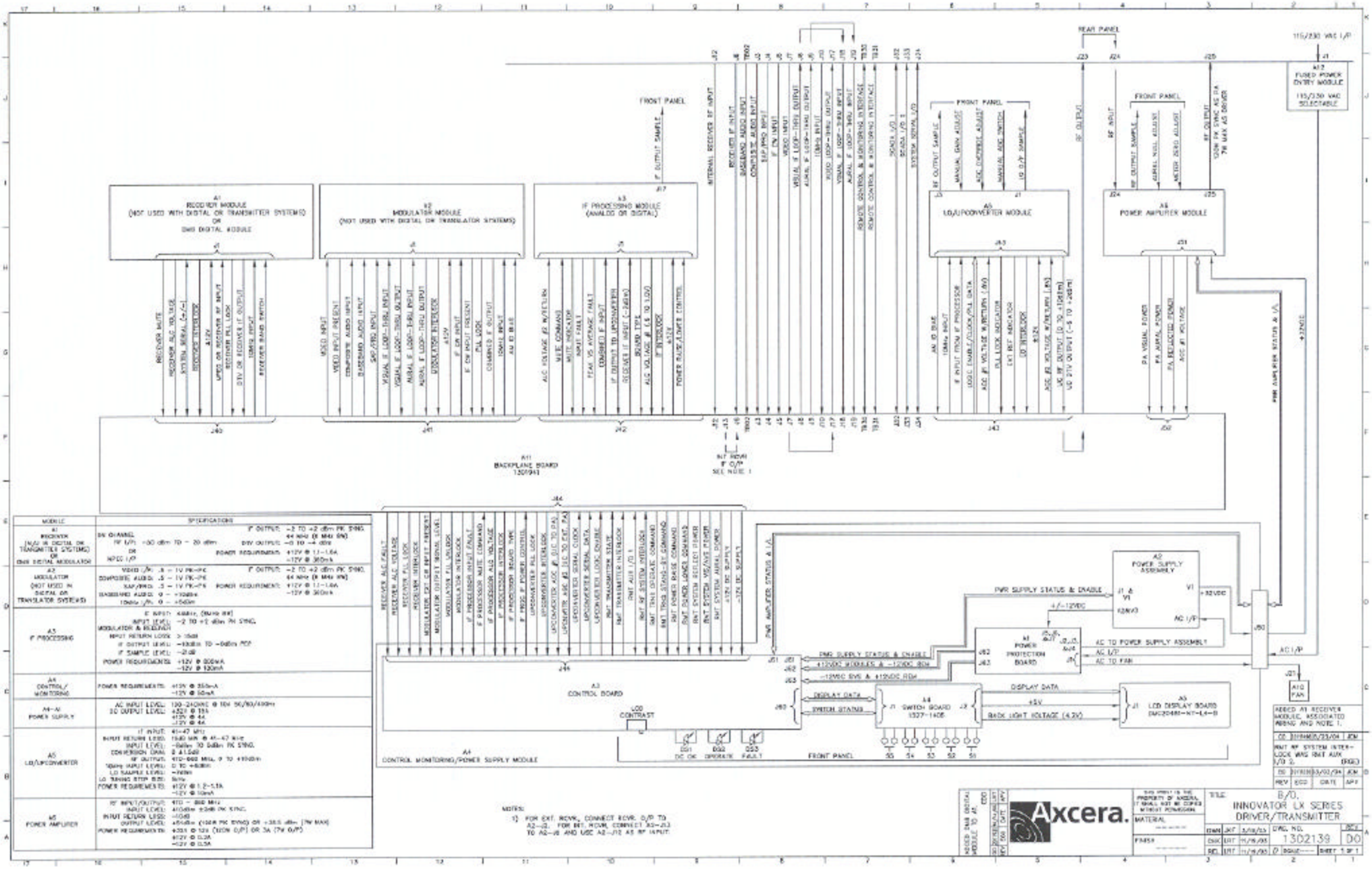
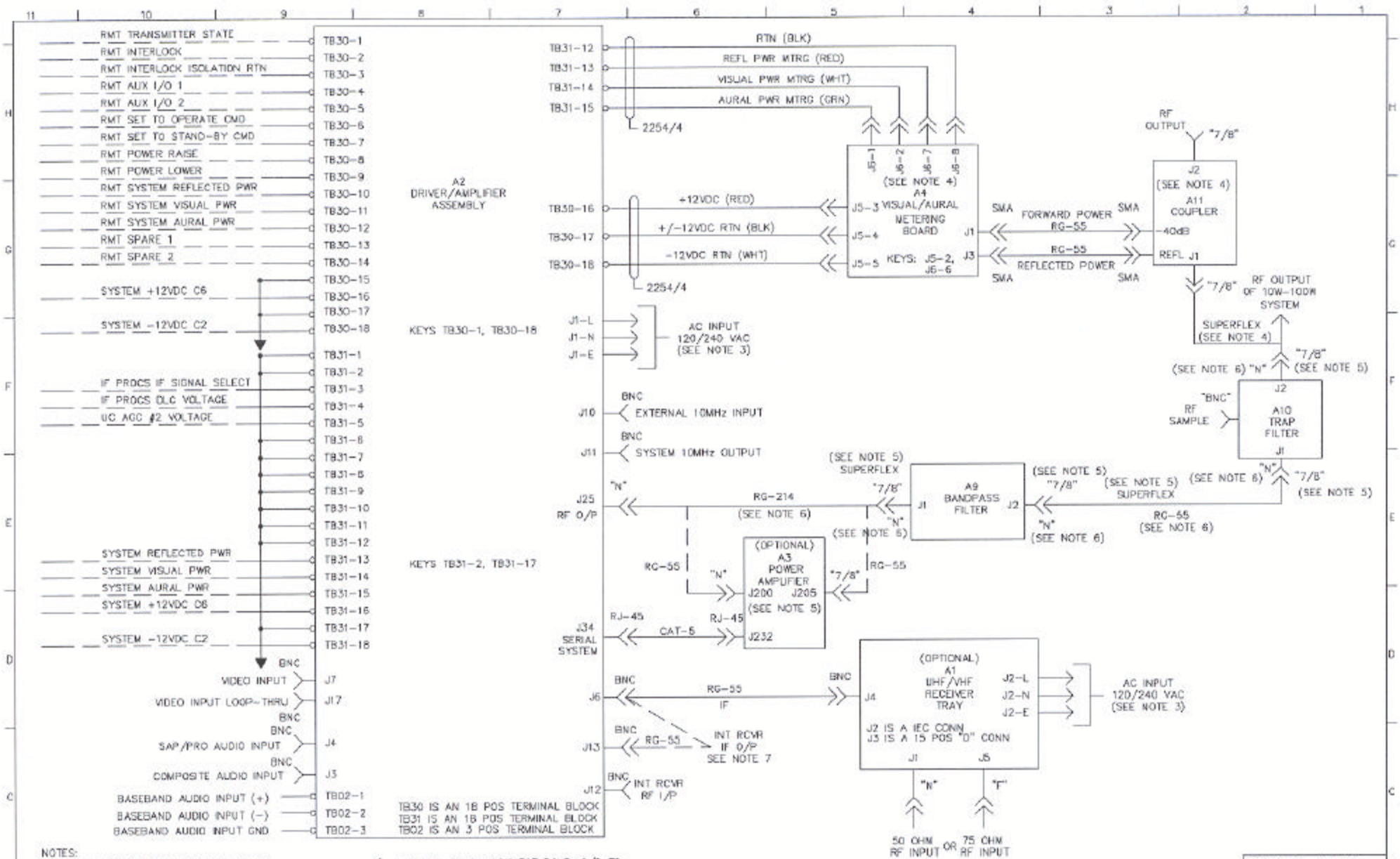


MODULE	SPECIFICATIONS
A1 RECEIVER (N/U IN DIGITAL OR TRANSMITTER SYSTEMS) OR DMS DIGITAL MODULATOR	IN CHANNEL: RF I/P: -90 dBm TO - 20 dBm OR IF OUTPUT: -2 TO +2 dBm PK SYNC 44 MHz (8 MHz BW) OUT CHANNEL: -0 TO -4 dBW POWER REQUIREMENTS: +12V @ 1.1-1.6A -12V @ 360mA
A2 MODULATOR (NOT USED IN DIGITAL OR TRANSLATOR SYSTEMS)	VIDEO I/P: .5 - 1V PK-PK COMPOSITE AUDIO: .5 - 1V PK-PK SAP/PRO: .5 - 1V PK-PK BASEBAND AUDIO: 0 - +10dBm 10MHz I/P: 0 - +5dBm IF OUTPUT: -2 TO +2 dBm PK SYNC 44 MHz (8 MHz BW) POWER REQUIREMENT: +12V @ 1.1-1.6A -12V @ 360mA
A3 IF PROCESSING	IF INPUT: 44MHz (8MHz BW) INPUT LEVEL: -2 TO +2 dBm PK SYNC MODULATOR & RECEIVER INPUT RETURN LOSS: > 15dB IF OUTPUT LEVEL: +10dBm TO -6dBm PCP IF SAMPLE LEVEL: -20dB POWER REQUIREMENTS: +12V @ 800mA -12V @ 130mA
A4 CONTROL/ MONITORING	POWER REQUIREMENTS: +12V @ 350mA -12V @ 50mA
A4-A1 POWER SUPPLY	AC INPUT LEVEL: 100-240VAC @ 50/60/400Hz DC OUTPUT LEVEL: +32V @ 19A +12V @ 4A -12V @ 4A
A5 LO/UPCONVERTER	IF INPUT: 41-47 MHz INPUT RETURN LOSS: 15dB MIN @ 41-47 MHz INPUT LEVEL: -8dBm TO 0dBm PK SYNC CONVERSION GAIN: 0 ±1.5dB RF OUTPUT: 470-860 MHz, 0 TO +10dBm 10MHz INPUT LEVEL: 0 TO +8dBm LO SAMPLE LEVEL: -14dBm LO TUNING STEP SIZE: 5kHz POWER REQUIREMENTS: +12V @ 1.2-1.5A -12V @ 10mA
A8 POWER AMPLIFIER	RF INPUT/OUTPUT: 470 - 860 MHz INPUT LEVEL: +10dBm ±3dB PK SYNC. INPUT RETURN LOSS: >10dB OUTPUT LEVEL: +54dBm (100W PK SYNC) OR +38.5 dBm (7W MAX) POWER REQUIREMENTS: +32V @ 12A (100W O/P) OR 3A (7W O/P) +12V @ 0.2A -12V @ 0.5A

THIS DRAWING IS THE PROPERTY OF AXCERA. IT SHALL NOT BE COPIED WITHOUT PERMISSION



NOTES:

1) ALL SINGLE WIRE 22 AWG UNLESS NOTED OTHERWISE.
2) ALL SHIELDED WIRE IS BELDEN YR40143 UNLESS NOTED OTHERWISE.
3) UNIT REQUIRES SPECIFIC INTERNAL WIRING CHANGES FOR 115/230VAC OPERATION. PLEASE CONSULT FACTORY.
4) THE A4 VISUAL/AURAL METERING BOARD AND A11 COUPLER ARE ONLY USED WITH AN EXTERNAL POWER AMPLIFIER ASSEMBLY AND ARE CONNECTED TO THE OUTPUT OF THE TRAP FILTER.
5) USED WITH HIGH POWER TRANSMITTERS
6) USED WITH 10W-100W TRANSMITTERS
7) FOR EXT. RCVR., CONNECT RCVR. O/P TO A2-J2. FOR INT. RCVR. CONNECT A2-J13 TO A2-J6 AND USE A2-J12 AS RF INPUT.

REV	ECO	DATE	APV
B0	2011148	8/23/04	JOM

ADDED J12, J13 AND NOTE 7.

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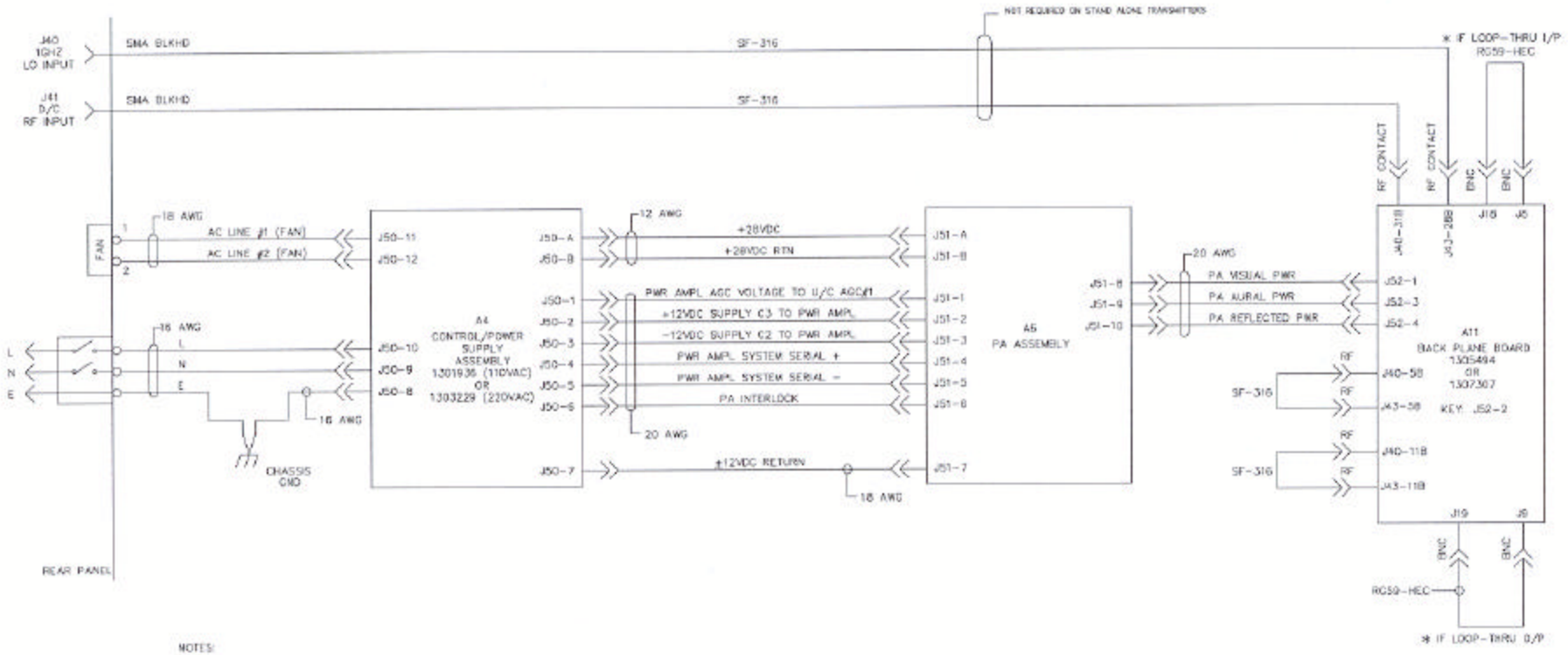
MATERIAL ------

FINISH ------

TITLE I/C – ANALOG LX SERIES TRANSMITTER/TRANSLATOR

DWN	CDO	10/14/03	DWG. NO. 1303478	REV B0
CHK	LRT	10/24/03		
REL	LRT	10/24/03	C SCALE ---	SHEET 1 OF 1



NOTES:

1) * INDICATES CABLE IS PART OF COAX ASSEMBLY.

REV	ECO	DATE	APV
CO	2012248	5/21/08	JGM
CO	2012248	5/28/08	JGM

ADDED CONNECTIONS BETWEEN A6-J51 AND A6-J52. NB

ADDED COAX AT J40 AND J41. ADDED 1307307 AT A11. ADDED NOTE 2. NB

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MATERIAL ------

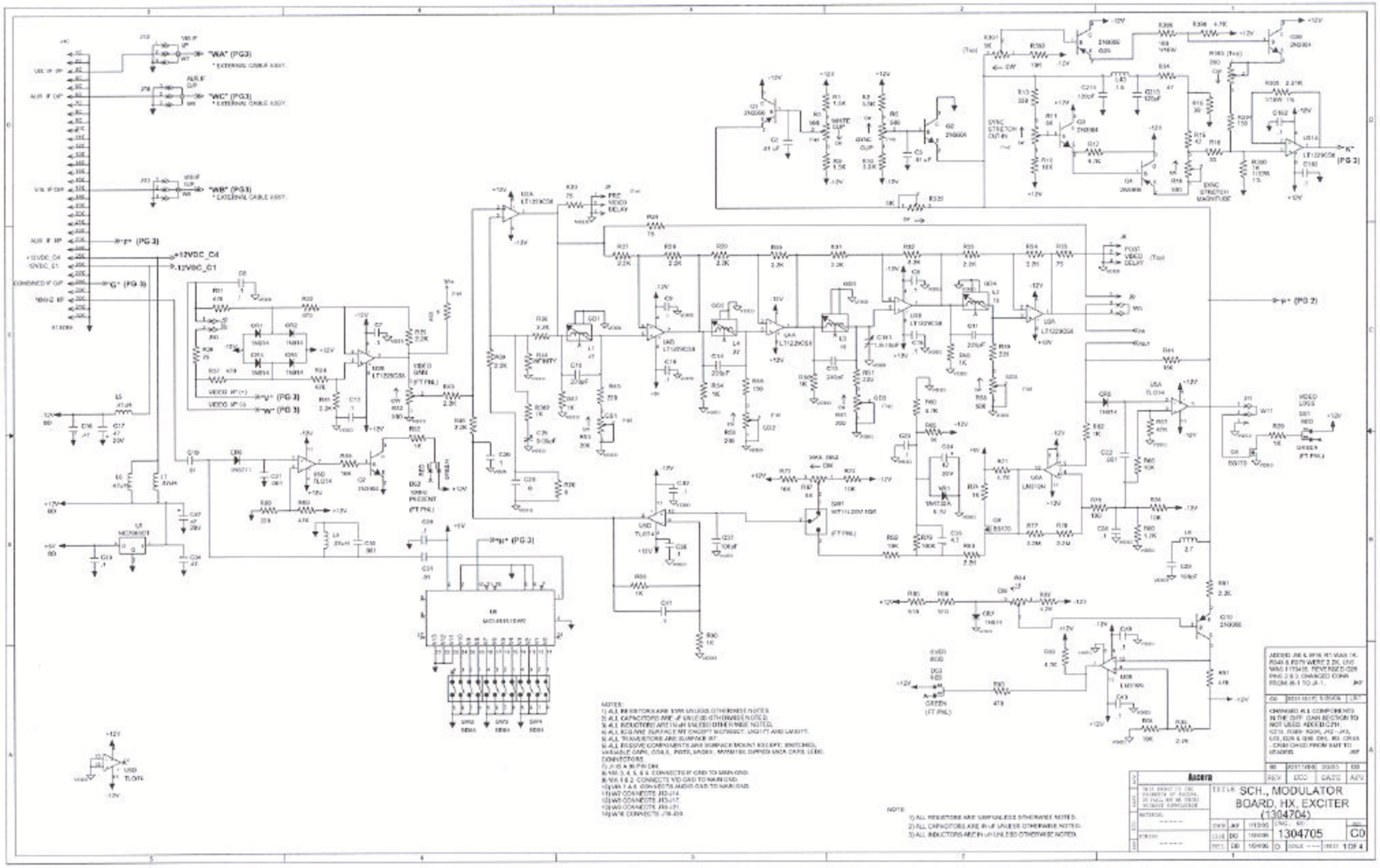
FINISH ------

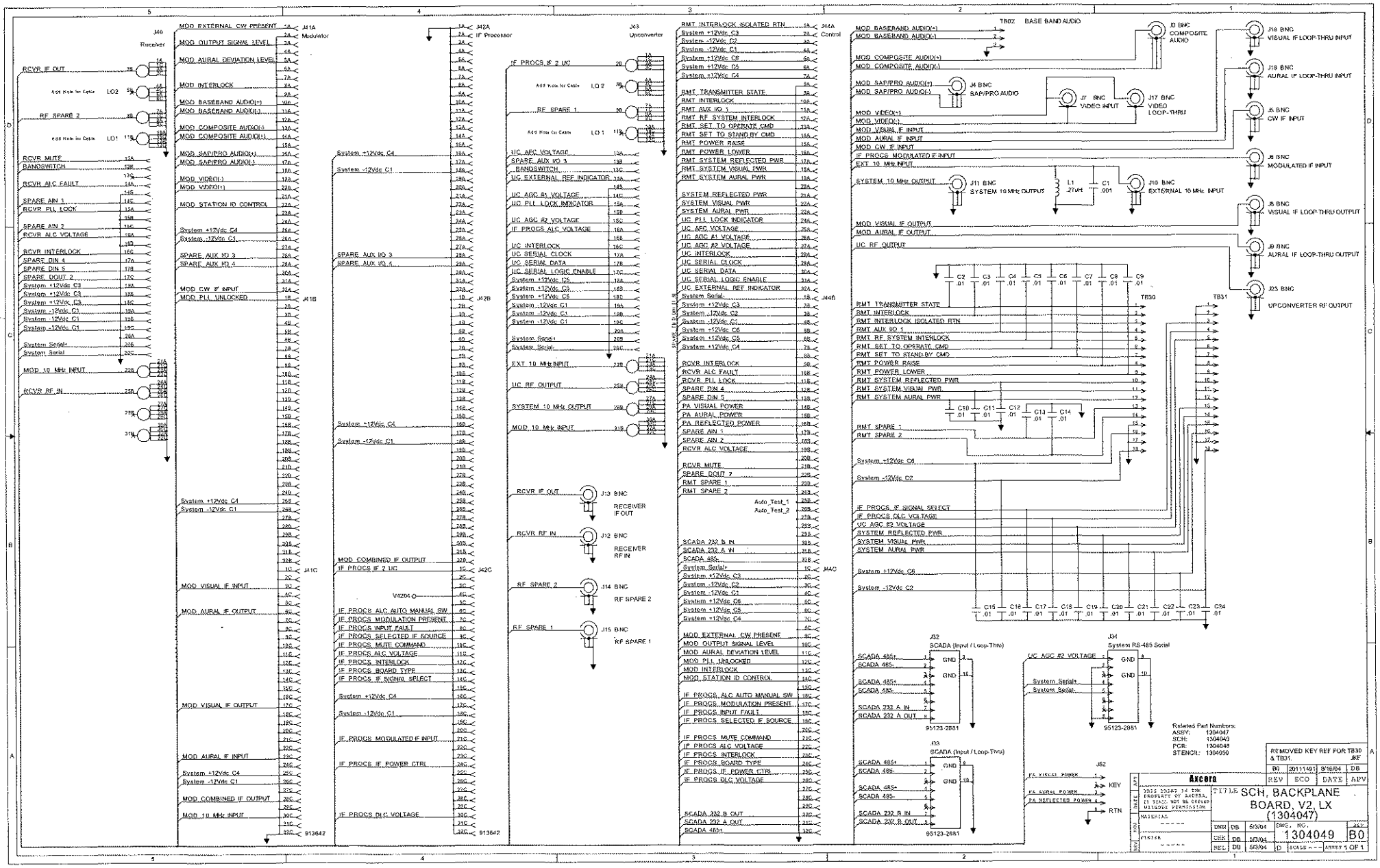
TITLE I/C, CHASSIS ASSEMBLY, DRIVER INNOVATOR HX

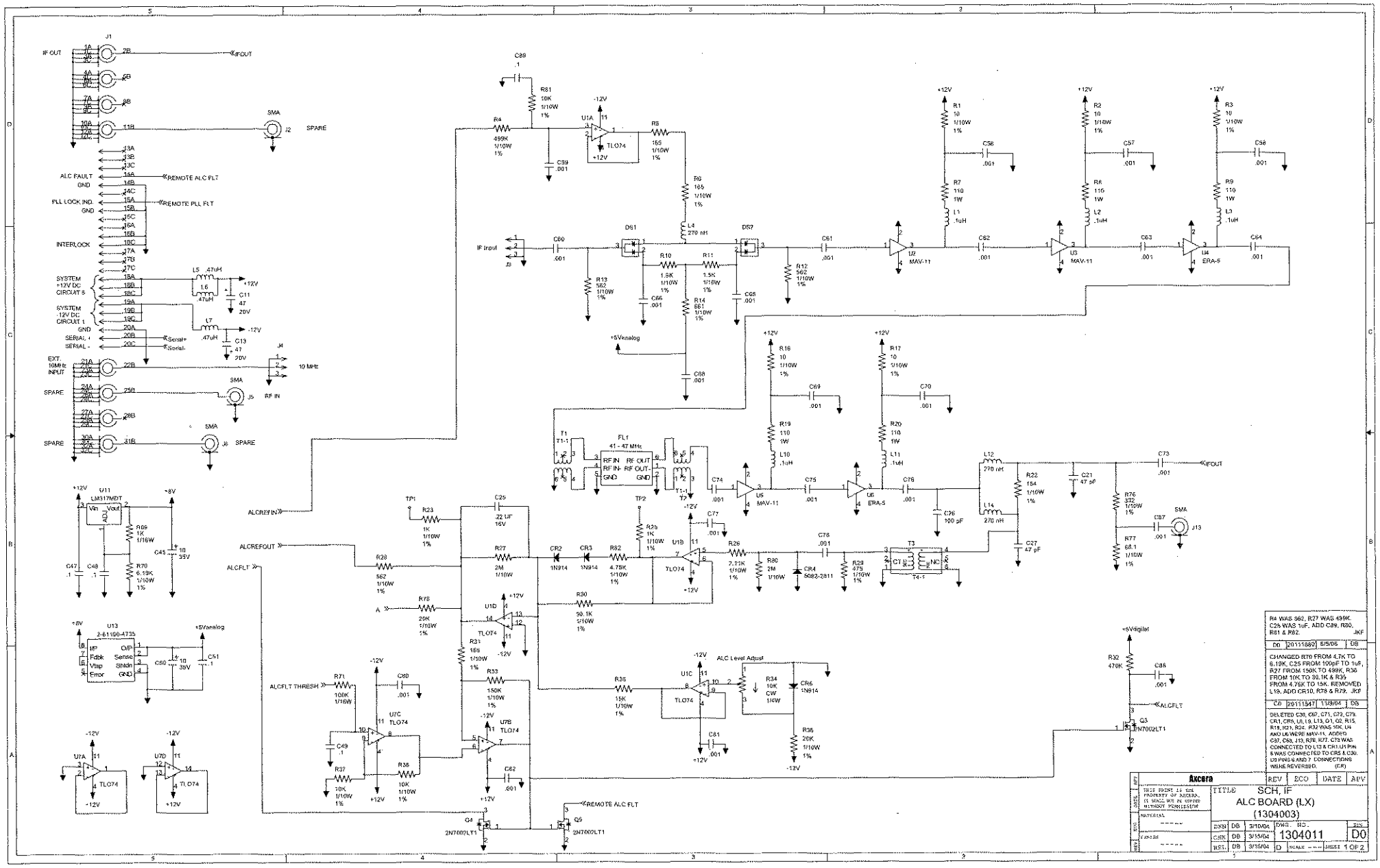
DWN			
CHK			
ISS			

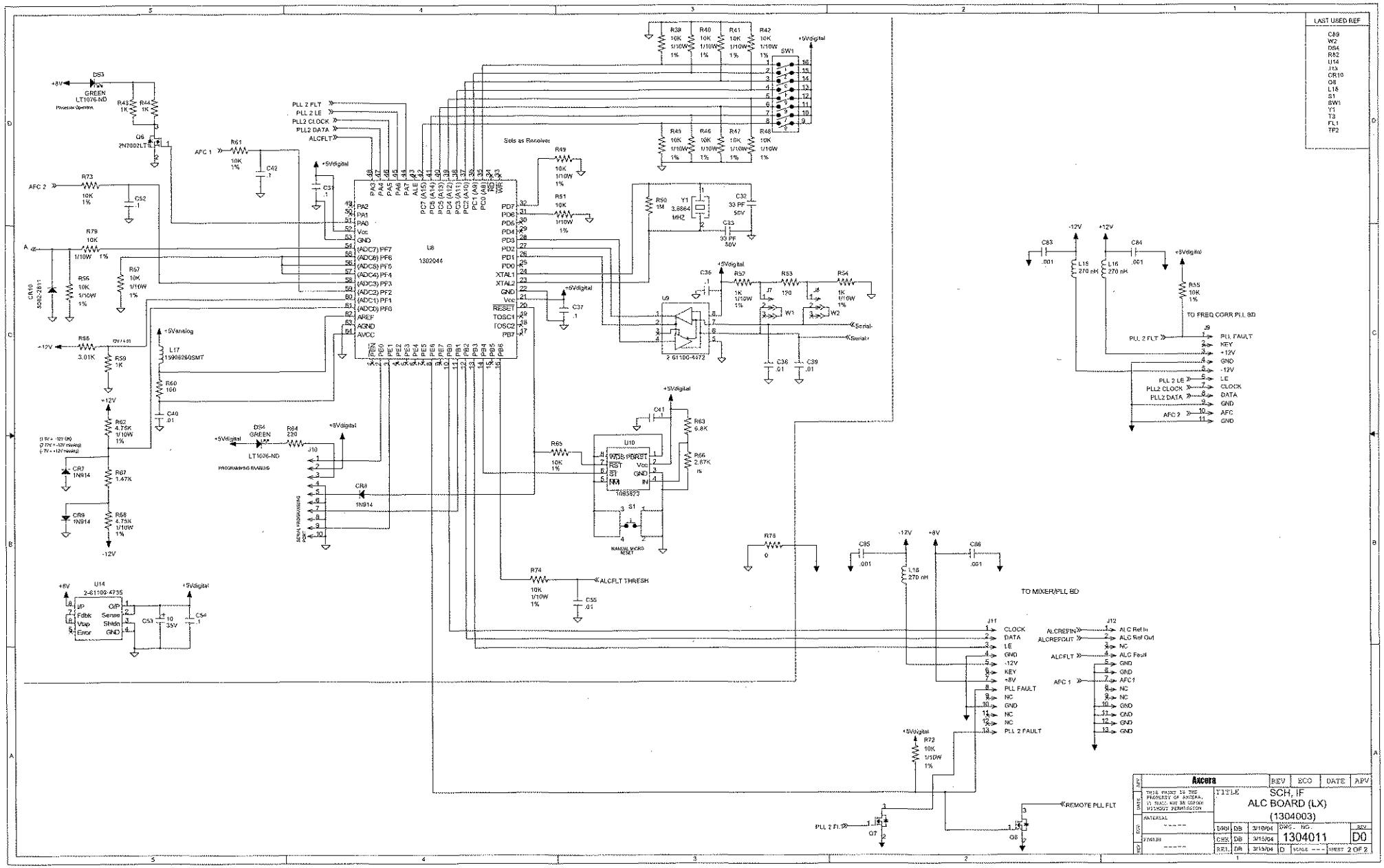
DWG NO. 1305554 REV. CO

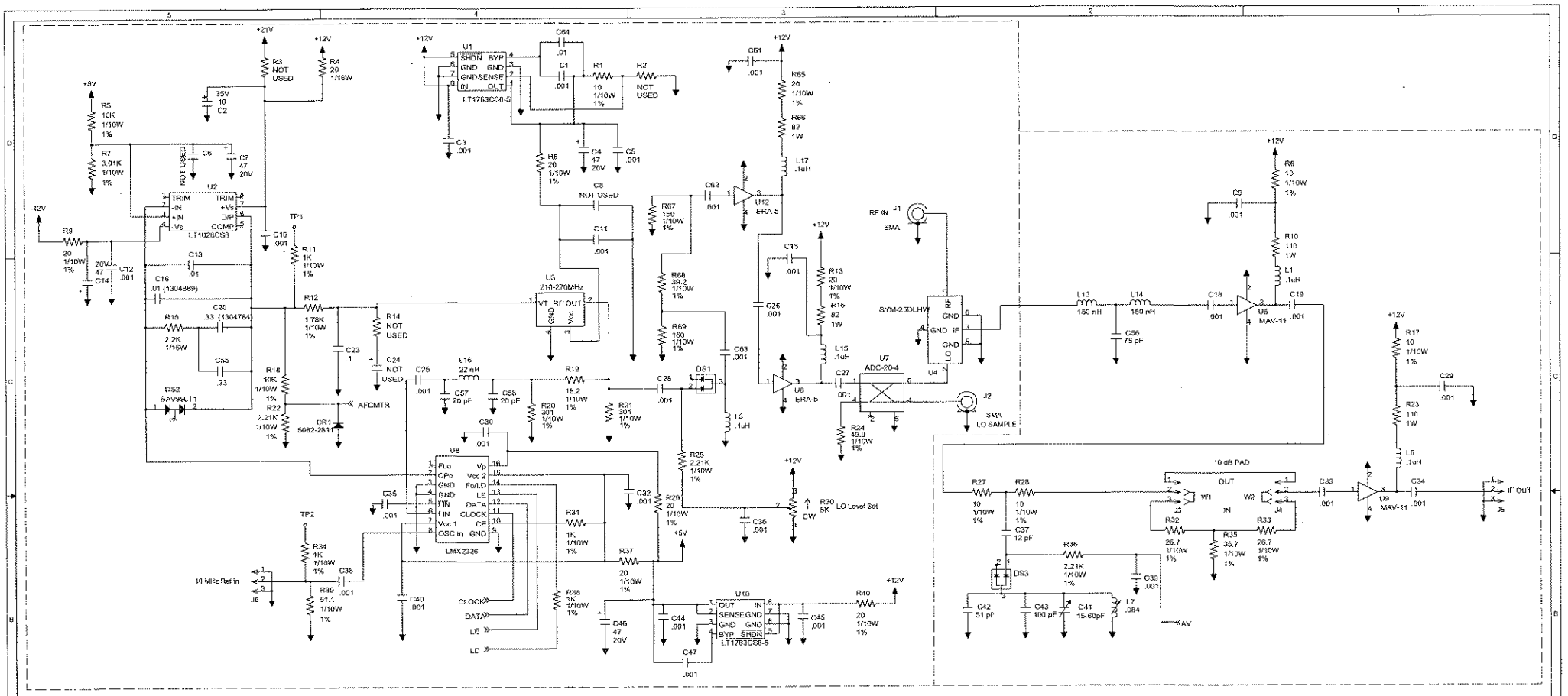
SIZE D SCALE --- SHEET 1 OF 1


SCH., MODULATOR
BOARD, HX, EXCITER
(1304704)
1304705
CD
1 OF 4
Ascera


J46 Receiver
J41A Modulator
J42A IF Processor
J43 Upconverter
J44A Control
J41B
J42B
J44B
J41C
J42C
J44C
TB02 BASE BAND AUDIO
J3 BNC COMPOSITE AUDIO
J18 BNC VISUAL IF LOOP-THRU INPUT
J19 BNC AURAL IF LOOP-THRU INPUT
J4 BNC SAP/PRO AUDIO
J7 BNC VIDEO INPUT
J17 BNC VIDEO LOOP-THRU
J5 BNC CW IF INPUT
J6 BNC MODULATED IF INPUT
J11 BNC SYSTEM 10 MHz OUTPUT
J10 BNC EXTERNAL 10 MHz INPUT
J8 BNC VISUAL IF LOOP-THRU OUTPUT
J9 BNC AURAL IF LOOP-THRU OUTPUT
J23 BNC UPCONVERTER RF OUTPUT
TB30
TB31
J13 BNC RECEIVER IF OUT
J12 BNC RECEIVER RF IN
J14 BNC RF SPARE 2
J15 BNC RF SPARE 1
J32 SCADA (Input / Loop-Thru)
J33 SCADA (Input / Loop-Thru)
J34 System RS-485 Serial
95123-2881
J52
KEY
RTN
Related Part Numbers:
ASSY: 1304047
SCH: 1304049
PCB: 1304048
STENCIL: 1304050
REMOVED KEY REF FOR TB30 & TB31. JKF
Axcera
TITLE SCH, BACKPLANE BOARD, V2, LX (1304047)
DWG. NO. 1304049
REV B0
SCALE ---
SHEET 1 OF 1


IF OUT
IFOUT
SPARE
ALC FAULT
GND
REMOTE ALC FLT
PLL LOCK IND.
REMOTE PLL FLT
INTERLOCK
SYSTEM +12V DC CIRCUIT 5
SYSTEM -12V DC CIRCUIT 1
SERIAL +
SERIAL -
Serial+
Serial-
EXT. 10MHz INPUT
10 MHz
RF IN
ALCREFIN
ALCREFOUT
ALCFLT
ALCFLT THRESH
ALC Level Adjust
IF Input
+5Vanalog
+5Vdigital
REMOTE ALC FLT
RF IN
RF OUT
GND
41 - 47 MHz
U1 MAV-11
U3 MAV-11
U4 ERA-5
U5 MAV-11
U6 ERA-5
U11 LM317MDT
U13 2-6100-4735
U1A TLO74
U1B TLO74
U1C TLO74
U1D TLO74
U7A TLO74
U7B TLO74
U7C TLO74
U7D TLO74
Q3 2N7002LT1
Q4 2N7002LT1
Q5 2N7002LT1
J1
J2 SPARE
J4
J5 RF IN
J6 SPARE
J13
R4 WAS 562, R27 WAS 499K.
C25 WAS 1uF. ADD C89, R80,
R81 & R82. JKF
D0 20111680 5/5/05 DB
CHANGED R70 FROM 4.7K TO
6.19K, C25 FROM 100pF TO 1uF,
R27 FROM 150K TO 499K, R30
FROM 10K TO 30.1K & R35
FROM 4.75K TO 15K. REMOVED
L19, ADD CR10, R78 & R79. JKF
C0 20111547 11/9/04 DB
DELETED C38, C67, C71, C72, C75,
CR1, CR5, U8, L9, L13, Q1, Q2, R15,
R18, R21, R24, R32 WAS 10K, U4
AND U6 WERE MAV-11. ADDED
C37, C68, J13, R76, R77. C73 WAS
CONNECTED TO L12 & CR11 U1 Pin
8 WAS CONNECTED TO CR5 & C30.
U3 PINS 6 AND 7 CONNECTIONS
WERE REVERSED. (C.R)
Axcera
REV ECO DATE APV
THIS PRINT IS THE PROPERTY OF AXCERA, IT MAY NOT BE COPIED WITHOUT PERMISSION
TITLE
SCH, IF
ALC BOARD (LX)
(1304003)
DRN DB 3/10/04
CHK DB 3/15/04
APL DB 3/15/04
DWG. NO. 1304011
REV D0
SCALE ---
SHEET 1 OF 2


LAST USED REF
C89
W2
D64
R82
U14
J13
CR10
Q8
L18
S1
SW1
Y1
T3
FL1
TP2
U8
1302044
U9
2-61109-4472
U10
1085823
U14
2-61109-4735
Y1
3.6864 MHz
SW1
J10
J11
J12
TO FREQ CORR PLL BD
TO MIXER/PLL BD
PLL FAULT
KEY
+12V
GND
-12V
LE
CLOCK
DATA
AFC
ALC Ref In
ALC Ref Out
ALC Fault
NC
PLL 2 FAULT
REMOTE PLL FLT
ALCFLT THRESH
Sets as Receiver
Serial-
Serial+
Ascera
SCH, IF
ALC BOARD (LX)
(1304003)
1304011
D0
SHEET 2 OF 2



NOTE:

1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.
4) Bd Material 30 mil FR4

REV	ECO	DATE	APV
B0	20111854	3/20/06	DB
ADDED C64			CR

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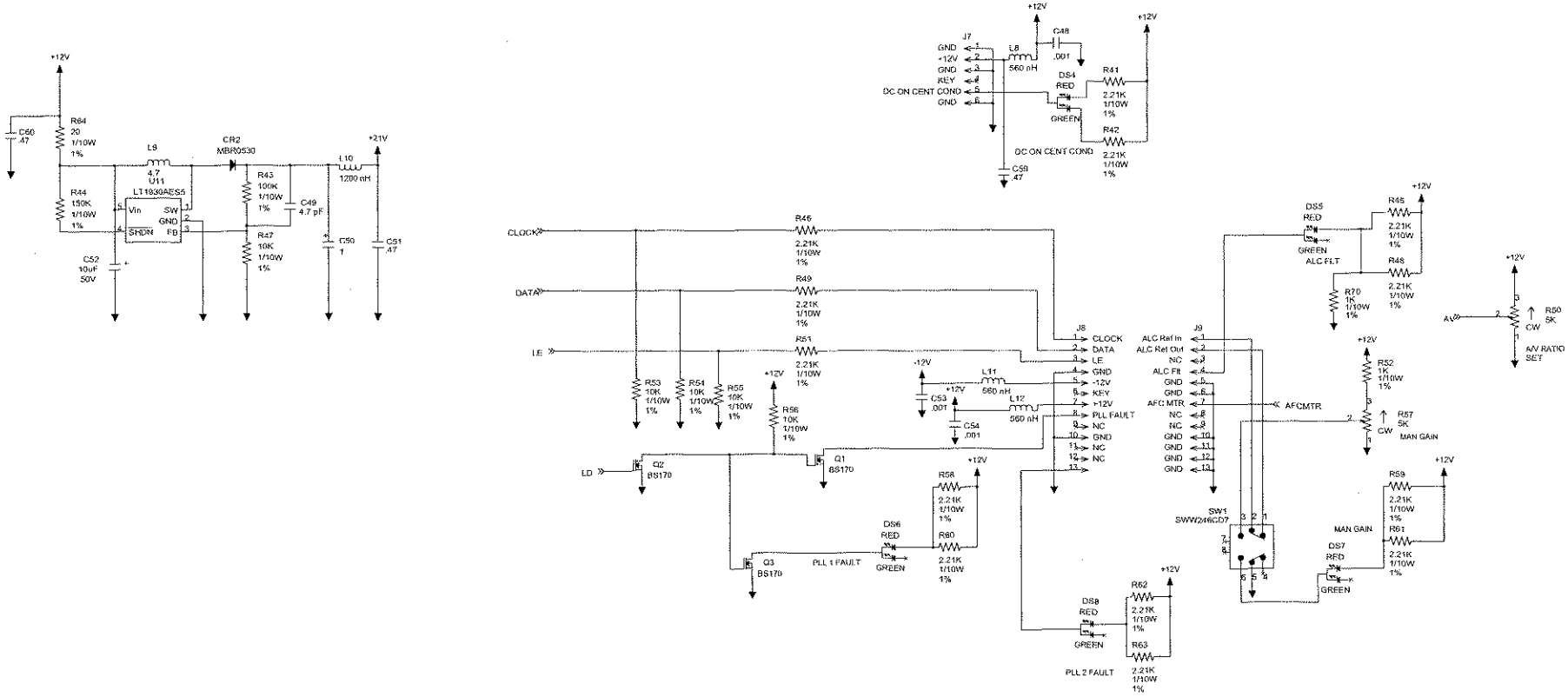
MATERIAL ----

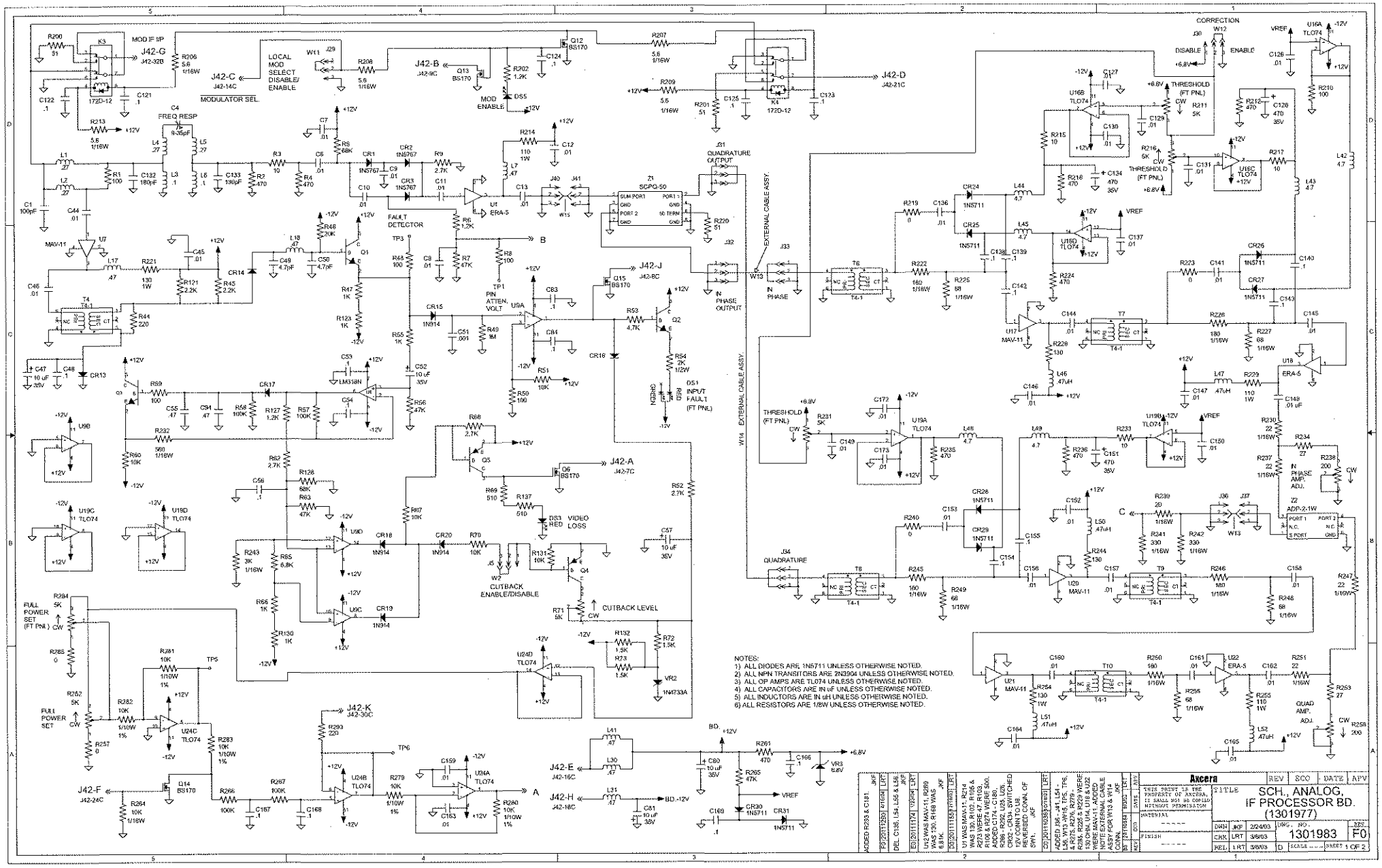
FINISH ----

TITLE SCH, HB MIXER / PLL BD., RECEIVER (1306472)

DWN	JKF	9/13/05	DWG. NO. 1306473 REV B0
CHK	DB	9/13/05	
REL	DB	9/13/05	D SCALE --- SHEET 1 OF 2



Axcera	REV	ECO	DATE	APV
THIS PRINT IS THE PROPERTY OF AXCERA. IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE	SCH, HB MIXER / PLL BD., RECEIVER (1306472)		
	DWN JKF	9/13/05	DWG. NO. 1306473	REV B0
	CHK DB	9/13/05		
	REL DB	9/13/05	D SCALE ----	SHEET 2 OF 2


MOD IF IP
J42-G
J42-32B
J42-C
J42-14C
MODULATOR SEL.
LOCAL MOD SELECT DISABLE/ ENABLE
J42-B
J42-8C
MOD ENABLE
J42-D
J42-21C
FREQ RESP
FAULT DETECTOR
PIN ATTEN. VOLT
IN PHASE OUTPUT
QUADRATURE OUTPUT
EXTERNAL CABLE ASSY.
IN PHASE
J42-J
J42-8C
INPUT FAULT (FT PNL)
J42-A
J42-7C
VIDEO LOSS
CUTBACK ENABLE/DISABLE
CUTBACK LEVEL
FULL POWER SET (FT PNL)
FULL POWER SET
J42-K
J42-30C
J42-F
J42-24C
J42-E
J42-16C
J42-H
J42-18C
CORRECTION
DISABLE
ENABLE
THRESHOLD (FT PNL)
THRESHOLD (FT PNL)
THRESHOLD (FT PNL)
IN PHASE AMP. ADJ.
QUAD AMP. ADJ.
J34 QUADRATURE
NOTES:
1) ALL DIODES ARE 1N5711 UNLESS OTHERWISE NOTED.
2) ALL NPN TRANSISTORS ARE 2N2904 UNLESS OTHERWISE NOTED.
3) ALL OP AMPS ARE TL074 UNLESS OTHERWISE NOTED.
4) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
5) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.
6) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
Axcera
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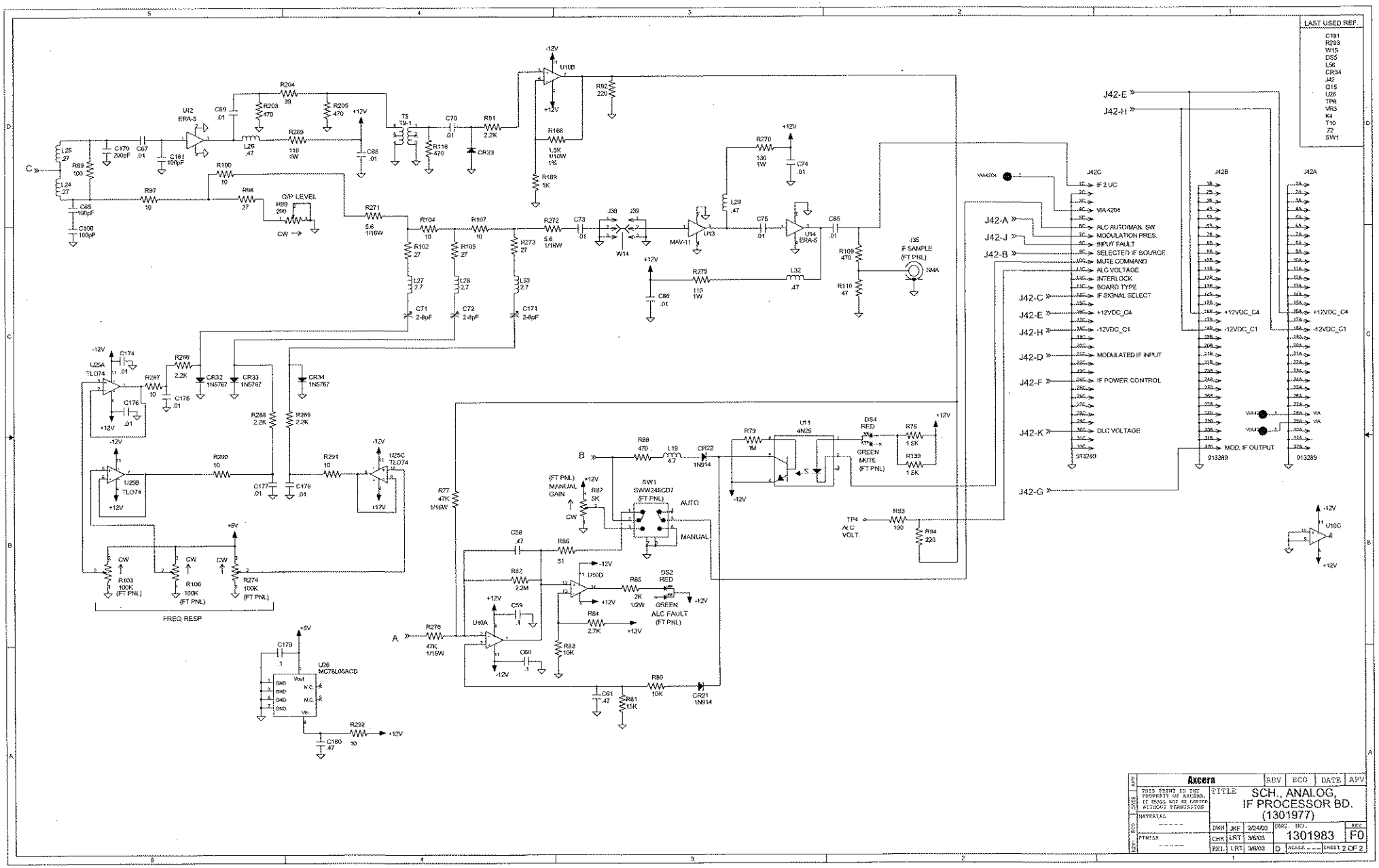
TITLE
SCH., ANALOG, IF PROCESSOR BD. (1301977)
DWN JKF 2/24/03
CHK LRT 3/6/03
REL LRT 3/6/03
DWG. NO. 1301983
REV F0
SCALE ----
SHEET 1 OF 2


LAST USED REF.
C181
R293
W15
DS5
L36
CR34
J42
Q15
U28
TP6
VR3
K4
T10
Z2
SW1
U12
ERA-5
U10B
U13
MAV-11
U14
ERA-5
J35
IF SAMPLE
(FT PNL)
SMA
O/P LEVEL
CW
U25A
TL074
U25B
TL074
U25C
TL074
FREQ RESP
U26
MC78L05ACD
U11
4N25
DS4
RED
GREEN
MUTE
(FT PNL)
TP4
ALC
VOLT.
(FT PNL)
MANUAL
GAIN
SW1
SWW246CD7
(FT PNL)
AUTO
MANUAL
U10D
DS2
RED
GREEN
ALC FAULT
(FT PNL)
U10A
U10C
J42C
J42B
J42A
IF 2 UC
VIA 4204
ALC AUTO/MAN. SW
MODULATION PRES.
INPUT FAULT
SELECTED IF SOURCE
MUTE COMMAND
ALC VOLTAGE
INTERLOCK
BOARD TYPE
IF SIGNAL SELECT
+12VDC_C4
-12VDC_C1
MODULATED IF INPUT
IF POWER CONTROL
DLC VOLTAGE
MOD. IF OUTPUT
913289
J42-A
J42-J
J42-B
J42-C
J42-E
J42-H
J42-D
J42-F
J42-K
J42-G
VIA4204
VIA
+12VDC_C4
-12VDC_C1
Axcera
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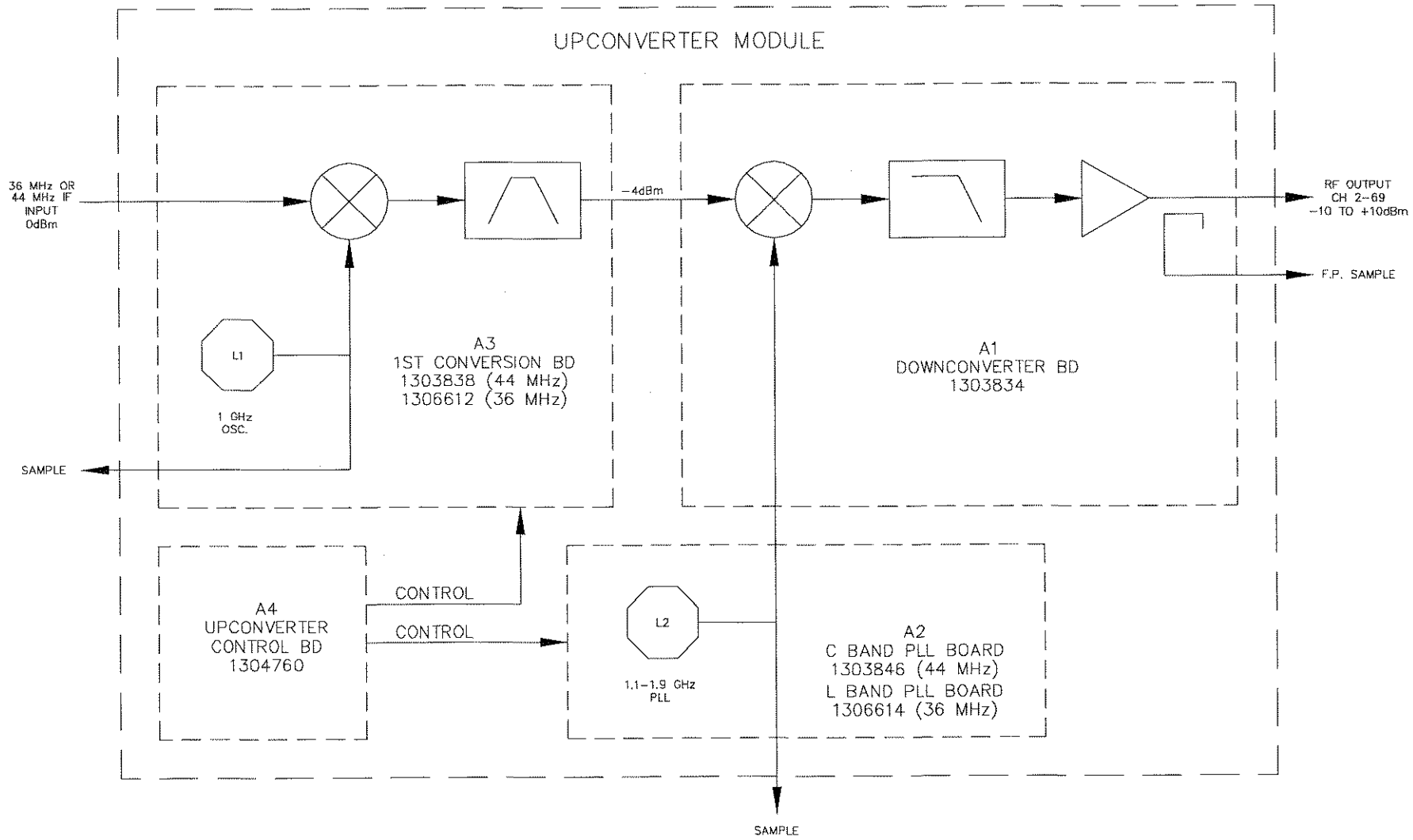
TITLE
SCH., ANALOG,
IF PROCESSOR BD.
(1301977)
MATERIAL
FINISH
DWN JKF 2/24/03
CHK LRT 3/6/03
PEL LRT 3/6/03
DWG. NO. 1301983
REV F0
SCALE
SHEET 2 OF 2



REV	ECO	DATE	APV

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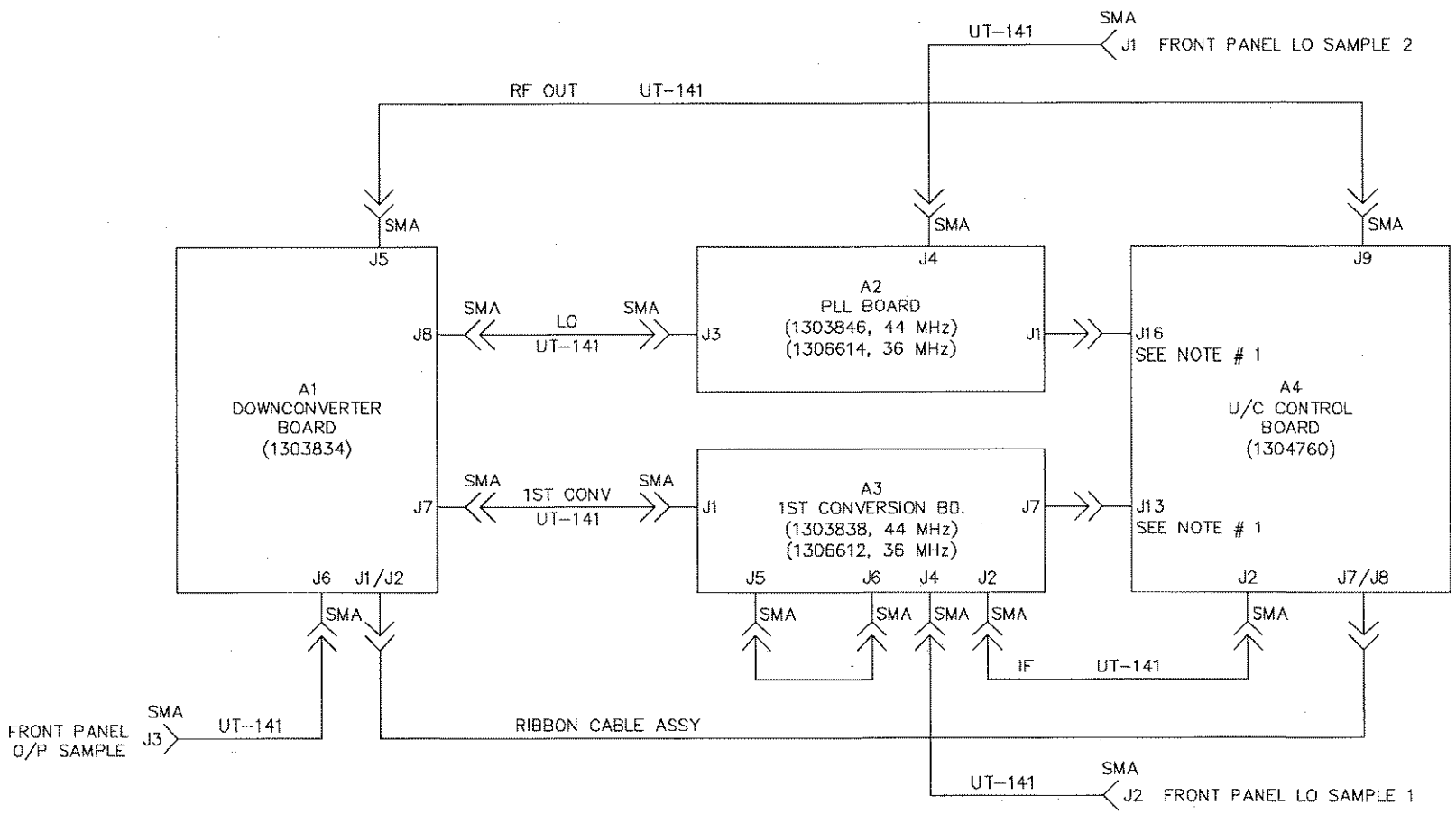
MATERIAL ------

FINISH ------

TITLE B/D, U/C ASSEMBLY, VHF/UHF LX

DWN	RGE	5/7/04	DWG. NO. 1303830	REV A0
CHK	DWB	9/30/04		
REL	DWB	9/30/04	C SCALE ---	SHEET 1 OF 1



NOTES:
1. CONNECTORS ARE BOARD TO BOARD AND NOT PART OF THE HARNESS.

A2-J3 WAS A2-J2 (TYPO)			RT
B0	20111728	4/1/05	DB
REV	ECO	DATE	APV

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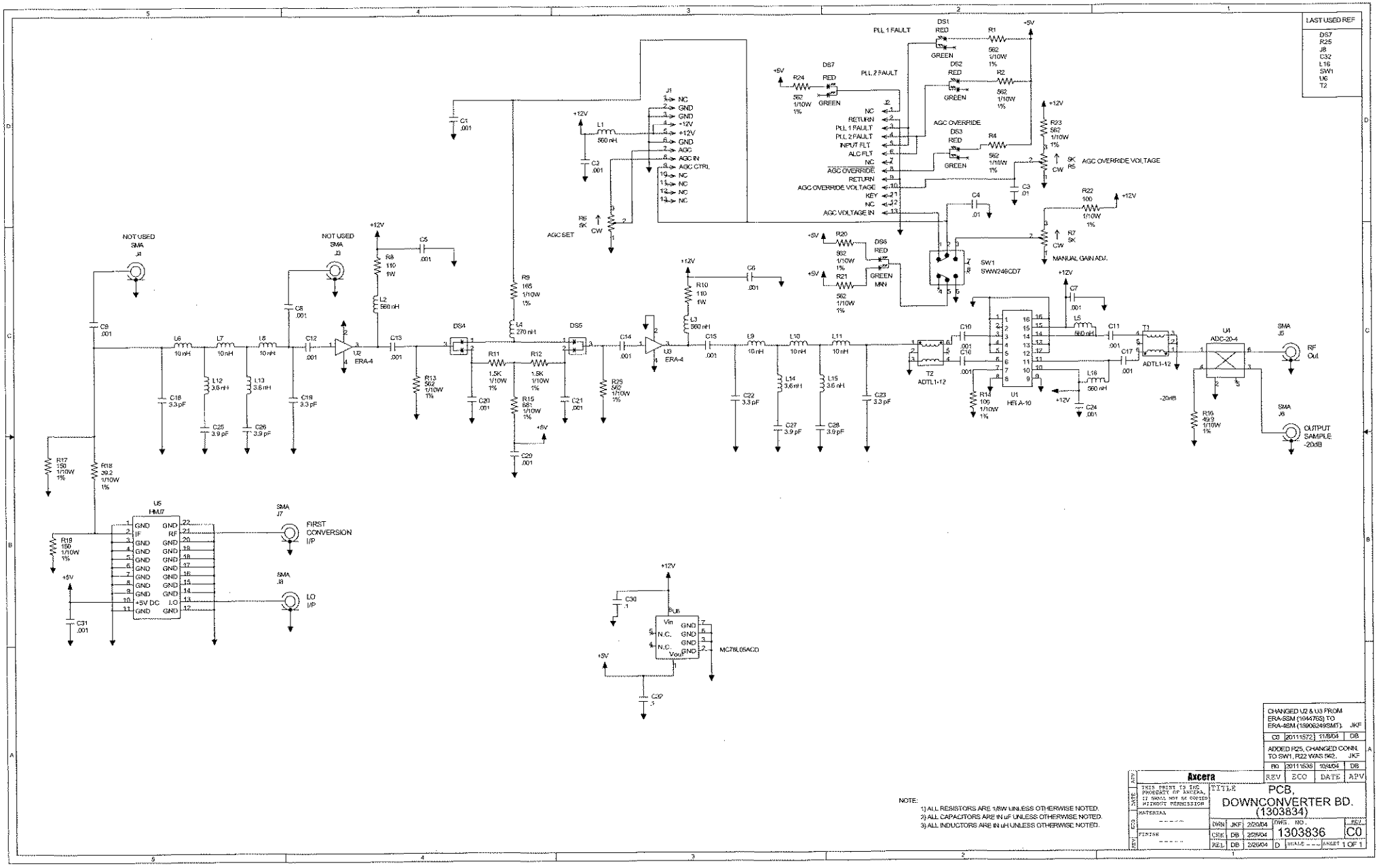
MATERIAL ------

FINISH ------

TITLE I/C, UPCONVERTER ASSY, VHF/UHF, LX

DWN	RGE	04/06/04	DWG. NO. 1303831	REV B0
CHK	DWB	9/30/04		
REL	DWB	9/30/04	B SCALE ---	SHEET 1 OF 1


LAST USED REF
DS7
R25
J8
C32
L16
SW1
U6
T2
PLL 1 FAULT
PLL 2 FAULT
AGC OVERRIDE
AGC OVERRIDE VOLTAGE
MANUAL GAIN ADJ.
AGC SET
SW1
SWW246CD7
U2
ERA-4
U3
ERA-4
U1
HELA-10
T2
ADTL1-12
T1
ADTL1-12
U4
ADC-20-4
-20dB
SMA
J5
RF
Out
SMA
J6
OUTPUT
SAMPLE
-20dB
NOT USED
SMA
J4
NOT USED
SMA
J3
U5
HMJ7
SMA
J7
FIRST
CONVERSION
I/P
SMA
J8
LO
I/P
U6
MC78L05ACD
NOTE:
1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.
CHANGED U2 & U3 FROM ERA-5SM (1045763) TO ERA-4SM (15906249SMT). JKF
C0 20111572 11/8/04 DB
ADDED R25, CHANGED CONN. TO SW1, R22 WAS 562. JKF
R0 20111535 10/4/04 DB
REV ECO DATE APV
Axcera
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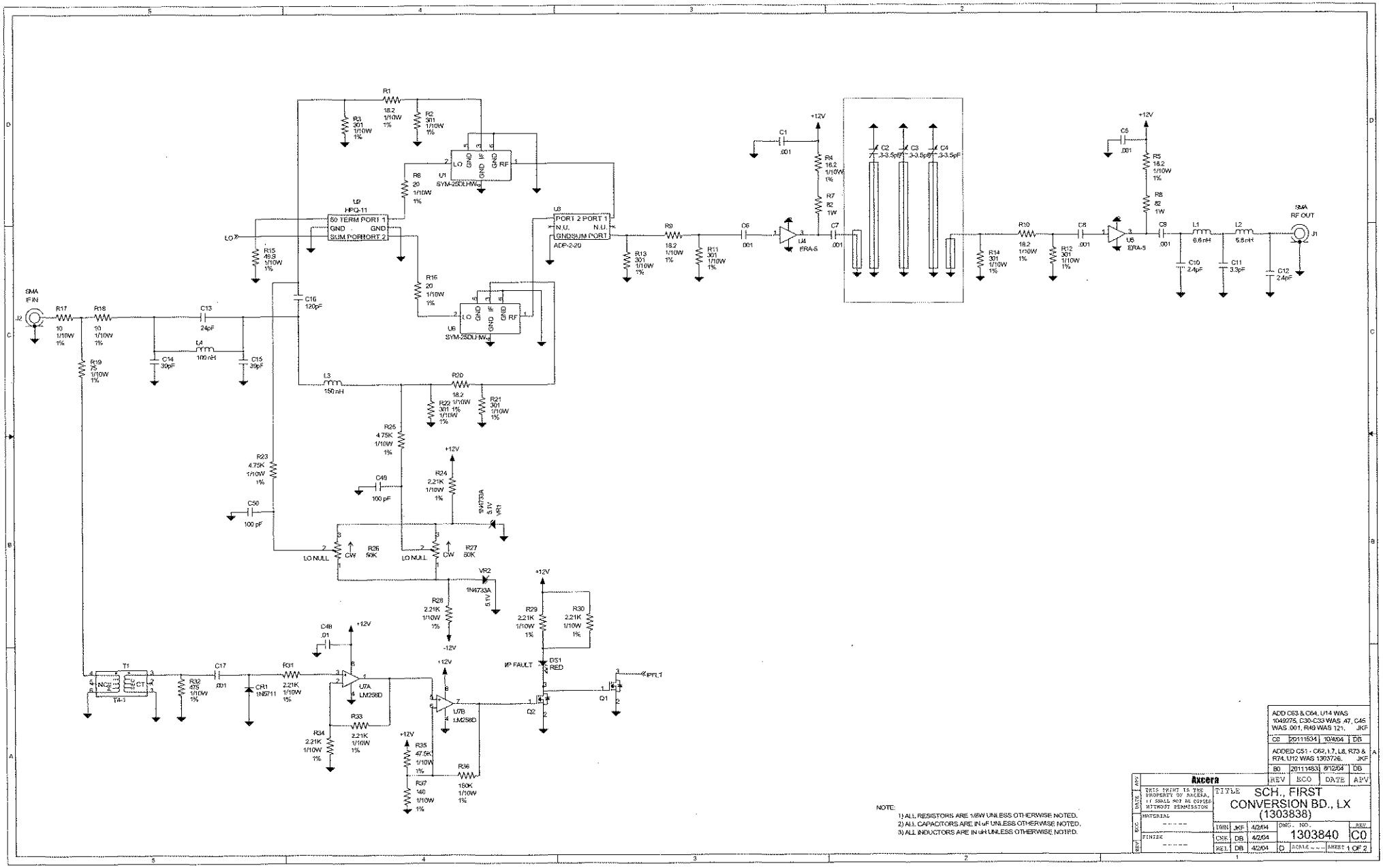
MATERIAL
FINISH
TITLE PCB, DOWNCONVERTER BD. (1303834)
DWN JKF 2/20/04
CHK DB 2/25/04
REL DB 2/26/04
DWG. NO. 1303836
REV C0
SCALE ---
SHEET 1 OF 1



NOTE:
1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.

REV	ECO	DATE	APV
C0	20111534	10/4/04	DB
B0	20111483	8/12/04	DB

ADD C63 & C64, U14 WAS 1040275, C30-C33 WAS .47, C45 WAS .001, R49 WAS 121. JKF

ADDED C51 - C62, L7, L8, R73 & R74, U12 WAS 1303726. JKF

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MATERIAL ----

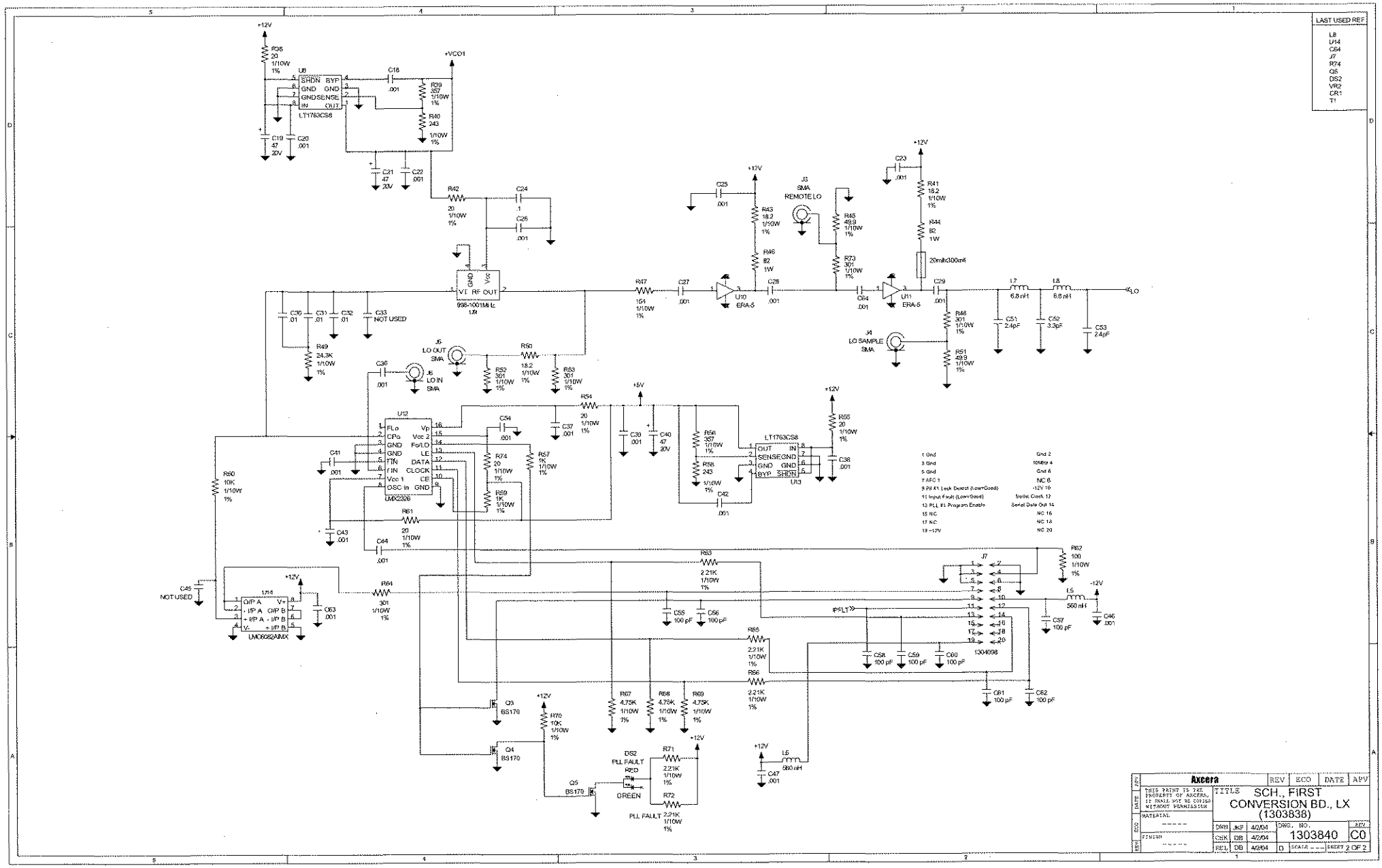
FINISH ----

TITLE SCH., FIRST CONVERSION BD., LX (1303838)

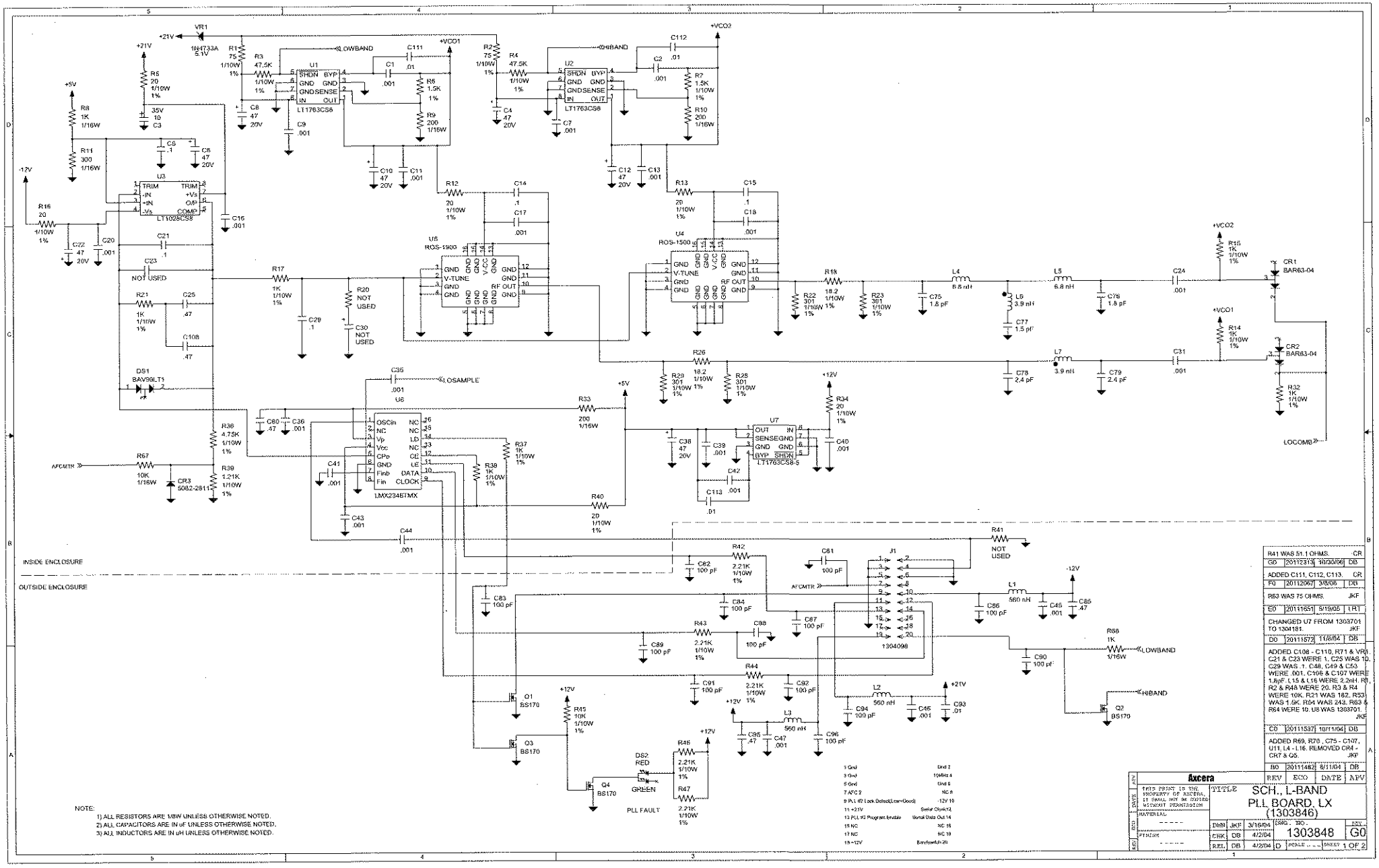
DWN	JKF	4/2/04	
CHK	DB	4/2/04	
REL	DB	4/2/04	

DWG. NO. 1303840 REV C0

D SCALE ---- SHEET 1 OF 2



Axcera		REV	ECO	DATE	APV
THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH., FIRST CONVERSION BD., LX (1303838)				
MATERIAL -----	DRN JKP 4/2/04	DWG. NO. 1303840		REV C0	
FINISH ------	CSK DB 4/2/04				
	REL DB 4/2/04	D	SCALE ---	SHEET 2 OF 2	



NOTE:
1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.

1 Gnd		Gnd 3	
3 Gnd		10MHz 4	
5 Gnd		Gnd 6	
7 AFC 2		NC 8	
9 PLL #2 Lock Detect(Low=Good)		12V 10	
11 +21V		Serial Clock 12	
13 PLL #2 Program Enable		Serial Data Out 14	
15 NC		NC 16	
17 NC		NC 18	
19 +12V		Bandswitch 20	

R41 WAS 51.1 OHMS.			CR
G0	20112313	10/30/06	DB
ADDED C111, C112, C113.			CR
F0	20112067	3/8/06	DB
R63 WAS 75 OHMS.			JKF
E0	20111651	9/19/05	LRT
CHANGED U7 FROM 1303701 TO 1304181.			JKF
D0	20111572	11/8/04	DB
ADDED C108 - C110, R71 & VR1. C21 & C23 WERE 1, C25 WAS 10. C29 WAS .1. C48, C49 & C53 WERE .001. C106 & C107 WERE 1.8pF. L15 & L16 WERE 2.2nH. R1, R2 & R46 WERE 20. R3 & R4 WERE 10K. R21 WAS 182. R53 WAS 1.5K. R54 WAS 243. R63 & R64 WERE 10. U8 WAS 1303701.			JKF
C0	20111537	10/11/04	DB
ADDED R69, R70 , C75 - C107, U11, L4 - L16. REMOVED CR4 - CR7 & Q5.			JKF
B0	20111462	9/11/04	DB

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REV	ECO	DATE	APV

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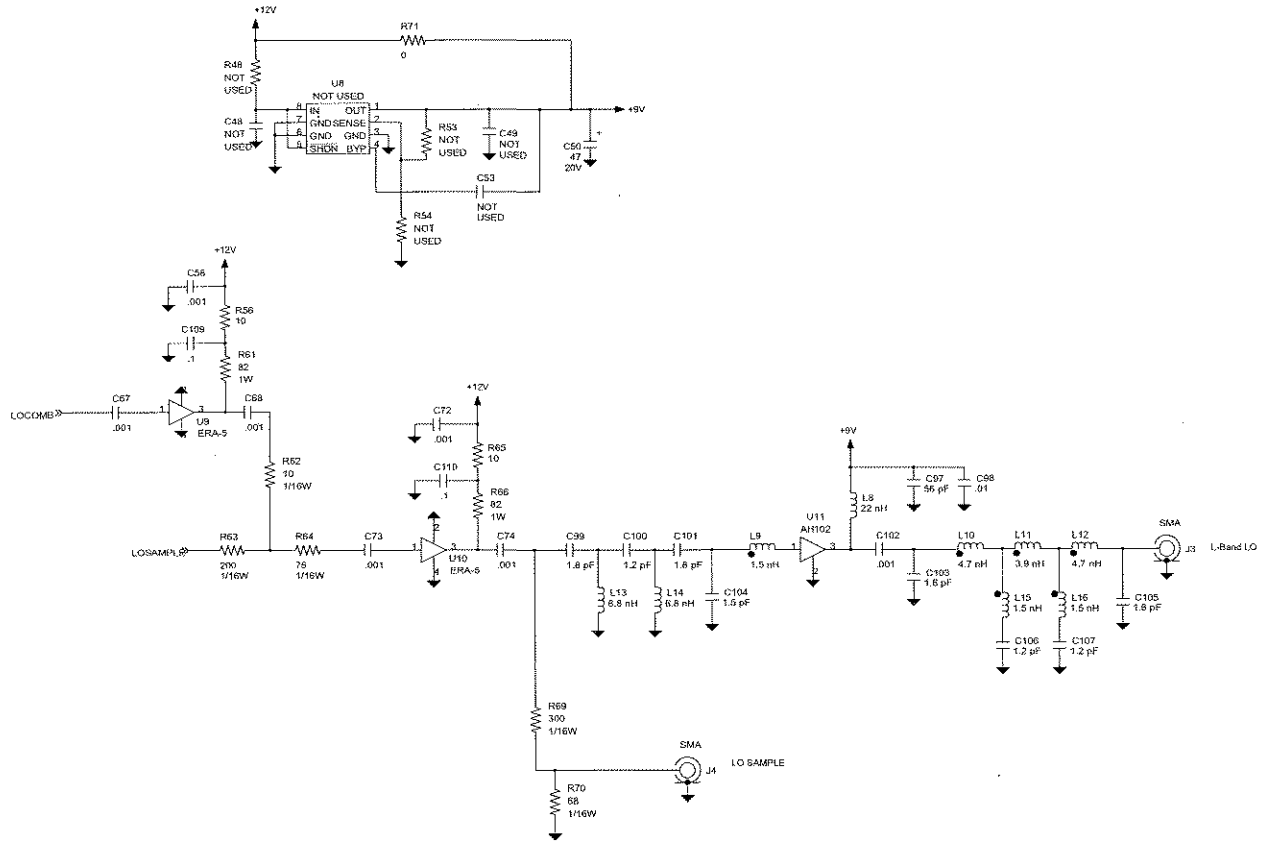
MATERIAL: ------

FINISH: ------

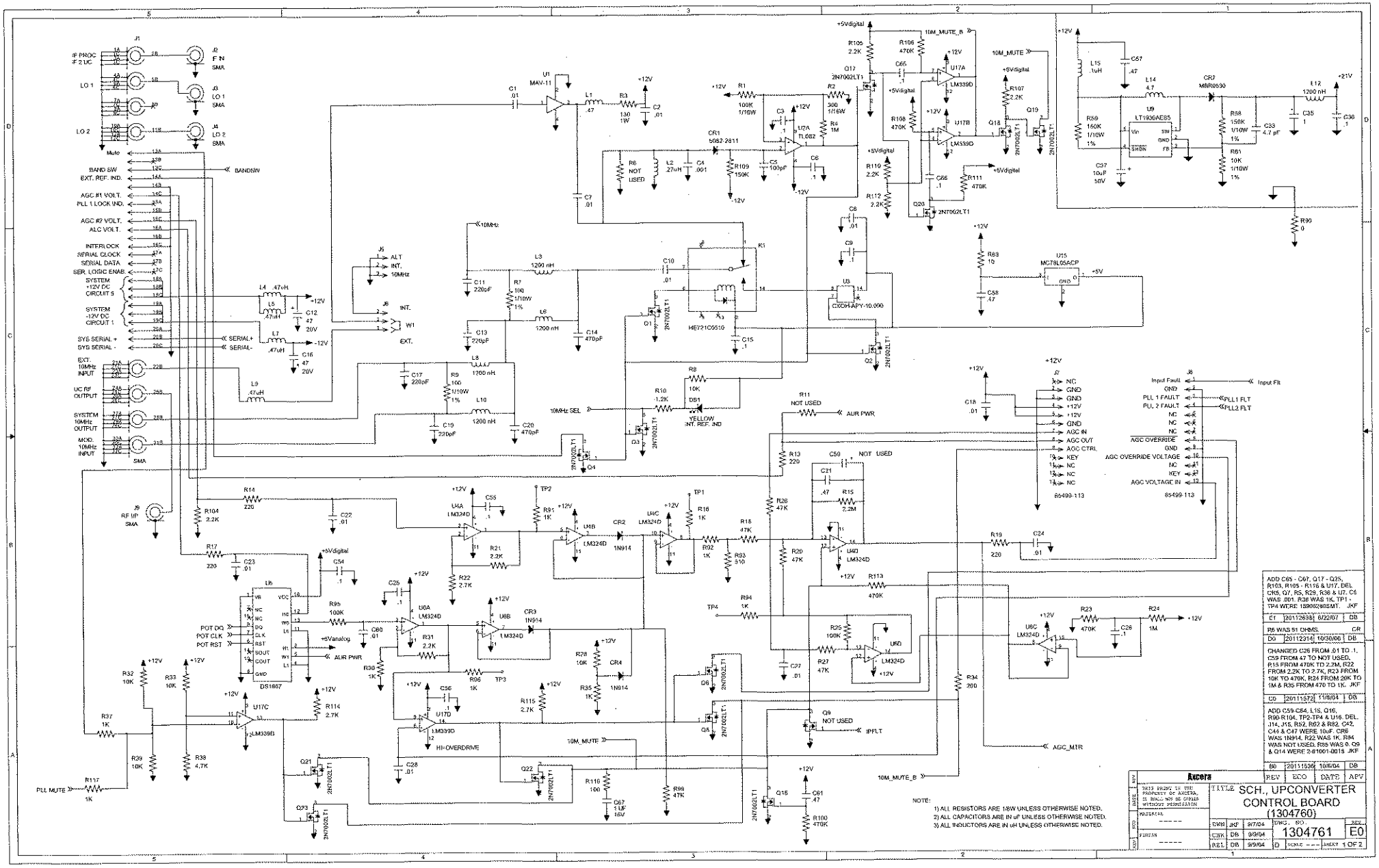
TITLE: SCH., L-BAND PLL BOARD, LX (1303846)

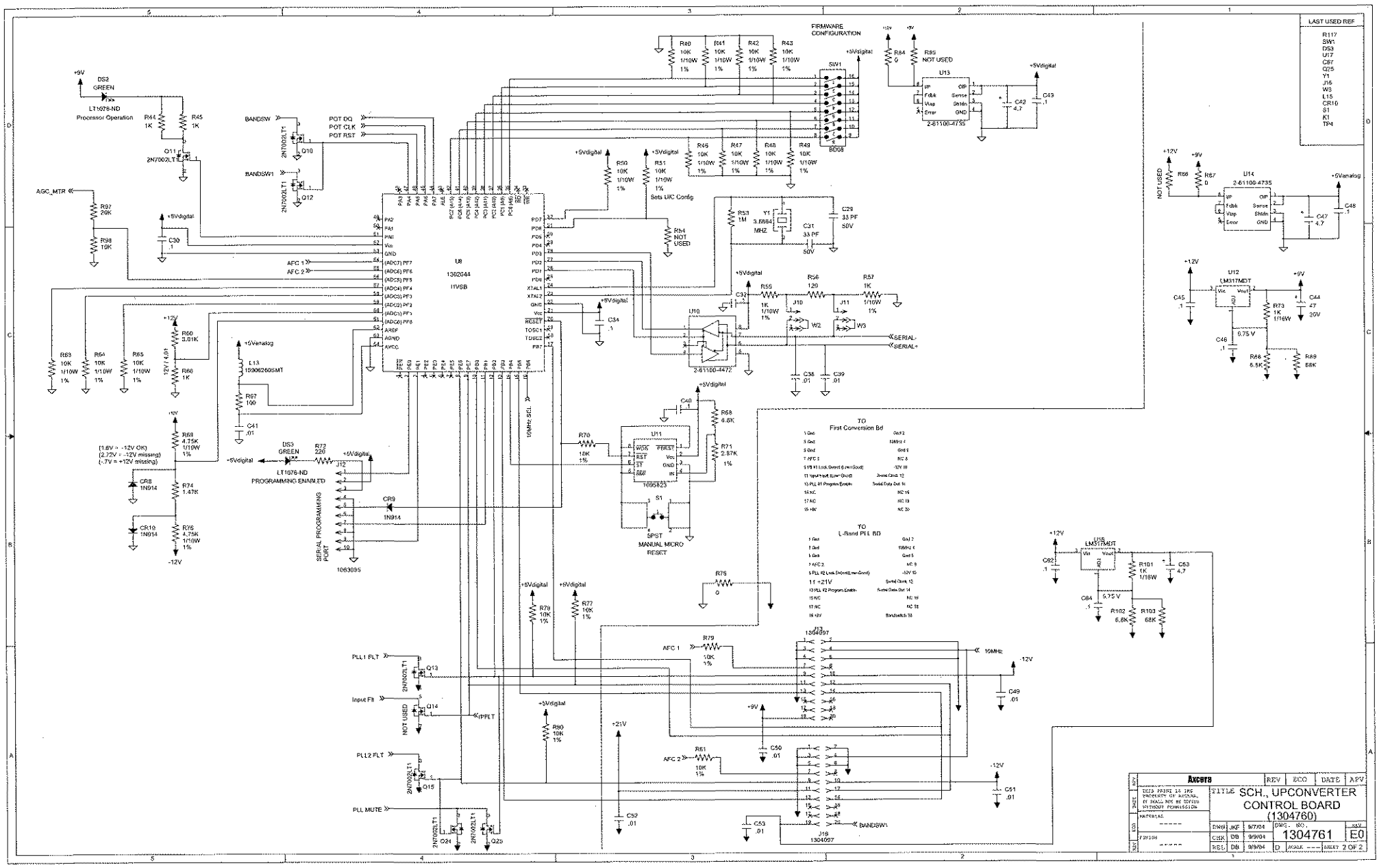
DRN	JKF	3/16/04	SIZE: B0 - 1303848	REV: G0
CHK	DB	4/2/04		
REL	DB	4/2/04	D SCALE: ----	SHEET 1 OF 2

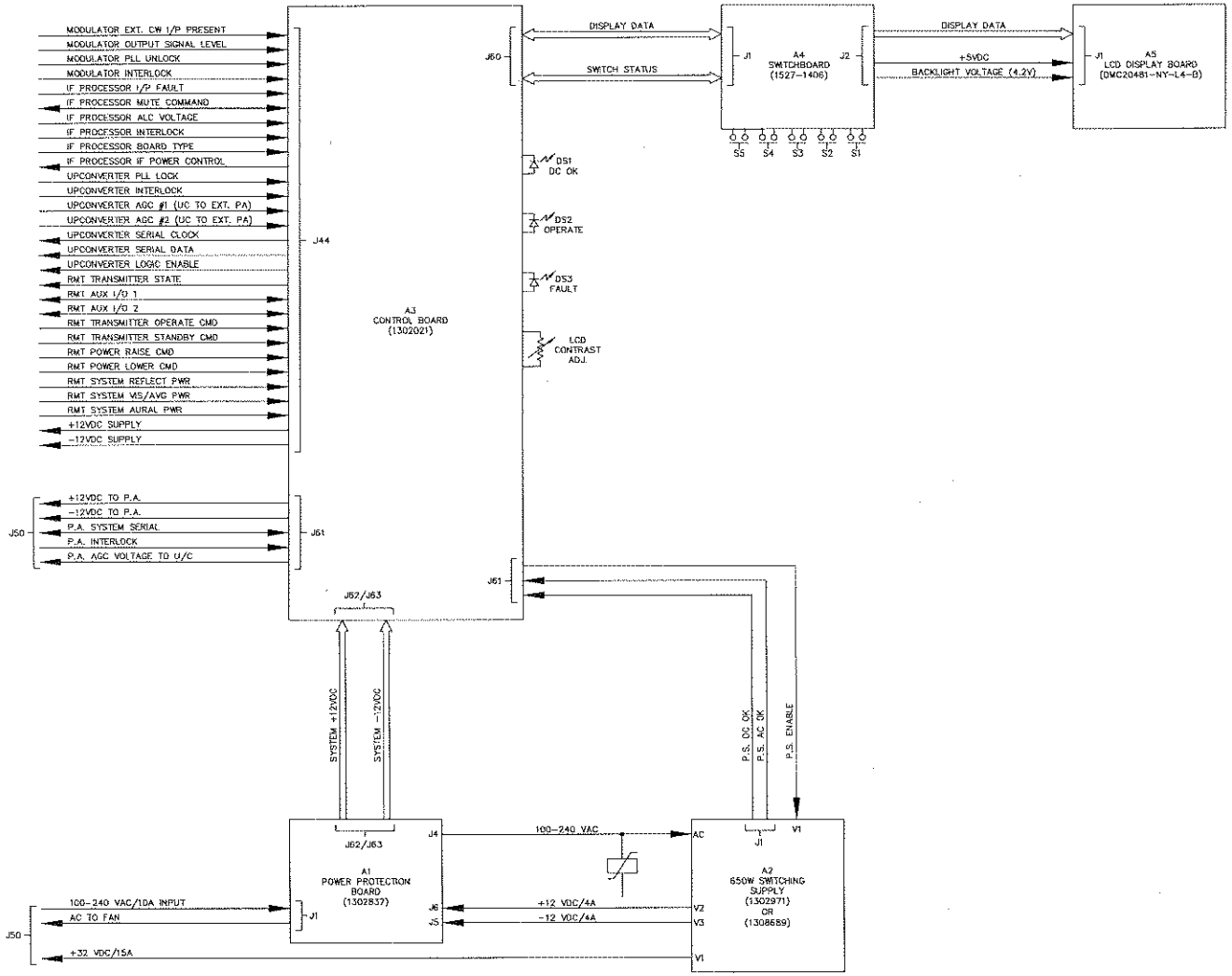
LAST USED REF
C113
L16
U11
R71
J4
Q4
CR3
DS2
VR1



Axcera	REV	ECO	DATE	APV
THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE	SCH., L-BAND PLL BOARD, LX (1303846)		
MATERIAL -----	DRW	JKF	3/10/04	DWG. NO. 1303848 REV G0
FINISH -----	CHK	DB	4/2/04	
	REL	DB	4/2/04	D SCALE --- SHEET 2 OF 2


IF PROC IF 2 UC
LO 1
LO 2
Mute
BAND SW
EXT. REF. IND.
AGC #1 VOLT.
PLL 1 LOCK IND.
AGC #2 VOLT.
ALC VOLT.
INTERLOCK
SERIAL CLOCK
SERIAL DATA
SER. LOGIC ENAB.
SYSTEM +12V DC CIRCUIT 5
SYSTEM -12V DC CIRCUIT 1
SYS SERIAL +
SYS SERIAL -
EXT. 10MHz INPUT
UC RF OUTPUT
SYSTEM 10MHz OUTPUT
MCXO 10MHz INPUT
RF IN
SMA
ALT
INT.
10MHz
EXT.
10MHz SEL
YELLOW INT. REF. IND
AUR PWR
Input Fault
PLL 1 FAULT
PLL 2 FAULT
AGC OVERRIDE
AGC OVERRIDE VOLTAGE
AGC VOLTAGE IN
Input Flt
PLL1 FLT
PLL2 FLT
AGC CTRL
AGC OUT
AGC IN
POT DQ
POT CLK
POT RST
PLL MUTE
10M_MUTE
10M_MUTE_B
AGC_MTR
IPFLT
HI-OVERDRIVE
NOT USED
NOTE:
1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.
ADD C65 - C67, Q17 - Q25, R103, R105 - R116 & U17. DEL. C55, Q7, R5, R29, R36 & U7. C5 WAS .001, R36 WAS 1K, TP1 - TP4 WERE 1S9082/80SMT. JKF
C1 20112698 6/22/07 DB
R5 WAS 51 OHMS. CR
D0 20112314 10/30/06 DB
CHANGED C26 FROM .01 TO .1, C59 FROM 47 TO NOT USED, R15 FROM 470K TO 2.2M, R22 FROM 2.2K TO 2.7K, R23 FROM 10K TO 470K, R24 FROM 56K TO 1M & R35 FROM 470 TO 1K. JKF
C0 20111572 11/8/04 DB
ADD C59-C64, L15, Q16, R90-R104, TP2-TP4 & U16. DEL. J14, J15, R52, R62 & R82. C42, C44 & C47 WERE 10uF. CR6 WAS 1N914, R22 WAS 1K, R84 WAS NOT USED, R85 WAS 0. C9 & Q14 WERE 2-81001-0015 JKF
B0 20111536 10/8/04 DB
Aucera
REV ECO DATE APV
THIS DRAWING IS THE PROPERTY OF AUCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION
MATERIAL
FINISH
DRN JKF 9/7/04
CHK DB 9/9/04
REL DB 9/9/04
TITLE SCH., UPCONVERTER CONTROL BOARD (1304760)
DWG. NO. 1304761
REV E0
SCALE NONE
SHEET 1 OF 2


LAST USED REF
R117
SW1
D53
U17
C87
Q25
Y1
J16
W3
L15
CR10
S1
K1
TP4
FIRMWARE CONFIGURATION
SW1
BD08
U13
2-61100-4735
U14
2-61100-4735
U12
LM317MDT
U8
1302044
11VSB
U10
2-61100-4472
U11
1095823
SPST
MANUAL MICRO RESET
SERIAL PROGRAMMING PORT
1063095
TO First Conversion Bd
TO L-Band PLL BD
U16
1304097
U18
1304097
Sets U/C Config
Processor Operation
PROGRAMMING ENABLED
BANDSW
POT DQ
POT CLK
POT RST
AGC_MTR
AFC 1
AFC 2
PLL1 FLT
Input Flt
PLL2 FLT
PLL MUTE
10MHz
SERIALS
Axcera
SCH., UPCONVERTER CONTROL BOARD (1304760)
1304761
E0
2 OF 2



REV	ECO	DATE	APV

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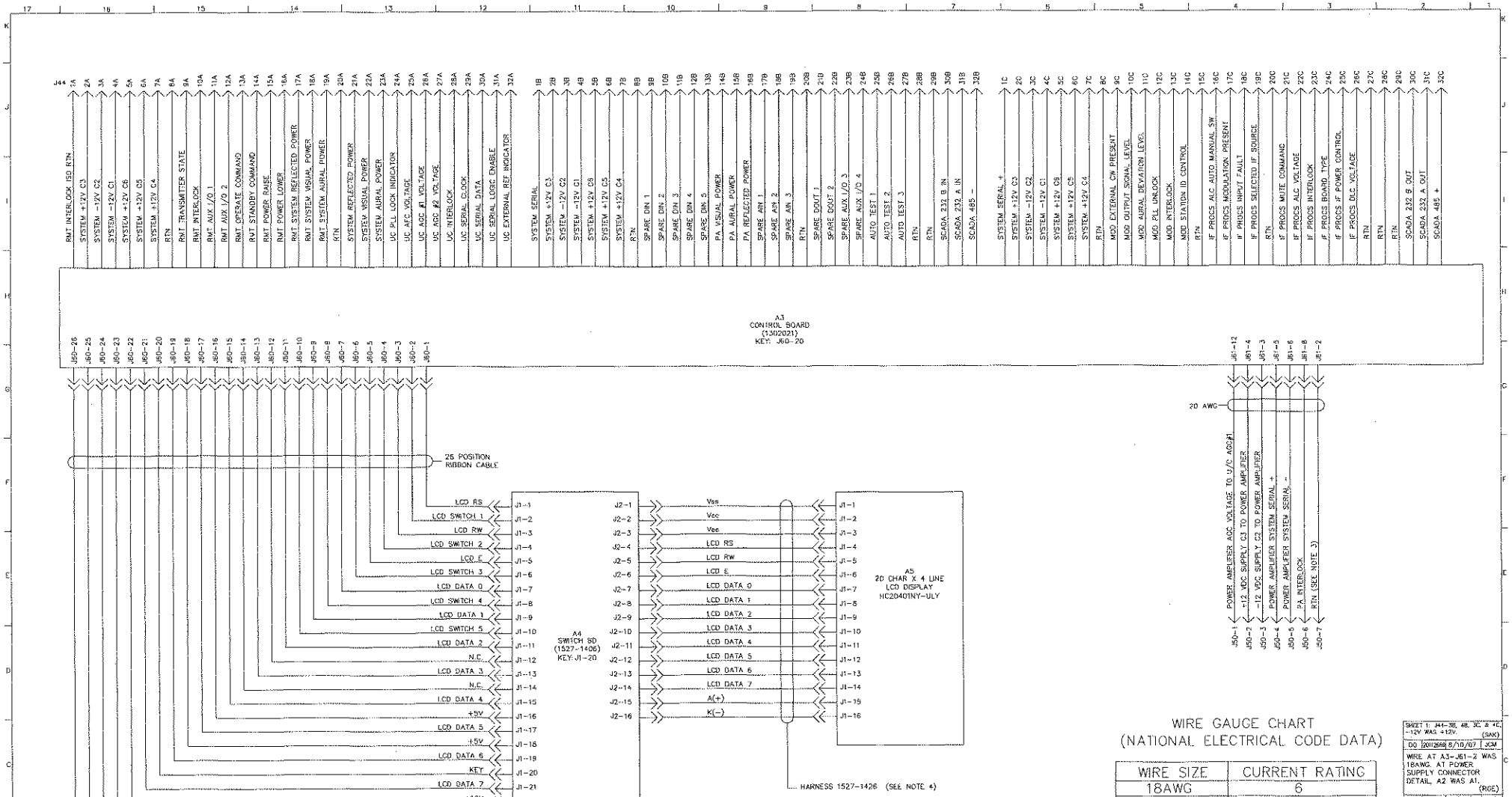
MATERIAL ——

FINISH ——

TITLE B/D, CONTROL/POWER SUPPLY ASSEMBLY, INNOVATOR LX

DWN	RGE	1/28/04	DWG. NO	REV
CHK	JCM	2/2/04	1303889	A0
REL	JCM	2/2/04	D SCALE ----	SHEET 1 OF 1



WIRE GAUGE CHART
(NATIONAL ELECTRICAL CODE DATA)

WIRE SIZE	CURRENT RATING
18AWG	6
16AWG	10
14AWG	20
12AWG	30

NOTES:
1) ALL SINGLE WIRE IS 18AWG UNLESS OTHERWISE NOTED.
2) VALUES FOR VR1, VR2 AND VR3 ARE PART OF VOLTAGE SELECTION KITS.
3) THIS CONNECTION MUST BE EQUIPPED WITH LONGER GROUND PIN (MAKE FIRST BREAK LAST).
4) CHANGE LABELING. "A2D-J1 TO A12-J2" BECOMES "A5-J1 TO A4-J2".

REV	ECO	DATE	APV

SHEET 1: J44-3B, 4B, 3C, & 4C, -12V WAS +12V. (SAK)
DO 20112668 8/10/07 JCM
WIRE AT A3-J61-2 WAS 18AWG. AT POWER SUPPLY CONNECTOR DETAIL A2 WAS A1. (RGE)
CC 20111260 02/27/04 LRT
ADDED NOTE 4. REVERESED A1-J2 AND A1-J3 AND REWIRED TO MAINTAIN THE SAME CONNECTIONS. (RGE)
BC 20113706 10/27/03 LRT

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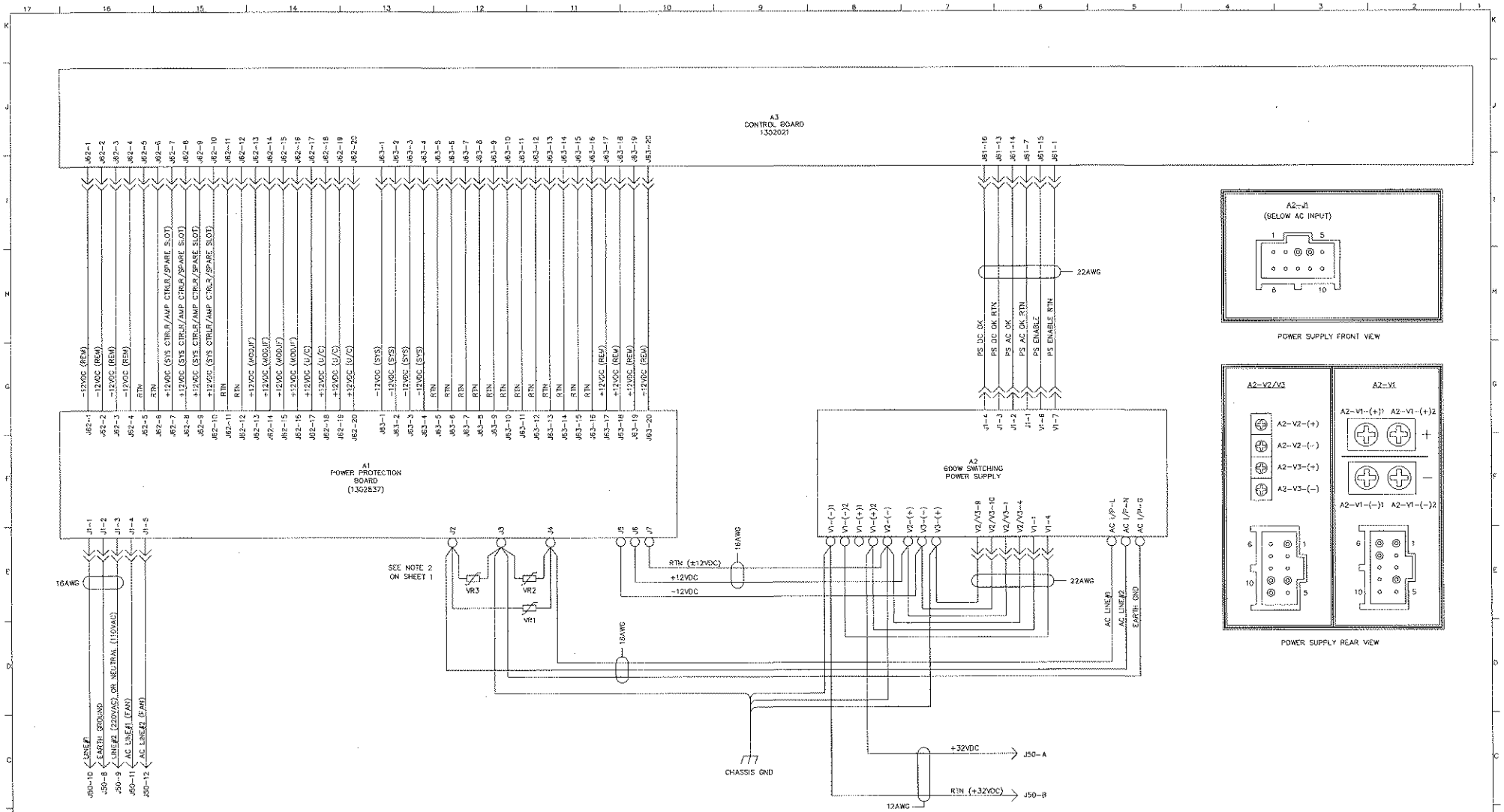
MATERIAL — — — —
FINISH — — — —

TITLE
I/C
CONTROL/POWER SUPPLY ASSEMBLY

DWN	MH	6/18/03	
CHK	JCM	8/27/03	
REL	JCM	9/27/03	

DWG. NO. 1302062 REV DO
D SCALE --- SHEET 1 OF 2



REV	ECO	DATE	APV

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MATERIAL - - - -

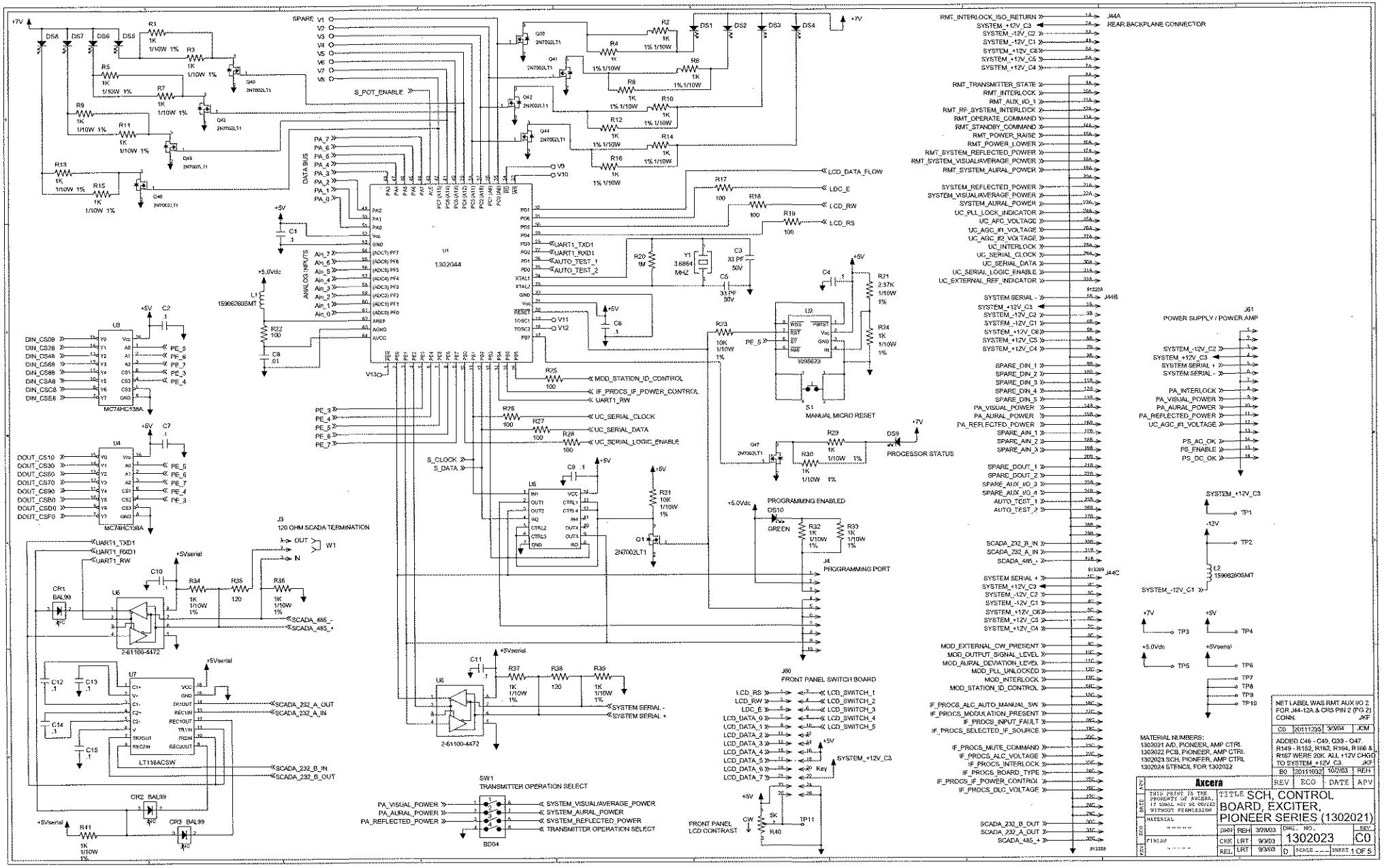
FINISH - - - -

TITLE I/C CONTROL/POWER SUPPLY ASSEMBLY

DWN	MH	6/18/03	
CHK	JCM	6/27/03	
REL	JCM	6/27/03	

DWG. NO. 1302062 REV. D0

D SCALE ~~~~ SHEET 2 OF 2


U1
1302044
J44A
REAR BACKPLANE CONNECTOR
J44B
J44C
J61
POWER SUPPLY / POWER AMP
J60
FRONT PANEL SWITCH BOARD
J4
PROGRAMMING PORT
J3
120 OHM SCADA TERMINATION
S1
MANUAL MICRO RESET
PROCESSOR STATUS
PROGRAMMING ENABLED
SW1
TRANSMITTER OPERATION SELECT
BD04
FRONT PANEL LCD CONTRAST
MC74HC138A
LT118ACSW
2-61100-4472
DATA BUS
ANALOG INPUTS
NET LABEL WAS RMT AUX I/O 2 FOR J44-12A & CR5 PIN 2 (FIG 2) CONN.
ADDED C46 - C49, C39 - C47. R149 - R152, R162, R164, R166 & R167 WERE 20K. ALL +12V CHGD TO SYSTEM +12V C3.
MATERIAL NUMBERS:
1302021 A/D, PIONEER, AMP CTRL
1302022 PCB, PIONEER, AMP CTRL
1302023 SCH, PIONEER, AMP CTRL
1302024 STENCIL FOR 1302022
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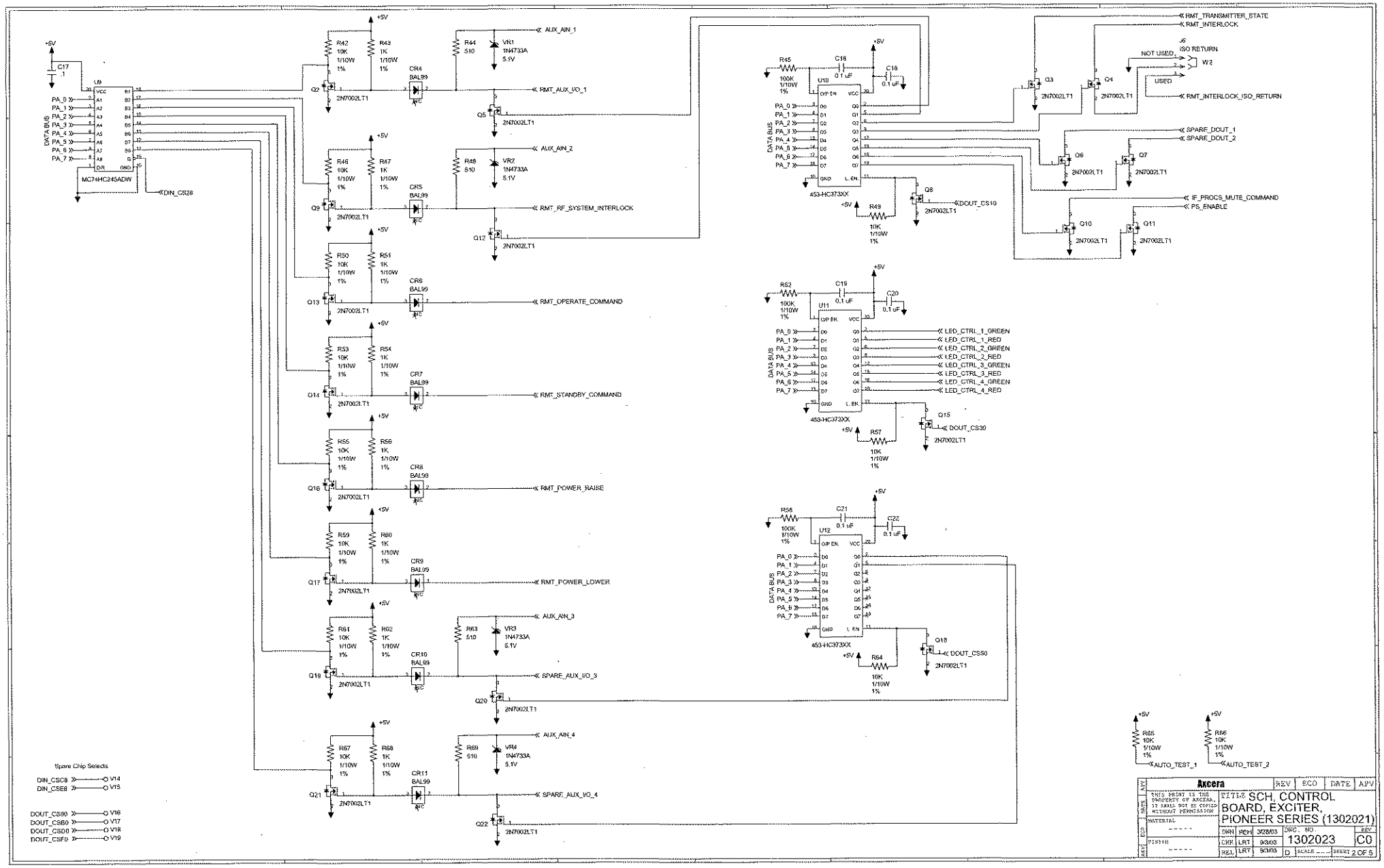
TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)
DWN REH 3/28/03
CHK LRT 9/3/03
REL LRT 9/3/03
DWG NO. 1302023
REV C0
SCALE ---
SHEET 1 OF 5


U9
MC74HC245ADW
DIN_CS26
DATA BUS
PA_0
PA_1
PA_2
PA_3
PA_4
PA_5
PA_6
PA_7
+5V
C17
.1
AUX_AIN_1
AUX_AIN_2
AUX_AIN_3
AUX_AIN_4
RMT_AUX_I/O_1
RMT_RF_SYSTEM_INTERLOCK
RMT_OPERATE_COMMAND
RMT_STANDBY_COMMAND
RMT_POWER_RAISE
RMT_POWER_LOWER
SPARE_AUX_I/O_3
SPARE_AUX_I/O_4
2N7002LT1
BAL99
VR1 1N4733A 5.1V
VR2 1N4733A 5.1V
VR3 1N4733A 5.1V
VR4 1N4733A 5.1V
R44 510
R48 510
R63 510
R69 510
RMT_TRANSMITTER_STATE
RMT_INTERLOCK
J6
ISO RETURN
NOT USED
USED
W2
RMT_INTERLOCK_ISO_RETURN
SPARE_DOUT_1
SPARE_DOUT_2
IF_PROCS_MUTE_COMMAND
PS_ENABLE
U10
453-HC373XX
DOUT_CS19
U11
DOUT_CS30
U12
DOUT_CS50
LED_CTRL_1_GREEN
LED_CTRL_1_RED
LED_CTRL_2_GREEN
LED_CTRL_2_RED
LED_CTRL_3_GREEN
LED_CTRL_3_RED
LED_CTRL_4_GREEN
LED_CTRL_4_RED
AUTO_TEST_1
AUTO_TEST_2
Spare Chip Selects
DIN_CS28 V14
DIN_CS29 V15
DOUT_CS30 V16
DOUT_CS50 V17
DOUT_CS60 V18
DOUT_CS70 V19
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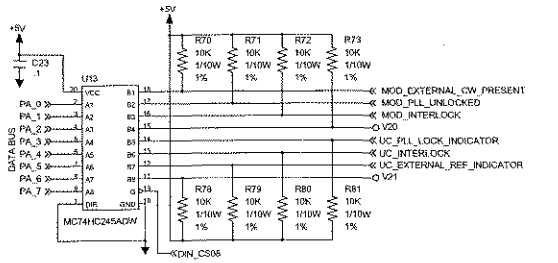
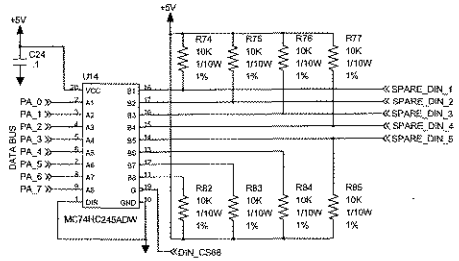
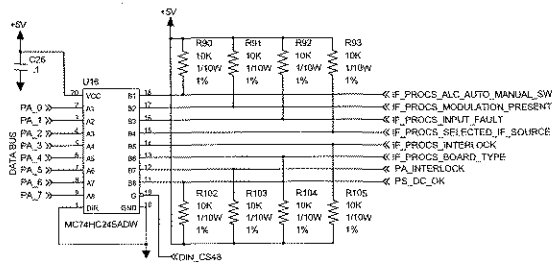
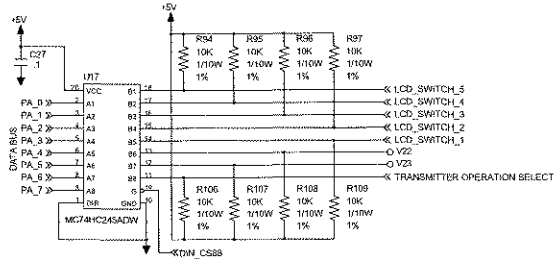
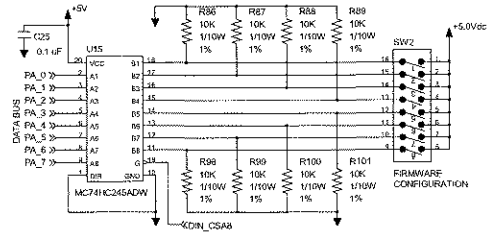
TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)
DWN REH 3/28/03
CHK LRT 9/3/03
APV LRT 9/3/03
DWG. NO. 1302023
REV C0
SCALE ---
SHEET 2 OF 5

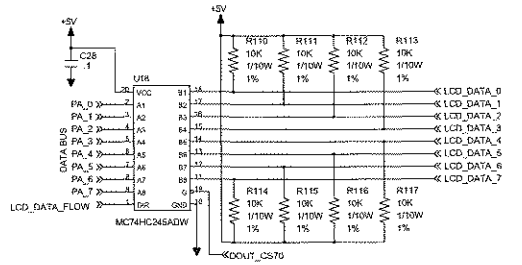




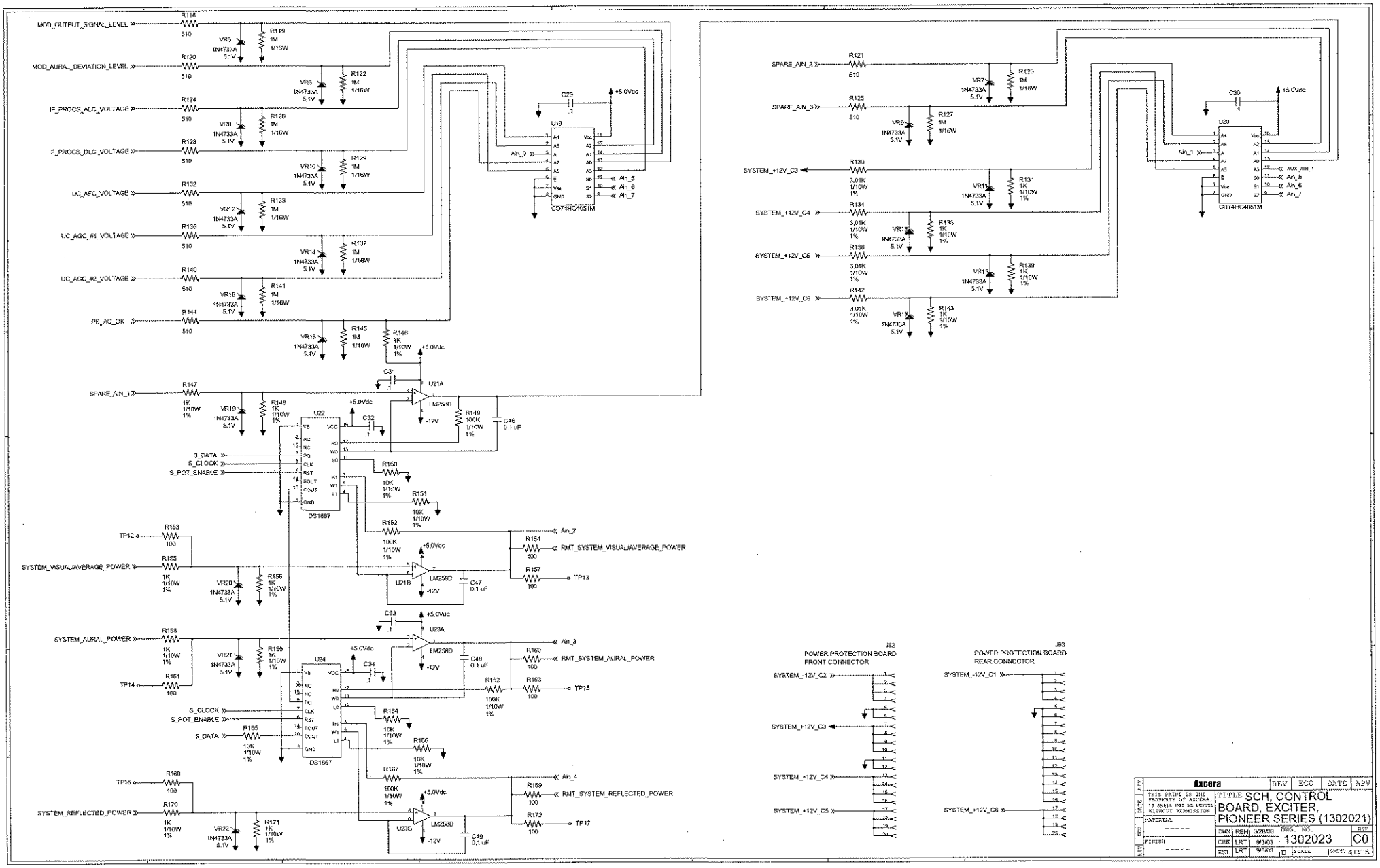


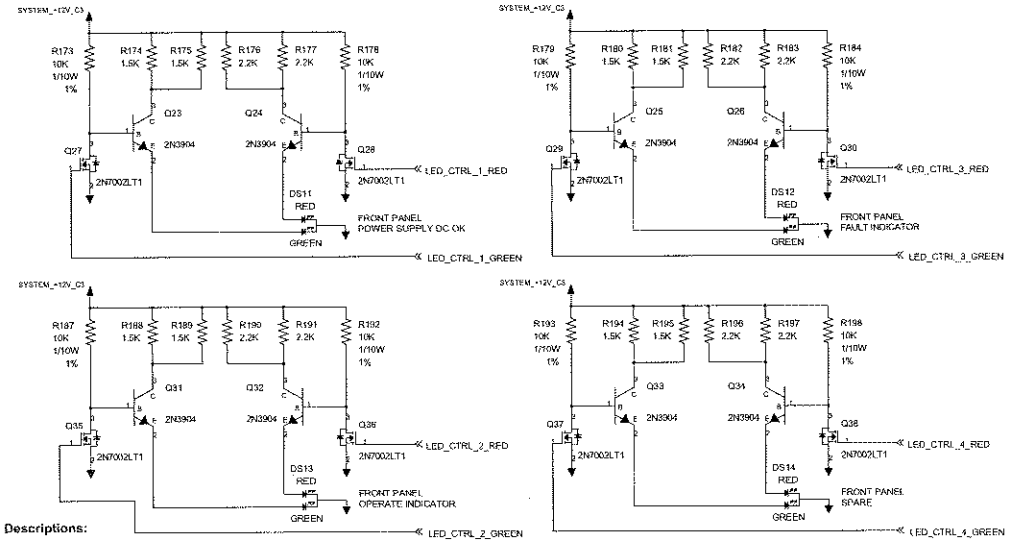


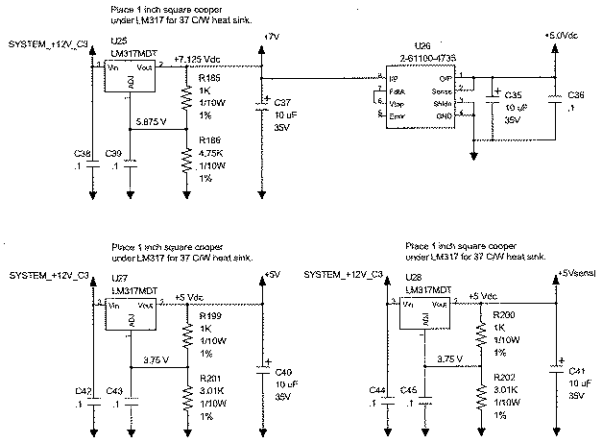




Axcera	REV	ECO	DATE	APV	
THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)				
MATERIAL	DWN RSH 3/28/03	DWG. NO. 1302023		REV C0	
FINISH	CHK LRT 9/3/03				
	SEL LRT 9/3/03	D	SCALE	SHEET 3 OF 5	


MOD_OUTPUT_SIGNAL_LEVEL
MOD_AURAL_DEVIATION_LEVEL
IF_PROCS_ALC_VOLTAGE
IF_PROCS_DLC_VOLTAGE
UC_AFC_VOLTAGE
UC_AGC_#1_VOLTAGE
UC_AGC_#2_VOLTAGE
PS_AC_OK
SPARE_AIN_1
SPARE_AIN_2
SPARE_AIN_3
SYSTEM_+12V_C3
SYSTEM_+12V_C4
SYSTEM_+12V_C5
SYSTEM_+12V_C6
SYSTEM_VISUALAVERAGE_POWER
SYSTEM_AURAL_POWER
SYSTEM_REFLECTED_POWER
S_DATA
S_CLOCK
S_POT_ENABLE
RMT_SYSTEM_VISUALAVERAGE_POWER
RMT_SYSTEM_AURAL_POWER
RMT_SYSTEM_REFLECTED_POWER
AUX_AIN_1
+5.0Vdc
-12V
CD74HC4051M
LM258D
DS1667
J62
POWER PROTECTION BOARD
FRONT CONNECTOR
J63
POWER PROTECTION BOARD
REAR CONNECTOR
Axcera
TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)
DWG. NO. 1302023
REV C0
SHEET 4 OF 5





LAST USED REF.

R202
C49
Q47
DS14
U28
VR22
J63
TP17
V23
SW2
CR11
W2
Y1
L2
S1

Circuit Descriptions:

PAGE 1:

U1 is an Atmel Atmega128 microcontroller. This part is in-circuit programmed using the serial programming port. When the microcontroller is held in reset by either the programming port or the external watchdog IC, a transistor inverts the reset signal while serial programming lines are connected to U1 through analog switch U5.

U2 is a watchdog IC used to hold the microcontroller in reset if the supply voltage is less than 4.21 Vdc; (1.25 Vdc < Pin 4 (IN) < Pin 2 (Vcc)). The watchdog momentarily resets the microcontroller if Pin 6 (IST) is not clocked every second. A manual reset switch is provided but should not be needed.

Diodes DS1 through DS8 are used for display of auto test results. A test board is used to execute self test routines. When the test board is installed, Auto_Test_1 is held low and Auto_Test_2 is allowed to float at 5 Vdc. This is the signal to start the auto test routines.

U3 and U4 are used to selectively enable various input and output ICs found on page 2 and 3 of the schematic.

U1 has two serial ports available. In this application, one port is used to communicate with transmitter system components where U1 is the master of a RS-485 serial bus. The other serial port is used to provide serial data I/O where U1 is not the master of the data port. A dual RS-232 port driver IC and a RS-485 port driver is also in the second serial data I/O system. The serial ports are wired such that serial data input can come through one of the three serial port channels. Data output is sent out through each of the three serial port channels.

Switch SW1 is used to select either transmitter operation or exciter driver operation. When the switches of SW1 are on, transmitter operation is selected and the power monitoring lines of the transmitter's power amplifier are routed to the system power monitoring lines.

PAGE 2:

Digital output latches are used to control system devices. Remote output circuits are implemented using open drain FETs with greater than 60 Volt drain to source voltage ratings.

Remote digital inputs are diode protected with a 1 Kohm pull-up resistor to 5Vdc. If the remote input voltage is greater than about 2 volts or floating, a FET is turned on and a logic low is applied to the digital input buffer. If the remote input voltage is less than the turn on threshold of the FET (about 2 Vdc), a logic high is applied to the digital input buffer.

Four of the circuits on page two are auxiliary I/O connections wired for future use. They are wired similar to the remote digital inputs but include a FET for digital output operation. To operate these signals as an input, the associated output FET must be turned off. These circuits are also connected to an analog input multiplexer IC.

PAGE 3:

Several ICs are used as input buffers to allow the microcontroller to monitor various digital input values. Most digital inputs use a 10 Kohm pull-up resistor. The buffer IC used for data transfer to the display is wired for read and write control.

PAGE 4:

Each analog input is expected to be between 0 and 5 Vdc. If a signal exceeds 5.1 Vdc, a 0.225 Watt zener diode clamps the signals voltage. Most signals are calibrated at their source however two dual serial potentiometer ICs are used to calibrate four signals. For these four circuits, the input value is divided in half before it is applied to an op-amp. The serial potentiometer is used to adjust the input signal between 80 and 120% of the input signal. Serial data to the second serial potentiometer is transferred through the first IC. The wiper position of the digital potentiometer circuit is used to set the gain of the op-amp. Lower digital values for the wiper setting increases the gain of the op-amp. If N= 0, gain = 6.0. If N = 255, gain = 3.00. If Vin = 1.0 at spare_Ain_1 and N = 128, U21A out = 4.0V with gain = 4.

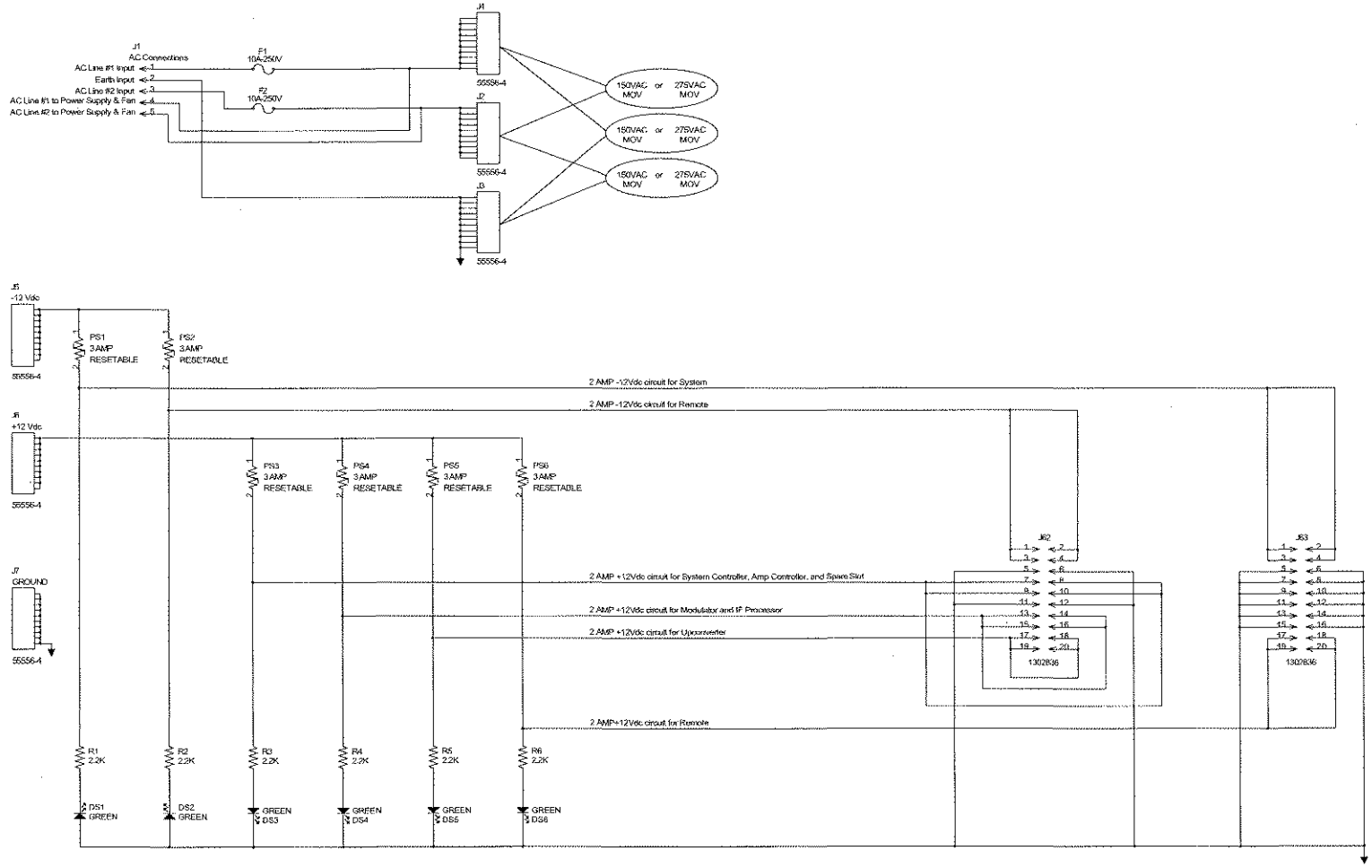
Two 20 position connectors are used to provide power to the backplane. J62 and J63 get power from the power supply after a nominal 3 amp resettable fuse. The Raychem polyswitch resettable fuses may open on a current as low as 2.43 amps at 50C, 3 amps at 25 C or 3.3 amps at 0C. They definately will open when the current is 4.86 amps at 50C, 6 amps at 20C, or 6.6 amps at 0C. Trace widths of these circuits are 0.140" (designed for maximum current).

PAGE 5:

Each of the four LED circuits drive a dual element common cathode LED. To make a good amber color, the current applied to the green element is slightly greater than the red element.

Several voltage regulators are used to power the board. Seven volts is typically applied to board LEDs and to the input of a precision 5.0 volt regulator. The 5.0 volt regulator is used for analog circuits and the microcontroller analog reference voltage. Another two 5 volt regulator circuits are used for most other board circuits.

Axcera		REV	ECO	DATE	APV
THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)				
MATERIAL -----	DWN REH 3/28/03	DWG. NO. 1302023			REV. C0
FINISH -----	CHK LRT 9/3/03				
	APV LRT 9/3/03	D	SCALE ----	SHEET 5 OF 5	



Circuit Design Notes:

1. Track widths of 0.140 inch minimum top and bottom of board shall be used to connections to J1, J2, J3, J4.
2. Track widths of 0.140 inch minimum top of board shall be used to connections to J5 and J6.
3. Track widths of 0.066 inch minimum shall be used to connections to J62 and J63.
4. Track widths of 0.020 inch minimum shall be used to connections between LEDs and resistors.
5. Board BOM needs the following items added to those exported from Orcad:

Part Number	Qty	Description
102071	4	Fuse Clip, PC BD Mnt., 15 Amp

MATERIAL NUMBERS:
1302837 PIONEER, POWER PROTECTION
1302838 PCB, PIONEER, PWR PROTECT
1302839 SCH, PIONEER, PWR PROTECT
1302840 STENCIL FOR 1302838

Axcera		REV	ECO	DATE	APV
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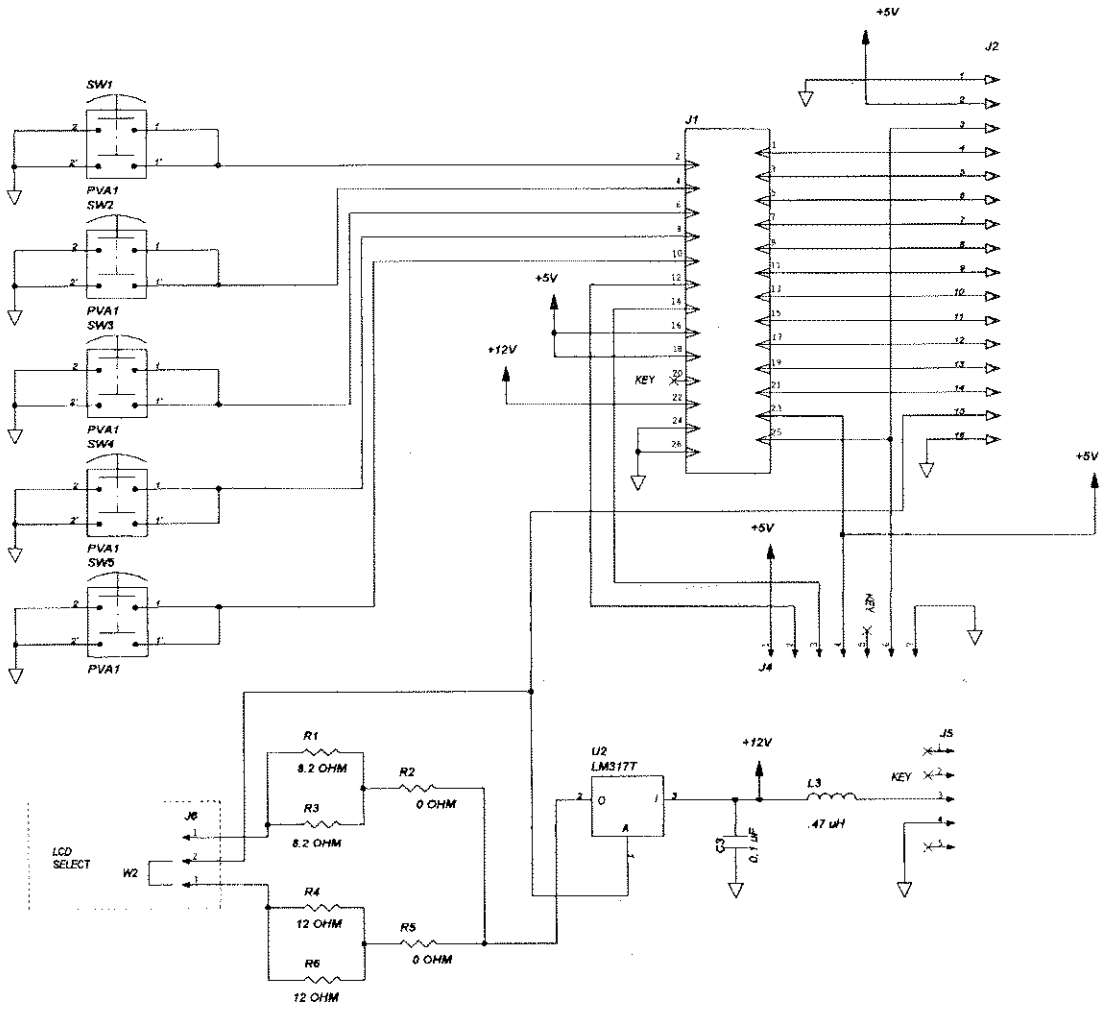
MATERIAL -----	DWN REH 5/29/03	DWG. NO. 1302839			REV AO
FINISH -----	CHK RTS 5/29/03				
	REL REH 5/29/03	D	SCALE ---	SHEET 1 OF 1	



DELETED C1, C2, L1, L2, U1, J3, & W1. MOVED W2 FROM J6-1,-2 TO J6 -2,-3.			JKF
3	8603	11/7/96	
AT J2 W2 WAS W1. (TMY)			
2	8424	9/29/96	JCM
SWITCHED PINS 1 & 2 OF U2.		(TMY)	
1	8368	8/27/96	RAS
REV	ECN	DATE	APV

ITS CORPORATION

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MATERIAL ---------

FINISH ---------

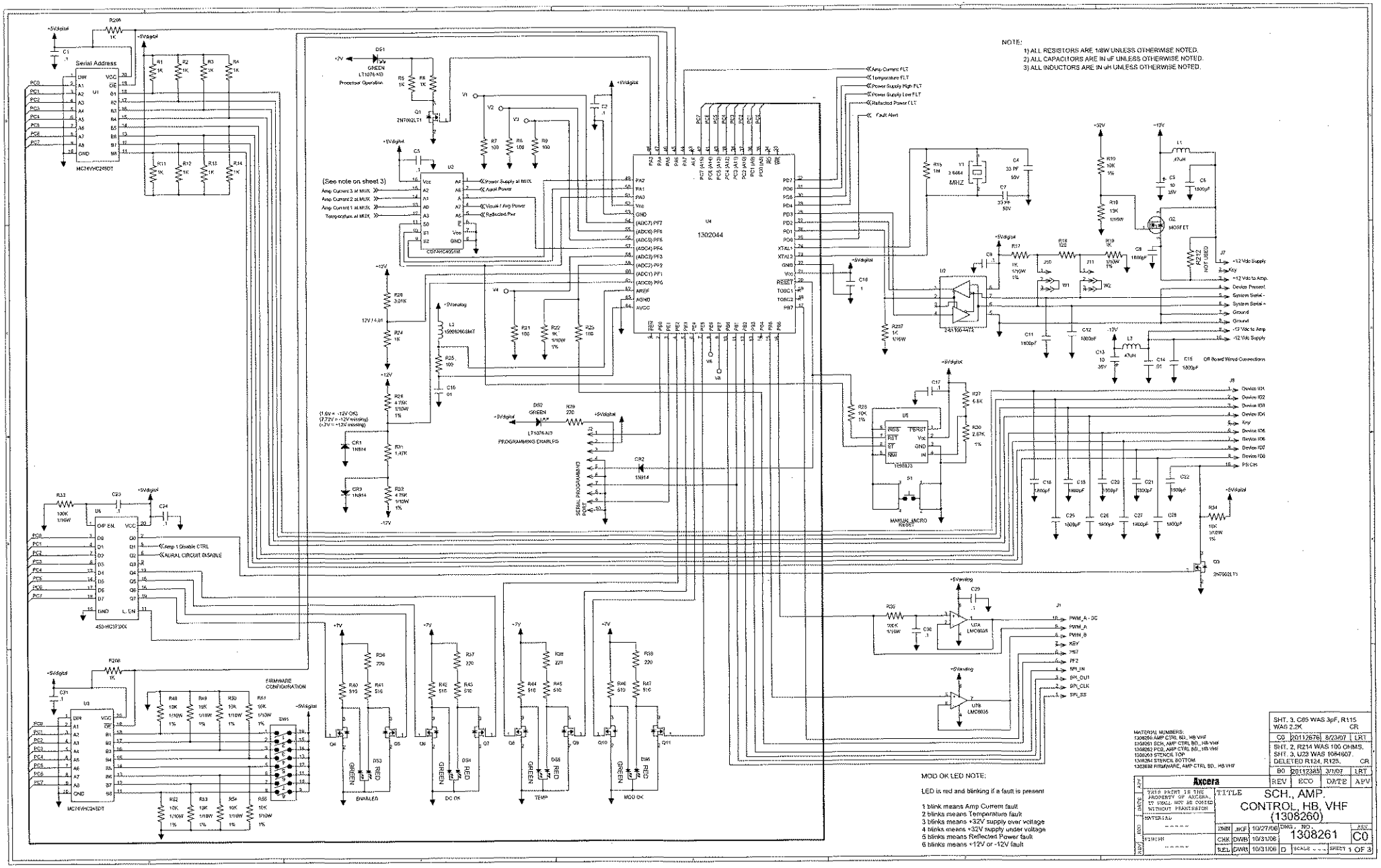
TITLE SCHEMATIC SWITCH BOARD (1527-1406)

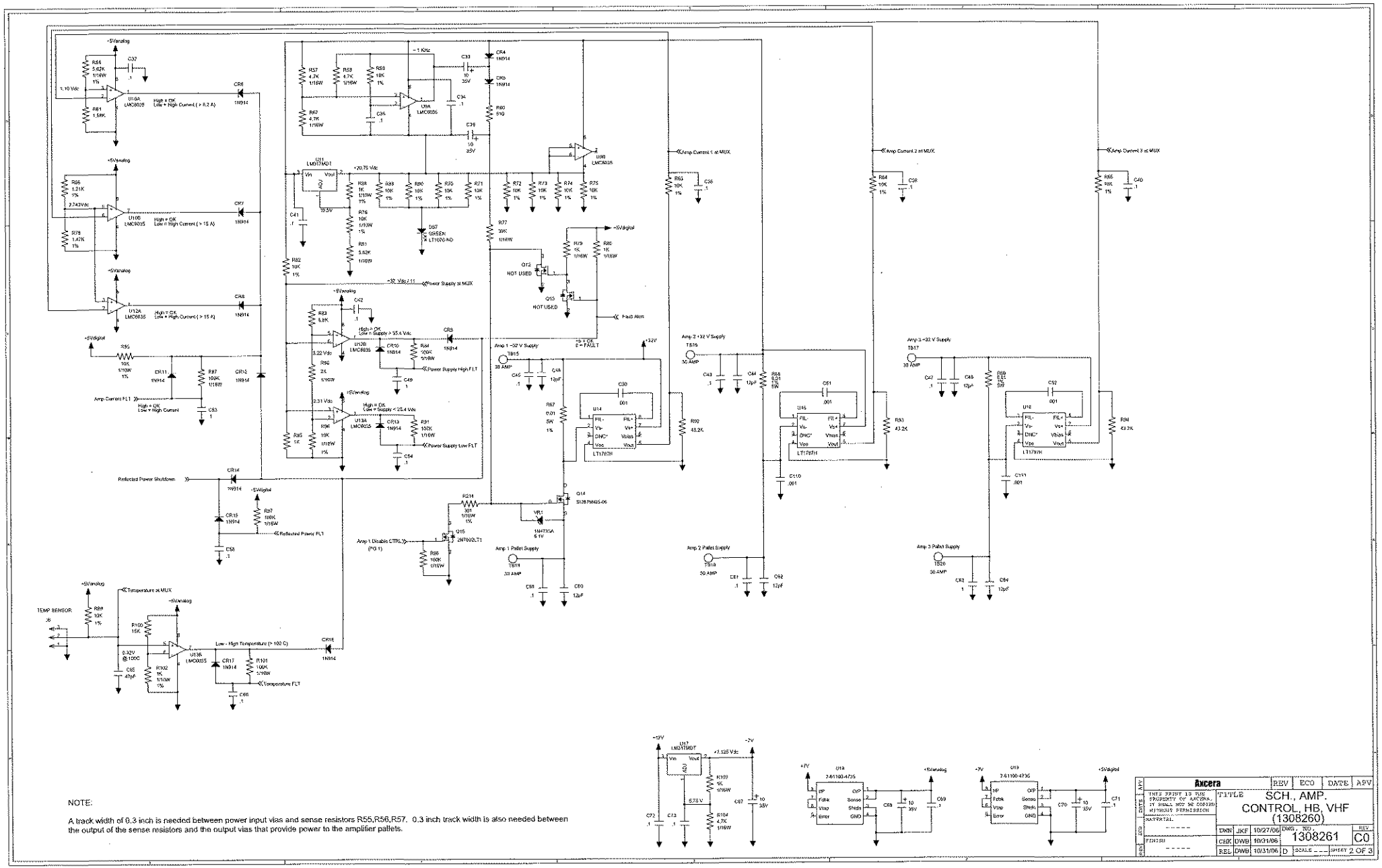
DWN	DLM	6/3/96
CHK	RAS	6/14/96
REL	RAS	6/14/96

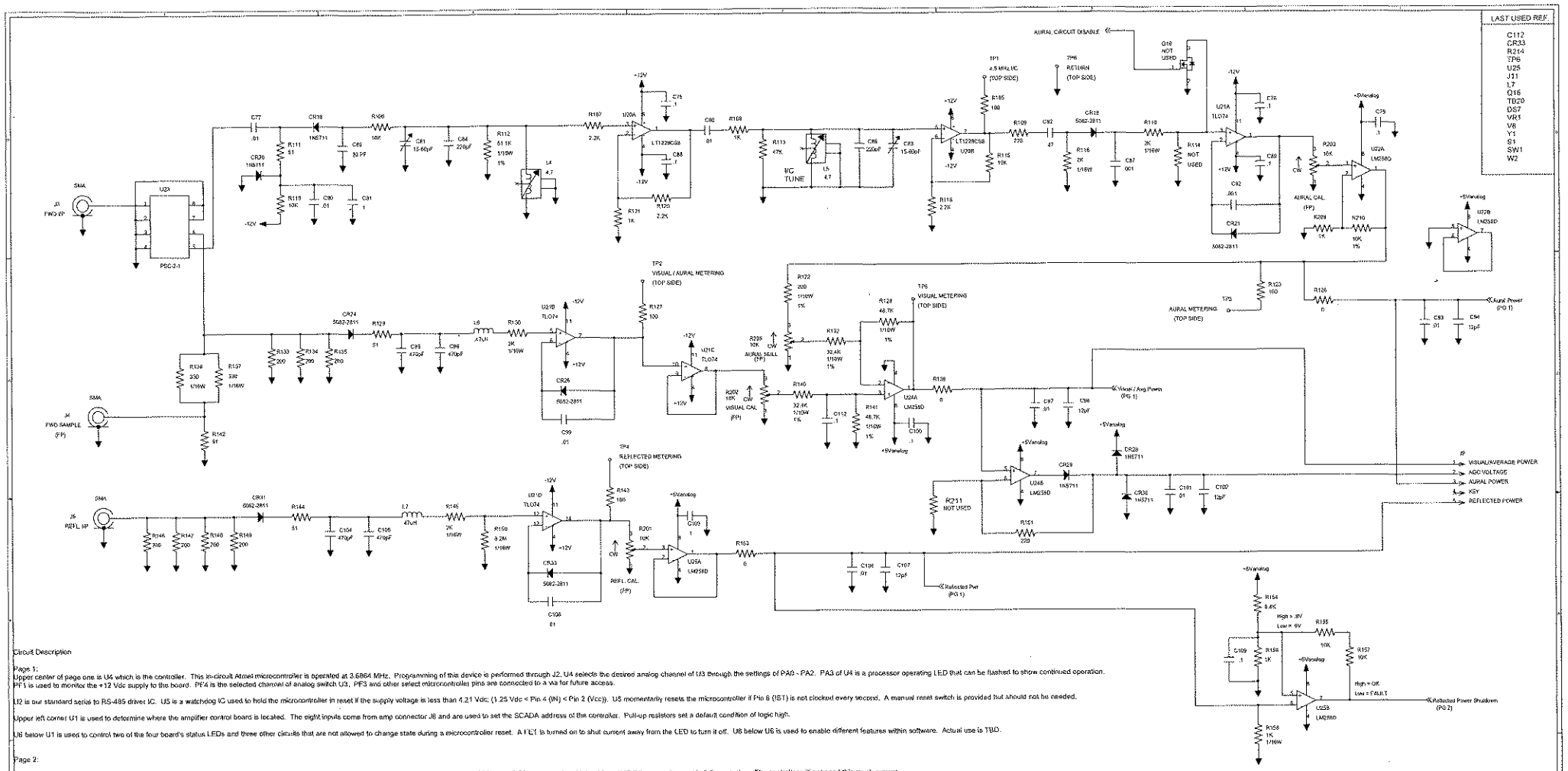
DWG. NO. 1527-3406 REV 3

B SCALE — SHEET 1 OF 1

APV DATE ECN REV


NOTE:
1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.
Serial Address
MC74VHC245DT
CD74HC4051M
1302044
(See note on sheet 3)
Amp Current 3 at MUX
Amp Current 2 at MUX
Amp Current 1 at MUX
Temperature at MUX
Power Supply at MUX
Audit Power
Visual / Amp Power
Reflected Pwr
Amp Current FLT
Temperature FLT
Power Supply High FLT
Power Supply Low FLT
Reflected Power FLT
Fault Alert
Processor Operation
PROGRAMMING ENABLED
SERIAL PROGRAMMING PORT
MANUAL MICRO RESET
Amp 1 Disable CTRL
AURAL CIRCUIT DISABLE
FIRMWARE CONFIGURATION
ENABLED
DC OK
TEMP
MOD OK
Off Board Wired Connections
MOD OK LED NOTE:
LED is red and blinking if a fault is present
1 blink means Amp Current fault
2 blinks means Temperature fault
3 blinks means +32V supply over voltage
4 blinks means +32V supply under voltage
5 blinks means Reflected Power fault
6 blinks means +12V or -12V fault
MATERIAL NUMBERS:
1308260 AMP CTRL BD., HB VHF
1308261 SCH., AMP CTRL BD., HB VHF
1308262 PCB, AMP CTRL BD., HB VHF
1308263 STENCIL TOP
1308264 STENCIL BOTTOM
1303838 FIRMWARE, AMP CTRL BD., HB VHF
SHT. 3, C85 WAS 3pF, R115 WAS 2.2K CR
C0 20112676 8/23/07 LRT
SHT. 2, R214 WAS 100 OHMS. SHT. 3, U23 WAS 10R4607. DELETED R124, R125. CR
B0 20112365 3/1/07 LRT
Axcera
TITLE
SCH., AMP. CONTROL, HB, VHF (1308260)
DRWN JKF 10/27/06
CHK DWB 10/31/06
SEL DWB 10/31/06
DWG. NO. 1308261
REV C0
SCALE ---
SHEET 1 OF 3


Axcera
SCH., AMP. CONTROL, HB, VHF (1308260)
1308261
C0
2 OF 3
NOTE:
A track width of 0.3 inch is needed between power input vias and sense resistors R55,R56,R57. 0.3 inch track width is also needed between the output of the sense resistors and the output vias that provide power to the amplifier pallets.



Circuit Description

Page 1:

Upper center of page one is U4 which is the controller. This in-circuit Atmel microcontroller is operated at 3.6864 MHz. Programming of this device is performed through J2. U4 selects the desired analog channel of U3 through the settings of PA0 - PA2. PA3 of U4 is a processor operating LED that can be flashed to show continued operation. PF1 is used to monitor the +12 Vdc supply to the board. PF4 is the selected channel of analog switch U3. PF5 and other select microcontroller pins are connected to a via for future access.

U2 is our standard serial to RS-485 driver IC. U5 is a watchdog IC used to hold the microcontroller in reset if the supply voltage in less than 4.21 Vdc (1.25 Vdc < Pin 4 (IN) < Pin 2 (Vcc)). U5 momentarily resets the microcontroller if Pin 6 (IST) is not clocked every sec/ond. A manual reset switch is provided but should not be needed.

Upper left corner U1 is used to determine where the amplifier control board is located. The eight inputs come from amp connector J8 and are used to set the SCADA address of the controller. Pull-up resistors set a default condition of logic high.

U6 below U1 is used to control two of the four board's status LEDs and three other circuits that are not allowed to change state during a microcontroller reset. A FET is turned on to shut current away from the LED to turn it off. U8 below U6 is used to enable different features within software. Actual use is TBD.

Page 2:

In the lower right corner are voltage regulator circuits. U17 should allow for 0.14 amps of power using its 92 C/W rating if Ta = 60C max and Tj = 125C max. 0.26 amps can be obtained from U17 if the mounting pad is 0.5 sqr. inches. The controller will not need this much current.

U18 and U19 are low drop-out voltage regulators with a tolerance greater than or equal to 1%. 100 mA is available from each device but again the controller will not need this much current.

In the upper left section are circuits with U9 and U11. U11 is used to generate a regulated voltage that is about 5 Volts less than the +32 Volt supply. When the +32 Volt supply is enabled, the circuitry around U9A is used to provide gate voltage to Q14 that is 5 volts greater than the source pin of this FET. The gate of Q14 can be turned off by any one of a few different circuits. These circuits are wired through Q12 and Q13. At this time these transistors are not installed but they may be installed to increase the shut-down time on a detected fault. Without Q12 and Q13 installed, Q14 is only turned off by the microcontroller through Q16.

U10A is used to detect high current in amplifier #1. At 1.10 Vdc, the current to amplifier #1 should be about 6.20 Amps. U10B and U12A are used to detect a high current condition in amplifier stages #2 or #3. With a 2.74 Vdc reference, high current shut down should be about 15 Amps.

U12B is used to detect high power supply voltage. U13A is used to indicate that the power supply voltage is less than 26 volts.

U25B on page 3 is used to detect high reflected power. U13B determines if the power supply temperature gets too hot.

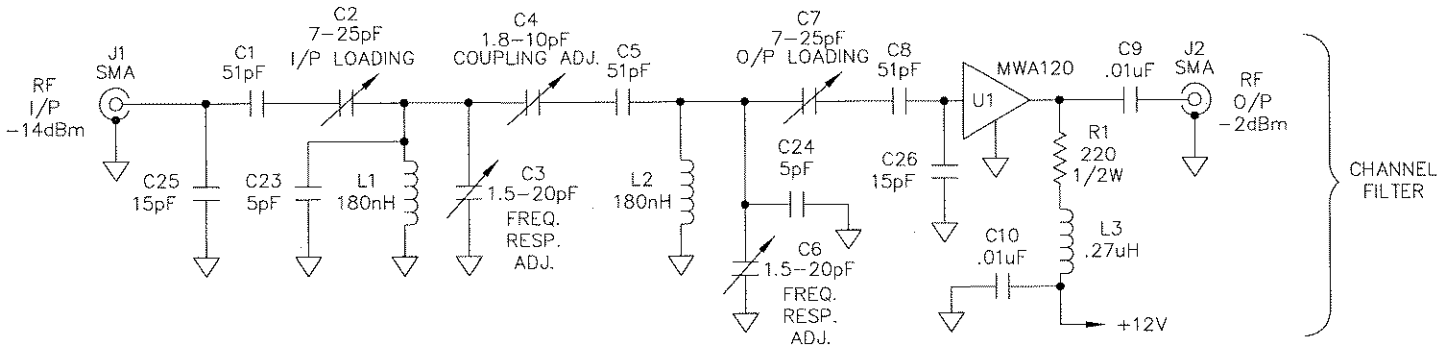
Current Monitoring Sections - A 0.01 ohm 1% 5 Watt thru-hole resistor is used for monitoring the current through several sections of the amplifier. The voltage developed across this resistor is amplified for current monitoring by U14, U15, or U16. The Linear Technology LT1787HVCS8 precision high side current sense amplifier accepts a maximum voltage of 60 Vdc. The 43.2 Kohm resistor from Pin 5 to ground sets the gain of the amplifier to about 17.28. This value is not set with much accuracy since the manufacture internal matches the resistors of this part but their actual resistance value is not closely defined. A trimming resistor is suggested to give a temperature stability of <200ppm/C but instead the microcontroller will determine the exact gain of the circuit and use a correction factor for measurements.

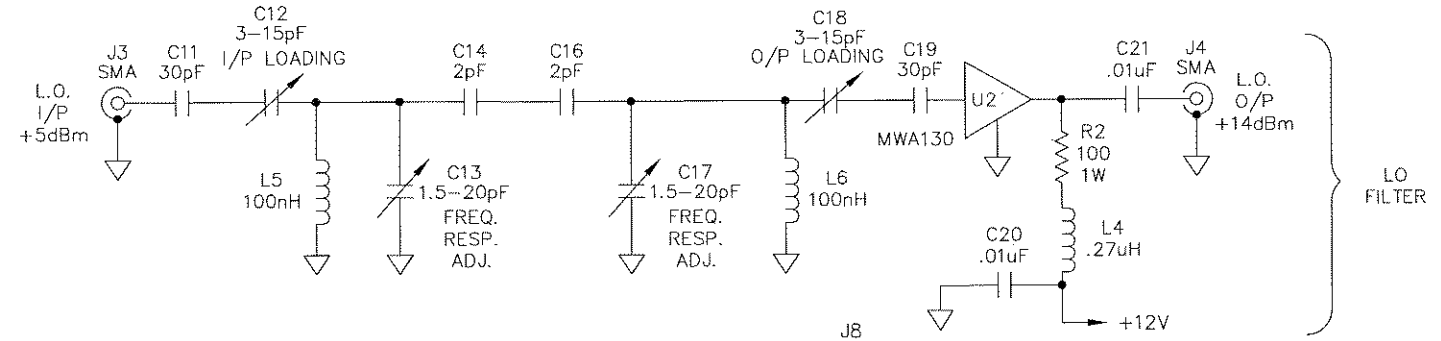
Page 3:

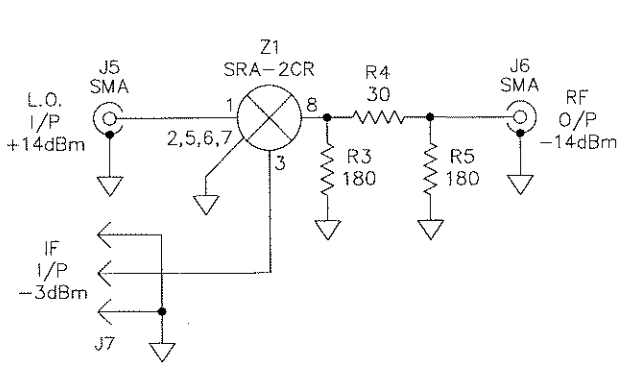
RF power detector circuits. Q16 is used by the microcontroller to disable the aural circuit of a digital transmitter or in external amplifiers where the amplifier is not to monitor visual power.

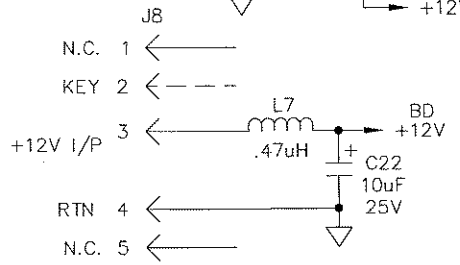
The Visual or Forward power circuit is calibrated and presented on the input of U24B pin 5. If this module has the highest detected forward power in a multi-amplifier system, it will have the highest forward power signal. This signal level into U24B pin 5 will be used to set the AGC output voltage of J9-2. If another amplifier has a higher forward power, the level into U24B pin 5 will be higher than pin5 and this amplifiers output signal will not be used to set the voltage level of J9-2.

APV	Axcera	REV	ECO	DATE	APV	
DATE	THIS DRAW IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH., AMP. CONTROL, HB, VHF (1308260)				
ECO	MATERIAL -----	DWN JKF 10/27/06	DWG. NO. 1308261		REV. C0	
	FINISH -----	CHK DWB 10/31/06				
NEXT		REL DWB 10/31/06	D	SCALE ----	SHEET 3 OF 3	









NOTE:
L1 & L2: 180nH = 7T
#18 .25" DIA.
L5 &L6: 100nH = 5T
#20 .25" DIA.
ALL RESISTOR VALUES ARE IN OHMS UNLESS OTHERWISE NOTED.

REV	ECO	DATE	APV
C4	WAS 1.5-6pF.SJM		RE
2	7472	3/29/94	
	ADDED MISC. LABELING		DD
1	2834	12/13/90	JCM

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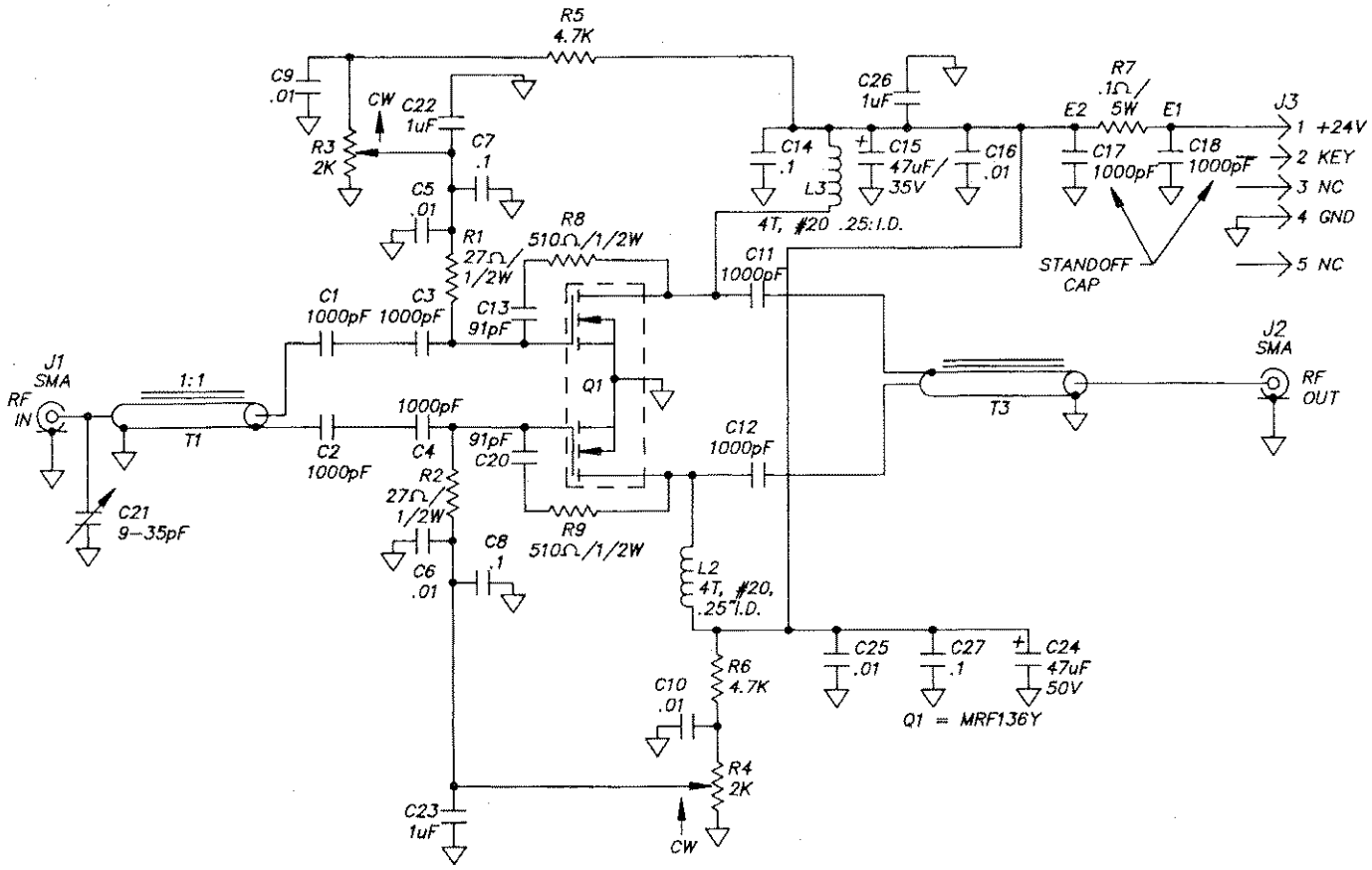
MATERIAL — — — —

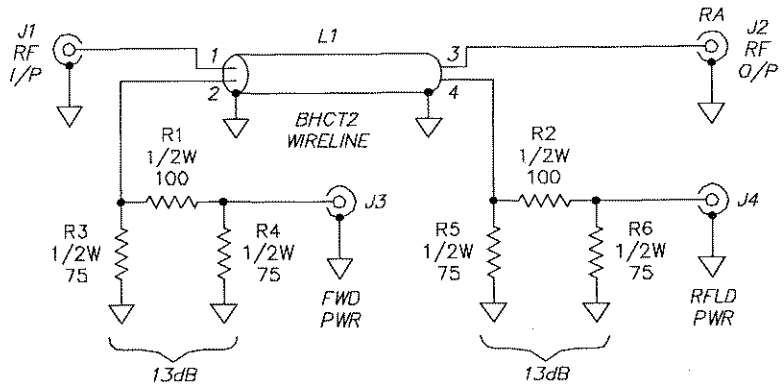
FINISH — — — —

TITLE SCHEMATIC — VHF FILTER/MIXER BOARD (1153-1101)

DWN	RLS	7/27/90	DWG. NO. 1153-3101	REV 2
CHK	JRA	7/31/90		
REL	JRA	8/2/90	B SCALE — —	SHEET 1 OF 1



ITS CORPORATION	REV	ECN	DATE	APV
THIS PRINT IS THE PROPERTY OF ITS CORP. IT SHALL NOT BE COPIED WITHOUT PERMISSION.	TITLE SCHEMATIC — LOW BAND VHF DRIVER BD. (1153-1107)			
MATERIAL -------	DWN BUD 8/1/90	DWG. NO. 1153-3107	REV 0	
FINISH -------	CHK DWB 8-3-90			
	REL DWB 8-3-90	B	SCALE ---	SHEET 1 OF 1



R1 & R2 WERE 1/4W, 16 OHMS. R3–R6 WERE 1/4W, 300 OHMS.			WB
A0	20112539	3/29/07	LRT
R3,R4,R5 AND R6 WERE 150. R1 AND R2 WERE 36.			SJM
1	7231	2/8/93	RE
REV	ECO	DATE	APV

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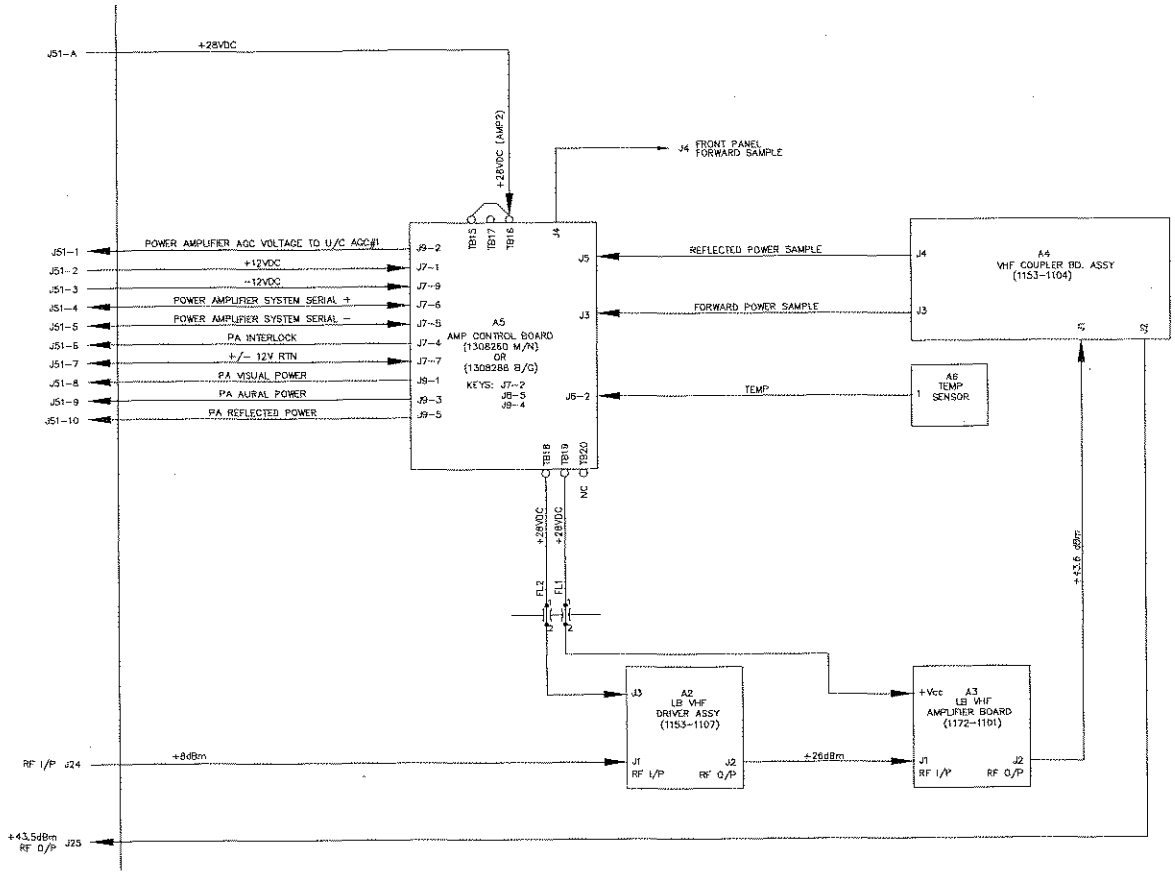
MATERIAL ----

FINISH ----

TITLE SCH, OUTPUT COUPLER BOARD, LOW BAND VHF

DWN	RLS	7/23/90	DWG. NO. 1153–3104	REV A0
CHK	KF	7/27/90		
REL	KF	7/30/90	B SCALE ---	SHEET 1 OF 1



NOTE:
1. ALL POWER LEVELS ARE PK-SYNC +10% AURAL. FOR DTV LEVELS, SUBTRACT 3dBm.

REV	ECO	DATE	APV
CO	2011264	7/10/07	LRT
B0	2011234	4/28/06	LRT

A5 WAS 1303682 M/N & 1304674 B/G. A4 WAS 1141-1002. CDD.

DELETED LOW PASS FILTER BOARDS BETWEEN A4 & A5.
A2 WAS 1307141.
ADDED A3. +28V WAS +30V. WB

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MATERIAL: ---

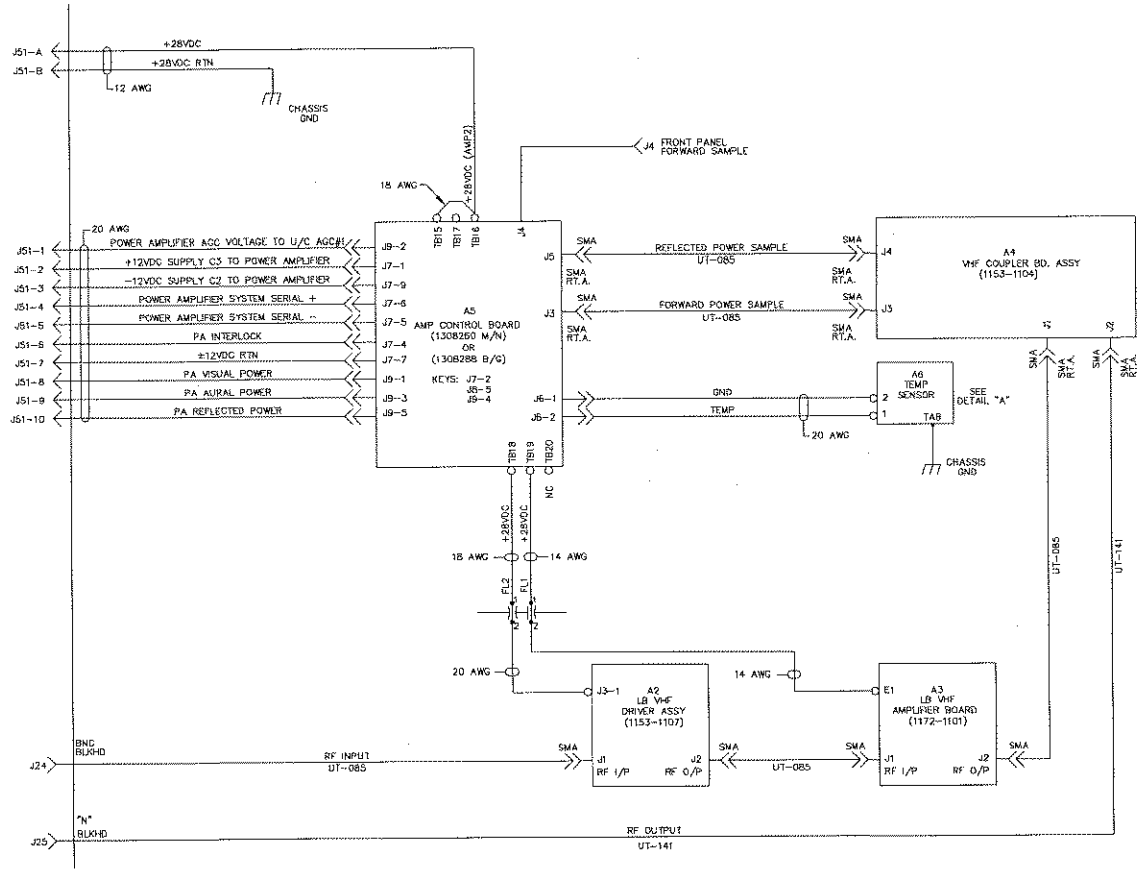
FINISH: ---

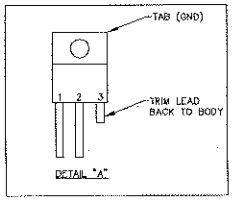
TITLE: B/D DRIVER ASSEMBLY 20W LB VHF

DWN	SAK	3/22/06	
CHK	LRT	3/28/06	
REL	LRT	3/28/06	

DWG. NO. 1307159 REV CO

D SCALE --- SHEET 1 OF 1





NOTE:
1. ALL WIRE IS 18AWG UNLESS OTHERWISE NOTED.

A5 WAS 1303682 M/N & 1304674 B/G. A4 WAS 1141-1002. CDD

REV	ECO	DATE	APV
C0	0010284	7/10/07	LRT
B0	0010213	4/26/06	LRT

DELETED LOW PASS FILTER BOARDS BETWEEN A4 & A5. A2 WAS 1307141. ADDED A3. +28V WAS +30V. WB

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MATERIAL

FINISH

TITLE I/C, DRIVER ASSEMBLY 20W LB VHF

DWN	SAK	03/22/06
CHK	LRT	3/28/06
REL	LRT	3/02/06

DWG. NO. 1307158 REV C0

SCALE SHEET 1 OF 1