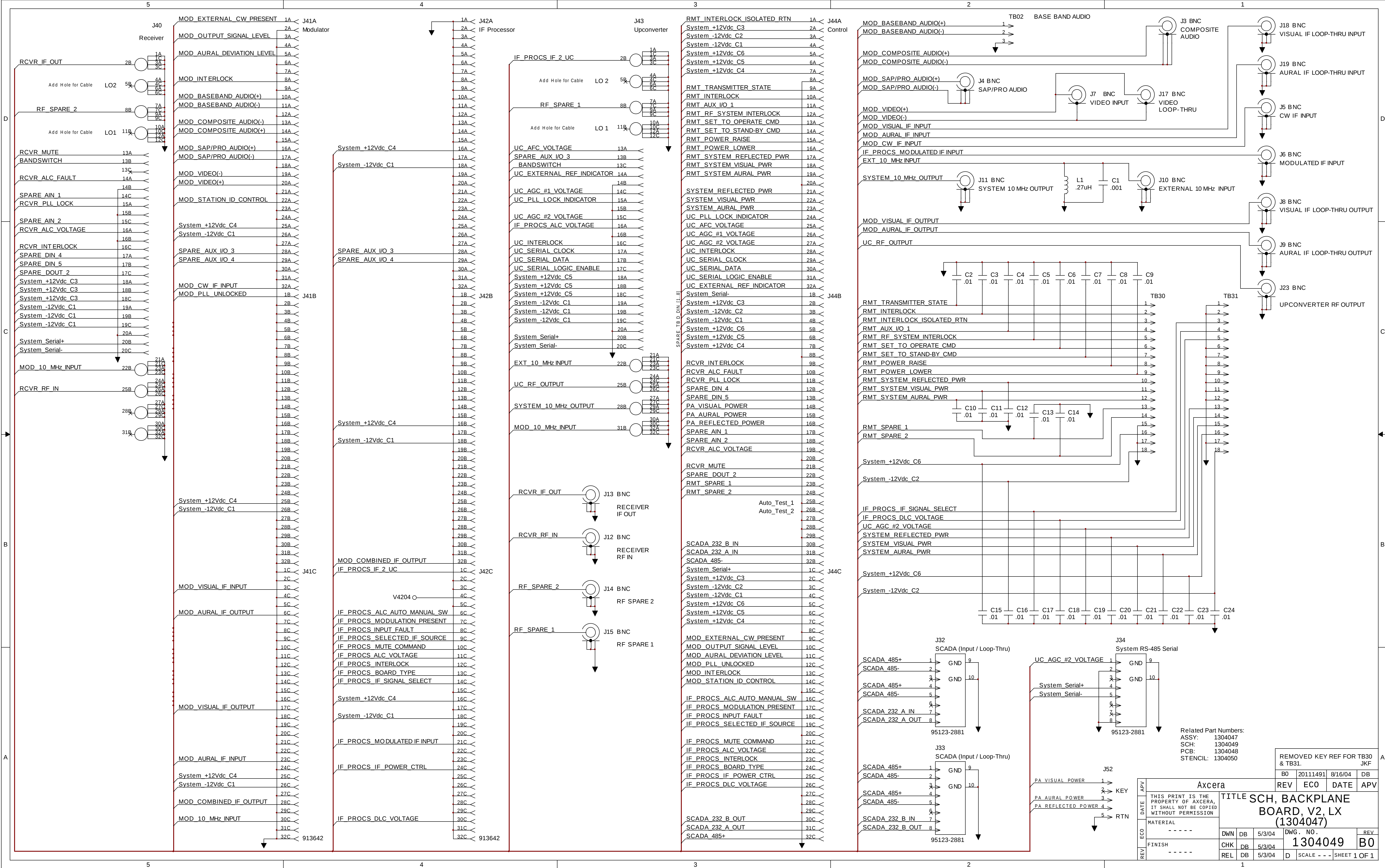
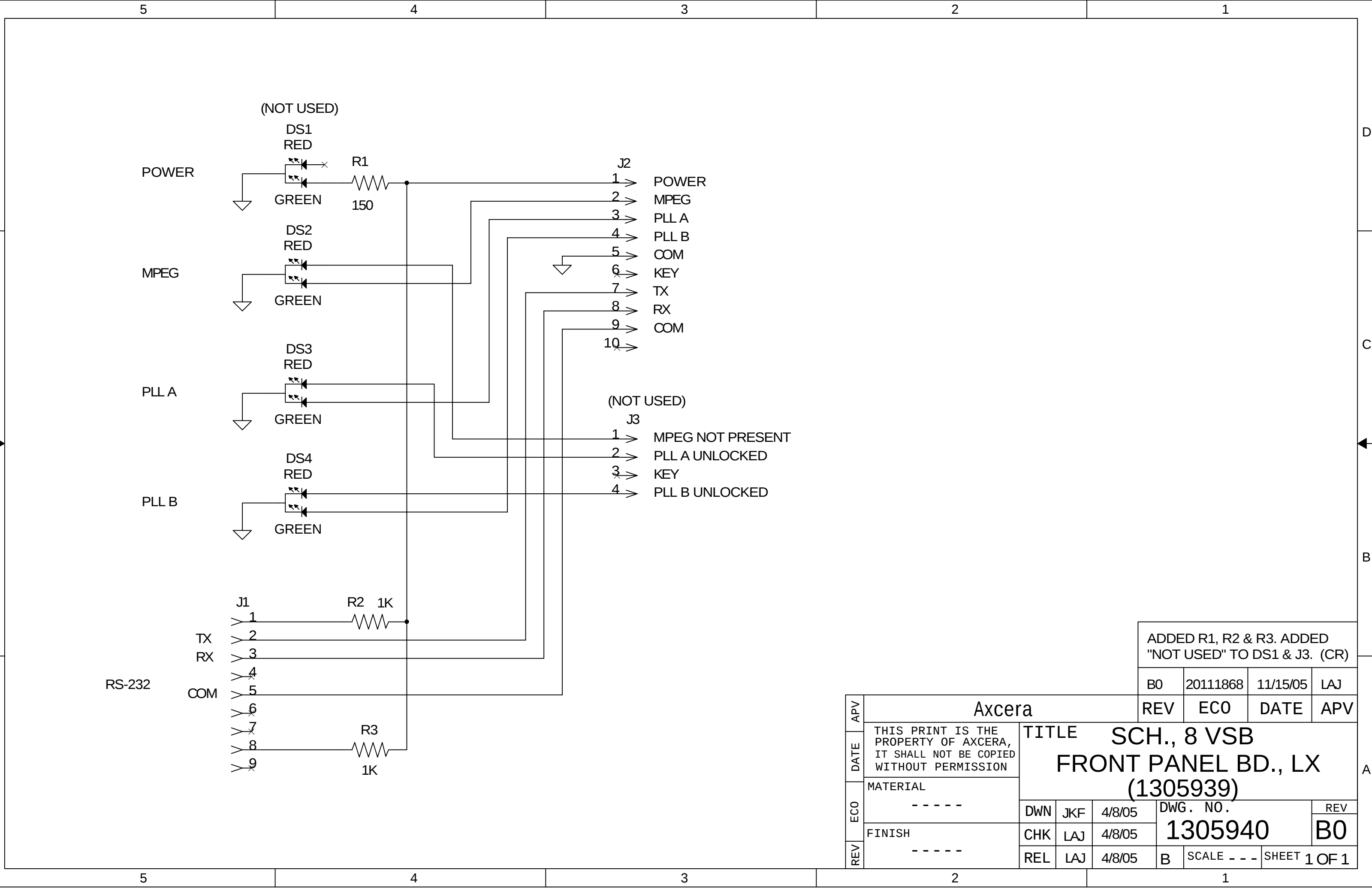




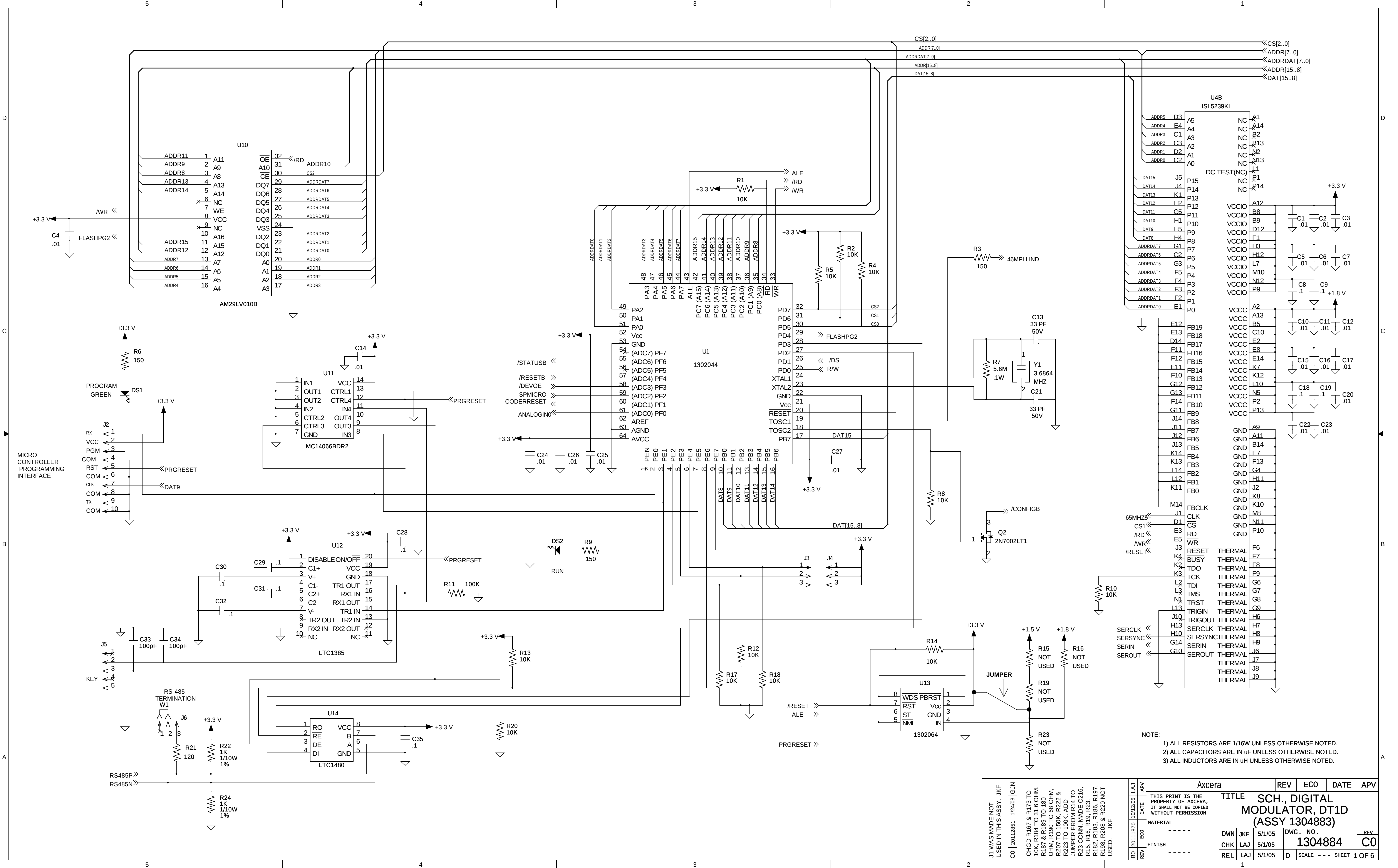


ADDED R1, R2 & R3. ADDED
"NOT USED" TO DS1 & J3. (CR)

B0	20111868	11/15/05	LAJ
----	----------	----------	-----

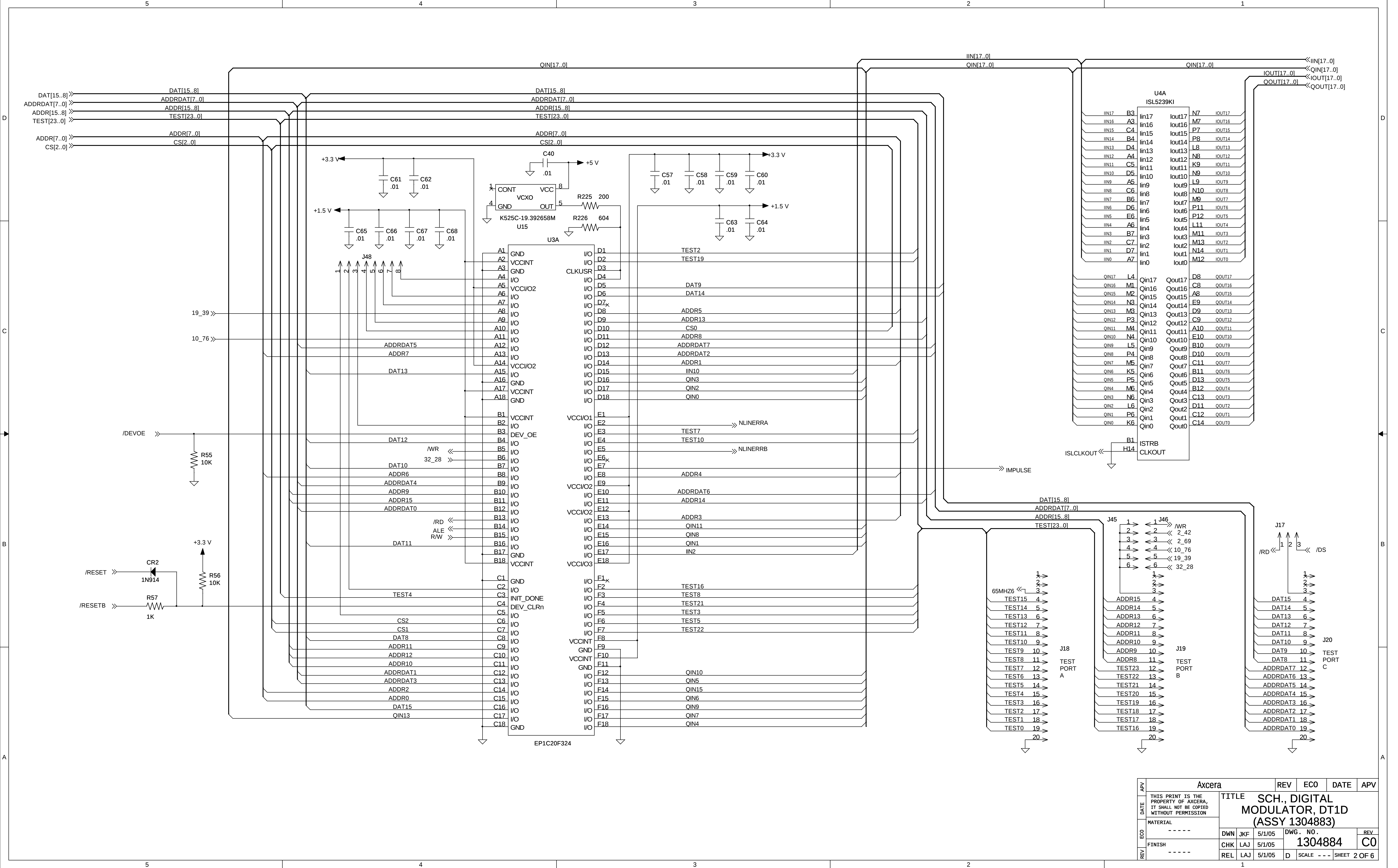
REV	ECO	DATE	APV
-----	-----	------	-----

APV	Axcera				REV	ECO		DATE		APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION		TITLE SCH., 8 VSB FRONT PANEL BD., LX (1305939)							
ECO	MATERIAL - - - - -		DWN	JKF	4/8/05	DWG. NO.			REV	
REV	FINISH - - - - -		CHK	LAJ	4/8/05	1305940			B0	
			REL	LAJ	4/8/05	B	SCALE - - -	SHEET 1 OF 1		

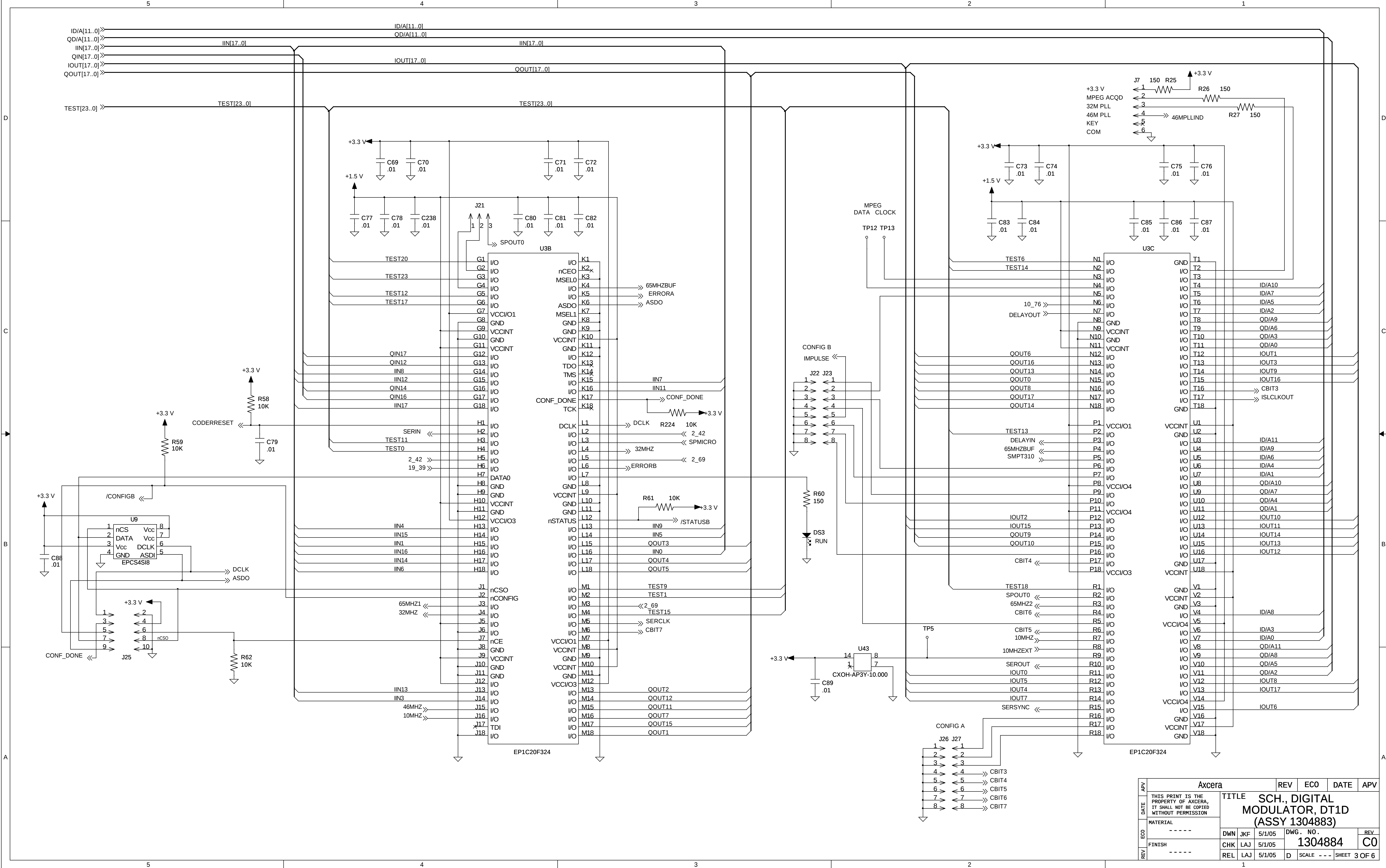


NOTE:
1) ALL RESISTORS ARE 1/16W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.

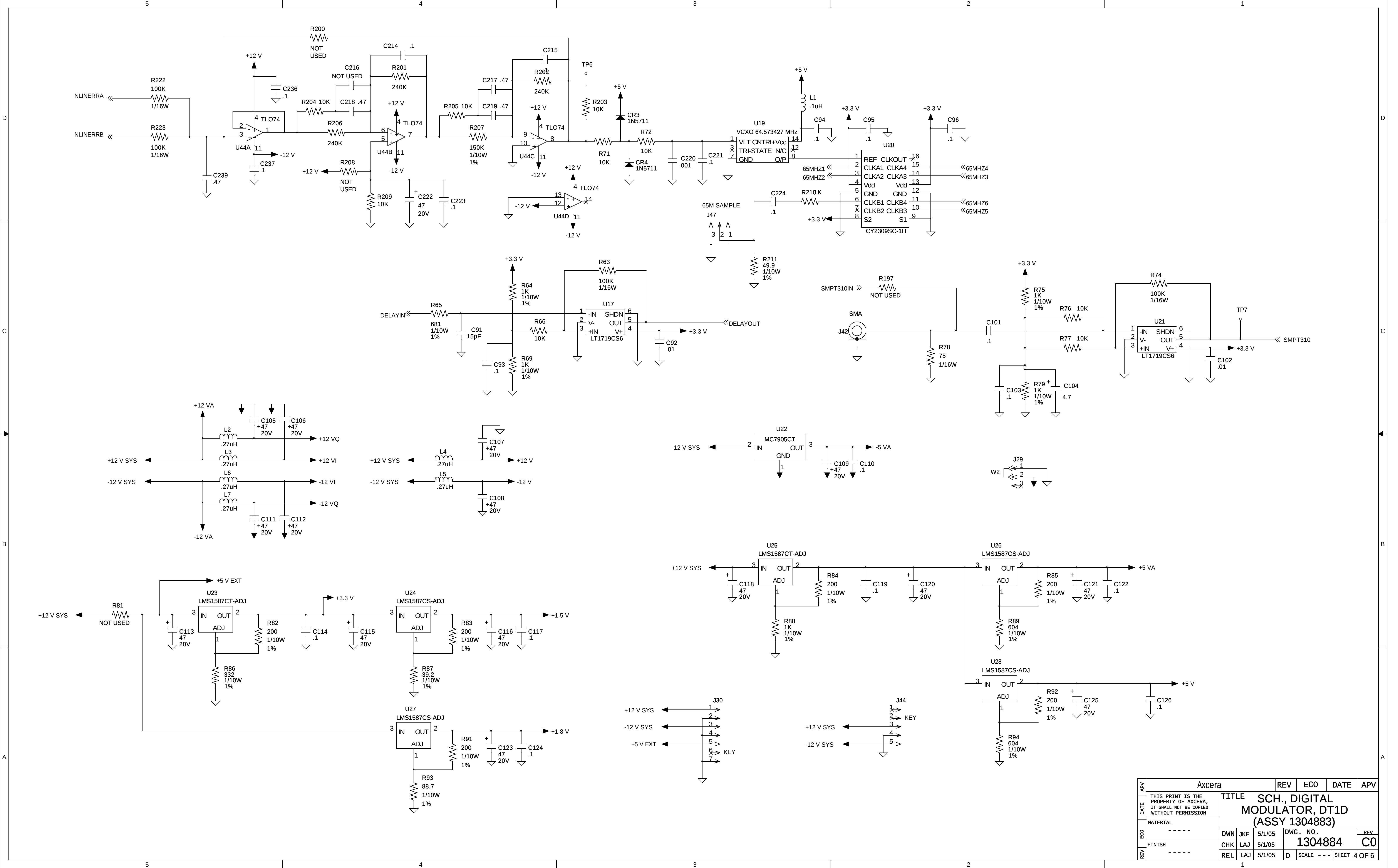
11 WAS MADE NOT USED IN THIS ASSY. JKF		C01 20112851 1/24/08 GJN		CHGD R167 & R173 TO 10K; R184 TO 31.6 OHM; R187 & R189 TO 180 OHM; R190 TO 68 OHM; R207 TO 150K; R222 & R223 TO 100K; ADD JUMPER FROM R14 TO R23 CONN. MADE C216, R15; R16; R19; R23; R182; R183; R186; R197; R198; R208 & R220 NOT USED. JKF	
REV		ECO	DATE	10/12/05	LAJ
MATERIAL		FINISH	-----	-----	-----
DWN		JKF	5/1/05	DWG. NO.	REV
CHK		LAJ	5/1/05	1304884	C0
REL		LAJ	5/1/05	D	SCALE - - - SHEET 1 OF 6



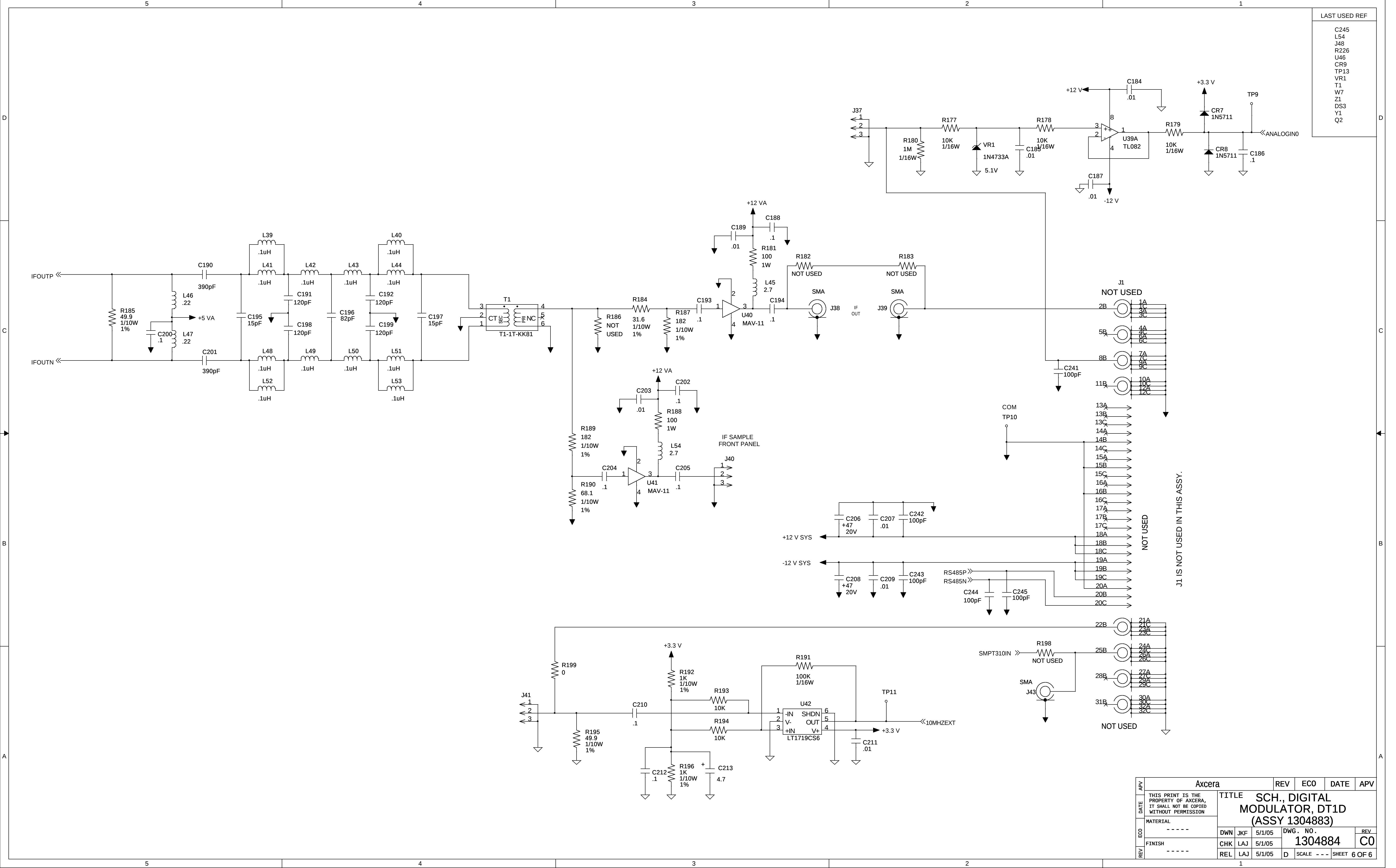
APV	Axcera			REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION			TITLE SCH., DIGITAL MODULATOR, DT1D (ASSY 1304883)			
ECO	MATERIAL			DWN	JKF	5/1/05	DWG. NO.
REV	FINISH			CHK	LAJ	5/1/05	1304884
	-----			REL	LAJ	5/1/05	D
				SCALE - - -			SHEET 2 OF 6
							REV C0



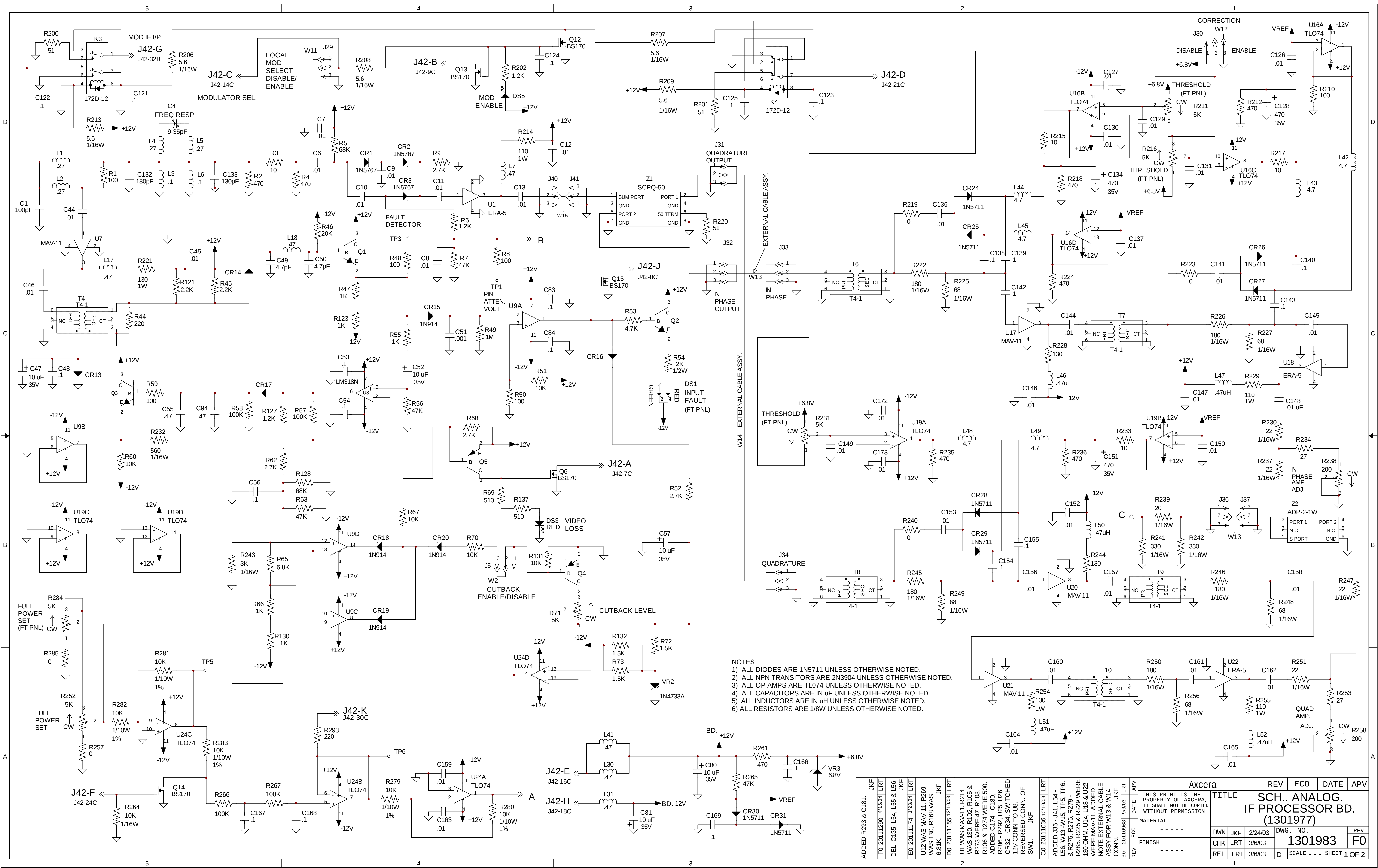
APV	Axcera				REV	ECO	DATE	APV	
DATE	THIS PRINT IS THE PROPERTY OF AXCERA. IT SHALL NOT BE COPIED WITHOUT PERMISSION		TITLE SCH., DIGITAL MODULATOR, DT1D (ASSY 1304883)						
ECO			-----		DWN	JKF	5/1/05	DWG. NO.	
REV			FINISH -----		CHK	LAJ	5/1/05	1304884	C0
					REL	LAJ	5/1/05	D SCALE ---	SHEET 3 OF 6

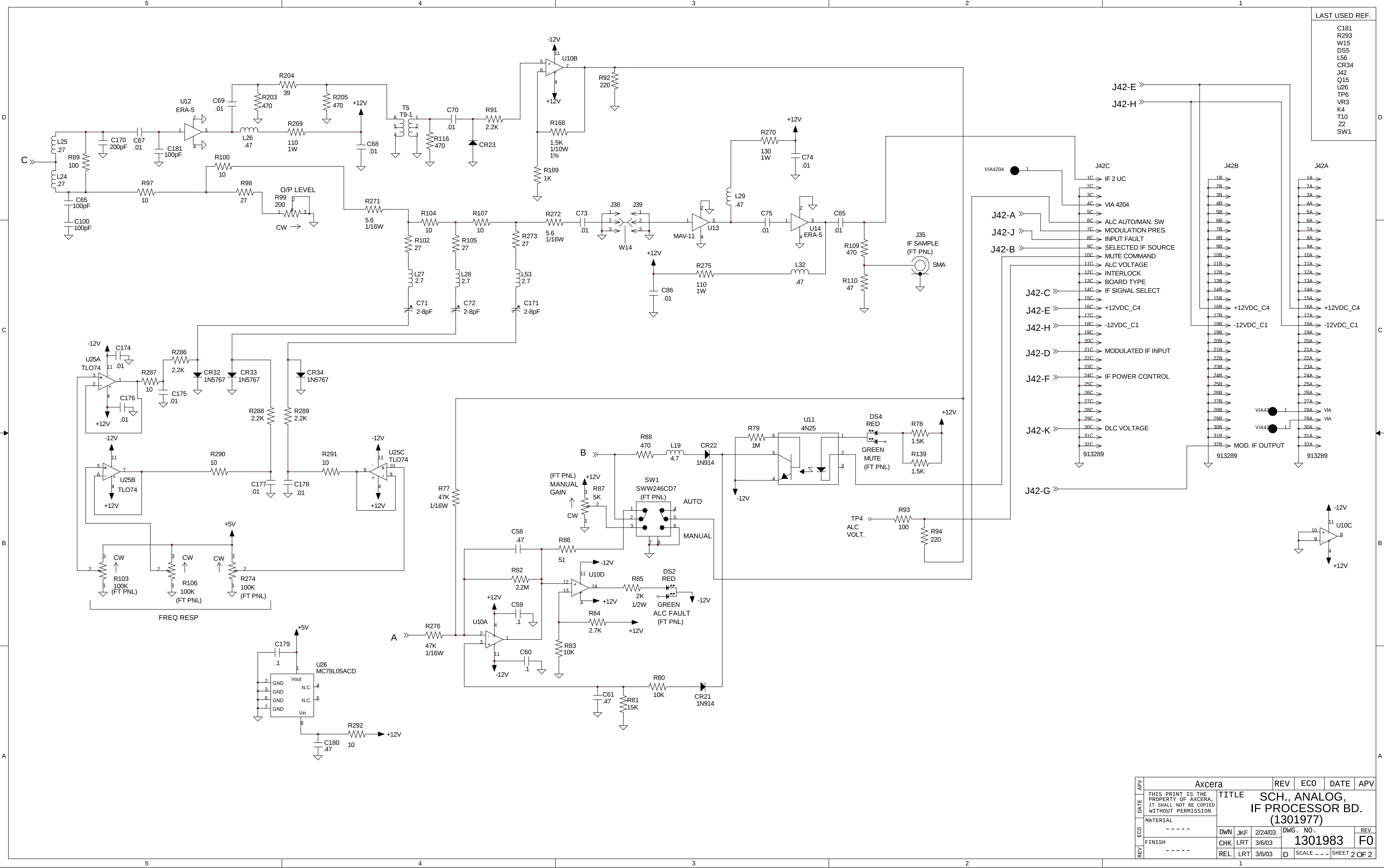


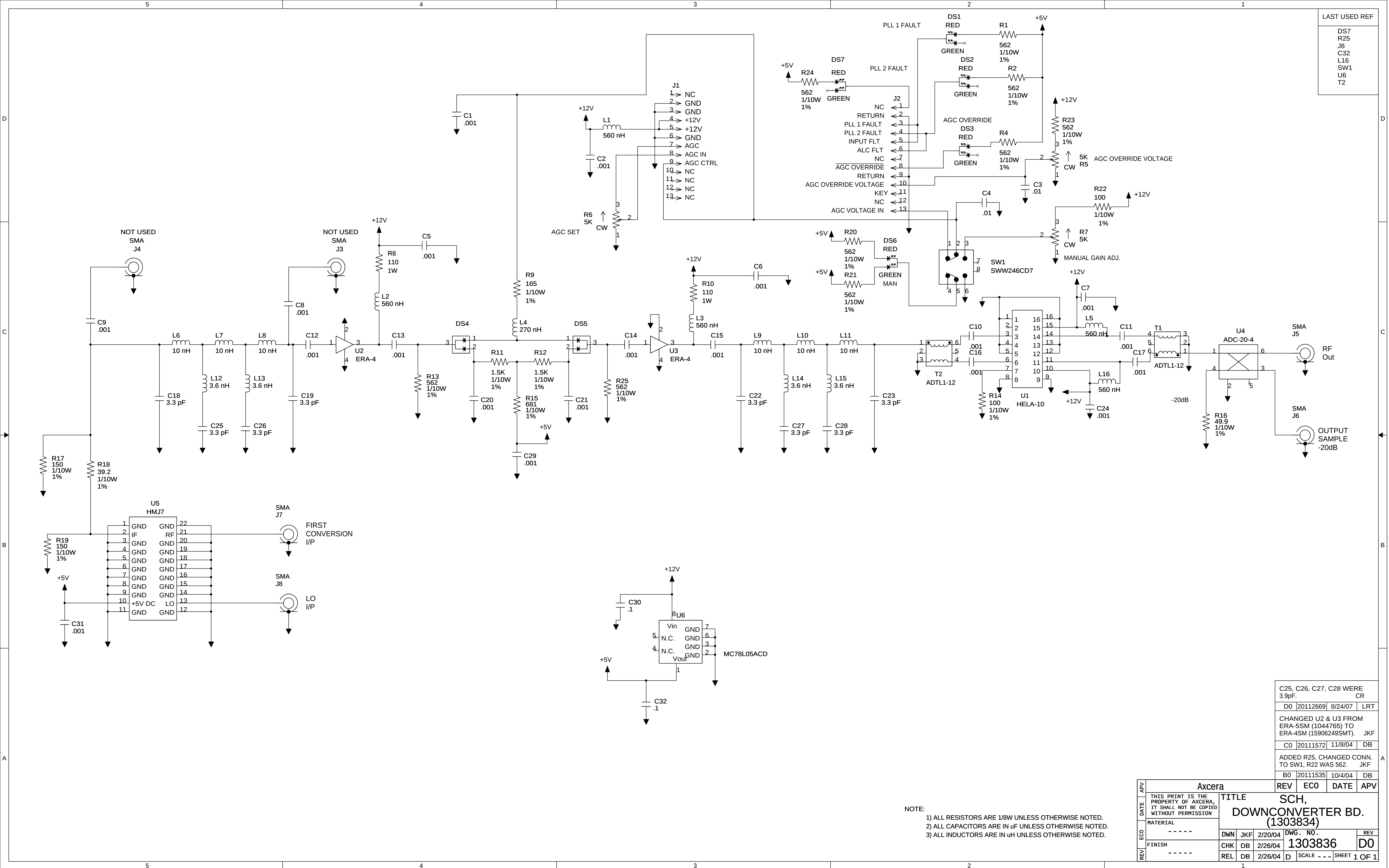
APV	Axcera			REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION			TITLE SCH., DIGITAL MODULATOR, DT1D (ASSY 1304883)			
ECO	MATERIAL			DWN	JKF	5/1/05	DWG. NO.
FINISH				CHK	LAJ	5/1/05	1304884
REV				REL	LAJ	5/1/05	D SCALE - - - SHEET 4 OF 6

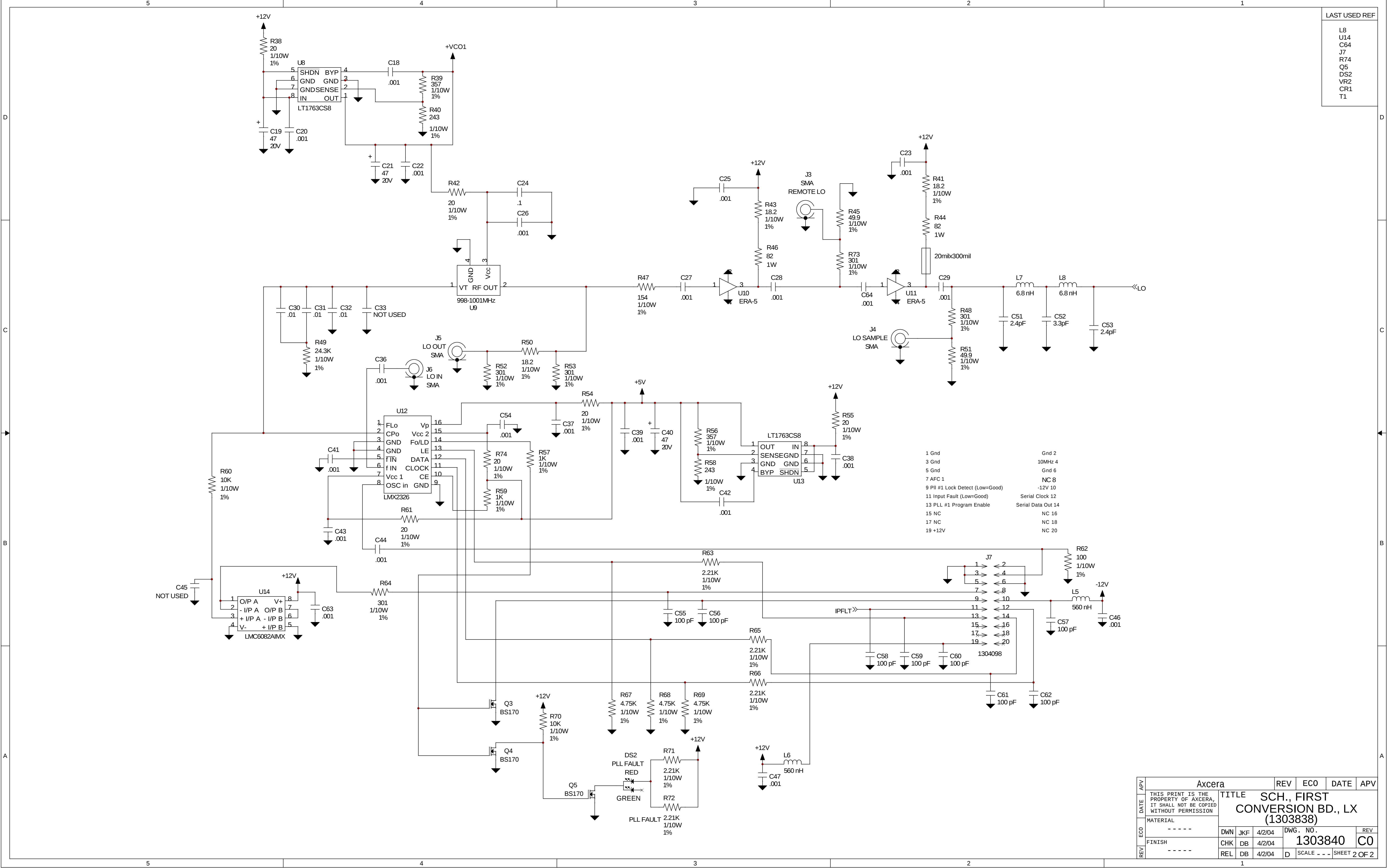


APV	Axcera			REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION			TITLE SCH., DIGITAL MODULATOR, DT1D (ASSY 1304883)			
MATERIAL	-----			DWN	JKF	5/1/05	DWG. NO. 1304884
FINISH	-----			CHK	LAJ	5/1/05	REV C0
REL	-----			REL	LAJ	5/1/05	D SCALE --- SHEET 6 OF 6









LAST USED REF
L8
U14
C64
J7
R74
Q5
DS2
VR2
CR1
T1

- 1 Gnd

3 Gnd

5 Gnd

7 AFC 1

9 Pll #1 Lock Detect (Low=Good)

11 Input Fault (Low=Good)

13 PLL #1 Program Enable

15 NC

17 NC

19 +12V
- Gnd 2

10MHz 4

Gnd 6

NC 8

-12V 10

Serial Clock 12

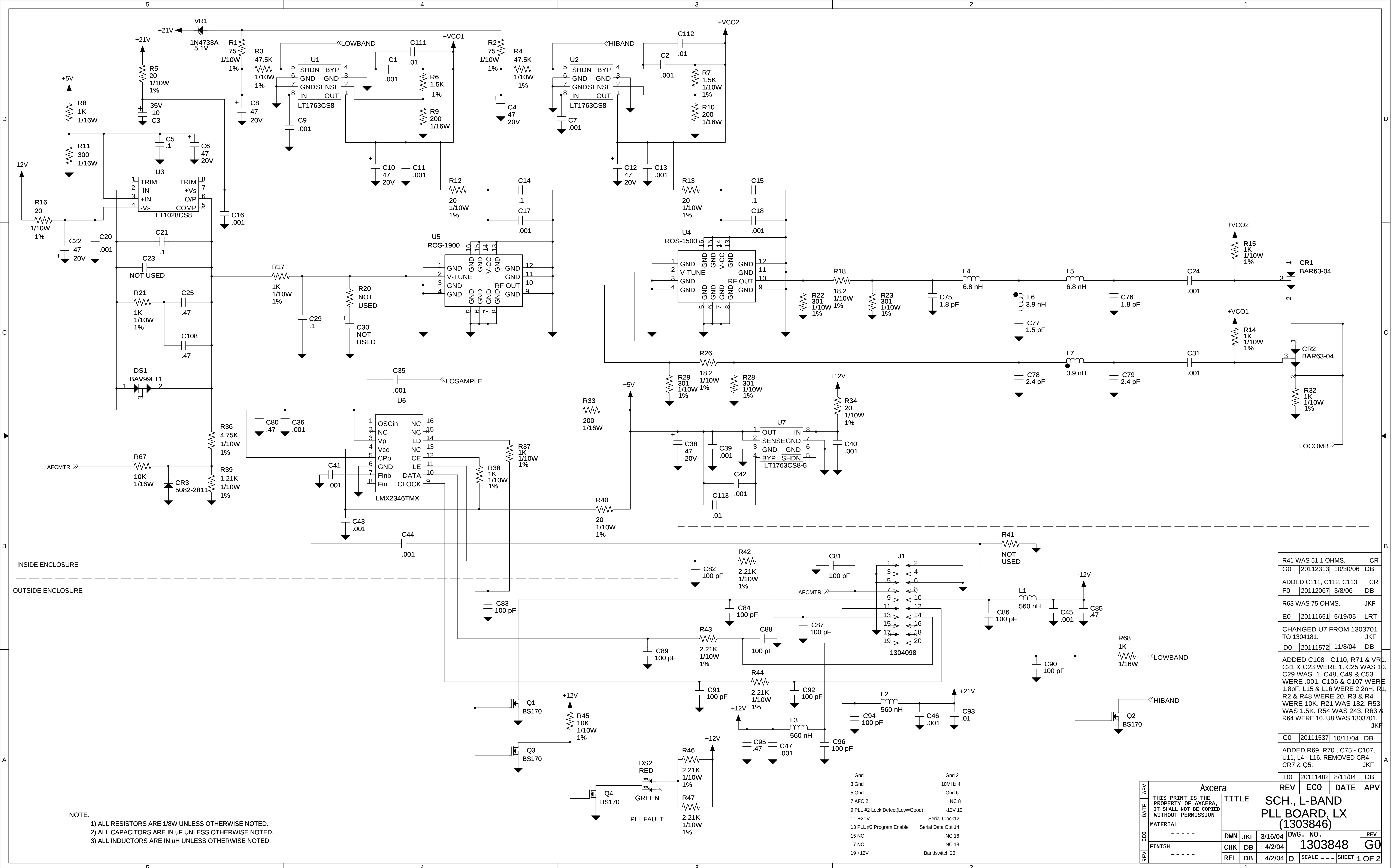
Serial Data Out 14

NC 16

NC 18

NC 20

APV	Axcera				REV	ECO	DATE	APV	
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION				TITLE SCH., FIRST CONVERSION BD., LX (1303838)				
MATERIAL									
ECO	-----				DWN	JKF	4/2/04	DWG. NO.	REV
REV	FINISH -----				CHK	DB	4/2/04	1303840	C0
	-----				REL	DB	4/2/04	D	SCALE --- SHEET 2 OF 2



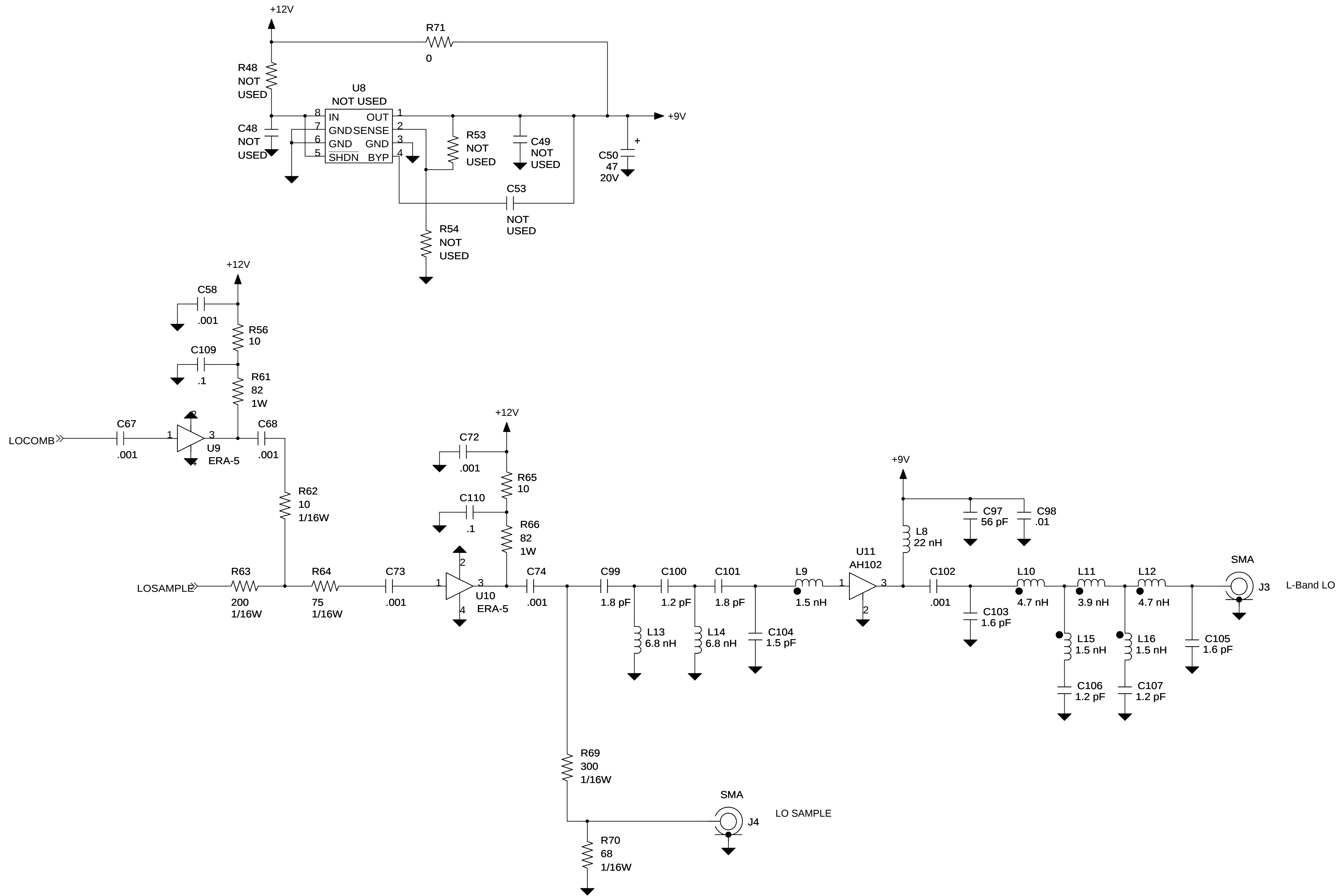
NOTE:
1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.

R41 WAS 51.1 OHMS.		CR
G0	[20112313]	10/30/06
ADDED C111, C112, C113.		CR
F0	[20112067]	3/8/06
R63 WAS 75 OHMS.		JKF
E0	[20111651]	5/19/05
CHANGED U7 FROM 1303701 TO 1304181.		JKF
D0	[20111572]	11/8/04
ADDED C108 - C110, R71 & VR1. C21 & C23 WERE 1. C25 WAS 10. C29 WAS 1. C48, C49 & C53 WERE .001. C106 & C107 WERE 1.8pF. L15 & L16 WERE 2.2nH. R1, R2 & R48 WERE 20. R3 & R4 WERE 10K. R21 WAS 182. R53 WAS 1.5K. R54 WAS 243. R63 & R64 WERE 10. U8 WAS 1303701.		JKF
C0	[20111537]	10/11/04
ADDED R69, R70 , C75 - C107, U11, L4 - L16. REMOVED CR4 - CR7 & Q5.		JKF
B0	[20111482]	8/11/04

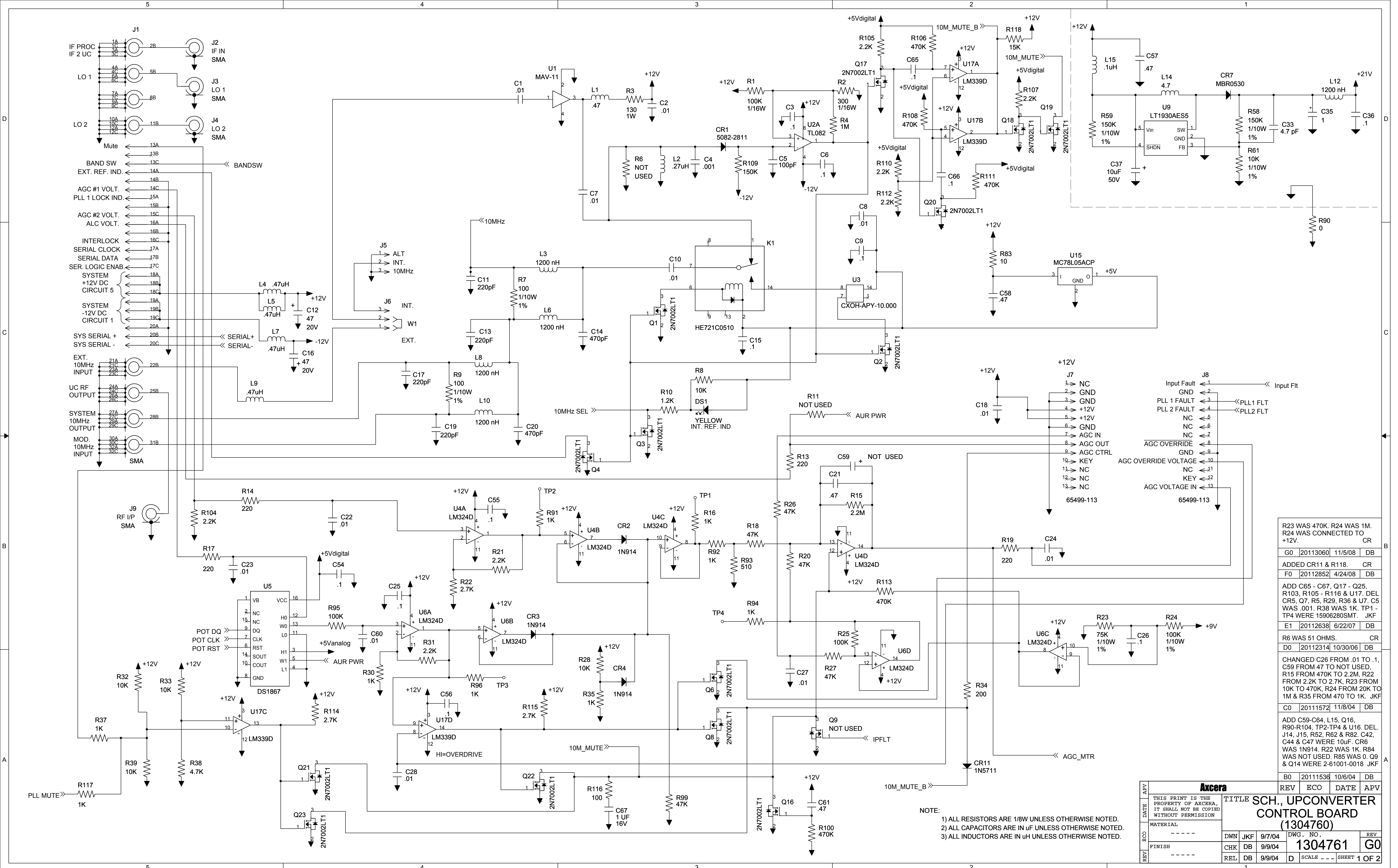
APV		Axcera		REV	ECO	DATE	APV
DATE		THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION		TITLE SCH., L-BAND PLL BOARD, LX (1303846)			
MATERIAL		-----		DWN	JKF	3/16/04	DWG. NO.
FINISH		-----		CHK	DB	4/2/04	1303848
REV		-----		REL	DB	4/2/04	D
				SCALE - - -		SHEET 1 OF 2	

1 Gnd	Gnd 2
3 Gnd	10MHz 4
5 Gnd	Gnd 6
7 AFC 2	NC 8
9 PLL #2 Lock Detect(Low=Good)	-12V 10
11 +21V	Serial Clock12
13 PLL #2 Program Enable	Serial Data Out 14
15 NC	NC 16
17 NC	NC 18
19 +12V	Bandswitch 20

LAST USED REF
C113
L16
U11
R71
J4
Q4
CR3
DS2
VR1



REV	ECO	DATE	APV	REV	ECO	DATE	APV
THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION				TITLE SCH., L-BAND PLL BOARD, LX (1303846)			
				DWG. NO. 1303848			
MATERIAL				DWN	JKF	3/16/04	REV
FINISH				CHK	DB	4/2/04	G0
				REL	DB	4/2/04	D
				SCALE - - - SHEET 2 OF 2			



R23 WAS 470K. R24 WAS 1M. R24 WAS CONNECTED TO +12V. CR

G0 [20113060] 11/5/08 DB

ADDED CR11 & R118. CR

F0 [20112852] 4/24/08 DB

ADD C65 - C67, Q17 - Q25, R103, R105 - R116 & U17. DEL CR5, Q7, R5, R29, R36 & U7. C5 WAS .001. R38 WAS 1K. TP1 - TP4 WERE 15906280SMT. JKF

E1 [20112638] 6/22/07 DB

R6 WAS 51 OHMS. CR

D0 [20112314] 10/30/06 DB

CHANGED C26 FROM .01 TO .1, C59 FROM 47 TO NOT USED, R15 FROM 470K TO 2.2M, R22 FROM 2.2K TO 2.7K, R23 FROM 10K TO 470K, R24 FROM 20K TO 1M & R35 FROM 470 TO 1K. JKF

C0 [20111572] 11/8/04 DB

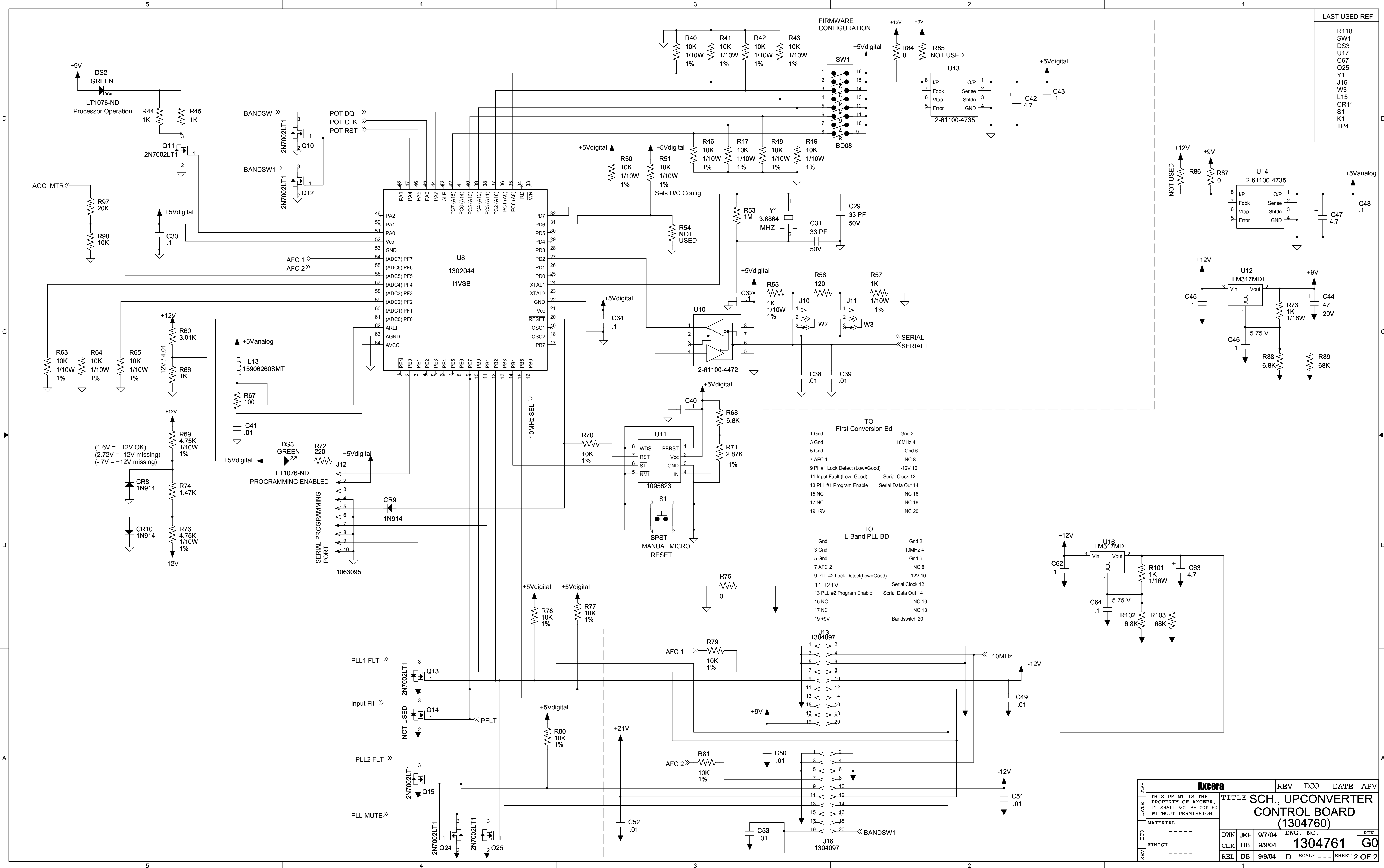
ADD C59-C64, L15, Q16, R90-R104, TP2-TP4 & U16. DEL. J14, J15, R52, R62 & R82. C42, C44 & C47 WERE 10uF. CR6 WAS 1N914. R22 WAS 1K. R84 WAS NOT USED. R85 WAS 0. Q9 & Q14 WERE 2-61001-0018 JKF

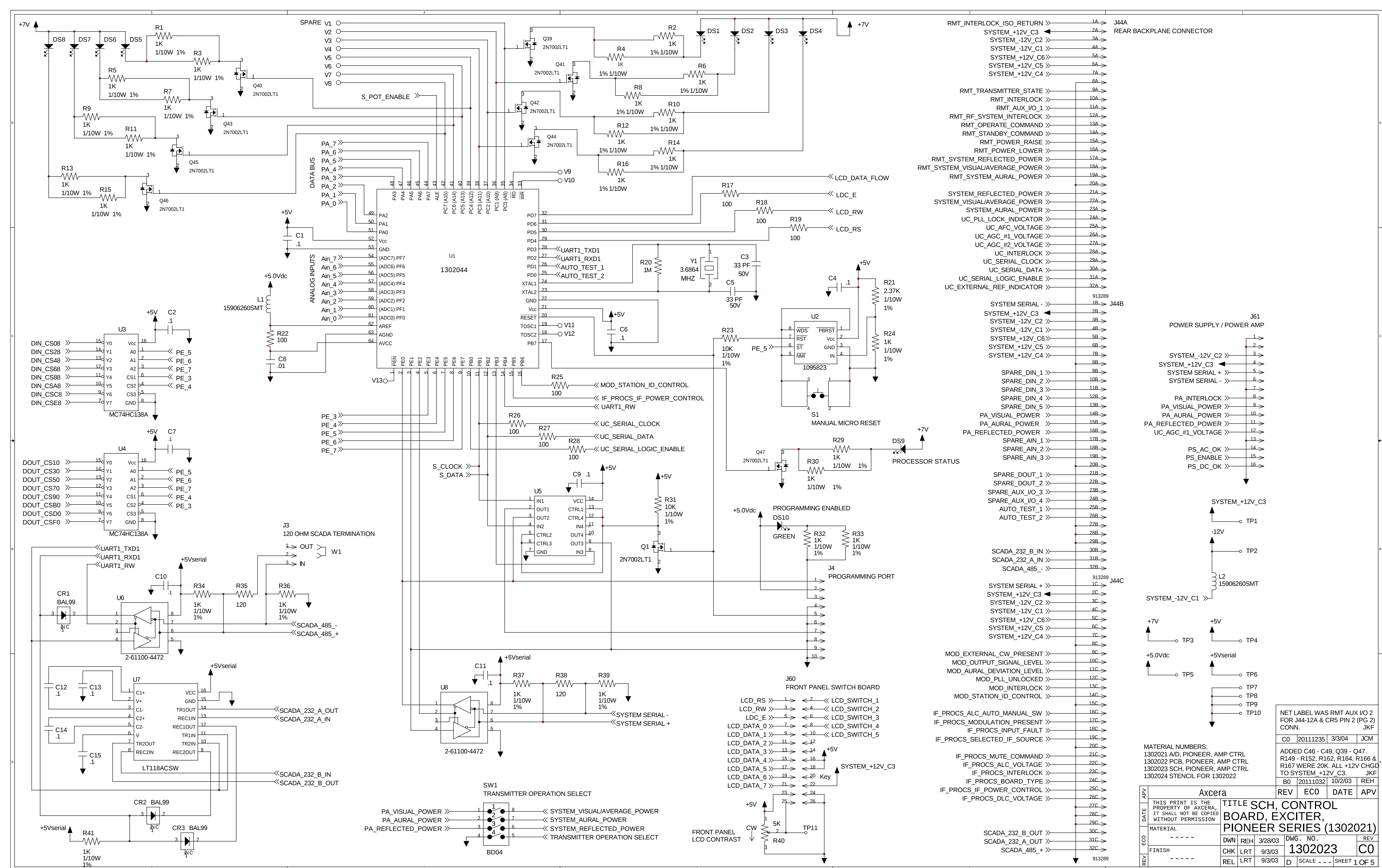
B0 [20111536] 10/6/04 DB

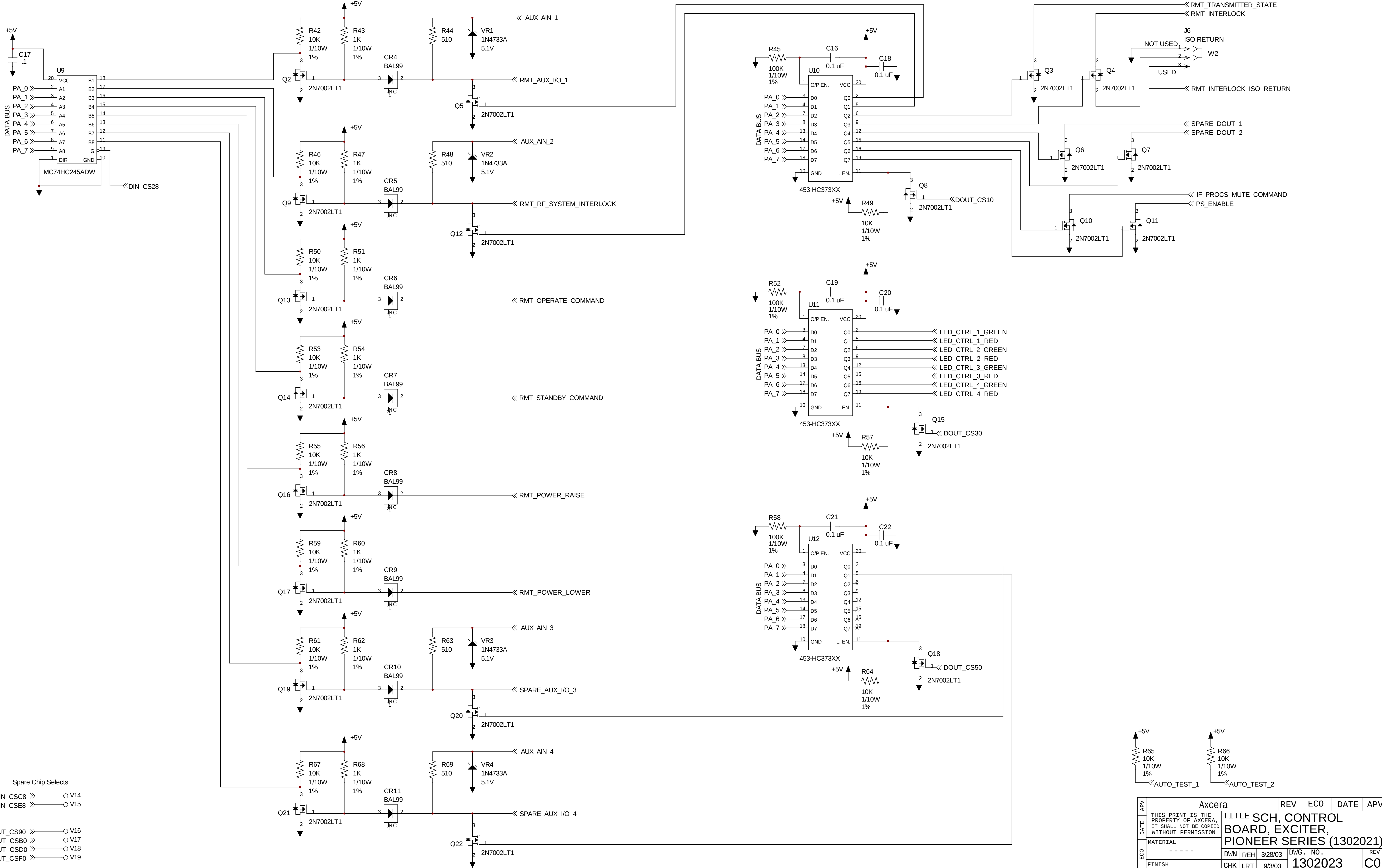
REV ECO DATE APV

Xacera				TITLE SCH., UPCONVERTER CONTROL BOARD (1304760)			
REV	ECO	DATE	APV	DWN	JKF	9/7/04	DWG. NO.
---	---	---	---	CHK	DB	9/9/04	1304761
---	---	---	---	REL	DB	9/9/04	1304761
				D	SCALE	---	SHBET 1 OF 2

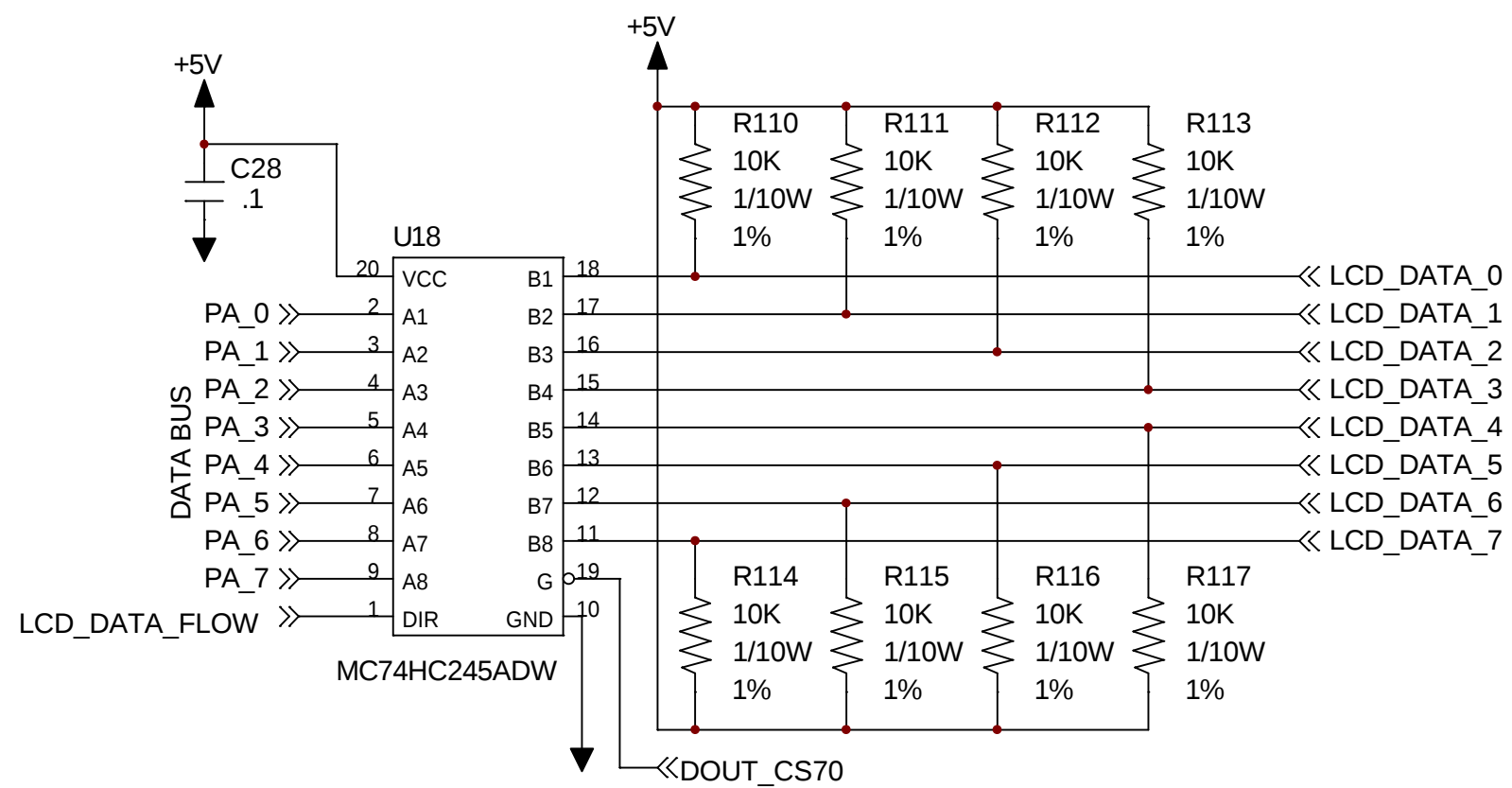
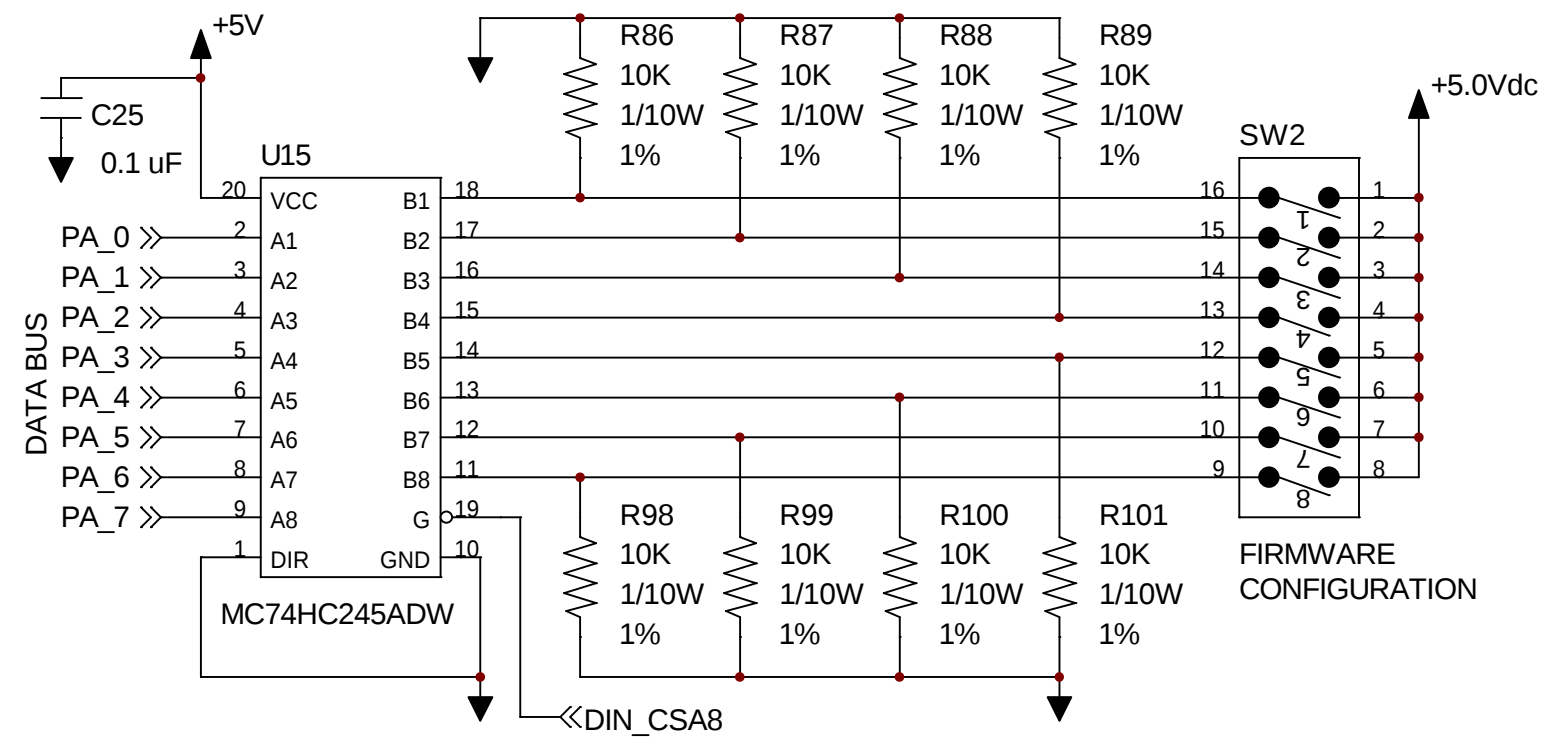
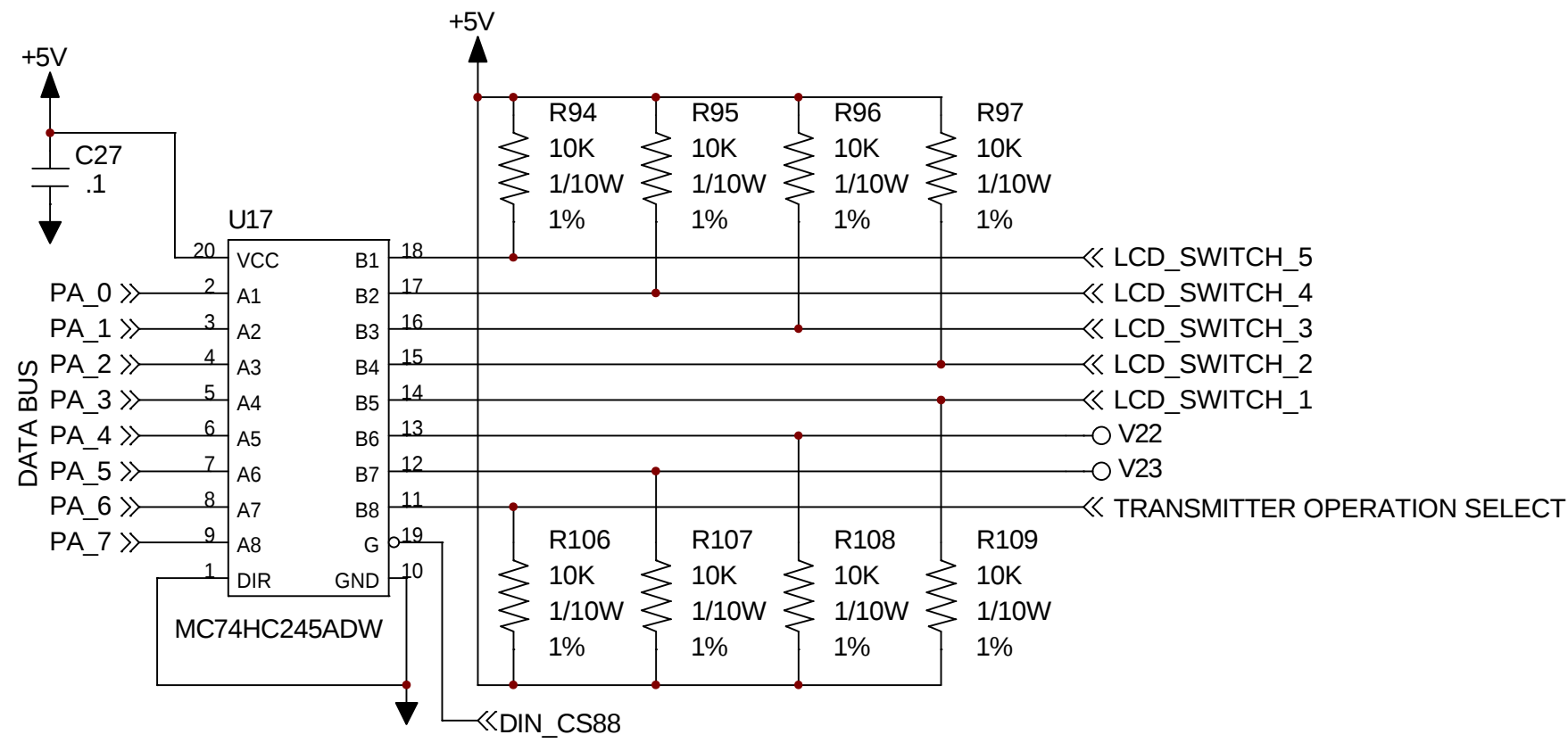
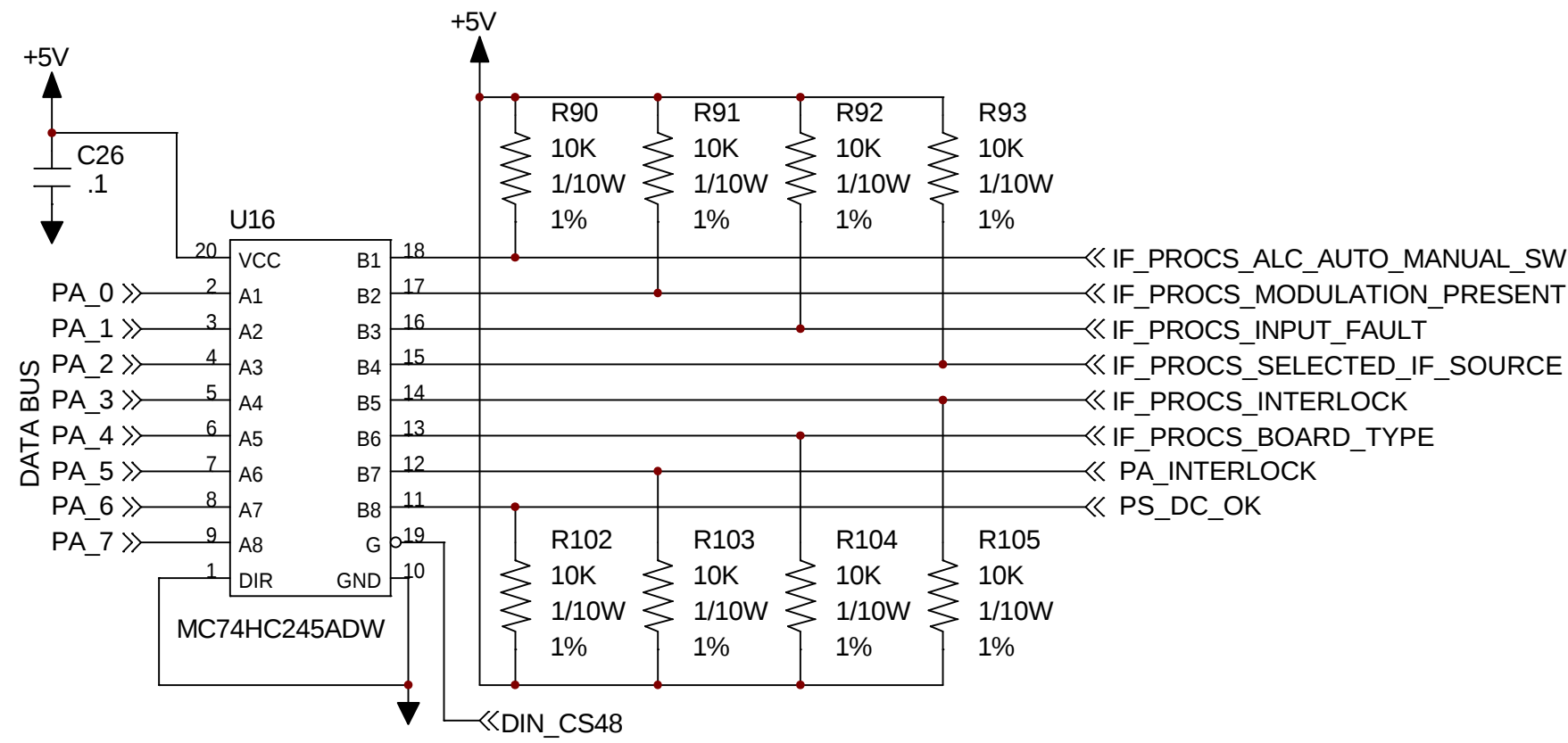
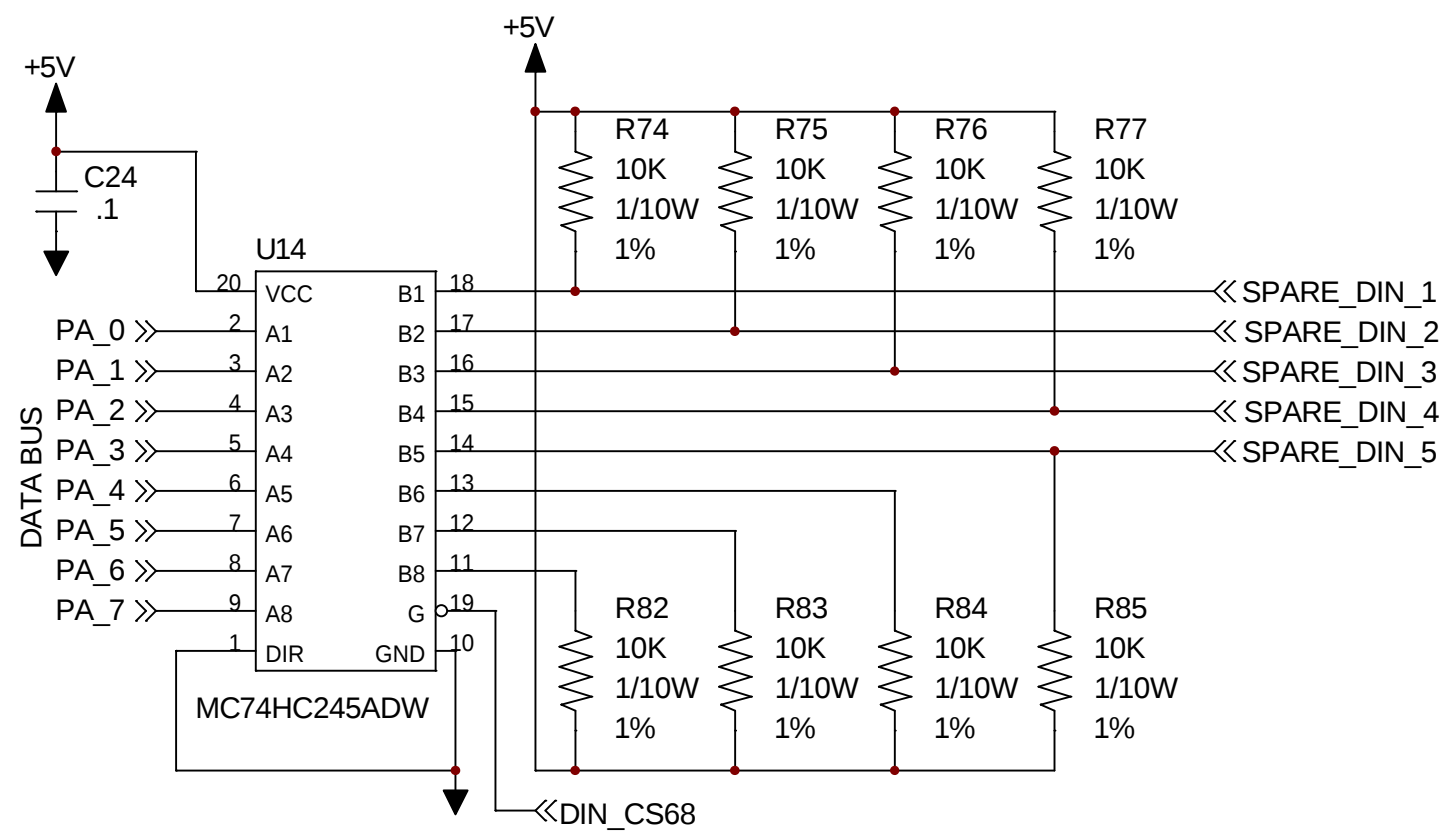
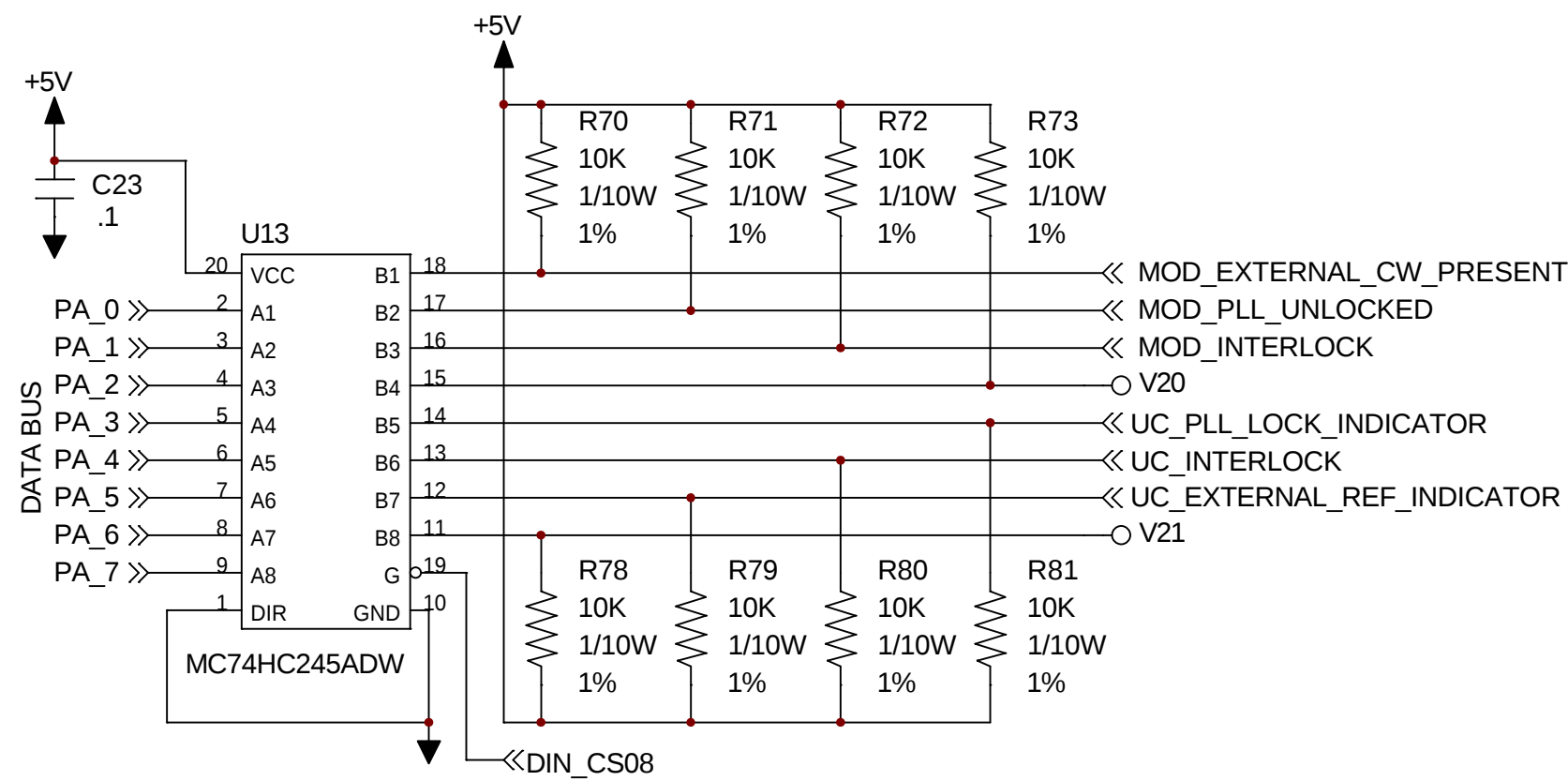
NOTE:
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2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.



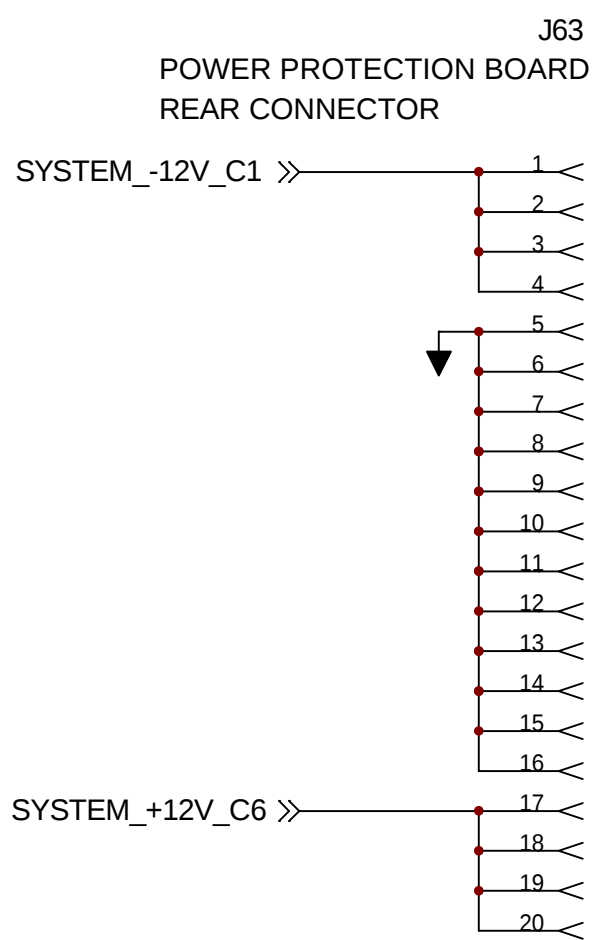
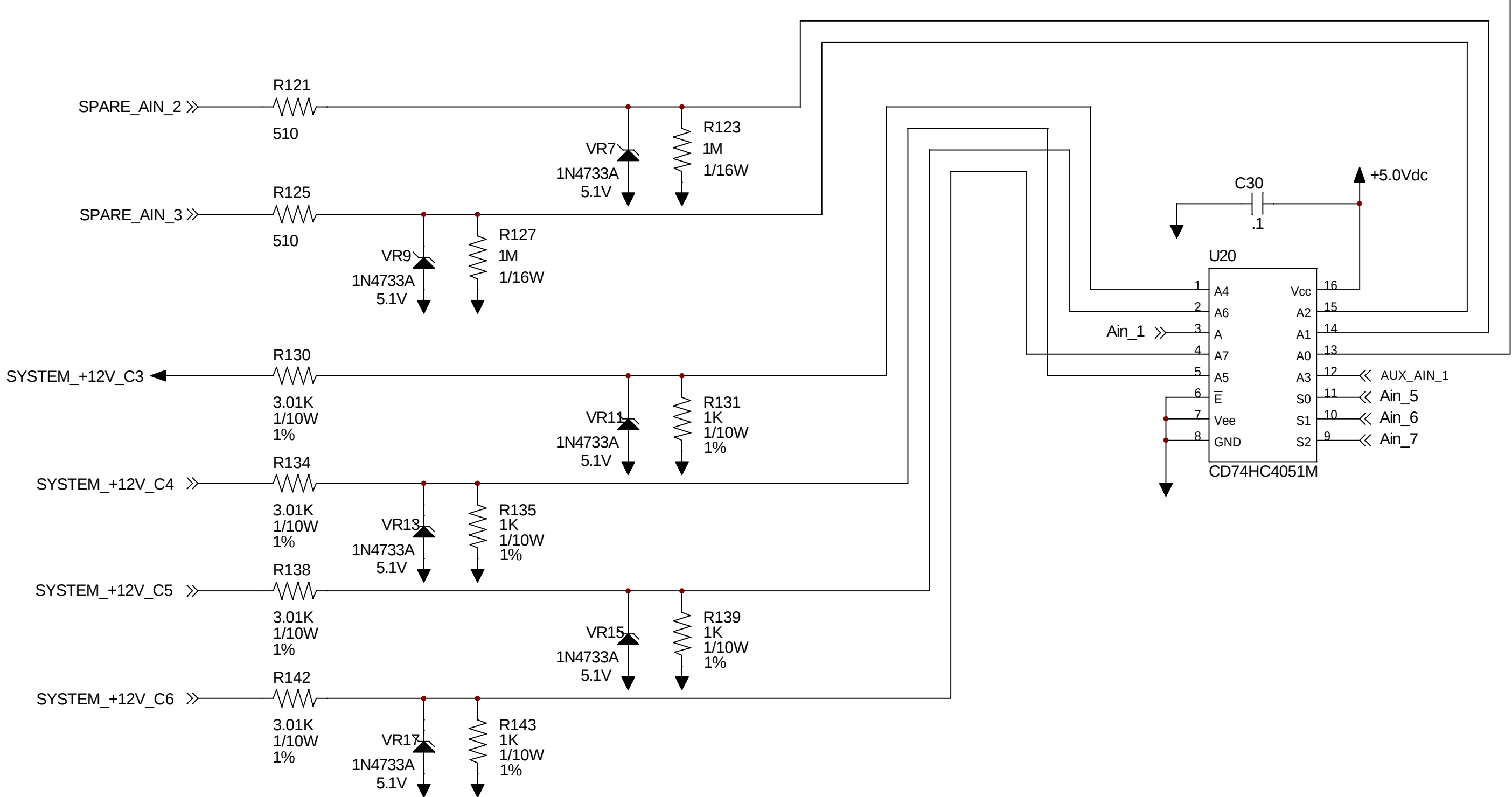
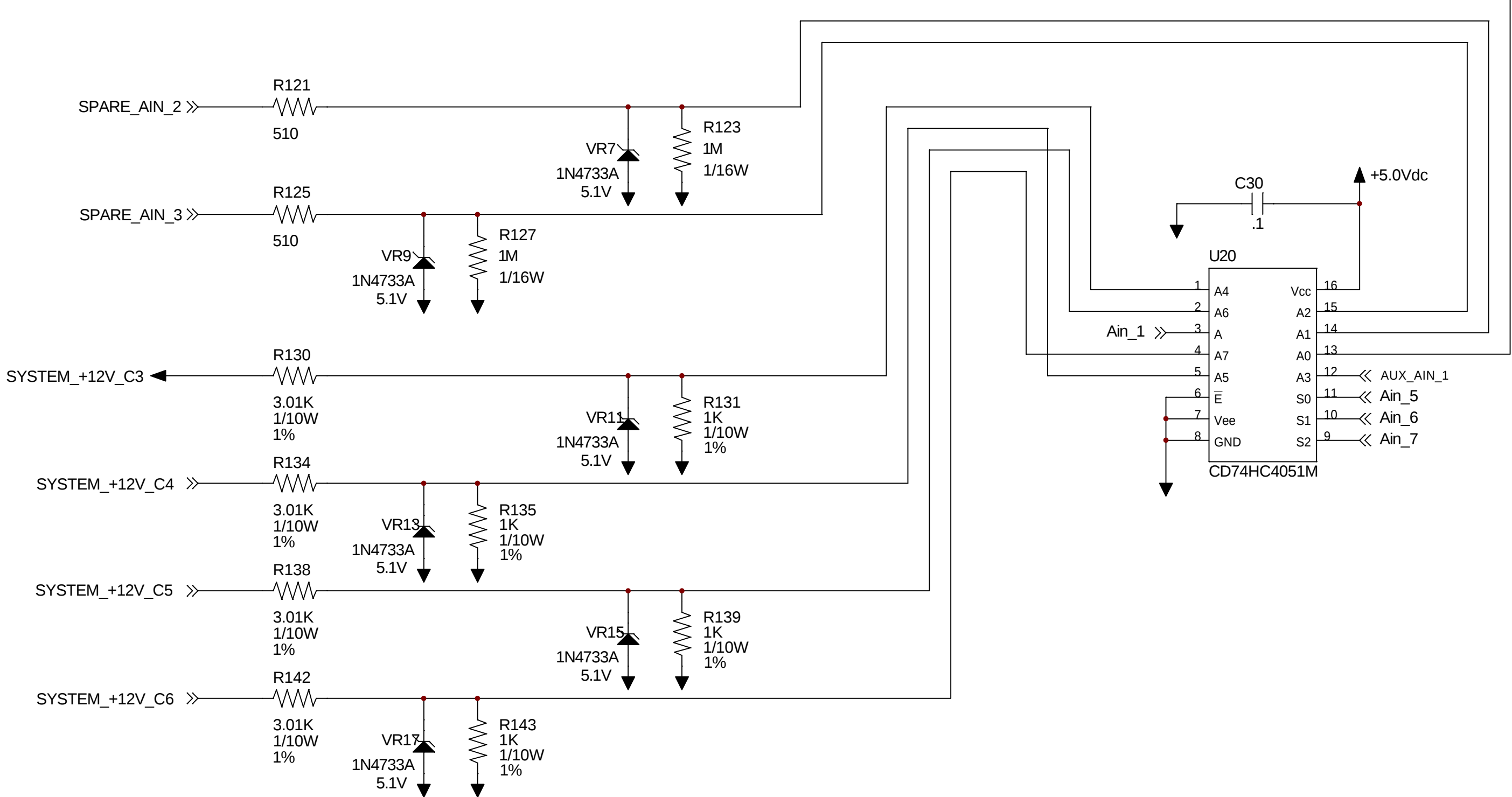




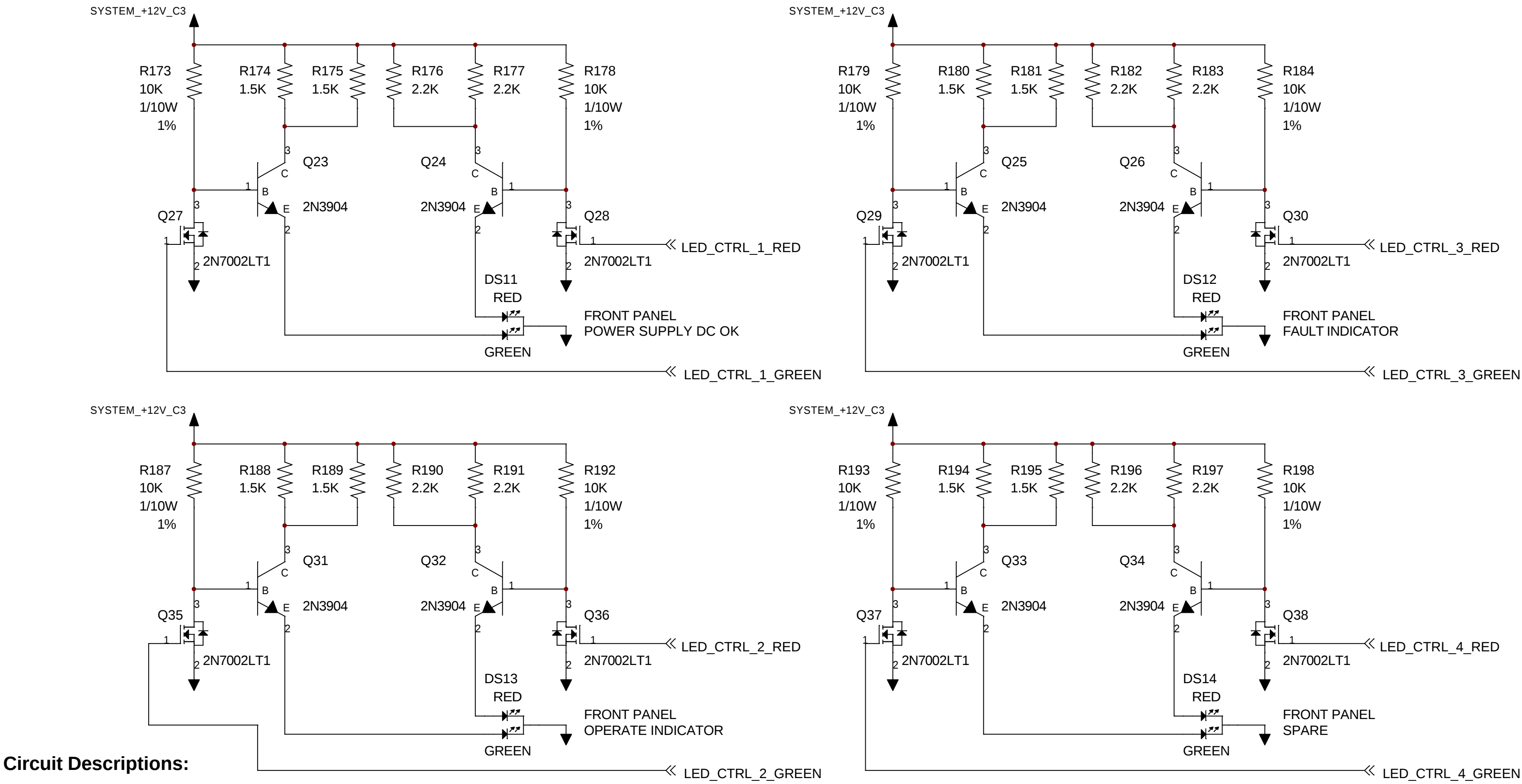
APV	Axcera				REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION				TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)			
ECO	MATERIAL				DWN	REH	3/28/03	DWG. NO.
REV	FINISH				CHK	LRT	9/3/03	1302023
					REL	LRT	9/3/03	C0



APV	Axcera			REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION			TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)			
ECO	MATERIAL			DWN	REH	3/28/03	DWG. NO.
REV	FINISH			CHK	LRT	9/3/03	1302023
				REL	LRT	9/3/03	C0
					SCALE	- - -	SHEET 3 OF 5



APV	Axcera				REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION		TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)					
ECO	MATERIAL		DWN REH 3/28/03 DWG. NO. REV					
REV	FINISH		CHK LRT 9/3/03 1302023				C0	
	-----		REL LRT 9/3/03 D SCALE --- SHEET 4 OF 5					



Circuit Descriptions:

PAGE 1:

U1 is an Atmel Atmega128 microcontroller. This part is in-circuit programmed using the serial programming port. When the microcontroller is held in reset by either the programming port or the external watchdog IC, a transistor inverts the reset signal while serial programming lines are connected to U1 through analog switch U5.

U2 is a watchdog IC used to hold the microcontroller in reset if the supply voltage is less than 4.21 Vdc; (1.25 Vdc < Pin 4 (IN) < Pin 2 (Vcc)). The watchdog momentarily resets the microcontroller if Pin 6 (IST) is not clocked every second. A manual reset switch is provided but should not be needed.

Diodes DS1 through DS8 are used for display of auto test results. A test board is used to execute self test routines. When the test board is installed, Auto_Test_1 is held low and Auto_Test_2 is allowed to float at 5 Vdc. This is the signal to start the auto test routines.

U3 and U4 are used to selectively enable various input and output ICs found on page 2 and 3 of the schematic.

U1 has two serial ports available. In this application, one port is used to communicate with transmitter system components where U1 is the master of a RS-485 serial bus. The other serial port is used to provide serial data I/O where U1 is not the master of the data port. A dual RS-232 port driver IC and a RS-485 port driver is also in the second serial data I/O system. The serial ports are wired such that serial data input can come through one of the three serial port channels. Data output is sent out through each of the three serial port channels.

Switch SW1 is used to select either transmitter operation or exciter driver operation. When the switches of SW1 are on, transmitter operation is selected and the power monitoring lines of the transmitter's power amplifier are routed to the system power monitoring lines.

PAGE 2:

Digital output latches are used to control system devices. Remote output circuits are implemented using open drain FETs with greater than 60 Volt drain to source voltage ratings.

Remote digital inputs are diode protected with a 1 Kohm pull-up resistor to 5Vdc. If the remote input voltage is greater than about 2 volts or floating, a FET is turned on and a logic low is applied to the digital input buffer. If the remote input voltage is less than the turn on threshold of the FET (about 2 Vdc), a logic high is applied to the digital input buffer.

Four of the circuits on page two are auxiliary I/O connections wired for future use. They are wired similar to the remote digital inputs but include a FET for digital output operation. To operate these signals as an input, the associated output FET must be turned off. These circuits are also connected to an analog input multiplexer IC.

PAGE 3:

Several ICs are used as input buffers to allow the microcontroller to monitor various digital input values. Most digital inputs use a 10 Kohm pull-up resistor. The buffer IC used for data transfer to the display is wired for read and write control.

PAGE 4:

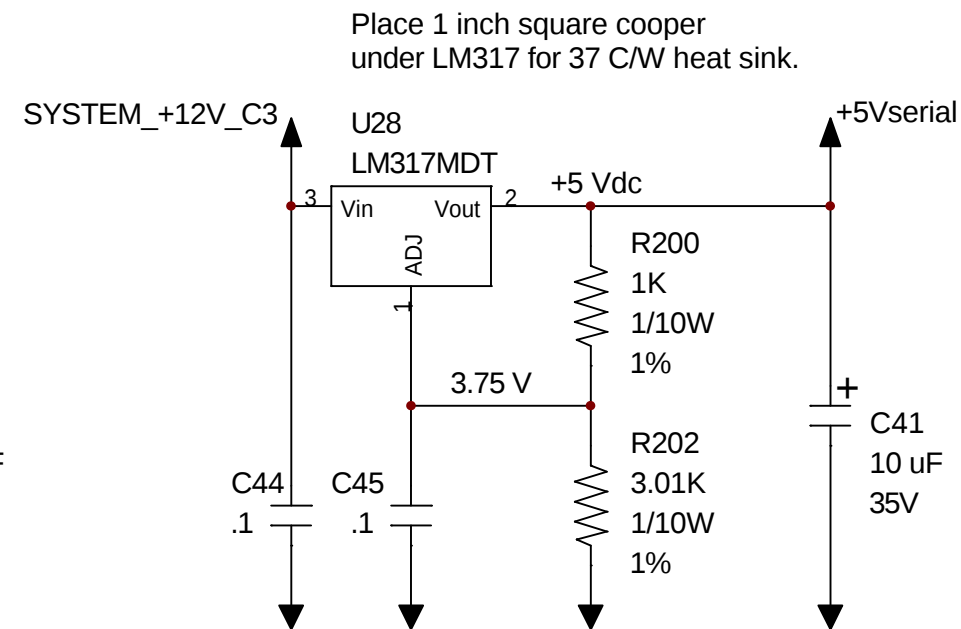
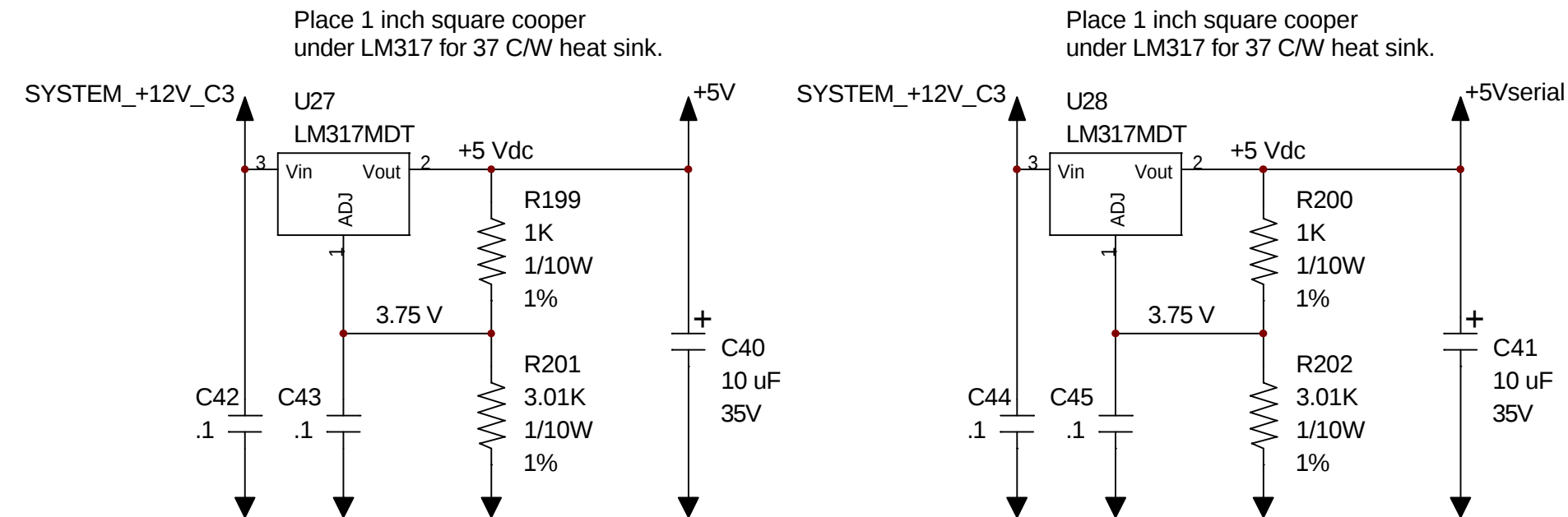
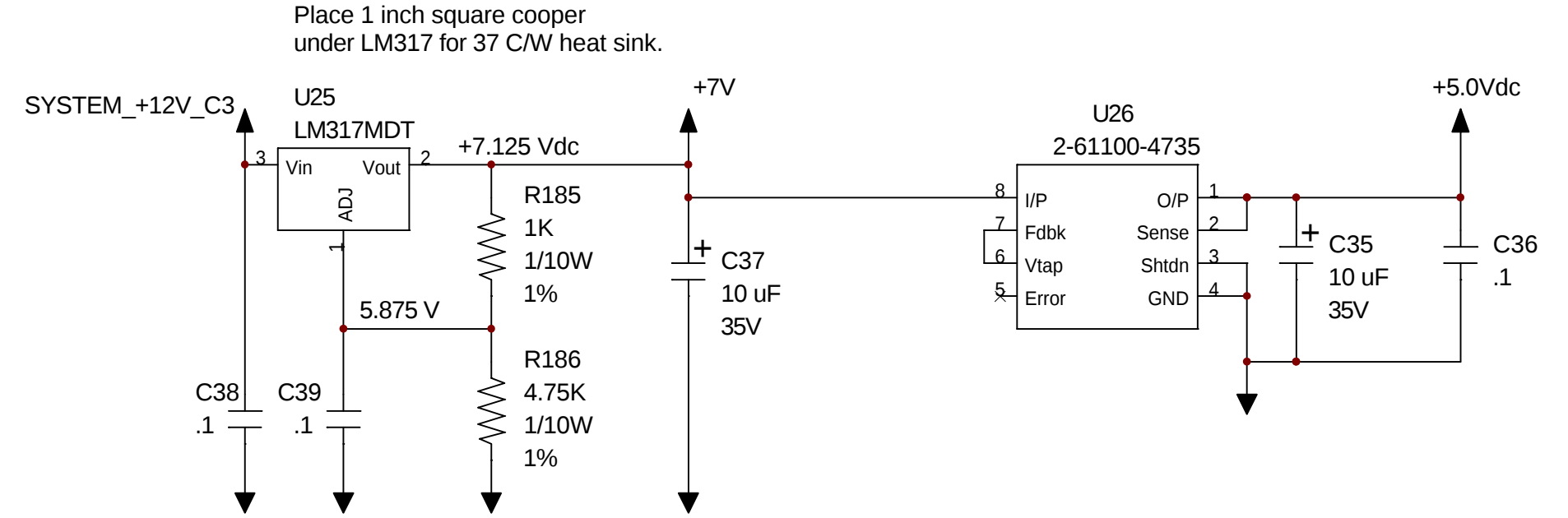
Each analog input is expected to be between 0 and 5 Vdc. If a signal exceeds 5.1 Vdc, a 0.225 Watt zenor diode clamps the signals voltage. Most signals are calibrated at their source however two dual serial potentiometer ICs are used to calibrate four signals. For these four circuits, the input value is divided in half before it is applied to an op-amp. The serial potentiometer is used to adjust the input signal between 80 and 120% of the input signal. Serial data to the second serial potentiometer is transferred through the first IC. The wiper position of the digital potentiometer circuit is used to set the gain of the op-amp. Lower digital values for the wiper setting increases the gain of the op-amp. If N= 0, gain = 6.0. If N = 255, gain = 3.00. If Vin = 1.0 at spare_Ain_1 and N = 128, U21A out = 4.0V with gain = 4.

Two 20 position connectors are used to provide power to the backplane. J62 and J63 get power from the power supply after a nominal 3 amp resettable fuse. The Raychem polyswitch resettable fuses may open on a current as low as 2.43 amps at 50C, 3 amps at 25 C or 3.3 amps at 0C. They definately will open when the current is 4.86 amps at 50C, 6 amps at 20C, or 6.6 amps at 0C. Trace widths of these circuits are 0.140" (designed for maximum current).

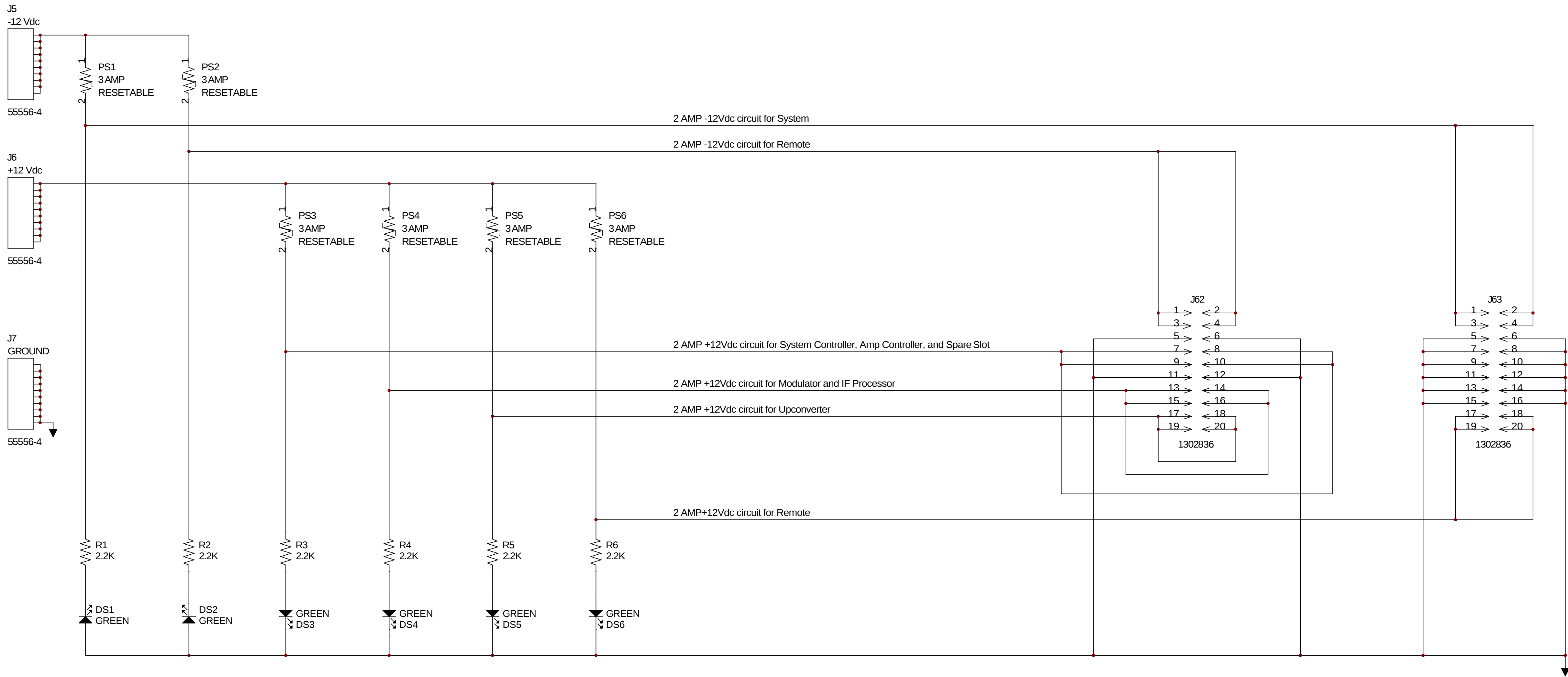
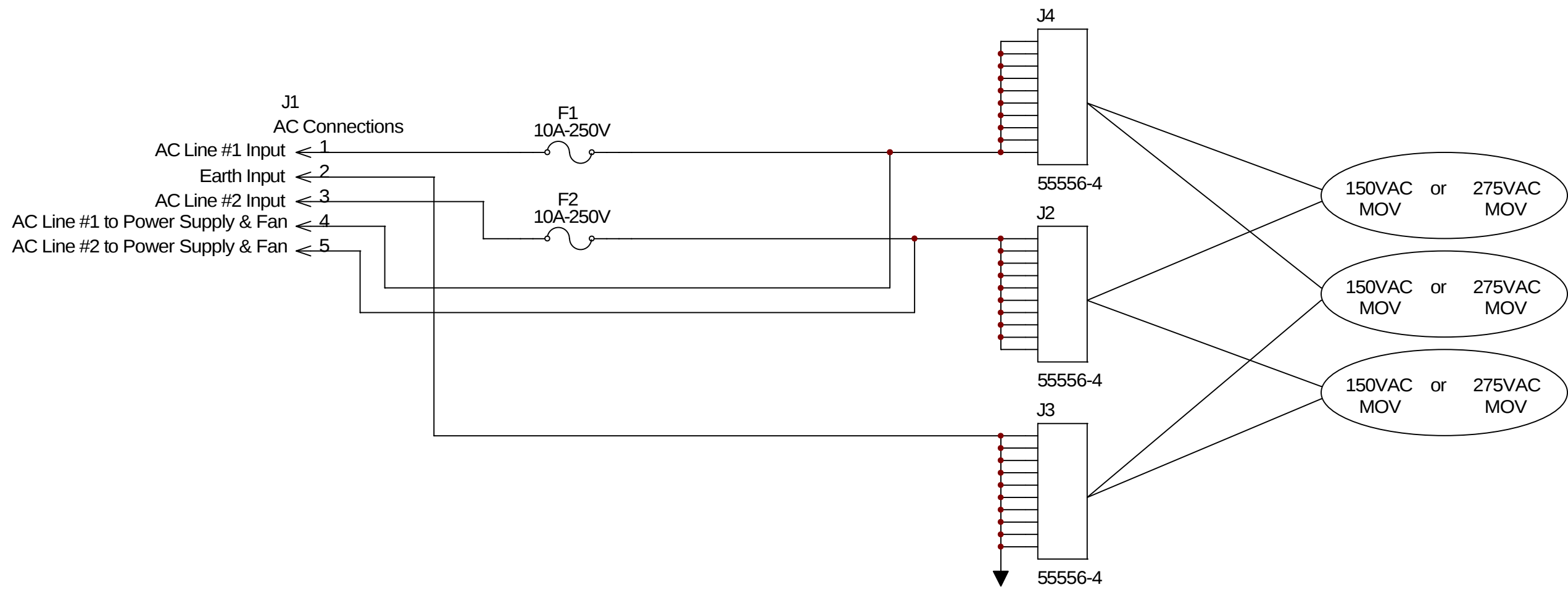
PAGE 5:

Each of the four LED circuits drive a dual element common cathode LED. To make a good amber color, the current applied to the green element is slightly greater than the red element.

Several voltage regulators are used to power the board. Seven volts is typically applied to board LEDs and to the input of a precision 5.0 volt regulator. The 5.0 volt regulator is used for analog circuits and the microcontroller analog reference voltage. Another two 5 volt regulator circuits are used for most other board circuits.



APV		Axcera				REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)							
ECO									
REV	MATERIAL	DWN	REH	3/28/03	DWG. NO.			REV	
	FINISH	CHK	LRT	9/3/03	1302023			C0	
	-----	REL	LRT	9/3/03	D	SCALE ---		SHEET 5 OF 5	



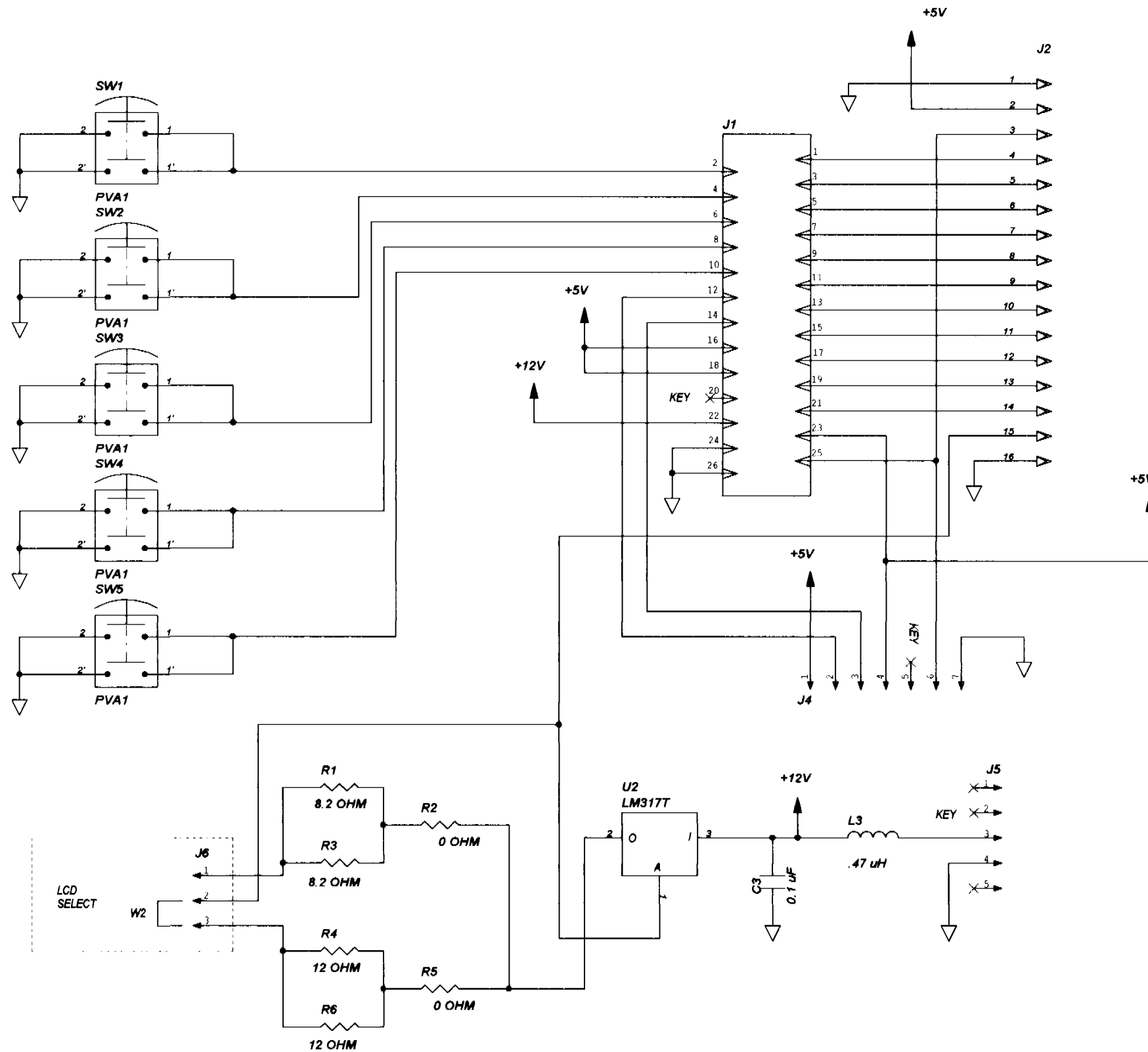
Circuit Design Notes:

- Track widths of 0.140 inch minimum top and bottom of board shall be used to connections to J1, J2, J3, J4.
- Track widths of 0.140 inch minimum top of board shall be used to connections to J5 and J6.
- Track widths of 0.065 inch minimum shall be used to connections to J62 and J63.
- Track widths of 0.020 inch minimum shall be used to connections between LEDs and resistors.
- Board BOM needs the following items added to those exported from Orcad:

Part Number	Qty	Description
102071	4	Fuse Clip, PC BD Mnt., 15 Amp

MATERIAL NUMBERS:
1302837 PIONEER, POWER PROTECTION
1302838 PCB, PIONEER, PWR PROTECT
1302839 SCH, PIONEER, PWR PROTECT
1302840 STENCIL FOR 1302838

REV	DATE	APV	ECO	REV	ECO	DATE	APV
1	5/29/03	REH	1	5/29/03	REH	5/29/03	REH
2	5/29/03	REH	2	5/29/03	REH	5/29/03	REH
3	5/29/03	REH	3	5/29/03	REH	5/29/03	REH
4	5/29/03	REH	4	5/29/03	REH	5/29/03	REH
5	5/29/03	REH	5	5/29/03	REH	5/29/03	REH
6	5/29/03	REH	6	5/29/03	REH	5/29/03	REH
7	5/29/03	REH	7	5/29/03	REH	5/29/03	REH
8	5/29/03	REH	8	5/29/03	REH	5/29/03	REH
9	5/29/03	REH	9	5/29/03	REH	5/29/03	REH
10	5/29/03	REH	10	5/29/03	REH	5/29/03	REH
11	5/29/03	REH	11	5/29/03	REH	5/29/03	REH
12	5/29/03	REH	12	5/29/03	REH	5/29/03	REH
13	5/29/03	REH	13	5/29/03	REH	5/29/03	REH
14	5/29/03	REH	14	5/29/03	REH	5/29/03	REH
15	5/29/03	REH	15	5/29/03	REH	5/29/03	REH
16	5/29/03	REH	16	5/29/03	REH	5/29/03	REH
17	5/29/03	REH	17	5/29/03	REH	5/29/03	REH
18	5/29/03	REH	18	5/29/03	REH	5/29/03	REH
19	5/29/03	REH	19	5/29/03	REH	5/29/03	REH
20	5/29/03	REH	20	5/29/03	REH	5/29/03	REH



DELETED C1, C2, L1, L2,
U1, J3, & W1. MOVED
W2 FROM J6-1,-2 TO J6
-2,-3. JKF

3 8603 11/7/96 RAS

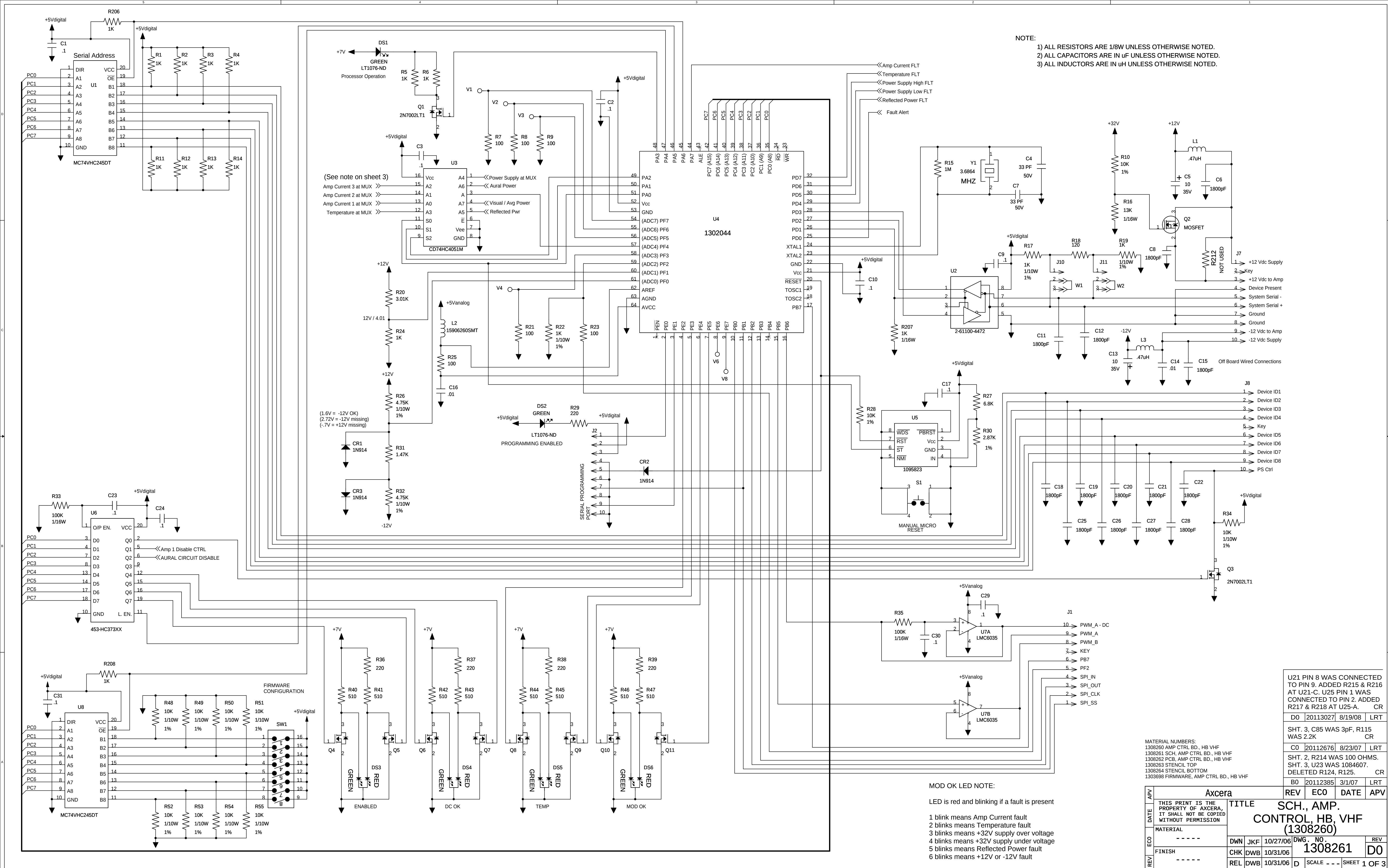
AT J2 W2 WAS W1. (TMY)

2 8424 9/29/96 JCM

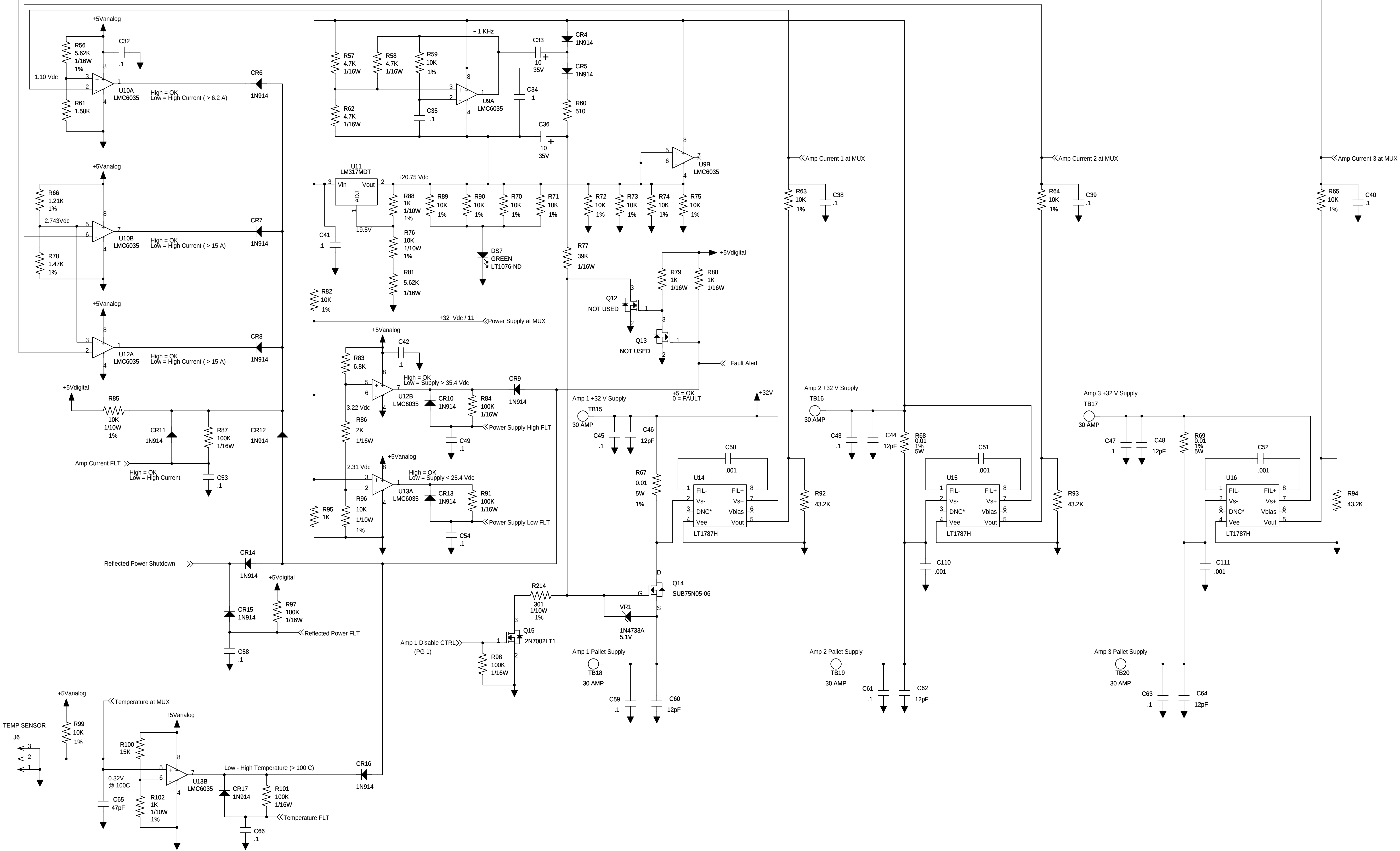
SWITCHED PINS 1 & 2 OF
U2. (TMY)

1 8368 8/27/96 RAS

ITS CORPORATION				REV	ECN	DATE	APV
THIS PRINT IS THE PROPERTY OF ITS CORP IT SHALL NOT BE COPIED WITHOUT PERMISSION				TITLE SCHEMATIC SWITCH BOARD (1527-1406)			
				MATERIAL			
FINISH				DWN	DLM	6/3/96	DWG. NO.
				CHK	RAS	6/14/96	1527-3406
				REL	RAS	6/14/96	3
				SCALE -- SHEET 1 OF 1			

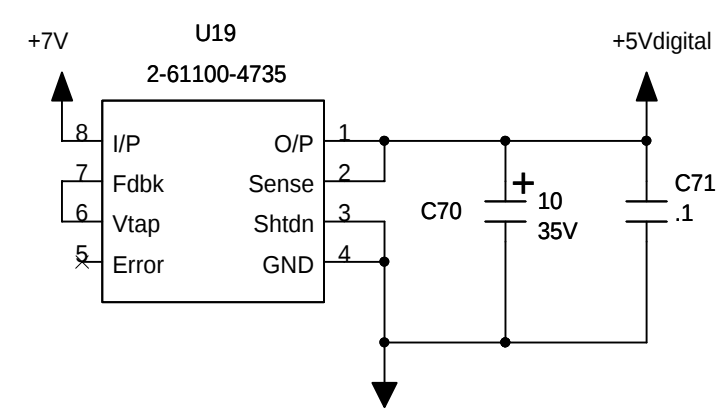
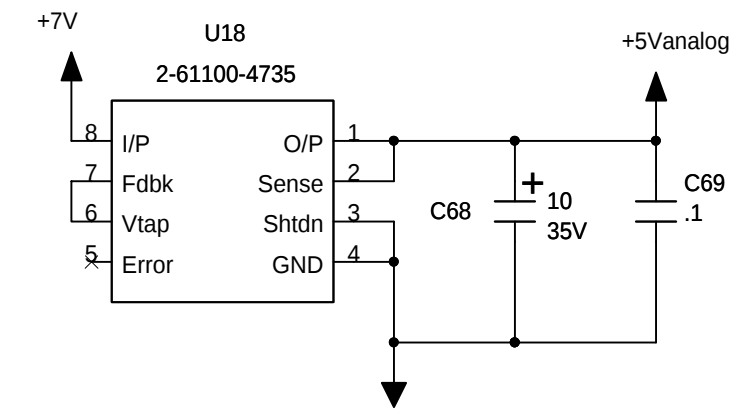
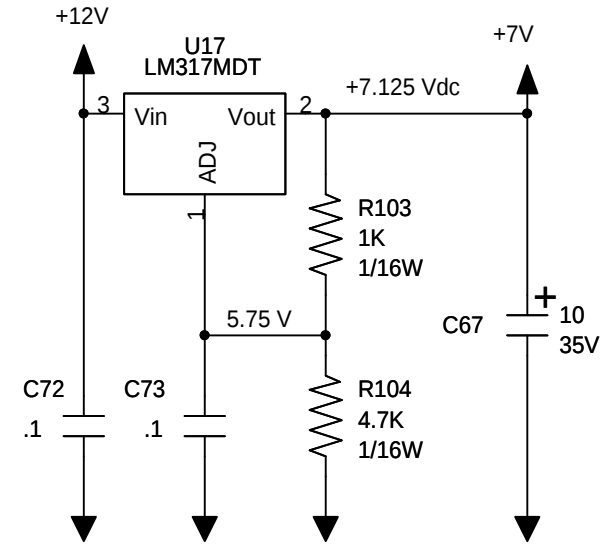


				U21 PIN 8 WAS CONNECTED TO PIN 9. ADDED R215 & R216 AT U21-C. U25 PIN 1 WAS CONNECTED TO PIN 2. ADDED R217 & R218 AT U25-A. CR	
		D0	20113027	8/19/08	LRT
		SHT. 3. C85 WAS 3pF, R115 WAS 2.2K		CR	
		C0	20112676	8/23/07	LRT
		SHT. 2. R214 WAS 100 OHMS. SHT. 3. U23 WAS 1084607. DELETED R124, R125.		CR	
		B0	20112385	3/1/07	LRT
		REV	ECO	DATE	APV
DATE	APV	Xcerra			
DATE	APV	THIS PRINT IS THE PROPERTY OF XCERRA, IT SHALL NOT BE COPIED WITHOUT PERMISSION TITLE SCH., AMP. CONTROL, HB, VHF (1308260)			
ECO	APV	MATERIAL -----			
REV	APV	FINISH -----			
		DWN	JKF	10/27/06	REV
		CHK	DWB	10/31/06	D0
		REL	DWB	10/31/06	D
			SCALE	---	SHEET 1 OF 3



NOTE:

A track width of 0.3 inch is needed between power input vias and sense resistors R55,R56,R57. 0.3 inch track width is also needed between the output of the sense resistors and the output vias that provide power to the amplifier pallets.



APV		Xxcera		REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE		SCH., AMP. CONTROL, HB, VHF (1308260)			
		MATERIAL		DWN JKF 10/27/06 DWG. NO. 1308261			
ECO	FINISH	CHK	DWB	10/31/06	REL	DWB	10/31/06
REV	---	REL	DWB	10/31/06	D	SCALE	SHEET 2 OF 3

