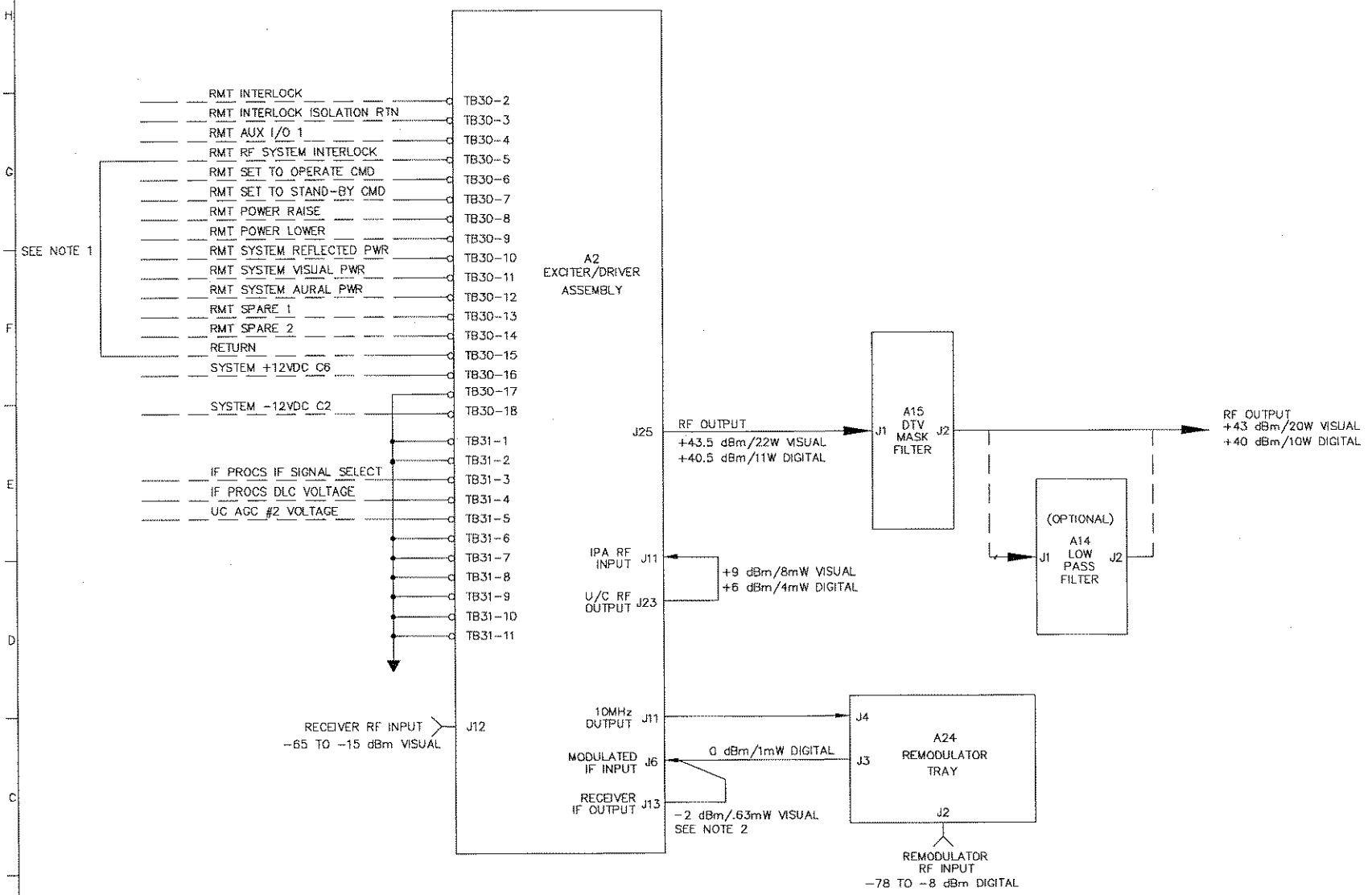


NOTES:

1) WIRE JUMPER FROM TB30-5 TO TB30-15 MUST BE INSTALLED TO PUT THE TRANSMITTER IN THE OPERATE MODE.

2) FOR ANALOG TRANSLATOR OPERATION THE RECEIVER RF OUTPUT AT A2-J13 IS CONNECTED TO THE MODULATED IF INPUT JACK A2-J6 AND THE ON CHANNEL RF INPUT CONNECTS TO A2-J12.
FOR DIGITAL TRANSLATOR OPERATION THE REMODULATOR RF OUTPUT AT A24-J3 IS CONNECTED TO THE MODULATED IF INPUT JACK A2-J6, THE 10MHz INPUT JACK A24-J4 IS CONNECTED TO THE 10 MHz OUTPUT JACK A2-J11, AND THE RF INPUT TO THE REMODULATOR CONNECTS TO A24-J2.

REV	ECO	DATE	APV

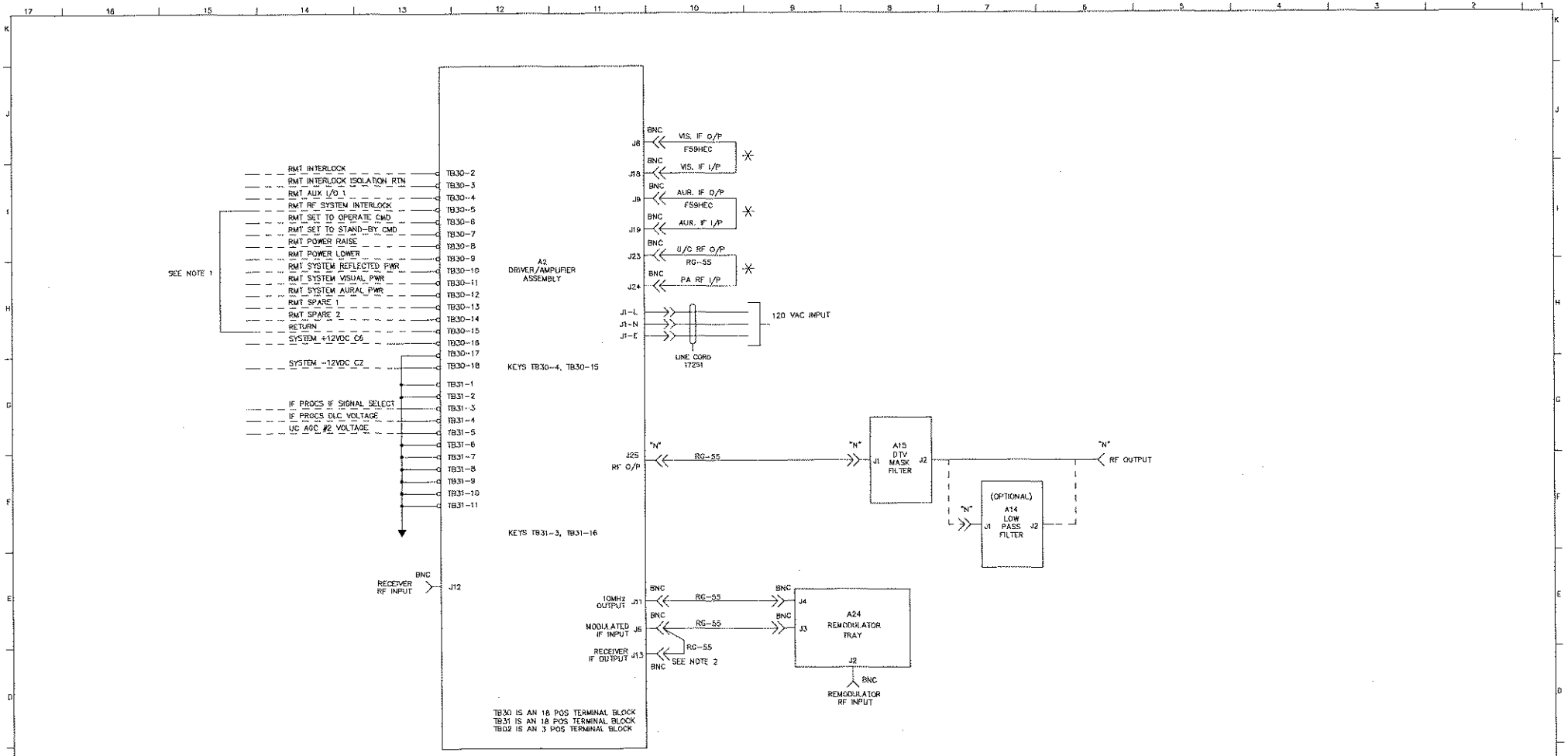
Axcera.

MATERIAL – – – –

FINISH – – – –

TITLE B/D, SYSTEM, VHF TRANSLATOR, w/REMODULATOR, LX SERIES

DWN	CDD	6/29/07	DWG. NO.	REV
CHK	LRT	6/29/07	1309398	A0
REL	LRT	6/29/07	C SCALE – –	SHEET 1 OF 1



NOTES:

1) WIRE JUMPER FROM TB30-5 TO TB30-15 MUST BE INSTALLED TO PUT THE TRANSLATOR IN THE OPERATE MODE.
2) * DENOTES CABLE/WIRE IS PART OF TRANSMITTER ASSY.
3) ALL WIRES ARE 22AWG UNLESS OTHERWISE NOTED.
4) FOR ANALOG TRANSLATOR OPERATION THE RECEIVER RF OUTPUT AT A2-J13 IS CONNECTED TO THE MODULATED IF INPUT JACK A2-J6 AND THE ON CHANNEL RF INPUT CONNECTS TO A2-J12.
   FOR DIGITAL TRANSLATOR OPERATION THE REMODULATOR RF OUTPUT AT A24-J3 IS CONNECTED TO THE MODULATED IF INPUT JACK A2-J6, THE 10MHz INPUT JACK A24-J4 IS CONNECTED TO THE 10 MHz OUTPUT JACK A2-J11, AND THE RF INPUT TO THE REMODULATOR CONNECTS TO A24-J2.

REV	ECO	DATE	APV

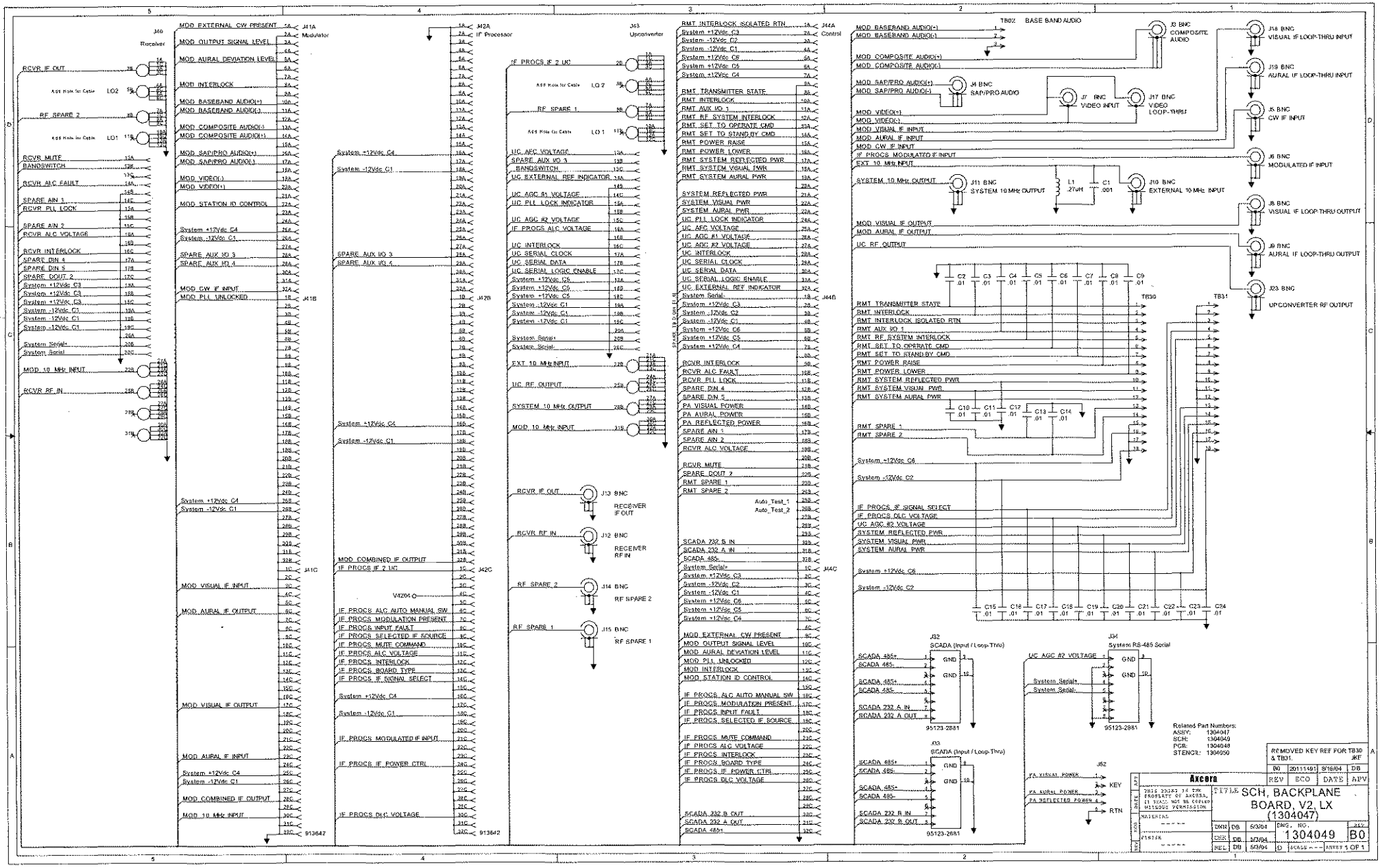
Axcera.

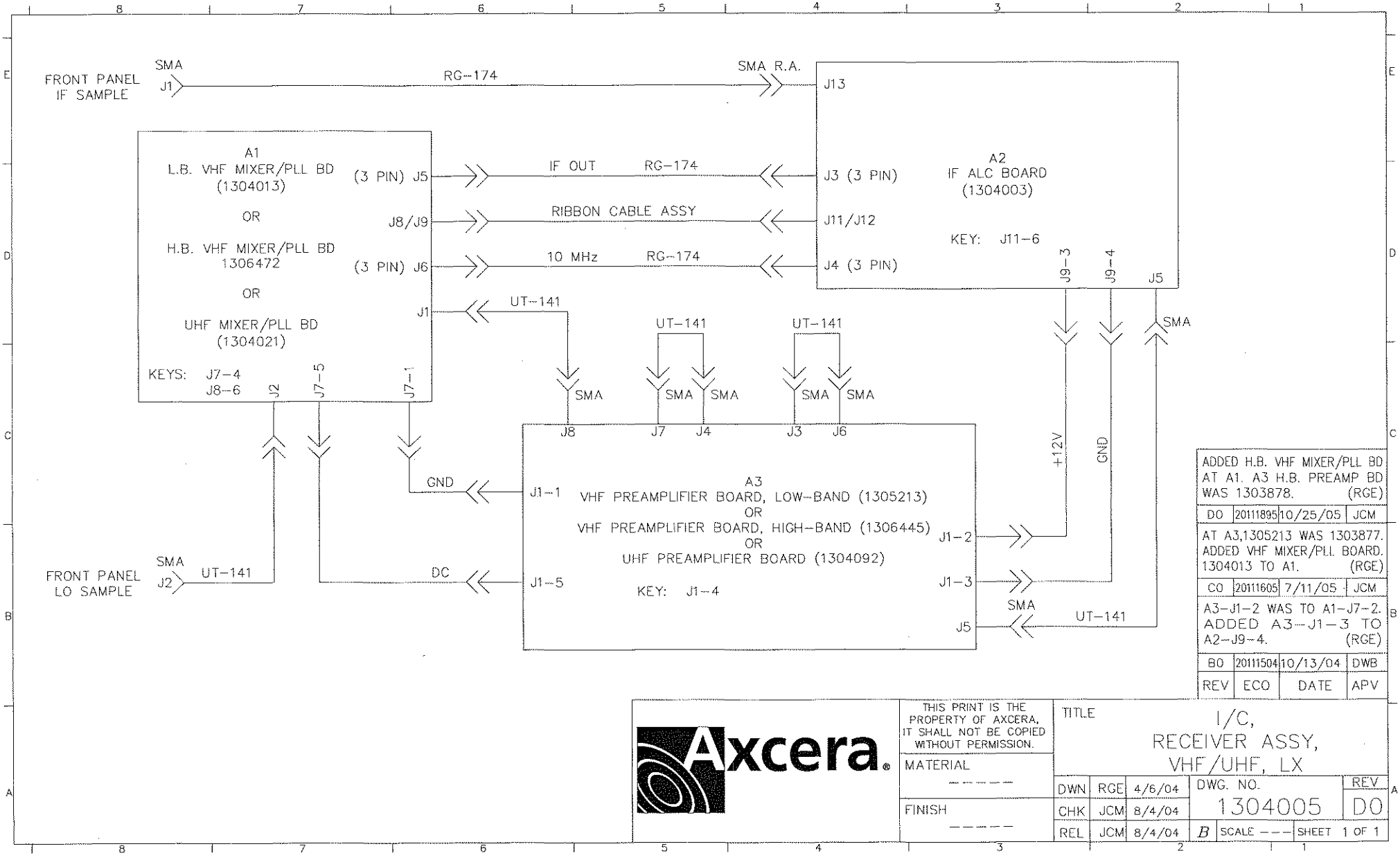
MATERIAL

FINISH

TITLE: I/C, SYSTEM, VHF TRANSLATOR, w/REMODULATOR, LX SERIES

DWN	CDD	6/29/07	DWG. NO. 1309399 REV. A0
CHK	LRT	6/29/07	
REL	LRT	6/29/07	D SCALE 1=1 SHEET 1 OF 1


J46 Receiver
RCVR IF OUT
RF SPARE 2
RCVR MUTE
BANDSWITCH
RCVR ALC FAULT
SPARE AIN 1
RCVR PLL LOCK
SPARE AIN 2
RCVR ALC VOLTAGE
RCVR INTERLOCK
SPARE DIN 4
SPARE DIN 5
SPARE DOUT 2
System +12Vdc C3
System +12Vdc C2
System -12Vdc C3
System -12Vdc C2
System -12Vdc C1
System +12Vdc C1
System Serial+
System Serial-
MOD 10 MHz INPUT
RCVR RF IN
J41A Modulator
MOD EXTERNAL CW PRESENT
MOD OUTPUT SIGNAL LEVEL
MOD AURAL DEVIATION LEVEL
MOD INTERLOCK
MOD BASEBAND AUDIO(+)
MOD BASEBAND AUDIO(-)
MOD COMPOSITE AUDIO(-)
MOD COMPOSITE AUDIO(+)
MOD SAP/PRO AUDIO(+)
MOD SAP/PRO AUDIO(-)
MOD VIDEO(-)
MOD VIDEO(+)
MOD STATION ID CONTROL
System +12Vdc C4
System -12Vdc C1
SPARE AUX I/O 3
SPARE AUX I/O 4
MOD CW IF INPUT
MOD PLL UNLOCKED
J41B
J41C
MOD VISUAL IF INPUT
MOD AURAL IF OUTPUT
MOD AURAL IF INPUT
System +12Vdc C4
System -12Vdc C1
MOD COMBINED IF OUTPUT
MOD 10 MHz INPUT
913642
J42A IF Processor
System +12Vdc C4
System -12Vdc C1
SPARE AUX I/O 3
SPARE AUX I/O 4
System +12Vdc C4
System -12Vdc C1
MOD COMBINED IF OUTPUT
IF PROCS IF 2 I/C
J42C
V4Z04
IF PROCS ALC AUTO MANUAL SW
IF PROCS MODULATION PRESENT
IF PROCS INPUT FAULT
IF PROCS SELECTED IF SOURCE
IF PROCS MUTE COMMAND
IF PROCS ALC VOLTAGE
IF PROCS INTERLOCK
IF PROCS BOARD TYPE
IF PROCS IF SIGNAL SELECT
System +12Vdc C4
System -12Vdc C1
IF PROCS MODULATED IF INPUT
IF PROCS IF POWER CTRL
IF PROCS DLC VOLTAGE
913642
J43 Upconverter
IF PROCS IF 2 I/C
RF SPARE 1
UC AFC VOLTAGE
SPARE AUX I/O 3
BANDSWITCH
UC EXTERNAL REF INDICATOR
UC AGC #1 VOLTAGE
UC PLL LOCK INDICATOR
UC AGC #2 VOLTAGE
IF PROCS ALC VOLTAGE
UC INTERLOCK
UC SERIAL CLOCK
UC SERIAL DATA
UC SERIAL LOGIC ENABLE
System +12Vdc C5
System -12Vdc C1
System Serial-
System Serial+
EXT 10 MHz INPUT
UC RF OUTPUT
SYSTEM 10 MHz OUTPUT
MOD 10 MHz INPUT
RCVR IF OUT
J13 BNC RECEIVER IF OUT
RCVR RF IN
J12 BNC RECEIVER RF IN
RF SPARE 2
J14 BNC RF SPARE 2
RF SPARE 1
J15 BNC RF SPARE 1
J44A Control
RMT INTERLOCK ISOLATED RTN
System +12Vdc C3
System -12Vdc C2
System -12Vdc C1
System +12Vdc C6
System +12Vdc C5
System +12Vdc C4
RMT TRANSMITTER STATE
RMT INTERLOCK
RMT AUX I/O 1
RMT RF SYSTEM INTERLOCK
RMT SET TO OPERATE CMD
RMT SET TO STAND BY CMD
RMT POWER RAISE
RMT POWER LOWER
RMT SYSTEM REFLECTED PWR
RMT SYSTEM VISUAL PWR
RMT SYSTEM AURAL PWR
SYSTEM REFLECTED PWR
SYSTEM VISUAL PWR
SYSTEM AURAL PWR
UC PLL LOCK INDICATOR
UC AFC VOLTAGE
UC AGC #1 VOLTAGE
UC AGC #2 VOLTAGE
UC INTERLOCK
UC SERIAL CLOCK
UC SERIAL DATA
UC SERIAL LOGIC ENABLE
UC EXTERNAL REF INDICATOR
System Serial-
J44B
RCVR INTERLOCK
RCVR ALC FAULT
RCVR PLL LOCK
SPARE DIN 4
SPARE DIN 5
PA VISUAL POWER
PA AURAL POWER
PA REFLECTED POWER
SPARE AIN 1
SPARE AIN 2
RCVR ALC VOLTAGE
RCVR MUTE
SPARE DOUT 2
RMT SPARE 1
RMT SPARE 2
Auto_Test_1
Auto_Test_2
SCADA 232 B IN
SCADA 232 A IN
SCADA 485-
System Serial+
System +12Vdc C3
System -12Vdc C2
System -12Vdc C1
System +12Vdc C6
System +12Vdc C5
System +12Vdc C4
J44C
MOD EXTERNAL CW PRESENT
MOD OUTPUT SIGNAL LEVEL
MOD AURAL DEVIATION LEVEL
MOD PLL UNLOCKED
MOD INTERLOCK
MOD STATION ID CONTROL
IF PROCS ALC AUTO MANUAL SW
IF PROCS MODULATION PRESENT
IF PROCS INPUT FAULT
IF PROCS SELECTED IF SOURCE
IF PROCS MUTE COMMAND
IF PROCS ALC VOLTAGE
IF PROCS INTERLOCK
IF PROCS BOARD TYPE
IF PROCS IF POWER CTRL
IF PROCS DLC VOLTAGE
SCADA 232 B OUT
SCADA 232 A OUT
SCADA 485+
TB02 BASE BAND AUDIO
MOD BASEBAND AUDIO(+)
MOD BASEBAND AUDIO(-)
MOD COMPOSITE AUDIO(+)
MOD COMPOSITE AUDIO(-)
MOD SAP/PRO AUDIO(+)
MOD SAP/PRO AUDIO(-)
MOD VIDEO(+)
MOD VIDEO(-)
MOD VISUAL IF INPUT
MOD AURAL IF INPUT
MOD CW IF INPUT
IF PROCS MODULATED IF INPUT
EXT 10 MHz INPUT
SYSTEM 10 MHz OUTPUT
MOD VISUAL IF OUTPUT
MOD AURAL IF OUTPUT
UC RF OUTPUT
J8 BNC COMPOSITE AUDIO
J4 BNC SAP/PRO AUDIO
J7 BNC VIDEO INPUT
J17 BNC VIDEO LOOP-THRU
J11 BNC SYSTEM 10 MHz OUTPUT
L1 .27uH
C1 .001
J10 BNC EXTERNAL 10 MHz INPUT
J16 BNC VISUAL IF LOOP-THRU INPUT
J18 BNC AURAL IF LOOP-THRU INPUT
J5 BNC CW IF INPUT
J6 BNC MODULATED IF INPUT
J48 BNC VISUAL IF LOOP-THRU OUTPUT
J9 BNC AURAL IF LOOP-THRU OUTPUT
J23 BNC UPCONVERTER RF OUTPUT
C2 .01
C3 .01
C4 .01
C5 .01
C6 .01
C7 .01
C8 .01
C9 .01
C10 .01
C11 .01
C12 .01
C13 .01
C14 .01
C15 .01
C16 .01
C17 .01
C18 .01
C19 .01
C20 .01
C21 .01
C22 .01
C23 .01
C24 .01
TB30
TB31
J32 SCADA (Input / Loop-Thru)
SCADA 485+
SCADA 485-
SCADA 485+
SCADA 485-
SCADA 232 A IN
SCADA 232 A OUT
GND
95123-2681
J33 SCADA (Input / Loop-Thru)
SCADA 485+
SCADA 485-
SCADA 485+
SCADA 485-
SCADA 232 B IN
SCADA 232 B OUT
95123-2681
J34 System RS-485 Social
UC AGC #2 VOLTAGE
System Serial+
System Serial-
95123-2681
J52
KEY
PA VISUAL POWER
PA AURAL POWER
PA REFLECTED POWER
RTN
Related Part Numbers:
ASSY: 1304047
SCH: 1304049
PCB: 1304048
STENCIL: 1304050
REMOVED KEY REF FOR TB30 & TB31. JKF
B0 20111491 9/16/04 DB
REV ECO DATE APV
Axcera
THIS ITEM IS THE PROPERTY OF AXCERA, IT MAY NOT BE COPIED WITHOUT PERMISSION
TITLE SCH, BACKPLANE BOARD, V2, LX (1304047)
DWN DB 5/3/04
CHK DB 5/3/04
APP DB 5/3/04
DWG. NO. 1304049
REV B0
SCALE --- SHEET 1 OF 1



ADDED H.B. VHF MIXER/PLL BD AT A1. A3 H.B. PREAMP BD WAS 1303878. (RGE)			
D0	20111895	10/25/05	JCM
AT A3,1305213 WAS 1303877. ADDED VHF MIXER/PLL BOARD, 1304013 TO A1. (RGE)			
C0	20111605	7/11/05	JCM
A3-J1-2 WAS TO A1-J7-2. ADDED A3-J1-3 TO A2-J9-4. (RGE)			
B0	20111504	10/13/04	DWB
REV	ECO	DATE	APV

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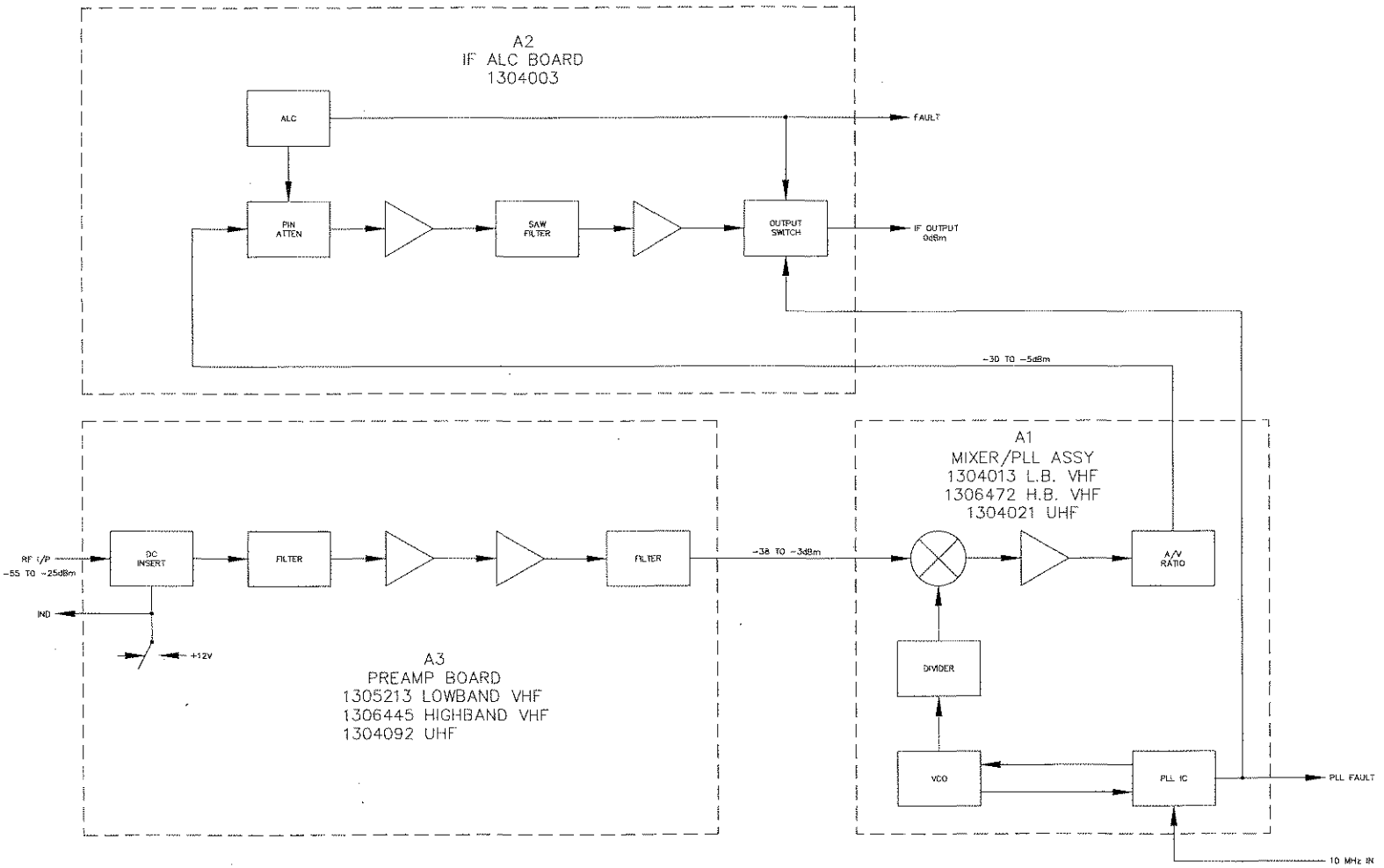
MATERIAL ———

FINISH ———

TITLE: I/C, RECEIVER ASSY, VHF/UHF, LX

DWN	RGE	4/6/04	DWG. NO. 1304005	REV D0	
CHK	JCM	8/4/04			
REL	JCM	8/4/04	B	SCALE ———	SHEET 1 OF 1



REV	ECO	DATE	APV
CO	20111805	10/25/05	JCH
BD	20111821	7/5/05	LRT

ADDED H.B. VHF MIXER/PLL BD AT A1. A3 H.B. PREAMP BD WAS 1303878. (RGE)

A3 LOWBAND VHF PYRE-AMP BD WAS 1303877. (RGE)

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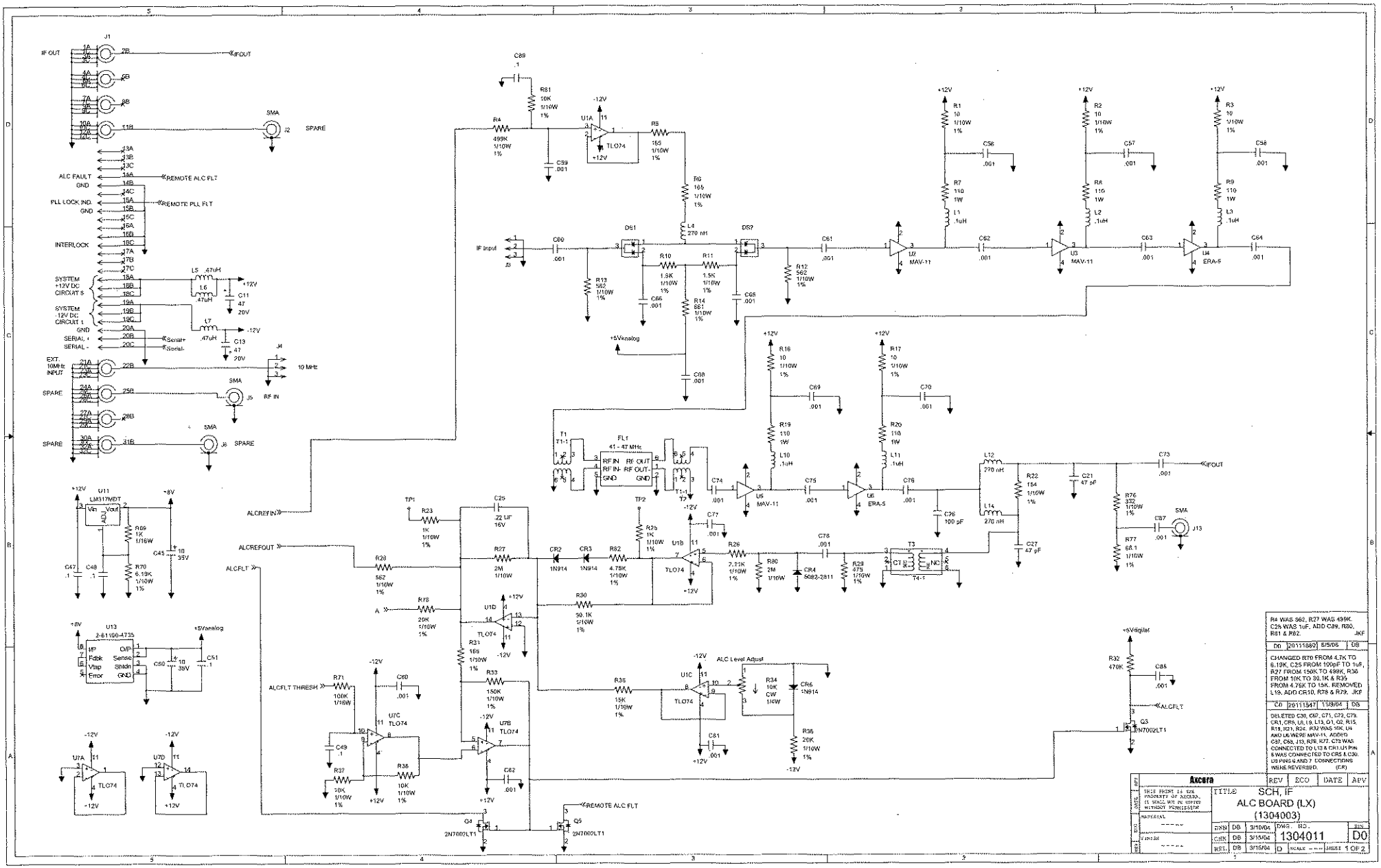
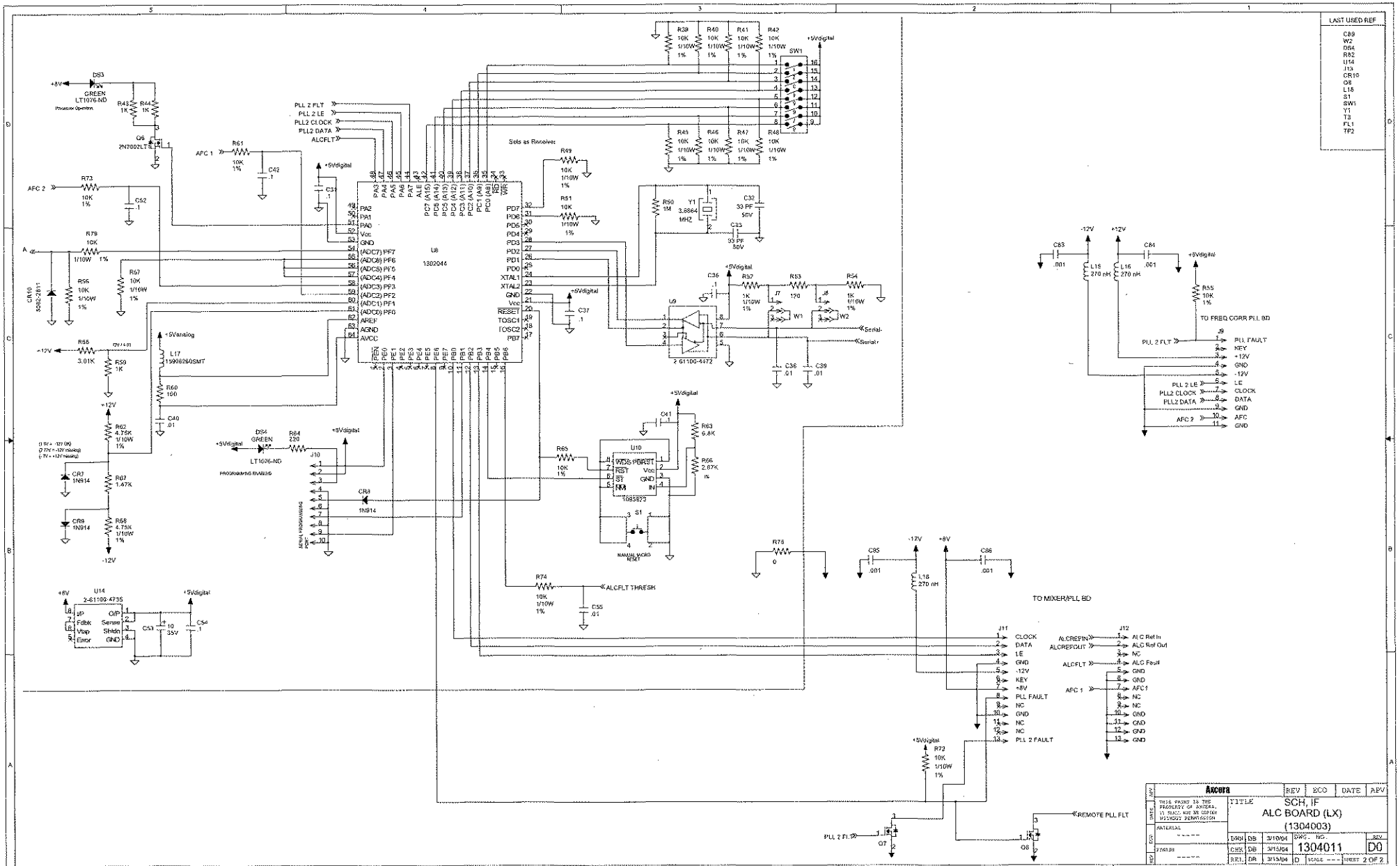
MATERIAL

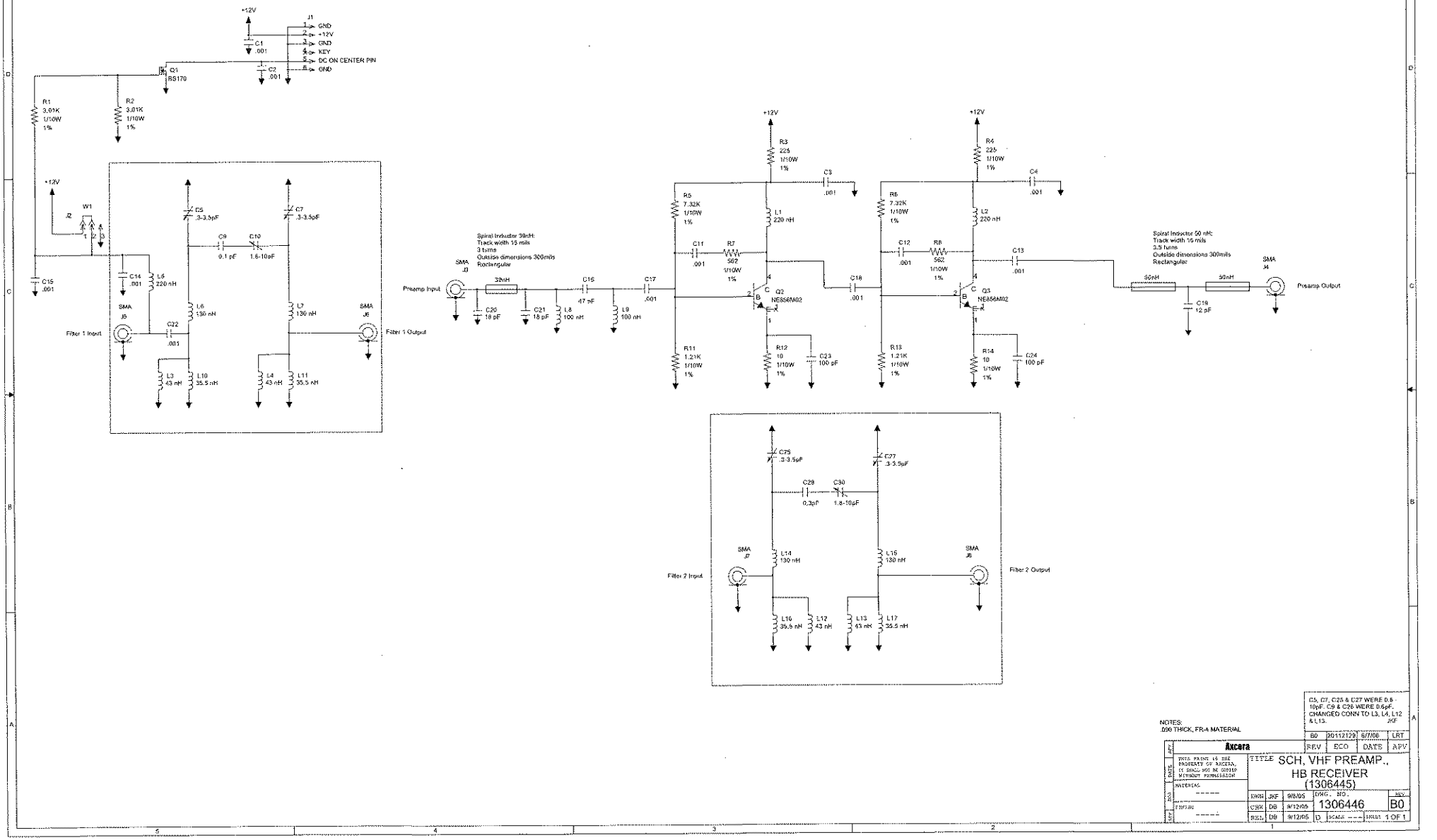
FINISH

TITLE: B/D, RECEIVER ASSEMBLY, VHF/UHF LX

DWN	RGE	2/4/04	DWG. NO. 1304004 REV CO
CHK	DWB	8/26/04	
REL	DWB	8/26/04	D SCALE --- SHEET 1 OF 1


IF OUT
IFOUT
SMA
J2
SPARE
ALC FAULT
GND
REMOTE ALC FLT
PLL LOCK IND.
GND
REMOTE PLL FLT
INTERLOCK
SYSTEM +12V DC CIRCUITS
SYSTEM -12V DC CIRCUIT 1
GND
SERIAL +
SERIAL -
Serial+
Serial-
EXT. 10MHz INPUT
10 MHz
SPARE
SMA
J5
RF IN
SPARE
SMA
J6
SPARE
IF Input
+5Vanalog
FL1
41 - 47 MHz
RF IN
RF IN-
GND
RF OUT
RF OUT-
GND
ALCREFIN
ALCREFOUT
ALCFLT
ALCFLT THRESH
ALC Level Adjust
REMOTE ALC FLT
+5Vdigital
IFOUT
SMA
J13
Axcera
SCH, IF
ALC BOARD (LX)
(1304003)
1304011
D0
SHEET 1 OF 2


LAST USED REF
C89
W2
D64
R82
U14
J13
CR10
Q8
L18
S1
SW3
Y1
T3
FL1
TP2
Sets as Receive
PLL 2 FLT
PLL 2 LE
PLL2 CLOCK
PLL2 DATA
ALCFLT
AFC 1
AFC 2
+5Vdigital
+5Vanalog
+8V
-8V
+12V
-12V
U8
1302044
U9
U10
U14
J10
J11
J12
SW1
W1
W2
Y1
3.6864 MHZ
TO MIXER/PLL BD
TO FREQ CORR PLL BD
REMOTE PLL FLT
ALC REF In
ALC Ref Out
ALC Fault
PLL FAULT
PLL 2 FAULT
Axcera
SCH, IF
ALC BOARD (LX)
(1304003)
1304011
D0
SHEET 2 OF 2



NOTES:
.090 THICK, FR-4 MATERIAL

C5, C7, C25 & C27 WERE 0.8 - 10pF. C9 & C26 WERE 0.5pF. CHANGED CONN TO L3, L4, L12 & L13.

REV	ECO	DATE	APV
B0	20112129	6/7/06	LRT

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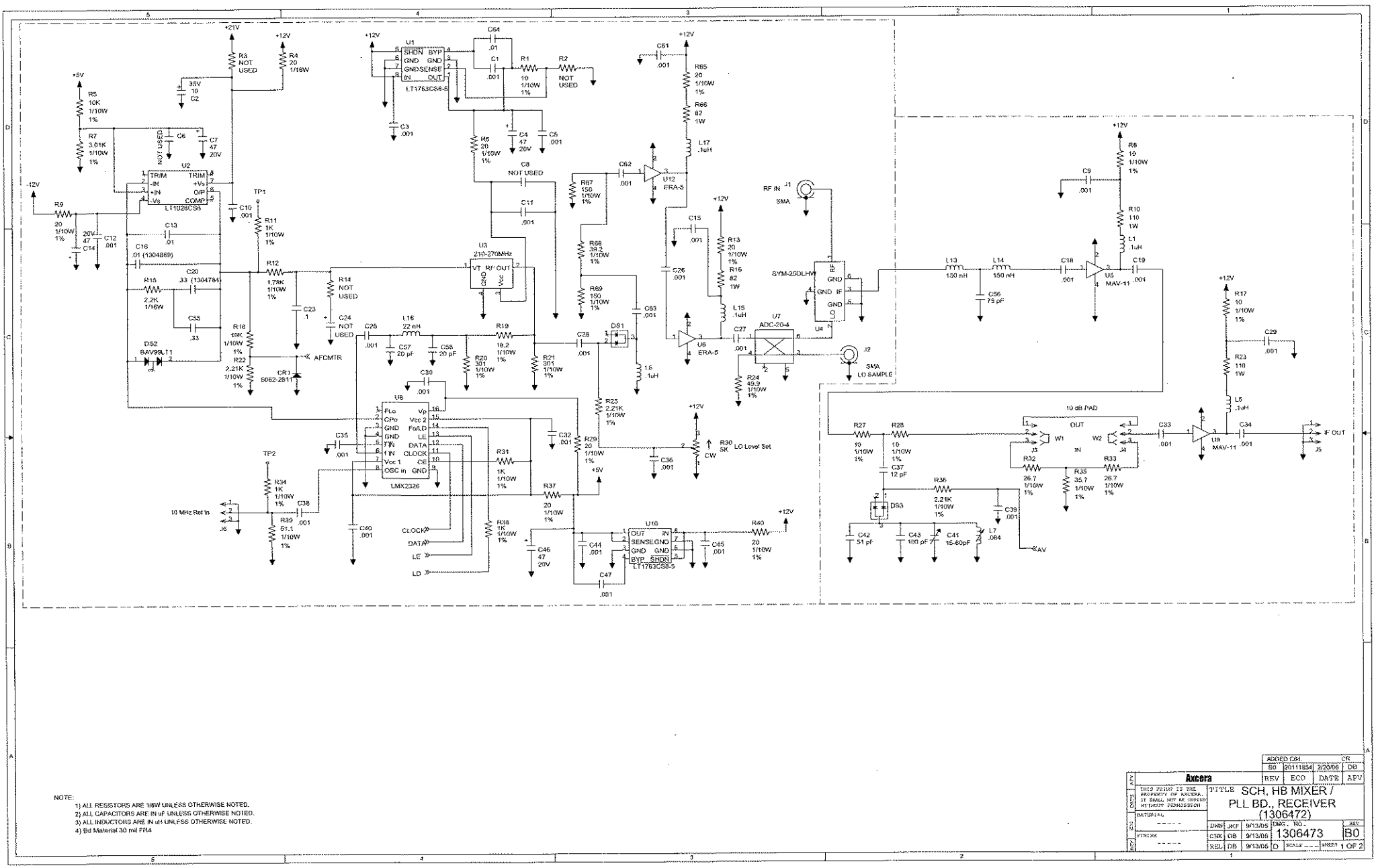
MATERIAL: ---

FINISH: ---

TITLE: SCH, VHF PREAMP., HB RECEIVER (1306445)

DRN	JKF	9/8/05	DWG. NO. 1306446 REV. B0
CHK	DB	9/12/05	
ENGR	DB	9/12/05	SCALE --- SHEET 1 OF 1



NOTE:
1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.
4) Bd Material 30 mil FR4

REV	ECO	DATE	APV
ADDED C64.			CR
B0	20111854	2/20/06	DB

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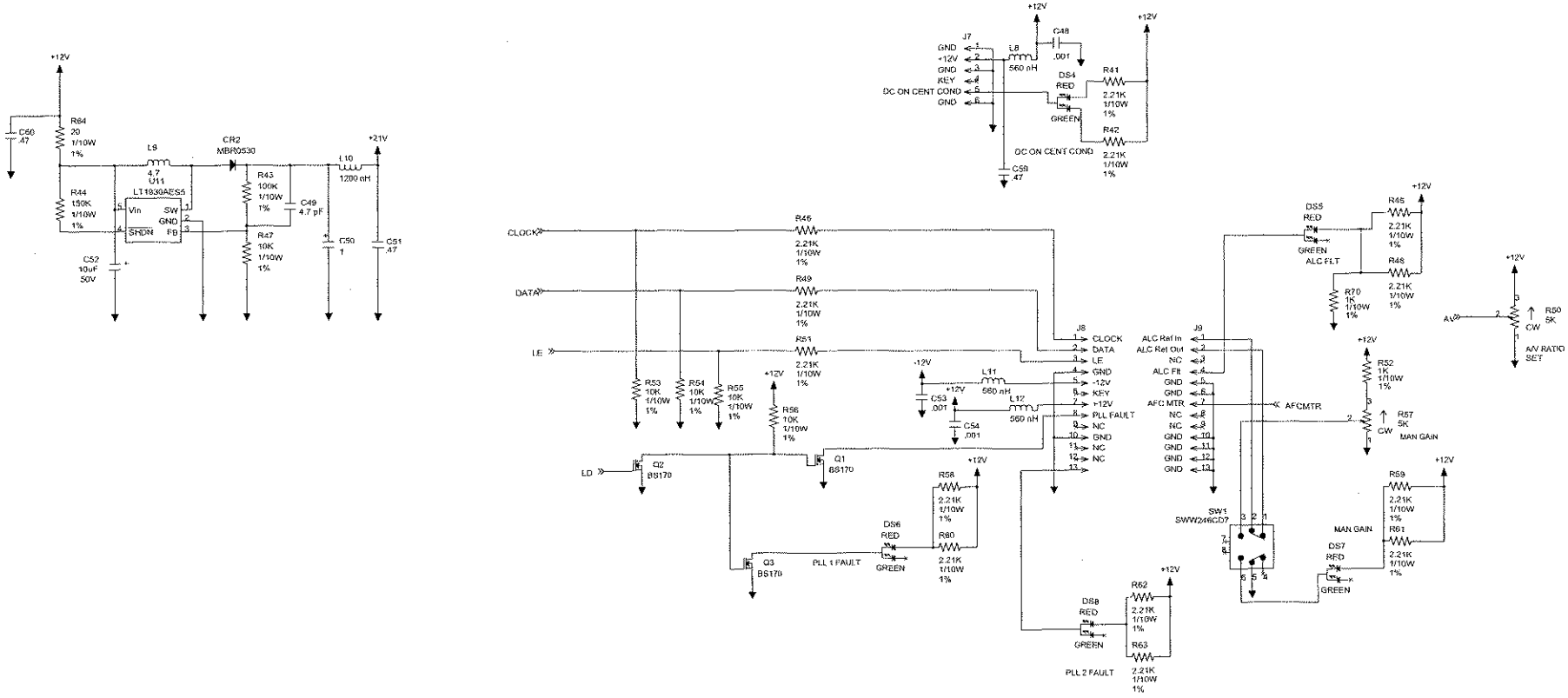
MATERIAL

FINISH

TITLE: SCH, HB MIXER / PLL BD., RECEIVER (1306472)

DWN	JKF	9/13/05	DWG. NO. 1306473 REV B0
CHK	DB	9/13/05	
ENGR	DB	9/13/05	D SCALE - - - SHEET 1 OF 2



Axcera	REV	ECO	DATE	APV

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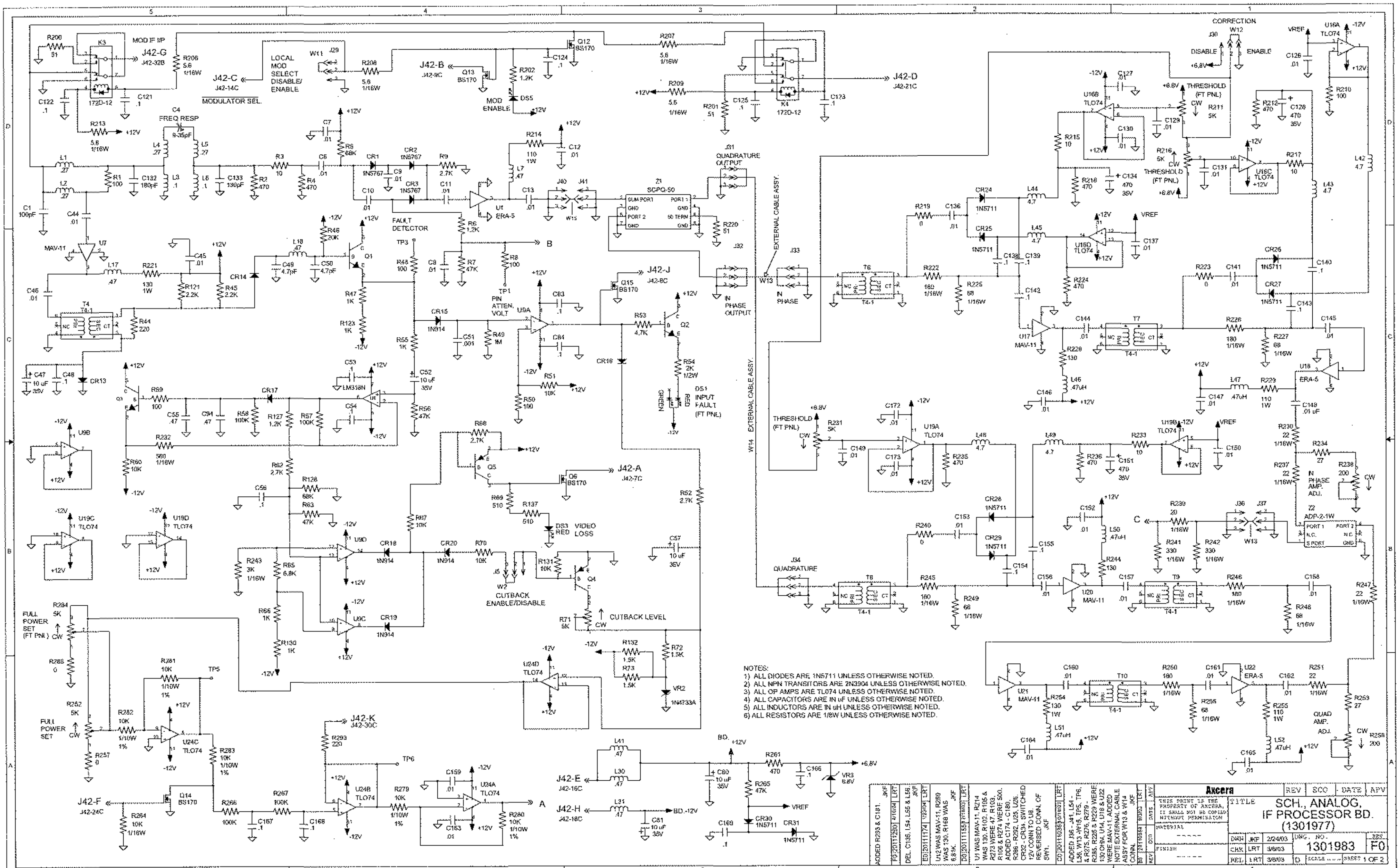
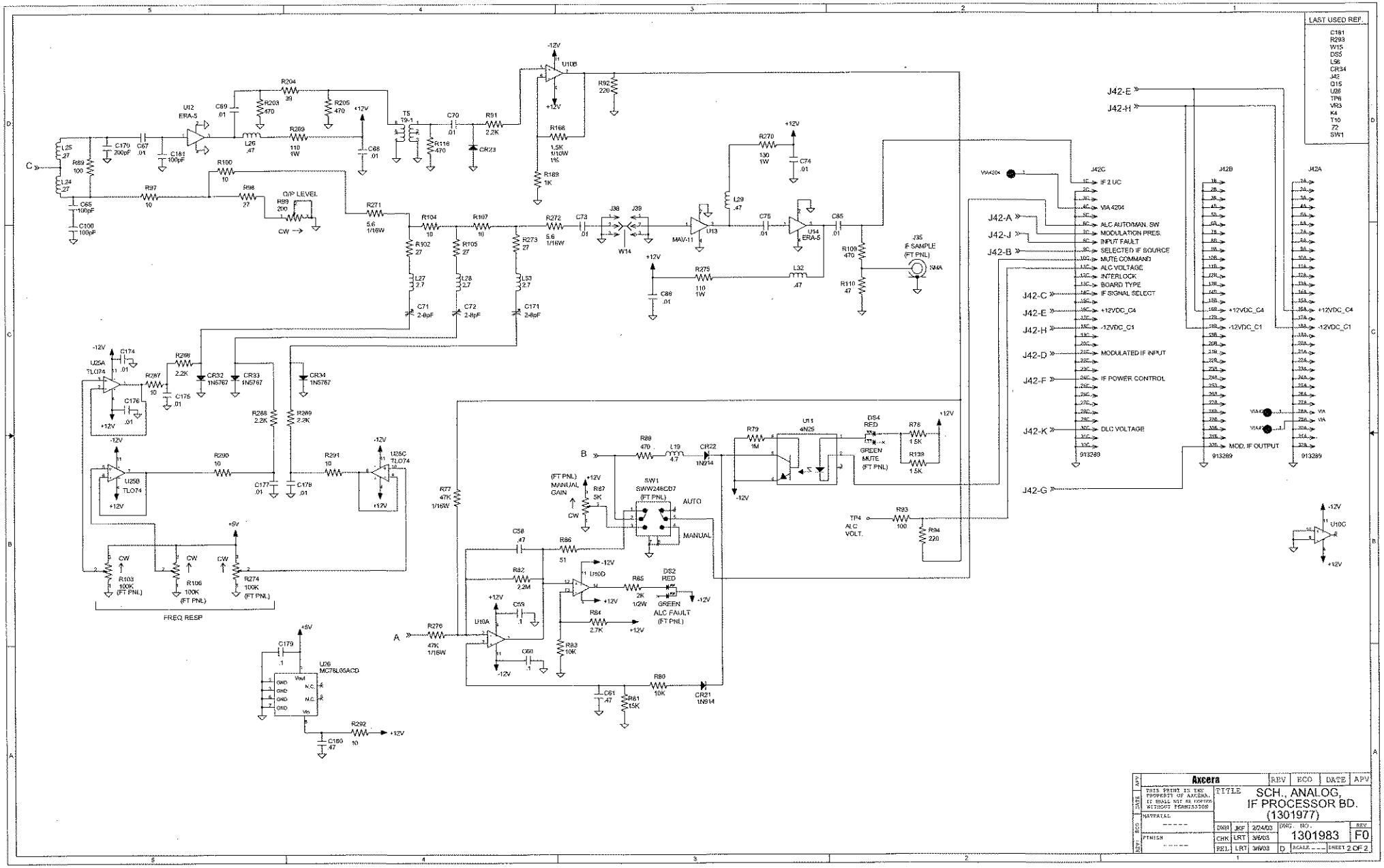
TITLE: SCH, HB MIXER / PLL BD., RECEIVER (1306472)

DWN	JKF	9/13/05	DWG. NO. 1306473	REV B0
CHK	DB	9/13/05		
REL	DB	9/13/05	D SCALE ----	SHEET 2 OF 2



NOTES:
1) ALL DIODES ARE 1N5711 UNLESS OTHERWISE NOTED.
2) ALL NPN TRANSISTORS ARE 2N3904 UNLESS OTHERWISE NOTED.
3) ALL OP AMPS ARE TL074 UNLESS OTHERWISE NOTED.
4) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
5) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.
6) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
Axcera
THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION
TITLE
SCH., ANALOG, IF PROCESSOR BD. (1301977)
DWG. NO. 1301983
REV F0
DRN JKF 2/24/03
CHK LRT 3/6/03
REL LRT 3/6/03
SHEET 1 OF 2
MODULATOR SEL.
LOCAL MOD SELECT DISABLE/ ENABLE
MOD ENABLE
FREQ RESP
FAULT DETECTOR
PIN ATTEN. VOLT
INPUT FAULT (FT PNL)
VIDEO LOSS
CUTBACK ENABLE/DISABLE
CUTBACK LEVEL
FULL POWER SET (FT PNL)
FULL POWER SET
QUADRATURE OUTPUT
IN PHASE OUTPUT
EXTERNAL CABLE ASSY.
CORRECTION
DISABLE
ENABLE
THRESHOLD (FT PNL)
IN PHASE AMP. ADJ.
QUAD AMP. ADJ.
QUADRATURE
IN PHASE



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REV	ECO	DATE	APV

TITLE: SCH., ANALOG, IF PROCESSOR BD. (1301977)

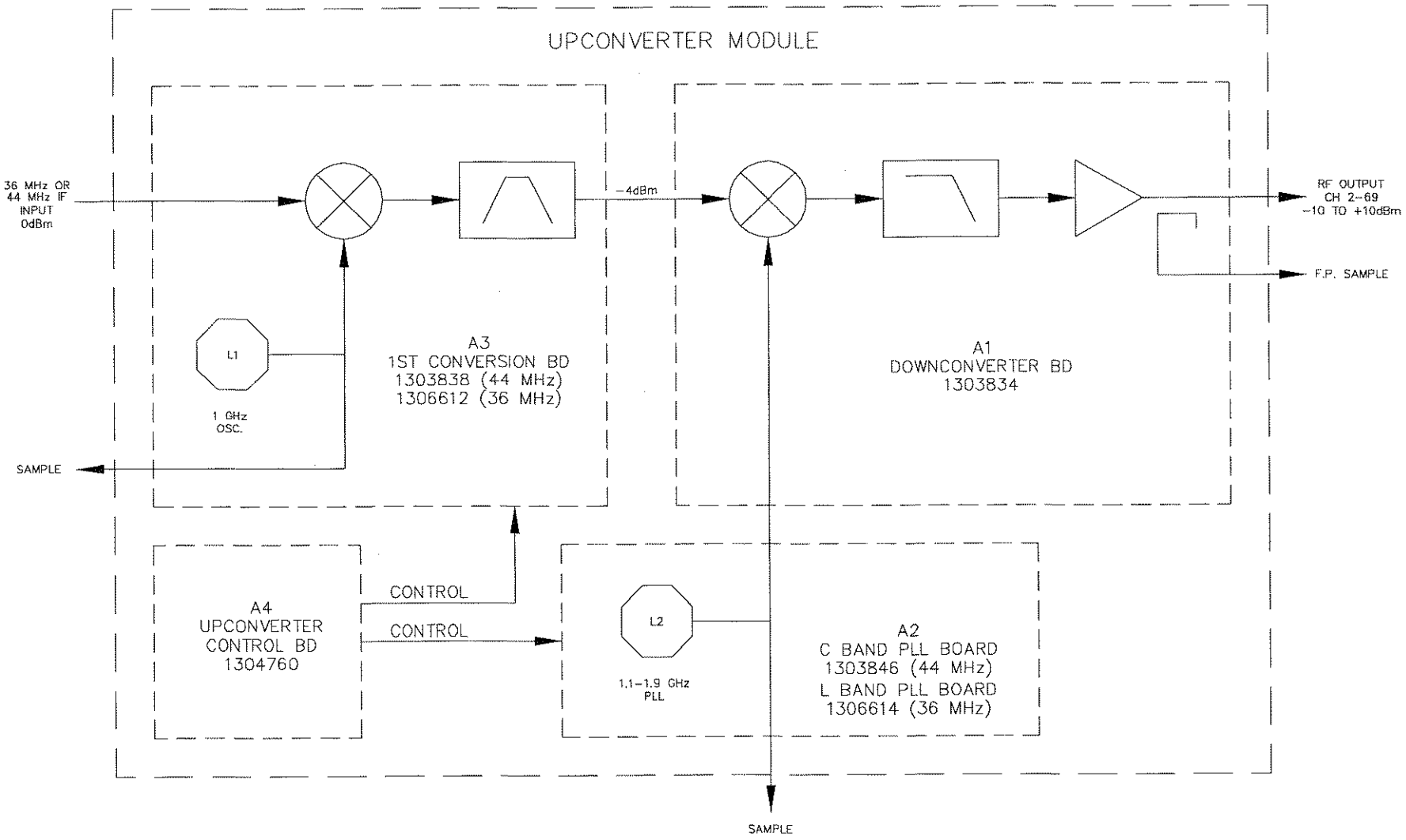
MATERIAL: -----

FINISH: -----

DWN	JKF	2/24/03	
CHK	LRT	3/6/03	
APV	LRT	3/6/03	

DWG. NO. 1301983 REV F0

SCALE: ---- SHEET 2 OF 2



REV	ECO	DATE	APV

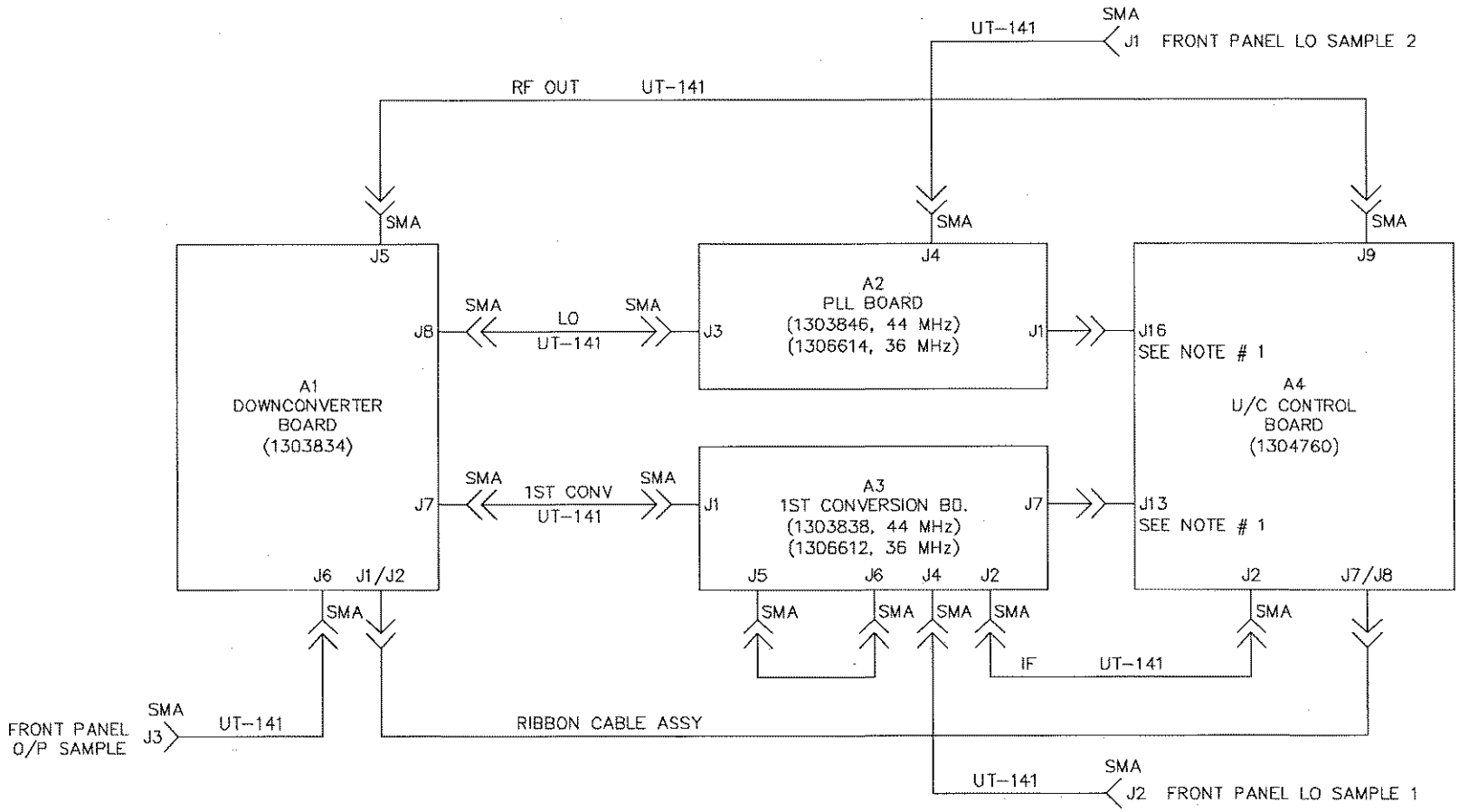
Axcera.

MATERIAL ------

FINISH ------

TITLE: B/D, U/C ASSEMBLY, VHF/UHF LX

DWN	RGE	5/7/04	DWG. NO. 1303830 REV A0
CHK	DWB	9/30/04	
REL	DWB	9/30/04	C SCALE ~~~ SHEET 1 OF 1



NOTES:
1. CONNECTORS ARE BOARD TO BOARD AND NOT PART OF THE HARNESS.

A2-J3 WAS A2-J2 (TYPO)			RT
B0	20111728	4/1/05	DB
REV	ECO	DATE	APV

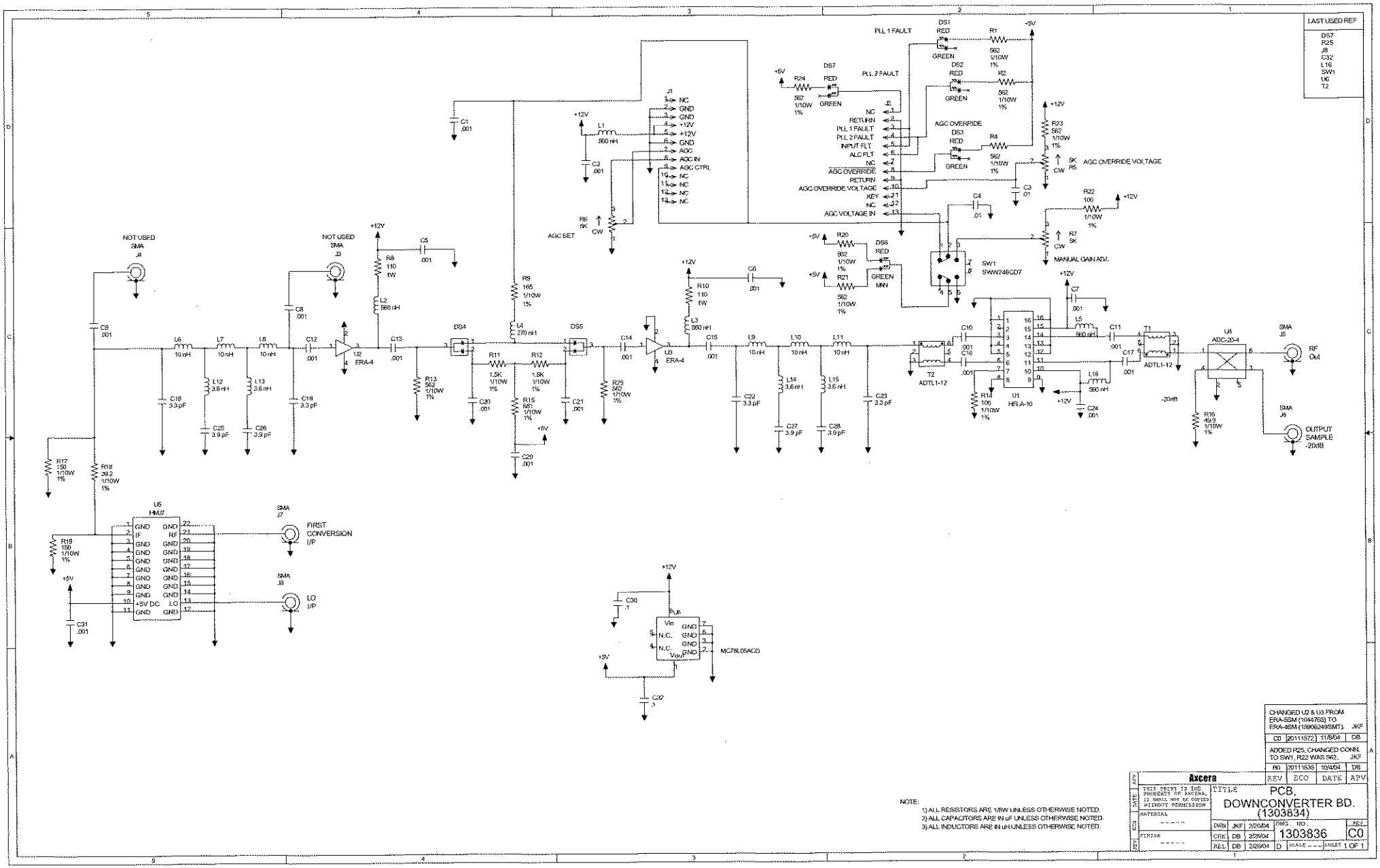
Axcera

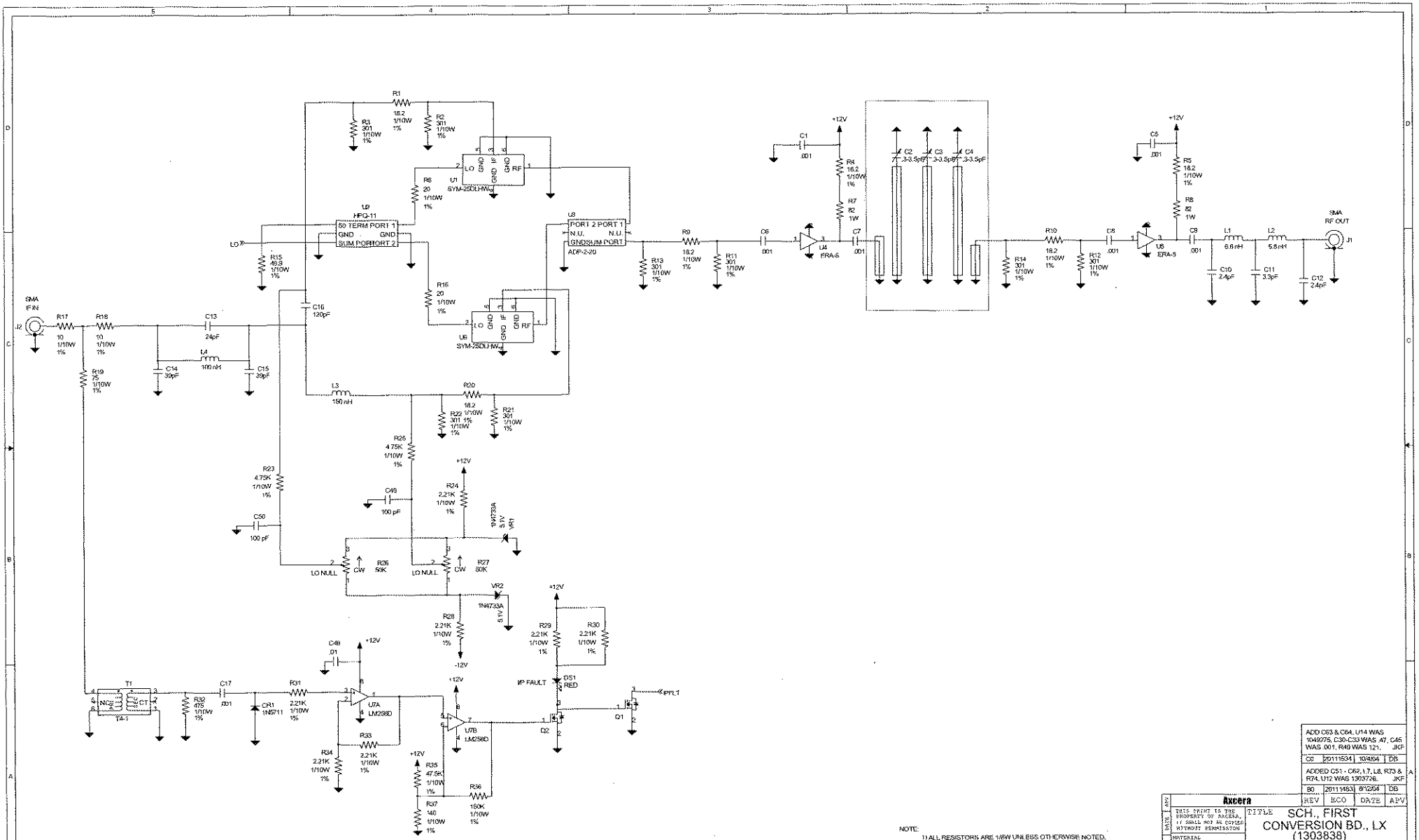
MATERIAL ------

FINISH ------

TITLE I/C, . UPCONVERTER ASSY, VHF/UHF, LX

DWN	RGE	04/06/04	DWG. NO.		REV
CHK	DWB	9/30/04	1303831		B0
REL	DWB	9/30/04	B	SCALE ---	SHEET 1 OF 1


LAST USED REF
DS7
R25
J8
C32
L16
SW1
U6
T2
PLL 1 FAULT
PLL 2 FAULT
AGC OVERRIDE
AGC OVERRIDE VOLTAGE
MANUAL GAIN ADJ.
SW1
SWW246CD7
NOT USED
SMA
J4
NOT USED
SMA
J3
AGC SET
U2
ERA-4
U3
ERA-4
U4
ADC-20-4
U1
HELA-10
T2
ADTL1-12
T3
ADTL1-12
SMA
J5
RF
Out
SMA
J6
OUTPUT
SAMPLE
-20dB
-20dB
U5
HMJ7
SMA
J7
FIRST
CONVERSION
I/P
SMA
J8
LO
I/P
U6
MC78L05ACD
NOTE:
1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.
CHANGED U2 & U3 FROM ERA-5SM (1044765) TO ERA-4SM (15906249SMT). JKF
C0 20111572 11/8/04 DB
ADDED R25, CHANGED CONN. TO SW1, R22 WAS 562. JKF
R0 20111535 10/4/04 DB
Axcera
REV ECO DATE APV
THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION
TITLE
PCB, DOWNCONVERTER BD. (1303834)
MATERIAL
FINISH
DWN JKF 2/20/04
CHK DB 2/20/04
REL DB 2/20/04
DWG NO. 1303836
REV C0
D
SCALE ---
SHEET 1 OF 1



NOTE:
1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.

ADD C63 & C64, U14 WAS 1049275, C30-C33 WAS .47, C45 WAS .001, R49 WAS 121. JKF

REV	ECO	DATE	APV
C0	20111534	10/4/04	DB

ADDED C51 - C62, L7, L8, R73 & R74. U12 WAS 1303736. JKF

REV	ECO	DATE	APV
B0	20111483	8/12/04	DB

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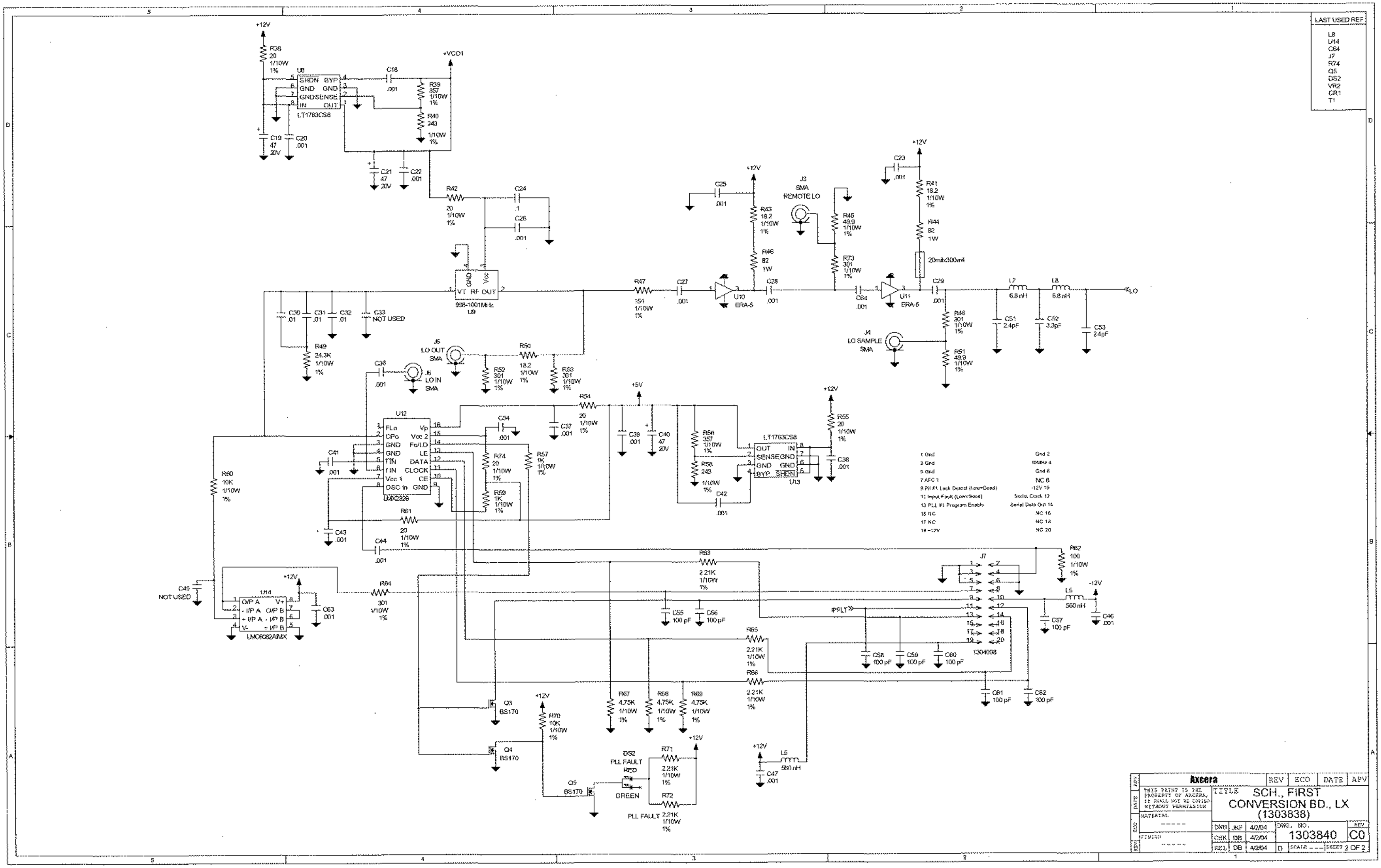
MATERIAL ----- FINISH -----

TITLE: SCH., FIRST CONVERSION BD., LX (1303838)

DWN	JKF	4/2/04	
CHK	DB	4/2/04	
REL	DB	4/2/04	D

DWG. NO. 1303840 REV C0

SCALE ----- SHEET 1 OF 2


LAST USED REF
L8
U14
C64
J7
R74
Q5
DS2
VR2
CR1
T1
+12V
+VCO1
R38 20 1/10W 1%
U8
SHDN BYP
GND GND
GND SENSE
IN OUT
LT1763CS8
C18 .001
R39 357 1/10W 1%
R40 243 1/10W 1%
C19 47 20V
C20 .001
C21 47 20V
C22 .001
R42 20 1/10W 1%
C24 .1
C26 .001
GND Vcc
VT RF OUT
998-1001MHz
U9
C30 .01
C31 .01
C32 .01
C33 NOT USED
R49 24.3K 1/10W 1%
J5 LO OUT SMA
R50 18.2 1/10W 1%
R52 301 1/10W 1%
R53 301 1/10W 1%
C35 .001
J6 LO IN SMA
R47 154 1/10W 1%
C27 .001
U10 ERA-5
C25 .001
R43 18.2 1/10W 1%
R46 82 1W
C28 .001
J3 SMA REMOTE LO
R45 49.9 1/10W 1%
R73 301 1/10W 1%
C64 .001
U11 ERA-5
C23 .001
R41 18.2 1/10W 1%
R44 82 1W
20milx300mil
C29 .001
L7 6.8nH
L8 6.8nH
LO
C51 2.4pF
C52 3.3pF
C53 2.4pF
R48 301 1/10W 1%
J4 LO SAMPLE SMA
R51 49.9 1/10W 1%
+5V
U12
FLo Vp
CPo Vcc 2
GND Fo/LD
GND LE
f IN DATA
f IN CLOCK
Vcc 1 CE
OSC in GND
LMX2326
C54 .001
R54 20 1/10W 1%
C37 .001
C39 .001
C40 47 20V
R74 20 1/10W 1%
R57 1K 1/10W 1%
R59 1K 1/10W 1%
C41 .001
R61 20 1/10W 1%
C43 .001
C44 .001
R56 357 1/10W 1%
R58 243 1/10W 1%
LT1763CS8
OUT IN
SENSE GND
GND GND
BYP SHDN
U13
C42 .001
R55 20 1/10W 1%
C38 .001
1 Gnd
3 Gnd
5 Gnd
7 AFC ?
9 PLL #1 Lock Detect (Low=Good)
11 Input Fault (Low=Good)
13 PLL #1 Program Enable
15 NC
17 NC
19 -12V
Gnd 2
10MHz 4
Gnd 6
NC 8
-12V 10
Serial Clock 12
Serial Data Out 14
NC 16
NC 18
NC 20
R60 10K 1/10W 1%
C45 NOT USED
U14
O/P A V+
- I/P A O/P B
+ I/P A - I/P B
V- + I/P B
LMC6682AIMX
C63 .001
R64 301 1/10W 1%
R63 2.21K 1/10W 1%
C55 100 pF
C56 100 pF
R62 100 1/10W 1%
J7
1304098
L5 560 nH
-12V
C57 100 pF
C46 .001
IPFLT
C58 100 pF
C59 100 pF
C60 100 pF
R65 2.21K 1/10W 1%
R66 2.21K 1/10W 1%
C61 100 pF
C62 100 pF
R67 4.75K 1/10W 1%
R68 4.75K 1/10W 1%
R69 4.75K 1/10W 1%
Q3 BS170
Q4 BS170
R70 10K 1/10W 1%
DS2 PLL FAULT RED
GREEN
PLL FAULT
Q5 BS170
R71 2.21K 1/10W 1%
R72 2.21K 1/10W 1%
L6 560 nH
C47 .001
Axcera
REV ECO DATE APV
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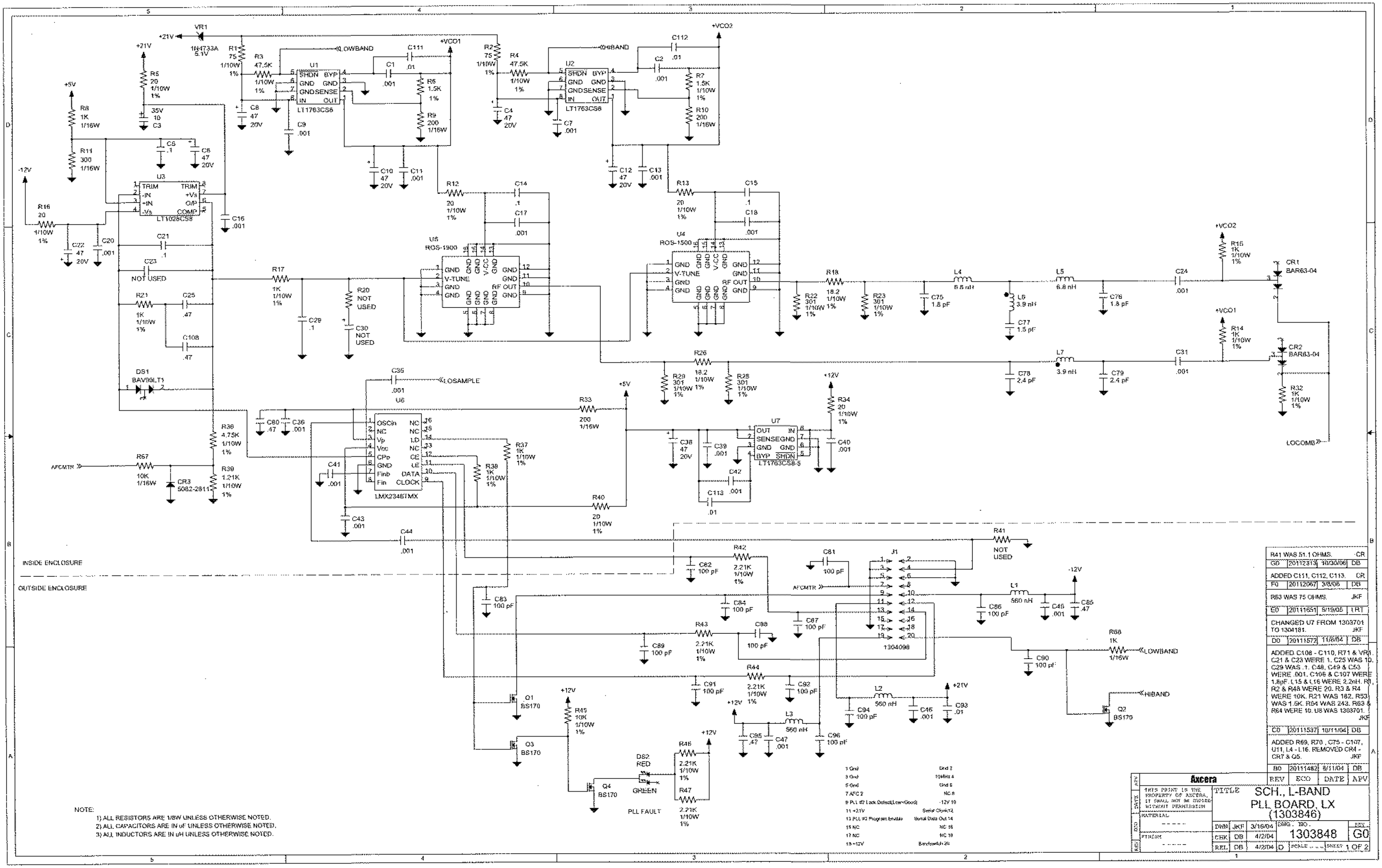
MATERIAL -----
FINISH
TITLE SCH., FIRST CONVERSION BD., LX (1303838)
DWN JKP 4/2/04
CHK DB 4/2/04
REL DB 4/2/04
DWG. NO. 1303840
REV C0
D
SCALE ---
SHEET 2 OF 2


INSIDE ENCLOSURE
OUTSIDE ENCLOSURE
NOTE:
1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.
PLL FAULT
1 Gnd
3 Gnd
5 Gnd
7 AFC 2
9 PLL #2 Lock Detect(Low=Good)
11 +21V
13 PLL #2 Program Enable
15 NC
17 NC
19 +12V
Gnd 2
10MHz 4
Gnd 6
NC 8
-12V 10
Serial Clock12
Serial Data Out 14
NC 16
NC 18
Bandswitch 20
R41 WAS 51.1 OHMS. CR
G0 20112313 10/30/06 DB
ADDED C111, C112, C113. CR
F0 20112067 3/8/06 DB
R63 WAS 75 OHMS. JKF
E0 20111651 5/19/05 LRT
CHANGED U7 FROM 1303701 TO 1304181. JKF
D0 20111572 11/6/04 DB
ADDED C108 - C110, R71 & VR1. C21 & C23 WERE 1. C25 WAS 10. C29 WAS .1. C48, C49 & C53 WERE .001. C106 & C107 WERE 1.8pF. L15 & L16 WERE 2.2nH. R1, R2 & R48 WERE 20. R3 & R4 WERE 10K. R21 WAS 182. R53 WAS 1.5K. R54 WAS 243. R63 & R64 WERE 10. U8 WAS 1303701. JKF
C0 20111537 10/11/04 DB
ADDED R69, R70, C75 - C107, U11, L4 - L16. REMOVED CR4 - CR7 & Q5. JKF
B0 20111482 8/11/04 DB
REV ECO DATE APV
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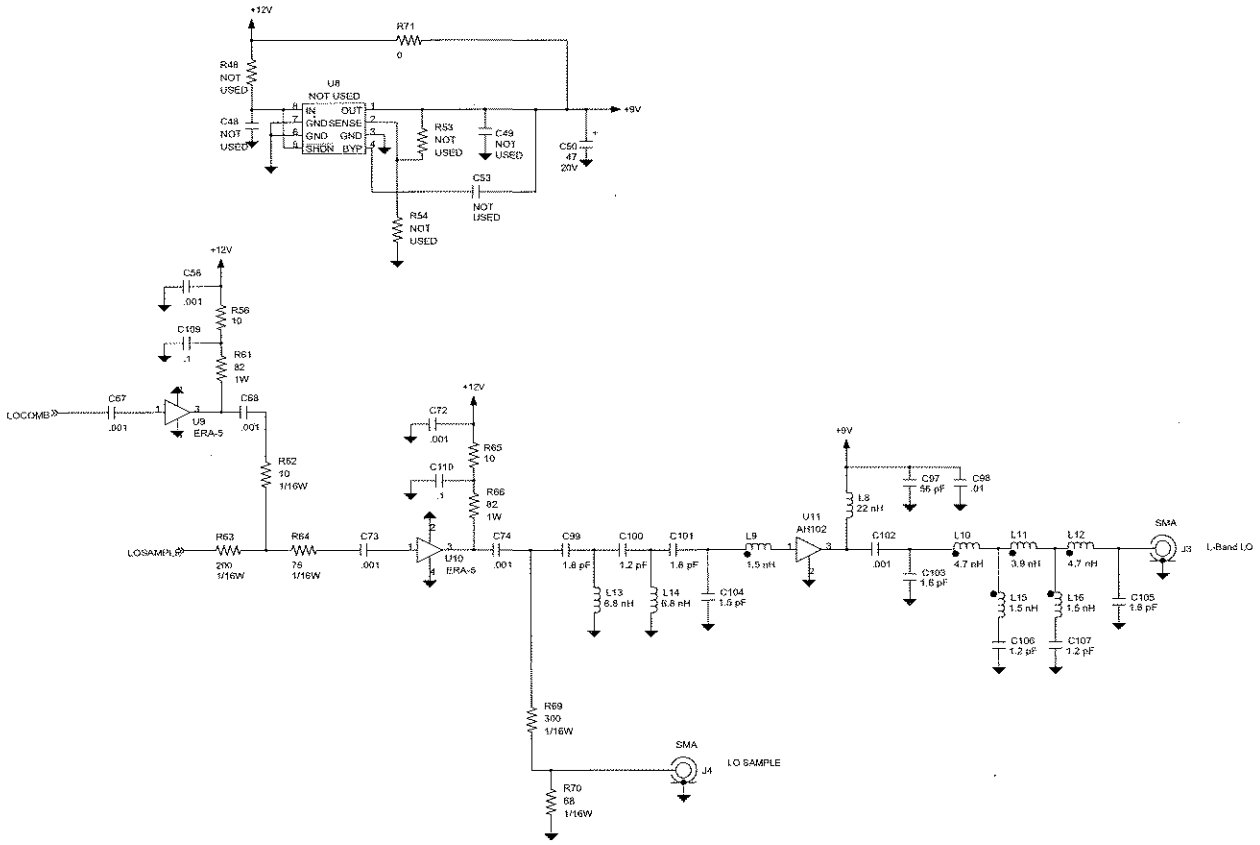
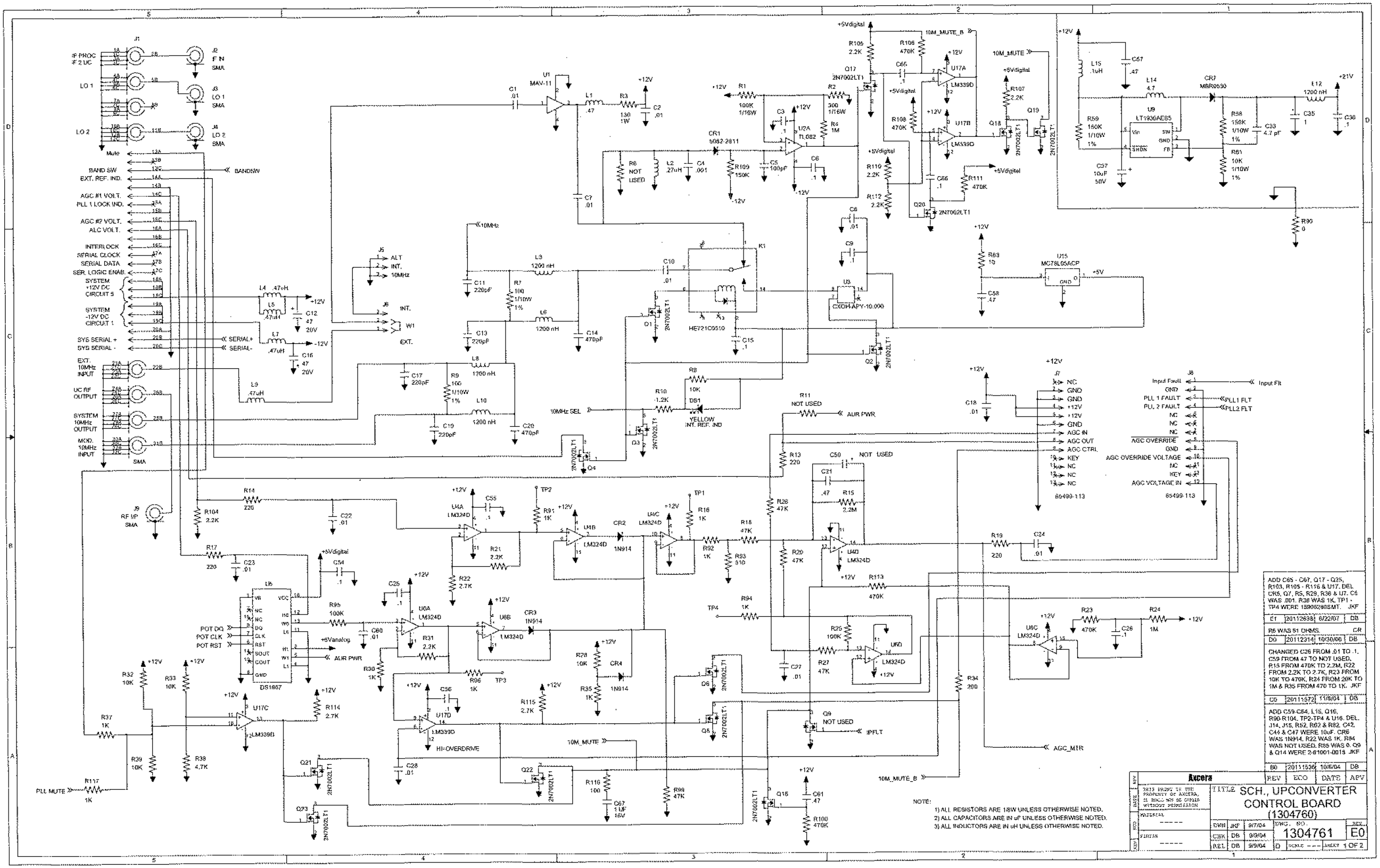
MATERIAL -----
FINISH -----
TITLE SCH., L-BAND PLL BOARD, LX (1303846)
DWN JKF 3/16/04
CHK DB 4/2/04
REL DB 4/2/04
DWG. NO. 1303848
REV. G0
D
SCALE ----
SHEET 1 OF 2

LAST USED REF

C113
L16
U11
R71
J4
Q4
CR3
DS2
VR1



Axcera		REV	ECO	DATE	APV
THIS PRINT IS THE PROPERTY OF AXCERA. IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE	SCH., L-BAND PLL BOARD, LX (1303846)			
MATERIAL -----	DWN	JKF	3/10/04	DWG. NO.	REV
FINISH -----	CHK	DB	4/2/04	1303848	G0
	REL	DB	4/2/04	D SCALE ---	SHEET 2 OF 2



ADD C65 - C67, Q17 - Q23, R103, R105 - R116 & U17. DEL CR5, Q7, R5, R29, R36 & U7. C6 WAS .001. R38 WAS 1K. TP1 - TP4 WERE 1590020SMT. JKF

E1	20112638	6/22/07	DB

R5 WAS 51 OHMS. CR

D0	20112314	10/30/06	DB

CHANGED C26 FROM .01 TO .1, C59 FROM 47 TO NOT USED, R15 FROM 470K TO 2.2M, R22 FROM 2.2K TO 2.7K, R23 FROM 10K TO 470K, R24 FROM 20K TO 1M & R35 FROM 470 TO 1K. JKF

C0	20111572	11/8/04	DB

ADD C59-C64, L15, Q16, R90-R104, TP2-TP4 & U16. DEL J14, J15, R52, R62 & R82, C42, C44 & C47 WERE 10uF. CR6 WAS 1N914, R22 WAS 1K, R84 WAS NOT USED, R85 WAS 0. Q9 & Q14 WERE 2-81001-0015 JKF

B0	20111536	10/6/04	DB
REV	ECO	DATE	APV

NOTE:
1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.

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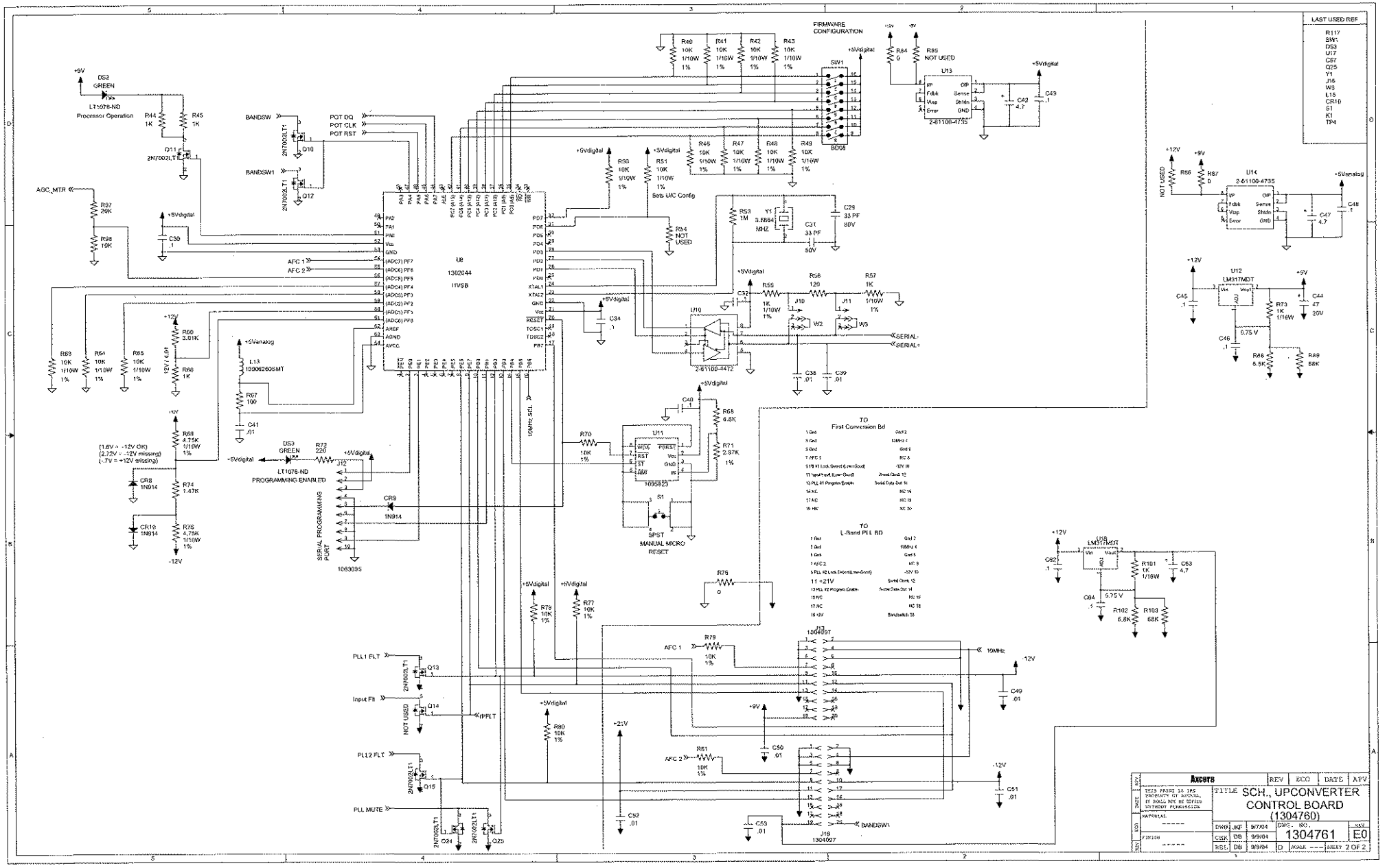
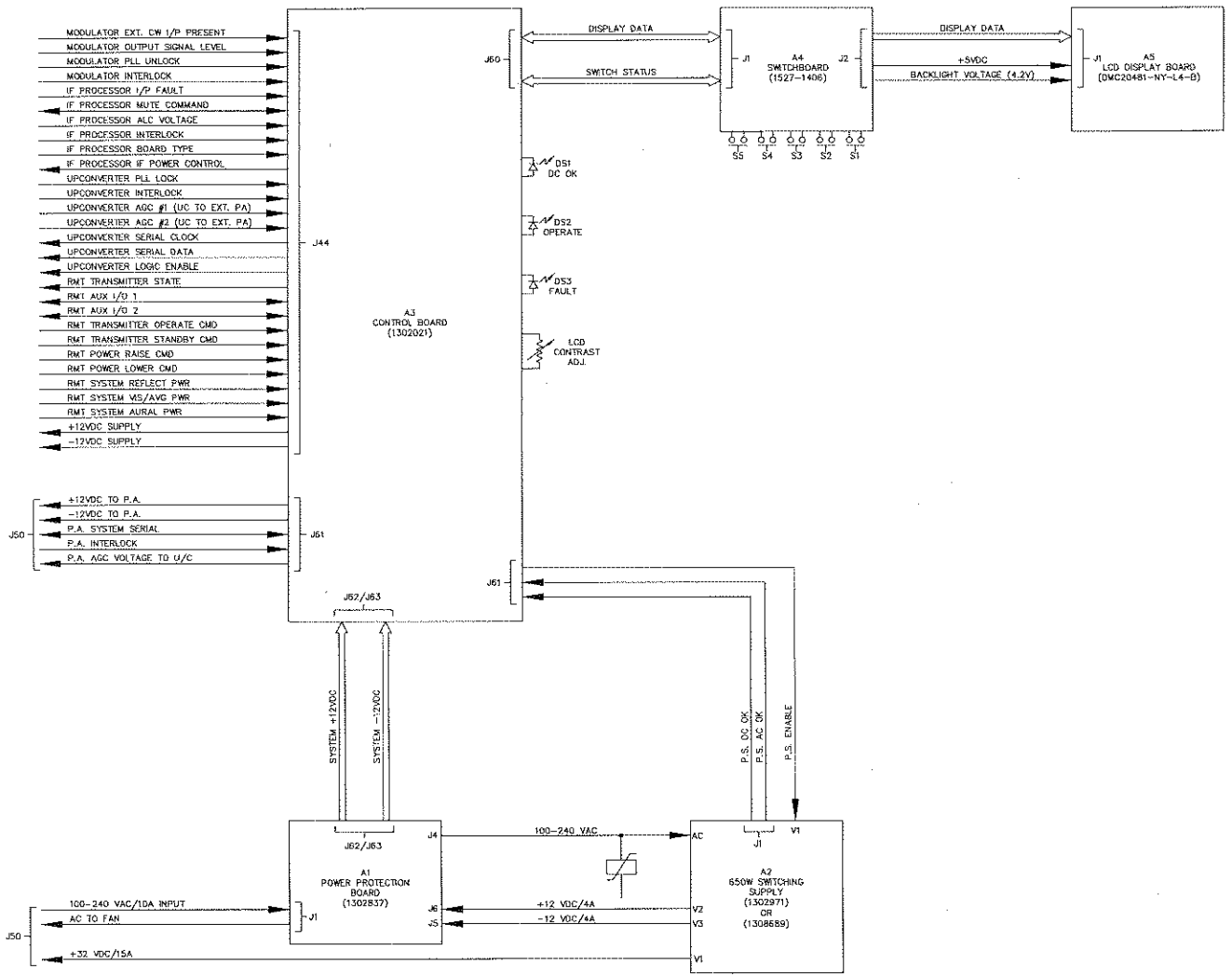
TITLE SCH., UPCONVERTER CONTROL BOARD (1304760)

DWN	JKF	9/7/04	DWG. NO. 1304761	REV. E0
CHK	DB	9/9/04	
REL	DB	9/9/04	D SCALE --- SHEET 1 OF 2


LAST USED REF
R117
SW1
DS3
U17
C87
Q25
Y1
J16
W3
L15
CR10
S1
K1
TP4
FIRMWARE CONFIGURATION
SW1
BD08
R84
0
R85
NOT USED
U13
2-61100-4735
C42
4.7
C43
.1
+5Vdigital
+9V
DS2
GREEN
LT1076-ND
Processor Operation
R44
1K
R45
1K
Q11
2N7002LT1
BANDSW
Q10
BANDSW1
Q12
POT DQ
POT CLK
POT RST
AGC_MTR
R97
20K
R98
10K
C30
.1
U8
1302044
I1VSB
AFC 1
AFC 2
R60
3.01K
12V / 4.01
R61
1K
R63
10K
1/10W
1%
R64
10K
1/10W
1%
R65
10K
1/10W
1%
R66
10K
1/10W
1%
+5Vanalog
L13
1890626SMT
R67
100
C41
.01
R50
10K
1/10W
1%
R51
10K
1/10W
1%
Sets UIC Config
R45
10K
1/10W
1%
R47
10K
1/10W
1%
R48
10K
1/10W
1%
R49
10K
1/10W
1%
R54
NOT USED
R53
1M
Y1
3.6864
MHZ
C29
33 PF
50V
C31
33 PF
50V
C32
.1
R55
1K
1/10W
1%
R56
120
R57
1K
1/10W
1%
J10
J11
W2
W3
U10
2-61100-4472
SERIAL-
SERIAL+
C36
.01
C39
.01
C34
.1
10MHz SCL
C40
.1
R68
6.8K
R70
10K
1%
U11
1095823
R71
2.87K
1%
S1
SPST
MANUAL MICRO
RESET
R75
0
TO
First Conversion Bd
TO
L-Band PLL BD
R68
4.75K
1/10W
1%
(1.6V = -12V OK)
(2.22V = -12V missing)
(-.7V = +12V missing)
CR8
1N914
R74
1.47K
CR10
1N914
R76
4.75K
1/10W
1%
-12V
DS3
GREEN
R73
220
LT1076-ND
PROGRAMMING ENABLED
J12
SERIAL PROGRAMMING PORT
1063095
CR9
1N914
R78
10K
1%
R72
10K
1%
R79
10K
1%
AFC 1
R61
10K
1%
AFC 2
U17
1304097
U18
1304097
10MHz
BANDSW
C49
.01
C50
.01
C51
.01
C52
.01
C53
.01
+21V
R80
10K
1%
PLL1 FLT
Q13
2N7002LT1
Input Filt
Q14
NOT USED
IPPLT
PLL2 FLT
Q15
2N7002LT1
PLL MUTE
Q24
2N7002LT1
Q25
2N7002LT1
R86
NOT USED
R87
0
U14
2-61100-4735
C48
.1
C47
4.7
+5Vanalog
U12
LM317MDT
C45
.1
C44
47
25V
R73
1K
1/16W
0.75 V
C46
.1
R88
5.5K
R89
68K
U19
LM317MDT
C82
.1
R101
1K
1/16W
C53
4.7
C84
.1
0.75 V
R102
6.8K
R103
68K
Axcera
REV
ECO
DATE
APV
TITLE
SCH., UPCONVERTER CONTROL BOARD (1304760)
DWG
JKF
5/7/04
SIZE
D
DWG. NO.
1304761
REV
E0
CHK
DB
9/9/04
APP
DB
9/9/04
SCALE ---
SHEET 2 OF 2



REV	ECO	DATE	APV

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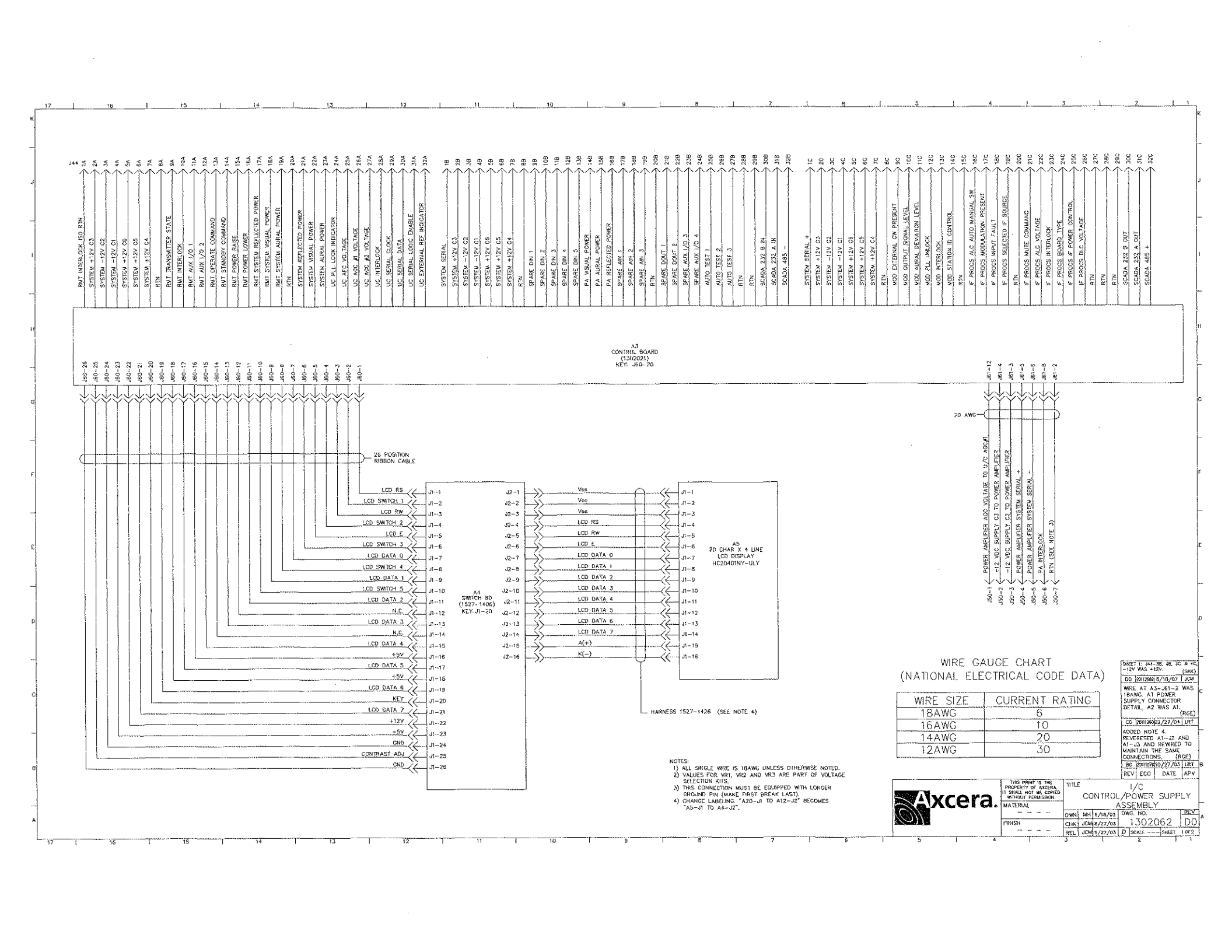
MATERIAL

FINISH

TITLE: B/D, CONTROL/POWER SUPPLY ASSEMBLY, INNOVATOR LX

			DWG. NO.	REV.
DWN	RGE	1/28/04	1303889	A0
CHK	JCM	2/2/04		
REL	JCM	2/2/04	D SCALE ----	SHEET 1 OF 1



NOTES:
1) ALL SINGLE WIRE IS 18AWG UNLESS OTHERWISE NOTED.
2) VALUES FOR VR1, VR2 AND VR3 ARE PART OF VOLTAGE SELECTION KITS.
3) THIS CONNECTION MUST BE EQUIPPED WITH LONGER GROUND PIN (MAKE FIRST BREAK LAST).
4) CHANGE LABELING, "A2D-J1 TO A12-J2" BECOMES "A5-J1 TO A4-J2".

WIRE GAUGE CHART
(NATIONAL ELECTRICAL CODE DATA)

WIRE SIZE	CURRENT RATING
18AWG	6
16AWG	10
14AWG	20
12AWG	30

REV	ECO	DATE	APV
SHEET 1: J44-3B, 4B, 3C, & 4C -12V WAS +12V. (SAK)			
00	20112686	8/10/07	JCM
WIRE AT A3-J61-2 WAS 18AWG. AT POWER SUPPLY CONNECTOR DETAIL A2 WAS A1. (RGE)			
CC	20111260	2/27/04	LRT
ADDED NOTE 4. REVERESED A1-J2 AND A1-J3 AND REWIRED TO MAINTAIN THE SAME CONNECTIONS. (RGE)			
80	20110700	10/27/03	LRT

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MATERIAL

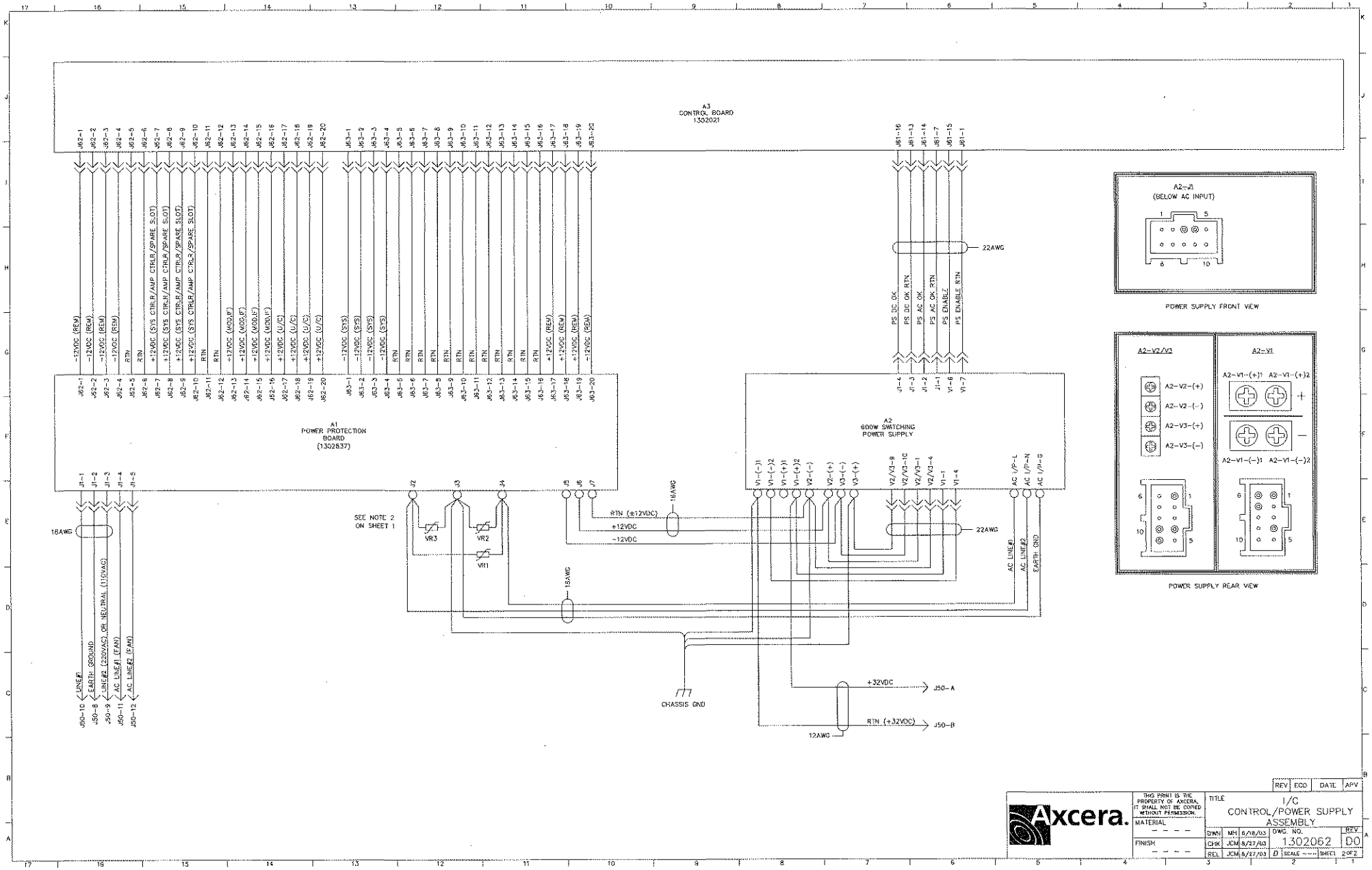
FINISH

TITLE: I/C CONTROL/POWER SUPPLY ASSEMBLY

DWN	MH	6/18/03	
CHK	JCM	8/27/03	
REL	JCM	9/27/03	

DWG. NO. 1302062 REV D0

SCALE: --- SHEET 1 OF 2



REV	ECO	DATE	APV

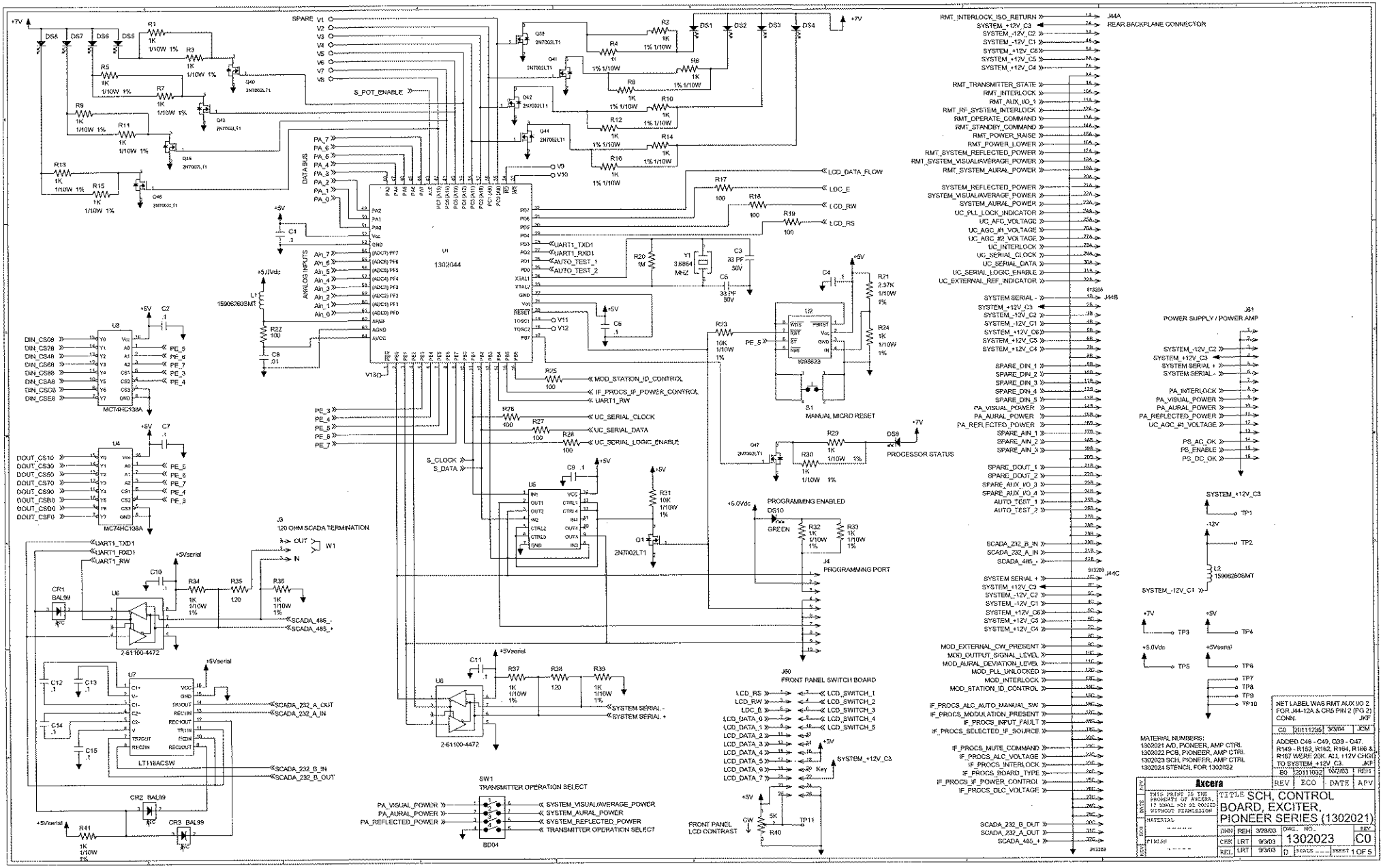
Axcera.

MATERIAL

FINISH

TITLE: I/C CONTROL/POWER SUPPLY ASSEMBLY

DWN	MH	6/18/03	DWG. NO. 1302062 REV. D0
CHK	JCM	8/27/03	
REL	JCM	8/27/03	D SCALE ~~~ SHEET 2 OF 2


J44A
REAR BACKPLANE CONNECTOR
J44B
J44C
J61
POWER SUPPLY / POWER AMP
J60
FRONT PANEL SWITCH BOARD
J4
PROGRAMMING PORT
J3
120 OHM SCADA TERMINATION
U1
1302044
SW1
TRANSMITTER OPERATION SELECT
S1
MANUAL MICRO RESET
DS9
PROCESSOR STATUS
DS10
GREEN
PROGRAMMING ENABLED
MATERIAL NUMBERS:
1302021 A/D, PIONEER, AMP CTRL
1302022 PCB, PIONEER, AMP CTRL
1302023 SCH, PIONEER, AMP CTRL
1302024 STENCIL FOR 1302022
NET LABEL WAS RMT AUX I/O 2 FOR J44-12A & CR3 PIN 2 (FIG 2) CONN. JKF
ADDED C46 - C49, Q39 - Q47, R149 - R152, R162, R164, R166 & R167 WERE 20K. ALL +12V CHGD TO SYSTEM +12V_C3. JKF
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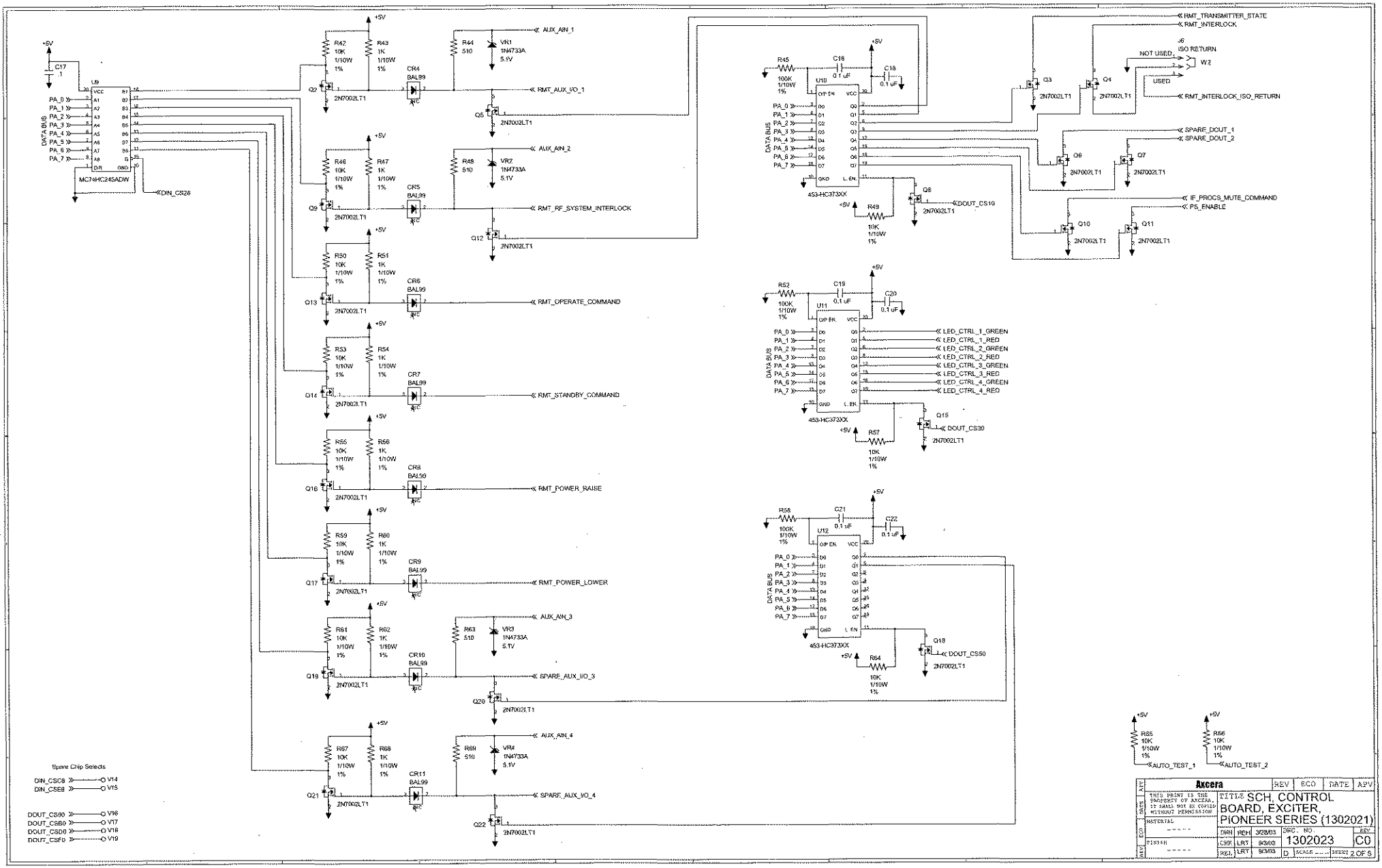
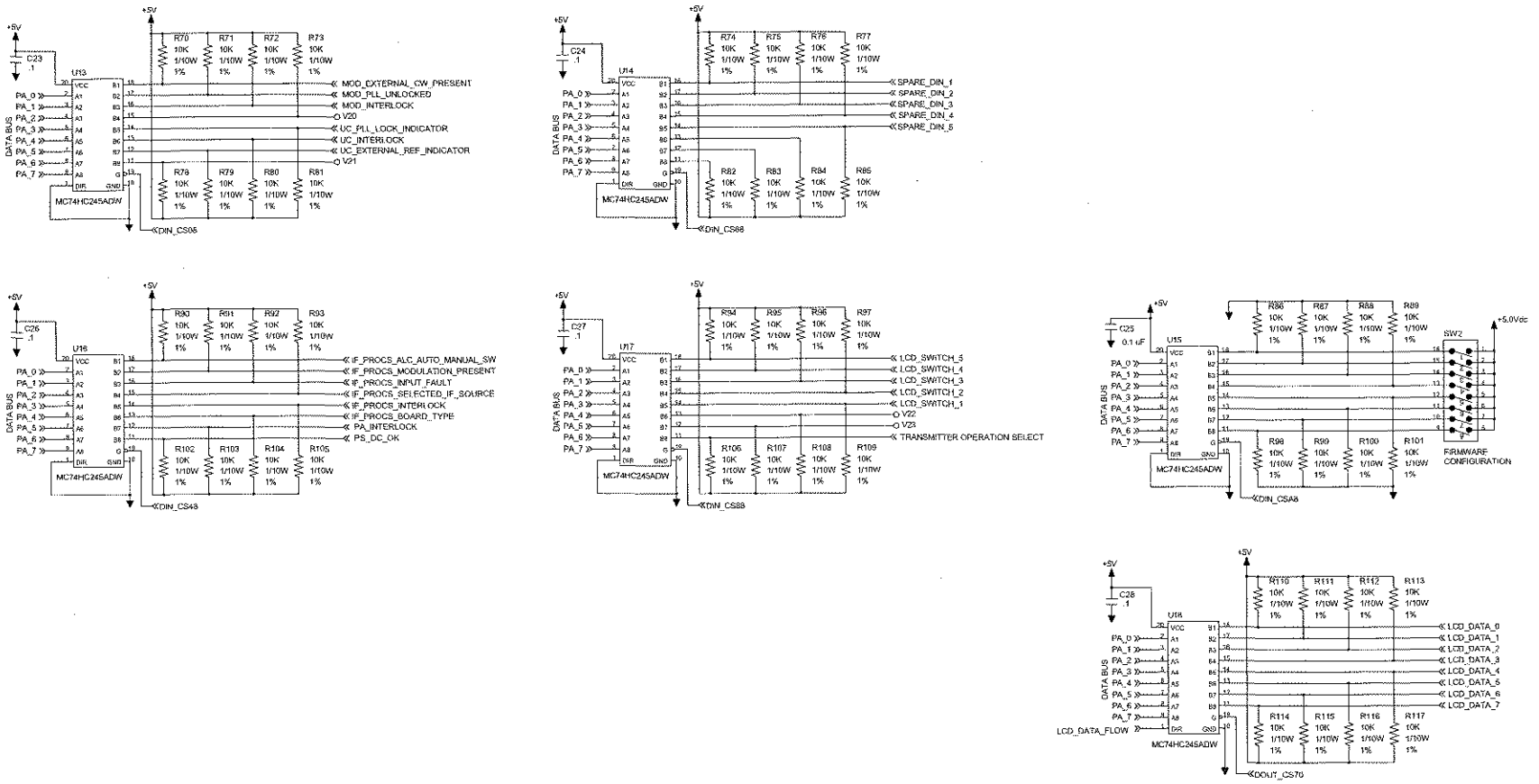
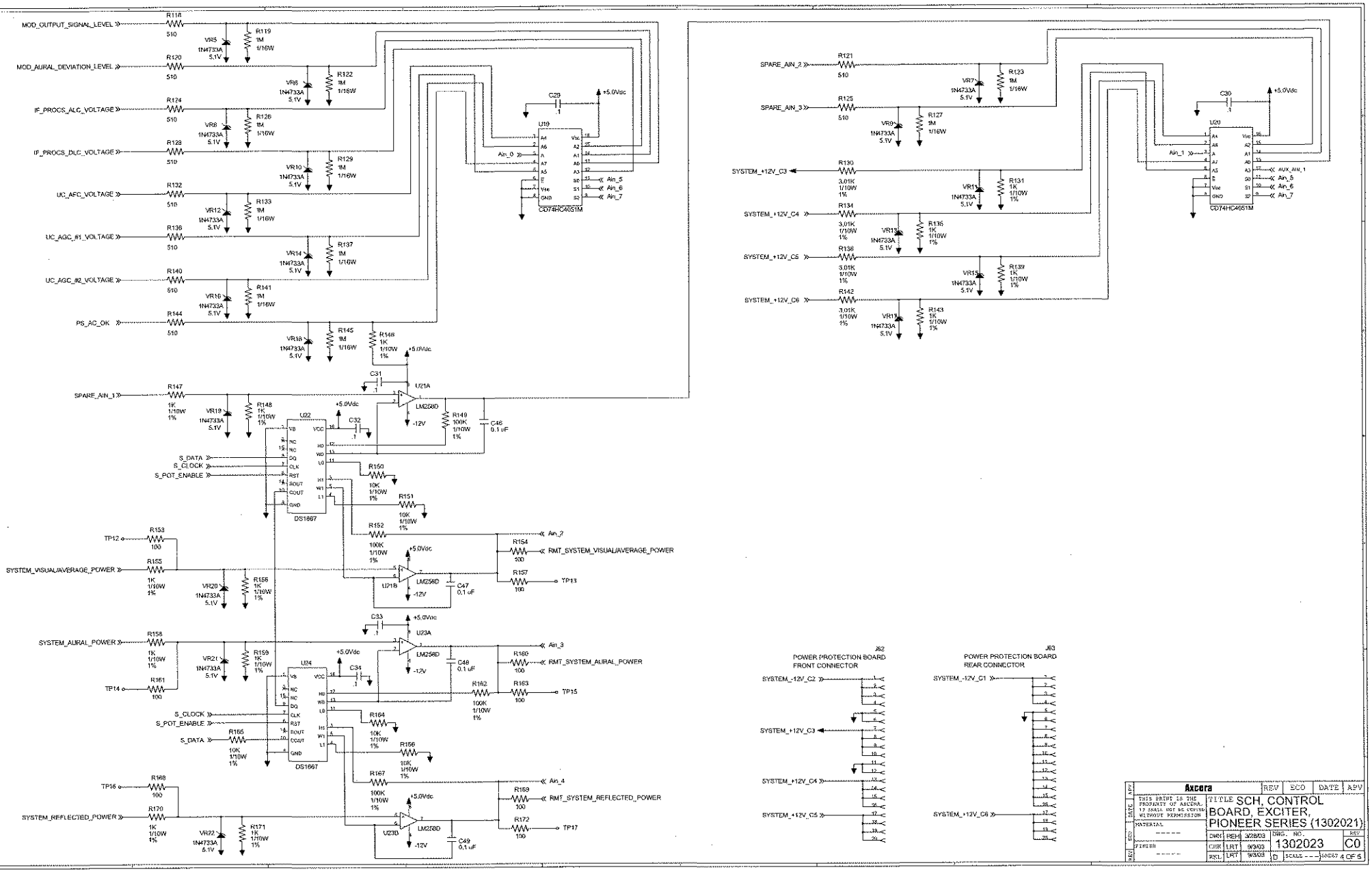
TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)
DWG NO. 1302023
REV C0
SHEET 1 OF 5



Axcera		REV	ECO	DATE	APV
THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)				
MATERIAL -----	DWN REH 3/28/03	DWG. NO. 1302023		REV C0	
FINISH -----	CHK LRT 9/3/03				
	APPD LRT 9/3/03	D	SCALE ----	SHEET 2 OF 5	



APP	Axcera	REV	ECO	DATE	APP
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)			
DES	MATERIAL	DWN REH 3/28/03	DWG. NO. 1302023	REV C0	
DATE	FINISH	CHK LRT 4/3/03			
		REL LRT 5/3/03	D SCALE ---	SHEET 3 OF 5	


MOD_OUTPUT_SIGNAL_LEVEL
MOD_AURAL_DEVIATION_LEVEL
IF_PROCS_ALC_VOLTAGE
IF_PROCS_DLC_VOLTAGE
UC_AFC_VOLTAGE
UC_AGC_#1_VOLTAGE
UC_AGC_#2_VOLTAGE
PS_AC_OK
SPARE_AIN_1
SPARE_AIN_2
SPARE_AIN_3
SYSTEM_+12V_C3
SYSTEM_+12V_C4
SYSTEM_+12V_C5
SYSTEM_+12V_C6
S_DATA
S_CLOCK
S_POT_ENABLE
SYSTEM_VISUAL/AVERAGE_POWER
SYSTEM_AURAL_POWER
SYSTEM_REFLECTED_POWER
RMT_SYSTEM_VISUAL/AVERAGE_POWER
RMT_SYSTEM_AURAL_POWER
RMT_SYSTEM_REFLECTED_POWER
+5.0Vdc
-12V
LM258D
DS1867
CD74HC4051M
POWER PROTECTION BOARD FRONT CONNECTOR
POWER PROTECTION BOARD REAR CONNECTOR
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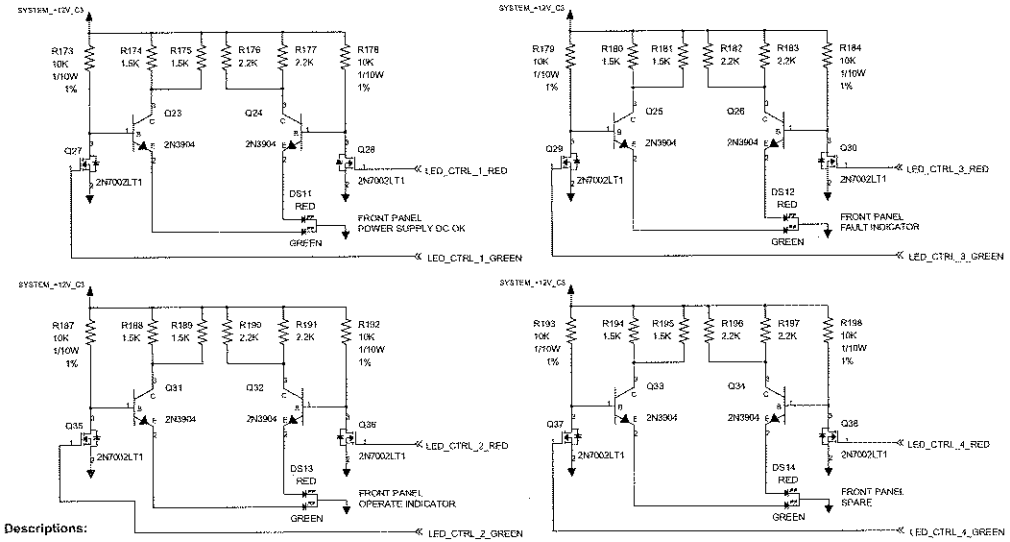
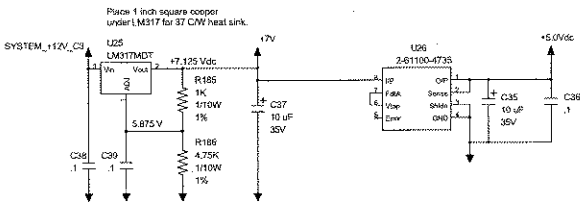
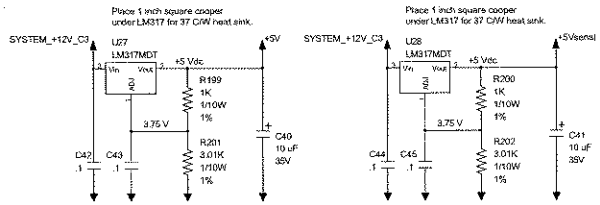
TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)
DWG. NO. 1302023
REV C0
SHEET 4 OF 5







LAST USED REF:
R202
C49
Q47
DS14
U28
VR22
J63
TP17
V23
SW2
CR11
W2
Y1
L2
S1

Circuit Descriptions:

PAGE 1:

U1 is an Atmel Atmega128 microcontroller. This part is in-circuit programmed using the serial programming port. When the microcontroller is held in reset by either the programming port or the external watchdog IC, a transistor inverts the reset signal while serial programming lines are connected to U1 through analog switch U5.

U2 is a watchdog IC used to hold the microcontroller in reset if the supply voltage is less than 4.21 Vdc; (1.25 Vdc < Pin 4 (IN) < Pin 2 (Vcc)). The watchdog momentarily resets the microcontroller if Pin 6 (IST) is not clocked every second. A manual reset switch is provided but should not be needed.

Diodes DS1 through DS8 are used for display of auto test results. A test board is used to execute self test routines. When the test board is installed, Auto_Test_1 is held low and Auto_Test_2 is allowed to float at 5 Vdc. This is the signal to start the auto test routines.

U3 and U4 are used to selectively enable various input and output ICs found on page 2 and 3 of the schematic.

U1 has two serial ports available. In this application, one port is used to communicate with transmitter system components where U1 is the master of a RS-485 serial bus. The other serial port is used to provide serial data I/O where U1 is not the master of the data port. A dual RS-232 port driver IC and a RS-485 port driver is also in the second serial data I/O system. The serial ports are wired such that serial data input can come through one of the three serial port channels. Data output is sent out through each of the three serial port channels.

Switch SW1 is used to select either transmitter operation or exciter driver operation. When the switches of SW1 are on, transmitter operation is selected and the power monitoring lines of the transmitter's power amplifier are routed to the system power monitoring lines.

PAGE 2:

Digital output latches are used to control system devices. Remote output circuits are implemented using open drain FETs with greater than 60 Volt drain to source voltage ratings.

Remote digital inputs are diode protected with a 1 Kohm pull-up resistor to 5Vdc. If the remote input voltage is greater than about 2 volts or floating, a FET is turned on and a logic low is applied to the digital input buffer. If the remote input voltage is less than the turn on threshold of the FET (about 2 Vdc), a logic high is applied to the digital input buffer.

Four of the circuits on page two are auxiliary I/O connections wired for future use. They are wired similar to the remote digital inputs but include a FET for digital output operation. To operate these signals as an input, the associated output FET must be turned off. These circuits are also connected to an analog input multiplexer IC.

PAGE 3:

Several ICs are used as input buffers to allow the microcontroller to monitor various digital input values. Most digital inputs use a 10 Kohm pull-up resistor. The buffer IC used for data transfer to the display is wired for read and write control.

PAGE 4:

Each analog input is expected to be between 0 and 5 Vdc. If a signal exceeds 5.1 Vdc, a 0.225 Watt zenor diode clamps the signals voltage. Most signals are calibrated at their source however two dual serial potentiometer ICs are used to calibrate four signals. For these four circuits, the input value is divided in half before it is applied to an op-amp. The serial potentiometer is used to adjust the input signal between 80 and 120% of the input signal. Serial data to the second serial potentiometer is transferred through the first IC. The wiper position of the digital potentiometer circuit is used to set the gain of the op-amp. Lower digital values for the wiper setting increases the gain of the op-amp. If N= 0, gain = 6.0. If N = 255, gain = 3.00. If Vin = 1.0 at spare_Ain_1 and N = 128, U21A out = 4.0V with gain = 4.

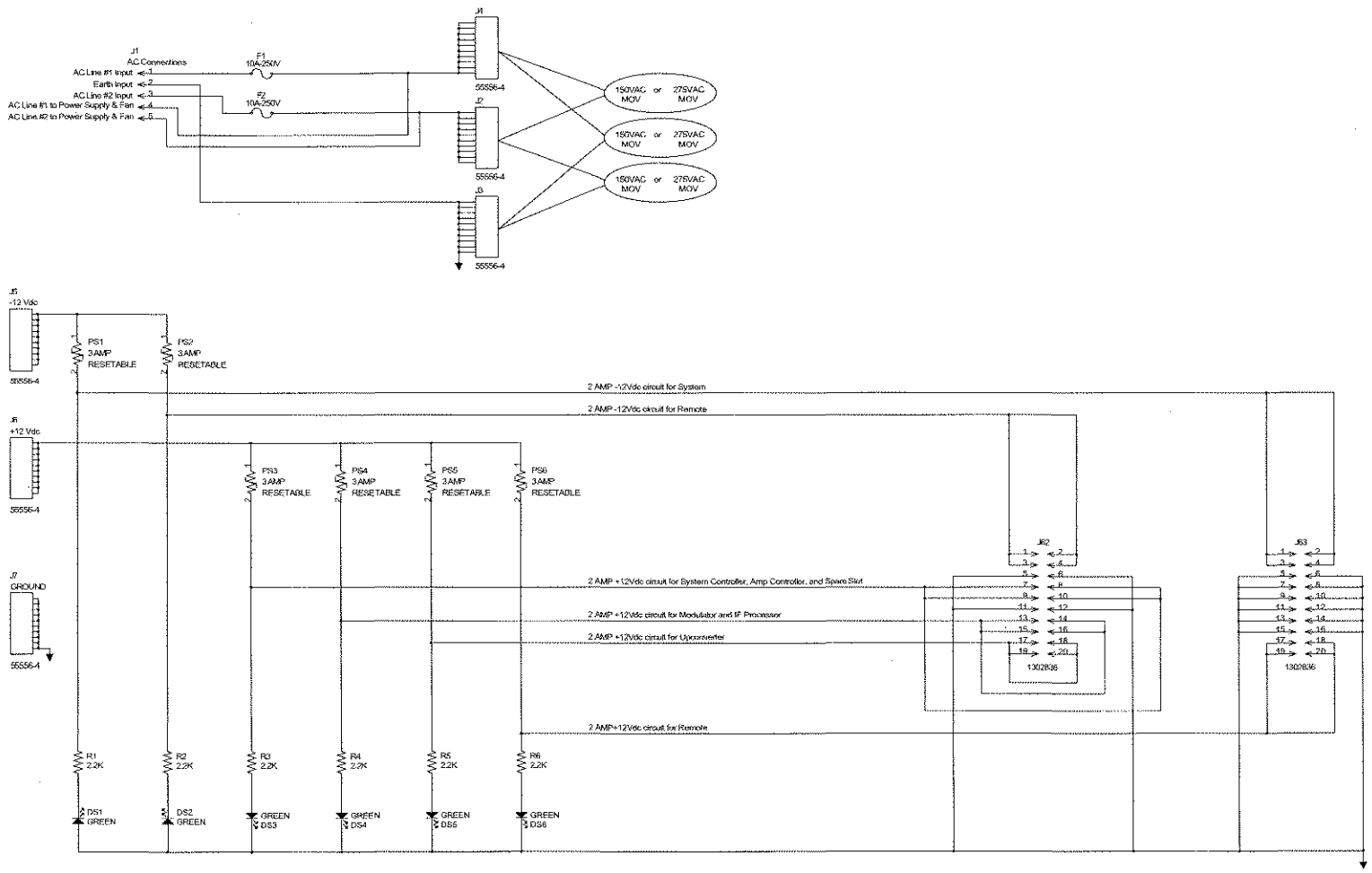
Two 20 position connectors are used to provide power to the backplane. J62 and J63 get power from the power supply after a nominal 3 amp resettable fuse. The Raychem polyswitch resettable fuses may open on a current as low as 2.43 amps at 50C, 3 amps at 25 C or 3.3 amps at 0C. They definately will open when the current is 4.86 amps at 50C, 6 amps at 20C, or 6.6 amps at 0C. Trace widths of these circuits are 0.140" (designed for maximum current).

PAGE 5:

Each of the four LED circuits drive a dual element common cathode LED. To make a good amber color, the current applied to the green element is slightly greater than the red element.

Several voltage regulators are used to power the board. Seven volts is typically applied to board LEDs and to the input of a precision 5.0 volt regulator. The 5.0 volt regulator is used for analog circuits and the microcontroller analog reference voltage. Another two 5 volt regulator circuits are used for most other board circuits.

	Axcera	REV	ECO	DATE	APV
ENG	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)			
MFG	MATERIAL ~~~~~	DWN REH 3/28/03	DWG. NO. 1302023		REV. C0
PUR	FINISH ~~~~~	CHK LRT 9/3/03			
		ENGR LRT 9/3/03	D	SCALE ~~~	SHEET 5 OF 5



Circuit Design Notes:

1. Track widths of 0.140 inch minimum top and bottom of board shall be used to connections to J1, J2, J3, J4.
2. Track widths of 0.140 inch minimum top of board shall be used to connections to J5 and J6.
3. Track widths of 0.065 inch minimum shall be used to connections to J62 and J63.
4. Track widths of 0.020 inch minimum shall be used to connections between LEDs and resistors.
5. Board BOM needs the following items added to those exported from Orcad:

Part Number	Qty	Description
102071	4	Fuse Clip, PC BD Mnt., 15 Amp

MATERIAL NUMBERS:
1302837 PIONEER, POWER PROTECTION
1302838 PCB, PIONEER, PWR PROTECT
1302839 SCH, PIONEER, PWR PROTECT
1302840 STENCIL FOR 1302838

Axcera		REV	ECO	DATE	APV
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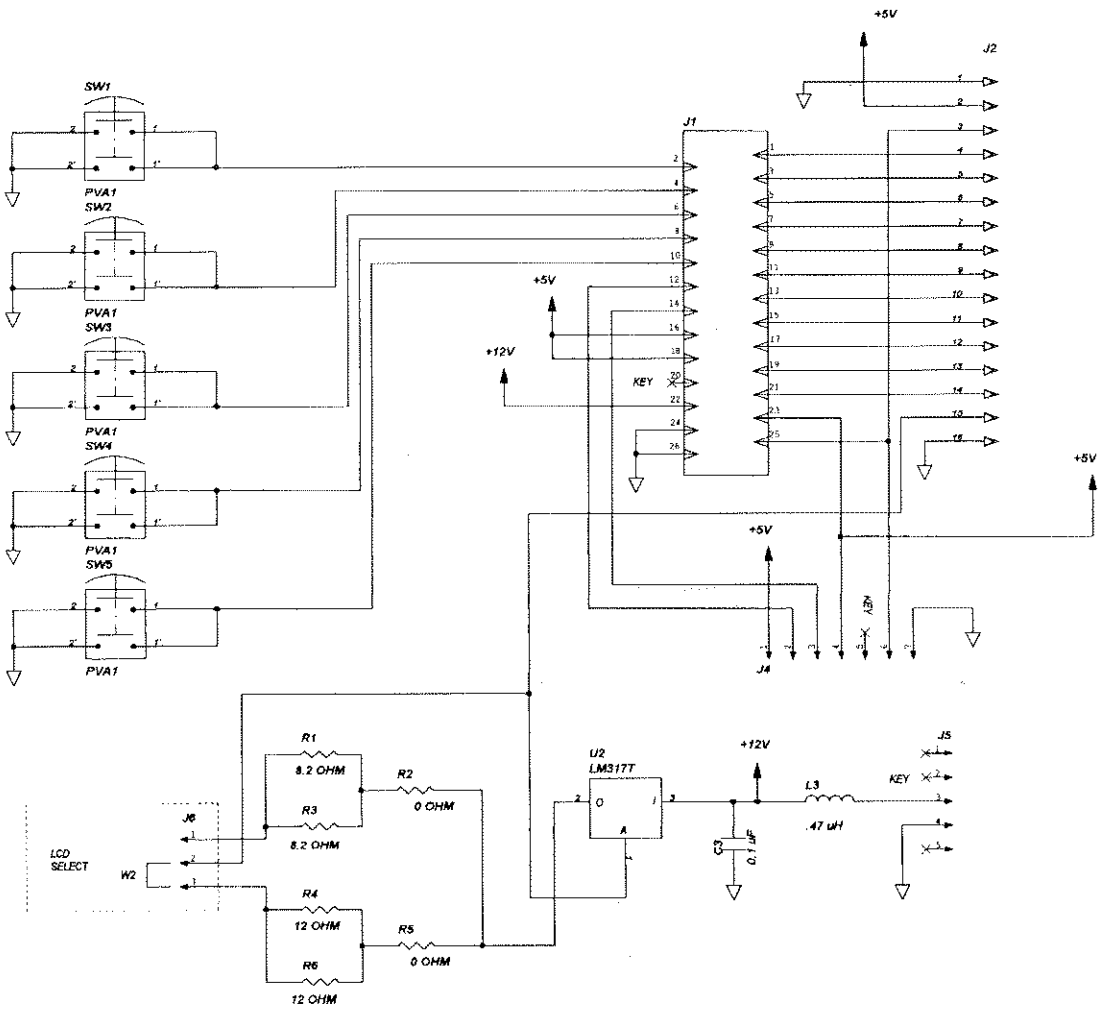
MATERIAL ------	DWN	REH	5/29/03	DWG. NO. 1302839	REV A0
FINISH ------	CHK	APV	5/29/03		
	REL	REH	5/29/03	D SCALE ---	SHEET 1 OF 1



DELETED C1, C2, L1, L2, U1, J3, & W1. MOVED W2 FROM J6-1,-2 TO J6 -2,-3. JKF

REV	ECN	DATE	APV
3	8603	11/7/96	
AT J2 W2 WAS W1. (TMY)			
2	8424	9/29/96	JCM
SWITCHED PINS 1 & 2 OF U2 (TMY)			
1	8368	8/27/96	RAS

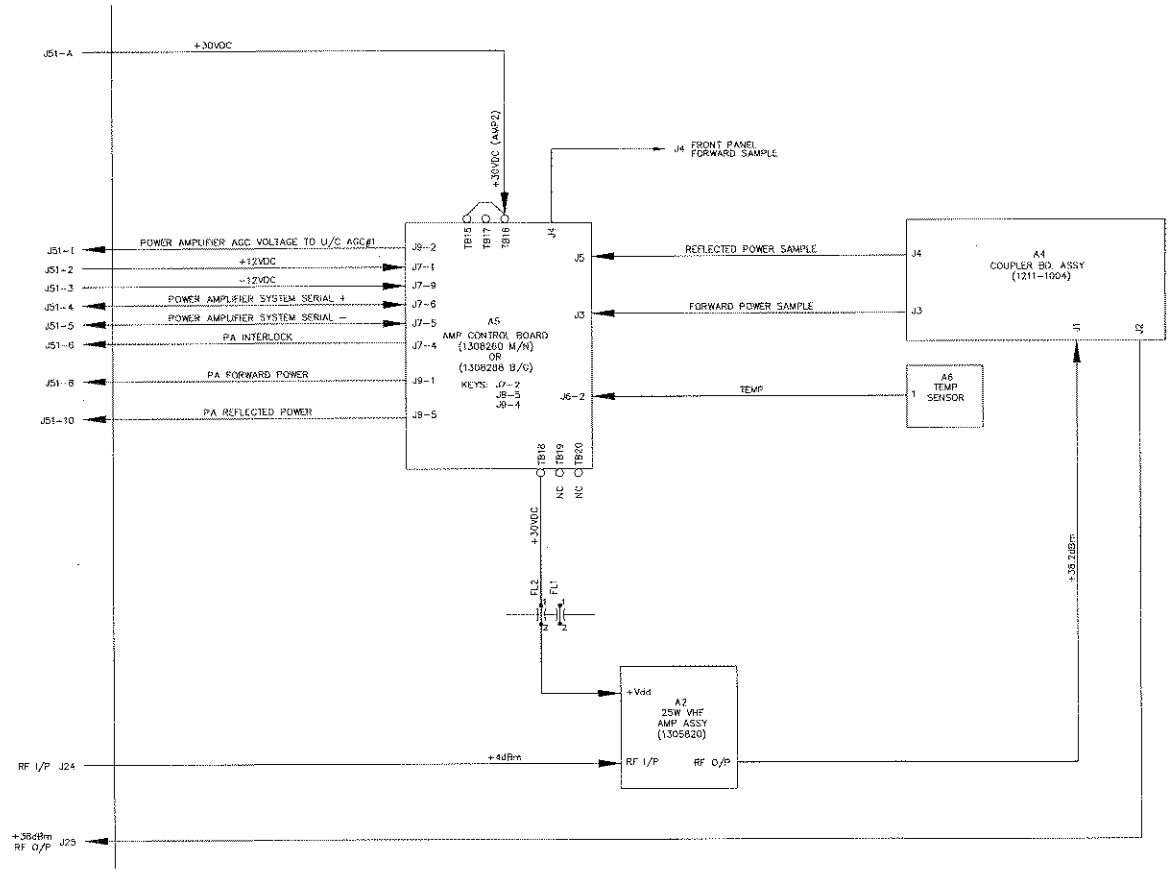
ITS CORPORATION

MATERIAL ---

FINISH ---

TITLE SCHEMATIC SWITCH BOARD (1527-1406)

DWN	DLM	6/3/96	DWG. NO. 1527-3406 REV 3
CHK	RAS	6/14/96	
REL	RAS	6/14/96	B SCALE — SHEET 1 OF 1



A5 WAS 1303682 OR 1304674 (SAK)			
BD	20112539	3/28/07	LRT
REV	ECO	DATE	APV

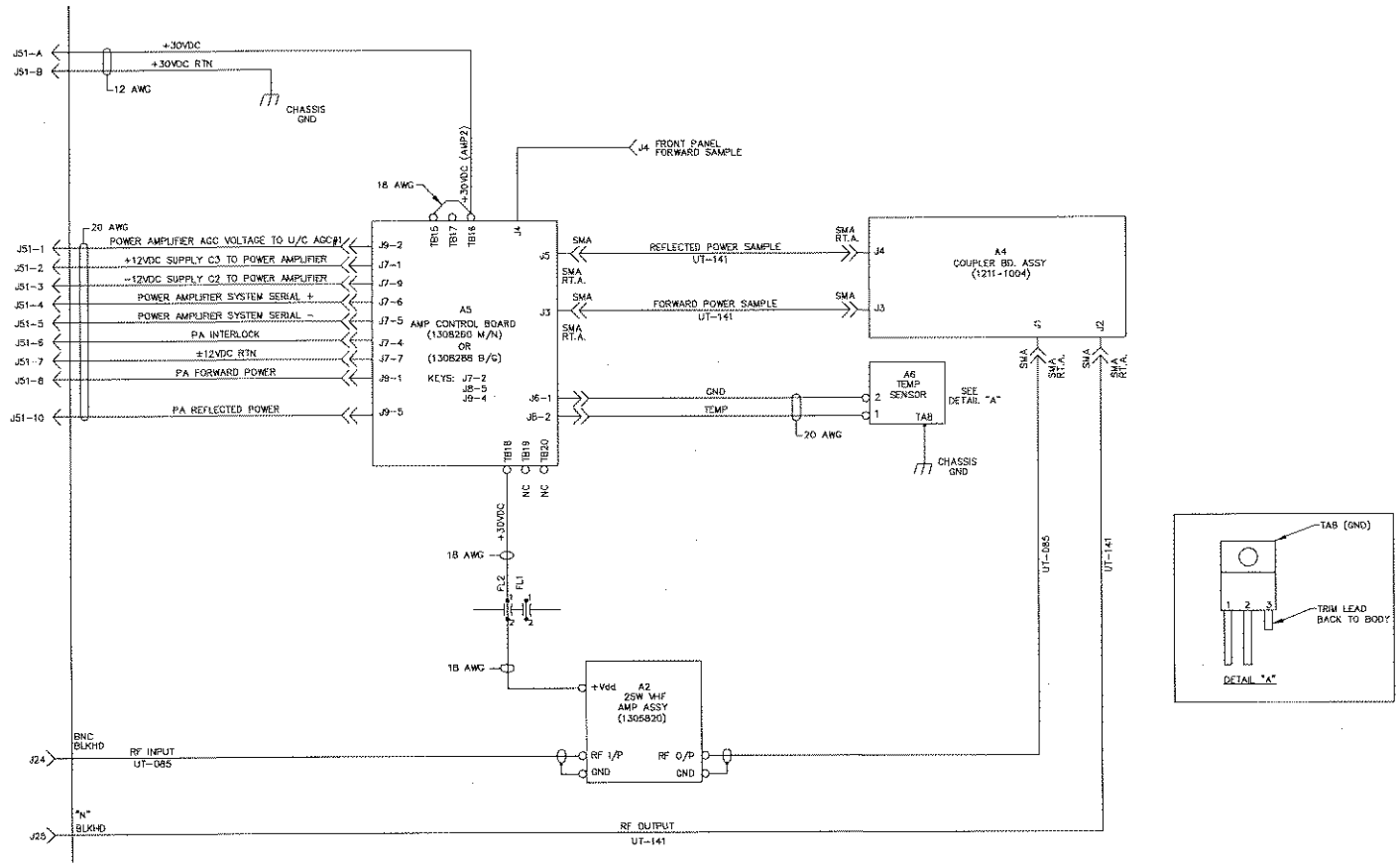
Axcera.

MATERIAL

FINISH

TITLE
B/D
DRIVER ASSEMBLY
5W HB VHF DTV

DWN	RGE	03/22/05	DWG. NO. 1305837 REV B0
CHK	LRT	04/18/05	
REL	LRT	04/18/05	D SCALE ~~~ SHEET 1 OF 1



NOTE:
1. ALL WIRE IS 18AWG UNLESS OTHERWISE NOTED.

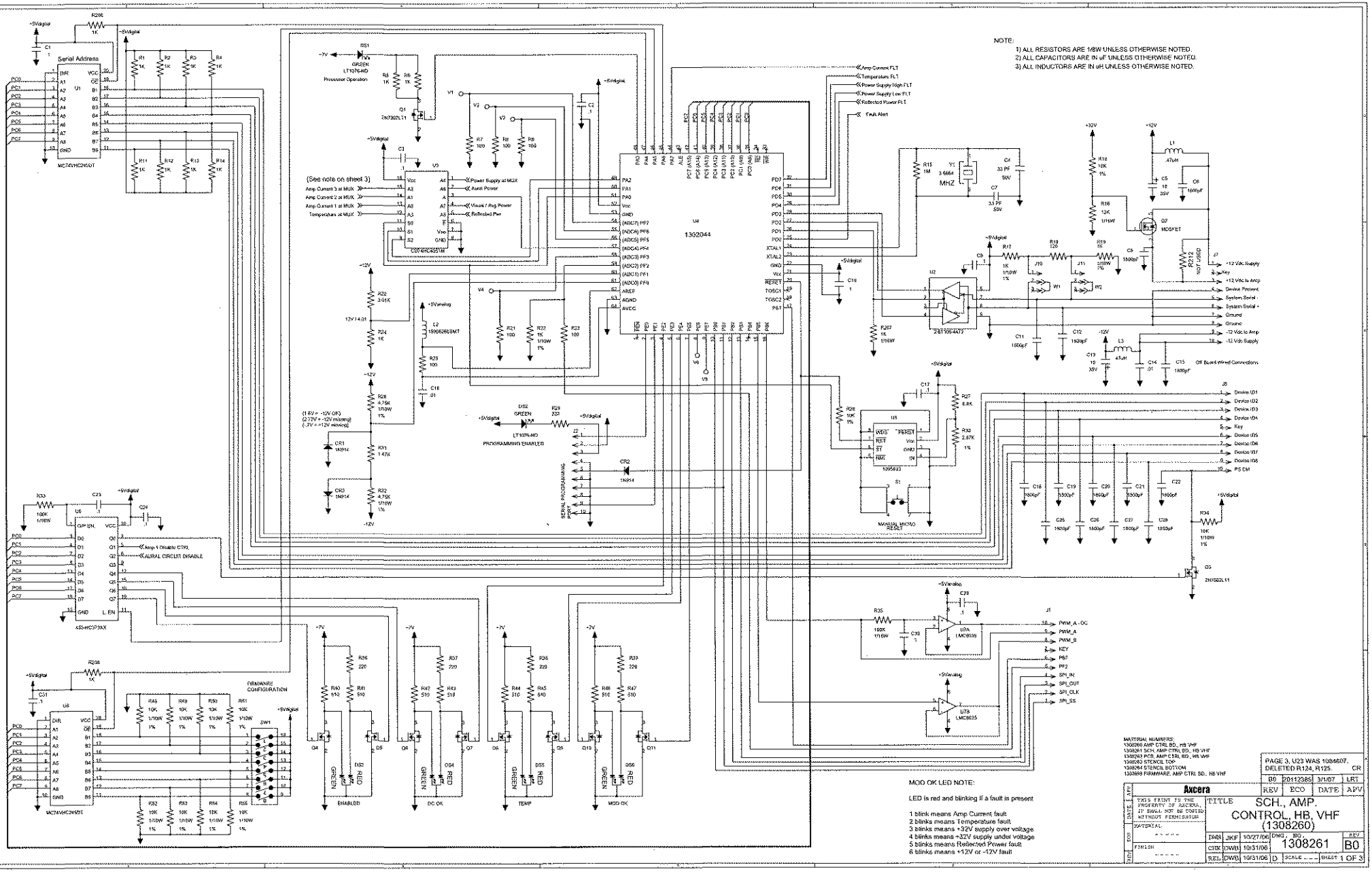
REV	ECO	DATE	APV
AS WAS 1303682 OR 1304674			(SAK)
B0	2001259	3/28/07	LRT

MATERIAL

FINISH

TITLE: I/C, DRIVER ASSEMBLY, 5W HB VHF DTV

DWN	RGE 02/22/05	DWG. NO. 1305836 REV. B0
CHK	LRT 04/11/05	
REL	LRT 04/11/05	D SCALE --- SHEET 1 OF 1


NOTE:
1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.
Serial Address
MC74VHC245DT
(See note on sheet 3)
Amp Current 3 at MUX
Amp Current 2 at MUX
Amp Current 1 at MUX
Temperature at MUX
Power Supply at MUX
Aural Power
Visual / Aug Power
Reflected Pwr
Amp Current FLT
Temperature FLT
Power Supply High FLT
Power Supply Low FLT
Reflected Power FLT
Fault Alert
1382044
MHZ
MOSFET
Device ID1
Device ID2
Device ID3
Device ID4
Key
Device ID5
Device ID6
Device ID7
Device ID8
PS Ctrl
PROGRAMMING ENABLED
SERIAL PROGRAMMING PORT
MANUAL MICRO RESET
Amp 1 Disable CTRL
AURAL CIRCUIT DISABLE
L_EN
FIRMWARE CONFIGURATION
ENABLED
DC OK
TEMP
MOD OK
PWM_A - DC
PWM_A
PWM_B
KEY
PB7
PF2
SPI_IN
SPI_OUT
SPI_CLK
SPI_SS
MOD OK LED NOTE:
LED is red and blinking if a fault is present
1 blink means Amp Current fault
2 blinks means Temperature fault
3 blinks means +32V supply over voltage
4 blinks means +32V supply under voltage
5 blinks means Reflected Power fault
6 blinks means +12V or -12V fault
MATERIAL NUMBERS:
1308260 AMP CTRL BD., HB VHF
1308261 SCH, AMP CTRL BD., HB VHF
1308262 PCB, AMP CTRL BD., HB VHF
1308263 STENCIL TOP
1308264 STENCIL BOTTOM
1308265 FIRMWARE, AMP CTRL BD., HB VHF
PAGE 3, U23 WAS 1084607.
DELETED R124, R125.
B0 20112385 3/1/07 LR3
Axcera
REV ECO DATE APV
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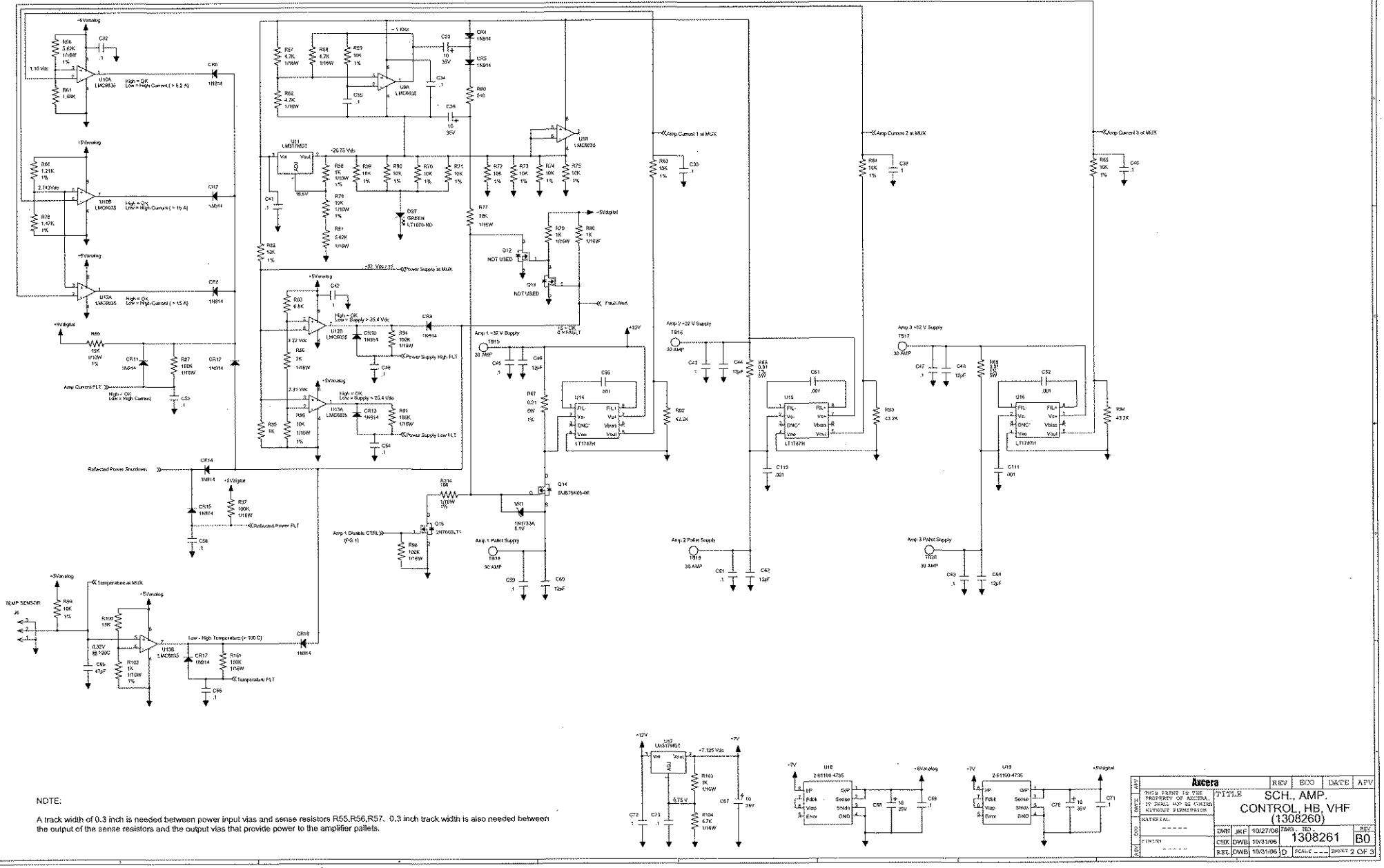
MATERIAL
FINISH
TITLE SCH., AMP. CONTROL, HB, VHF (1308260)
DWN JKF 10/27/06
CHK DWB 10/31/06
REL DWB 10/31/06
DWG. NO. 1308261
REV B0
D
SCALE ---
SHEET 1 OF 3



NOTE:

A track width of 0.3 inch is needed between power input vias and sense resistors R55,R56,R57. 0.3 inch track width is also needed between the output of the sense resistors and the output vias that provide power to the amplifier pallets.

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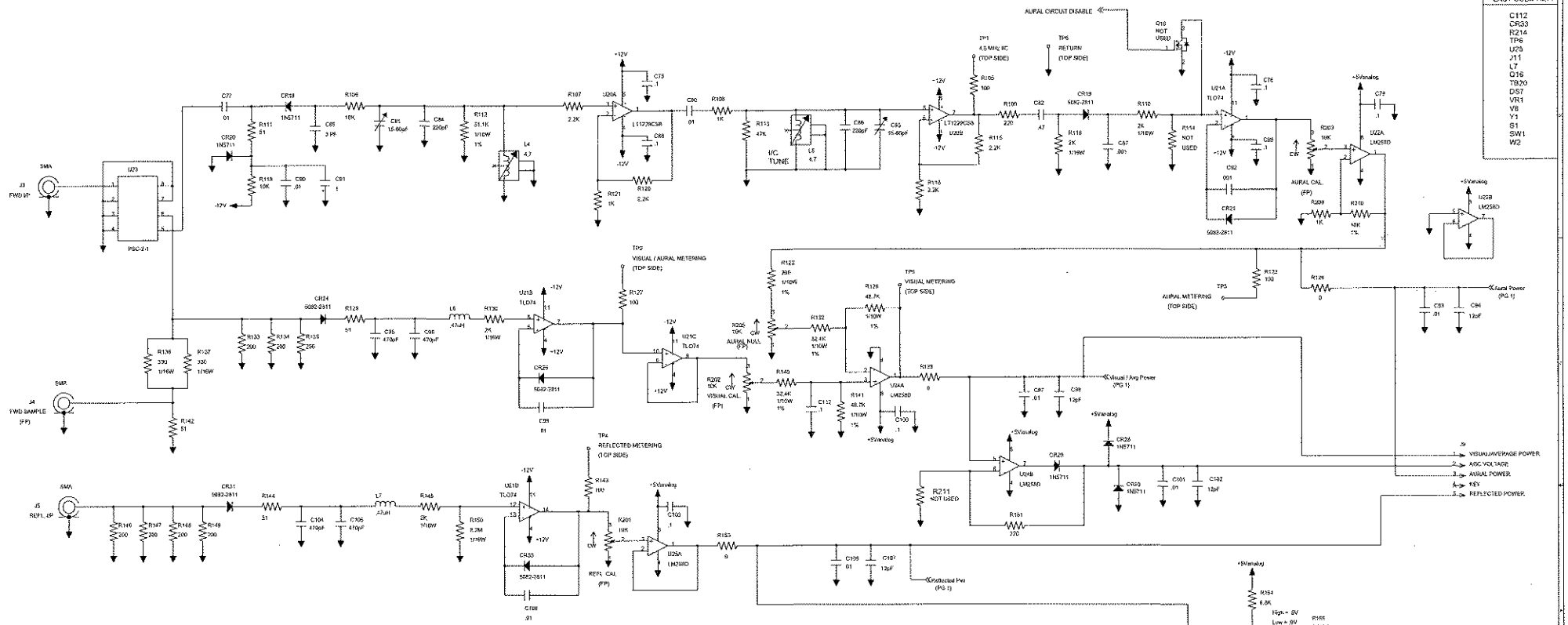
MATERIAL	DWN	JKF	10/27/06	TRAK NO. 1308261	REV B0
FINISH	CHK	DWB	10/31/06		
	REL	DWB	10/31/06	D SCALE ---	SHEET 2 OF 3



Circuit Description

Page 1:

Upper center of page one is U4 which is the controller. This in-circuit Atmel microcontroller is operated at 3.6864 MHz. Programming of this device is performed through J2. U4 selects the desired analog channel of U3 through the settings of PA0 - PA2. PA3 of U4 is a processor operating LED that can be flashed to show continued operation. PF1 is used to monitor the +12 Vdc supply to the board. PF4 is the selected channel of analog switch U3. PF3 and other select microcontroller pins are connected to a via for future access.

U2 is our standard serial to RS-485 driver IC. U5 is a watchdog IC used to hold the microcontroller in reset if the supply voltage is less than 4.21 Vdc; (1.25 Vdc < Pin 4 (IN) < Pin 2 (Vcc)). U5 momentarily resets the microcontroller if Pin 6 (IST) is not clocked every second. A manual reset switch is provided but should not be needed.

Upper left corner U1 is used to determine where the amplifier control board is located. The eight inputs come from amp connector J8 and are used to set the SCADA address of the controller. Pull-up resistors set a default condition of logic high.

U6 below U1 is used to control two of the four board's status LEDs and three other circuits that are not allowed to change state during a microcontroller reset. A FET is turned on to shut current away from the LED to turn it off. U8 below U6 is used to enable different features within software. Actual use is TBD.

Page 2:

In the lower right corner are voltage regulator circuits. U17 should allow for 0.14 amps of power using its 92 C/W rating if Ta = 60C max and Tj = 125C max. 0.26 amps can be obtained from U17 if the mounting pad is 0.5 sqr. inches. The controller will not need this much current.

U18 and U19 are low drop-out voltage regulators with a tolerance greater than or equal to 1%. 100 mA is available from each device but again the controller will not need this much current.

In the upper left section are circuits with U9 and U11. U11 is used to generate a regulated voltage that is about 5 Volts less than the +32 Volt supply. When the +32 Volt supply is enabled, the circuitry around U9A is used to provide gate voltage to Q14 that is 5 volts greater than the source pin of this FET. The gate of Q14 can be turned off by any one of a few different circuits. These circuits are wired through Q12 and Q13. At this time these transistors are not installed but they may be installed to increase the shut-down time on a detected fault. Without Q12 and Q13 installed, Q14 is only turned off by the microcontroller through Q16.

U10A is used to detect high current in amplifier #1. At 1.10 Vdc, the current to amplifier #1 should be about 8.20 Amps. U10B and U12A are used to detect a high current condition in amplifier stages #2 or #3. With a 2.74 Vdc reference, high current shut down should be about 15 Amps.

U12B is used to detect high power supply voltage. U13A is used to indicate that the power supply voltage is less than 26 volts.

U13B on page 3 is used to detect high reflected power. U13B determines if the power supply temperature gets too hot.

Current Monitoring Sections - A 0.01 ohm 1% 5 Watt thru-hole resistor is used for monitoring the current through several sections of the amplifier. The voltage developed across this resistor is amplified for current monitoring by U14, U15, or U16. The Linear Technology LT1787HVCS8 precision high side current sense amplifier accepts a maximum voltage of 60 Vdc. The 43.2 Kohm resistor from Pin 5 to ground sets the gain of the amplifier to about 17.28. This value is not set with much accuracy since the manufacture internal matches the resistors of this part but their actual resistance value is not closely defined. A trimming resistor is suggested to give a temperature stability of ~200ppm/C but instead the microcontroller will determine the exact gain of the circuit and use a correction factor for measurements.

Page 3:

RF power detector circuits. Q16 is used by the microcontroller to disable the aural circuit of a digital transmitter or in external amplifiers where the amplifier is not to monitor visual power.

The Visual or Forward power circuit is calibrated and presented on the input of U24B pin 5. If this module has the highest detected forward power in a multi-amplifier system, it will have the highest forward power signal. This signal level into U24B pin 5 will be used to set the AGC output voltage of J9-2. If another amplifier has a higher forward power, the level into U24B pin 6 will be higher than pin5 and this amplifiers output signal will not be used to set the voltage level of J9-2.

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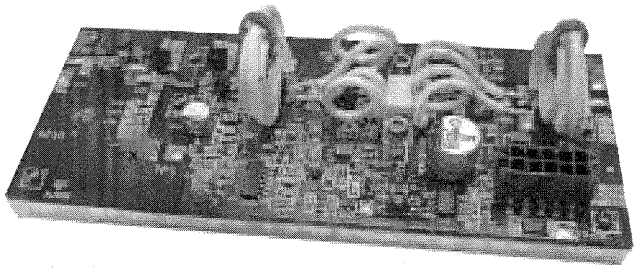
FINISH	CHK	DWB	10/31/06	1308261	B0
	REL	DWB	10/31/06	SCALE - - - -	SHEET 3 OF 3
				D	

PA25-VHF-H-34-A0

High Power RF Amplifiers and Accessories

25W VHF Band III TV Linear Pallet Amplifier

The **PA25-VHF-H-34-A0** is a versatile output or driver pallet amplifier. Offering a minimum of 34dB gain, this two stage amplifier can be used as a driver or output stage depending on the application. With no circuit changes required, the PA25-VHF-H-34 can be configured as a Class A driver or Class AB output stage offering excellent flexibility. A gold metallized LDMOS driver and gold metallized MOSFET output are used in this design.



- No RF assembly or circuit tuning!
- 25 Watts of Linear Output Minimum!
- 34dB typical gain at Channel 13!
- Combined Video and Aural at full rated power!
- Modular Construction for ease of Integration!

Specifications:

Vsup=+32V_{dc}, I_{dq}=0.8A, 170-230MHz

Parameter	Min	Typ	Max	Units
Fundamental Pout, PEP 2-tone, 215-216MHz, IMD3 -30dBc		50		Watts
Linear Power Out, Pk Sync	25	35		Watts
Power Input	8	10	13	+dBm
Power Gain		34		dB
IMD, Full Field Red, NTSC-NA For input signal 10dB better than desired output	-54	-58		dBc
Drain Current		3		A
Input VSWR		1.1:1	1.4:1	
Insertion Phase Variation (unit to unit)		±5		°
Power Gain Variation (unit to unit)		±1		dB
F2 Second Harmonic		-15		dBc
F3 Third Harmonic		-25		dBc
Baseplate Operating Temp	0		+60	°C
Physical Dimensions	2.0" x 5.0" x 1.0" / 5cm x 13cm x 3cm			

All values listed are without pre-correction.

Absolute Maximum Ratings:

Parameter	Value	Units
Maximum Operating Voltage	+32.0	V DC
Stable Operating Voltage	+26.0 to +32.0	V DC
Maximum Bias Current, Q1 Factory set to 0.020A.	0.25	A
Maximum Bias Current, Q4 Factory set to 2.75A.	3.0	A
Maximum Total Drain Current	5	A
Load Mismatch Survival At all phase angles with the base plate held at 40C and Id current limited to 5A, 2 seconds maximum	3:1	
Storage Temperature	-40 to +105	°C
Maximum Operating Baseplate Temperature	+60	°C

Features Include:

- Temperature Compensated Bias
- Temperature Controller- Analog Temp Output
- High Temp alarm with automatic PA disable
- High Temp alarm output
- Amplifier Disable
- Current Sense, Each Transistor
- Connectorized Power and I/O

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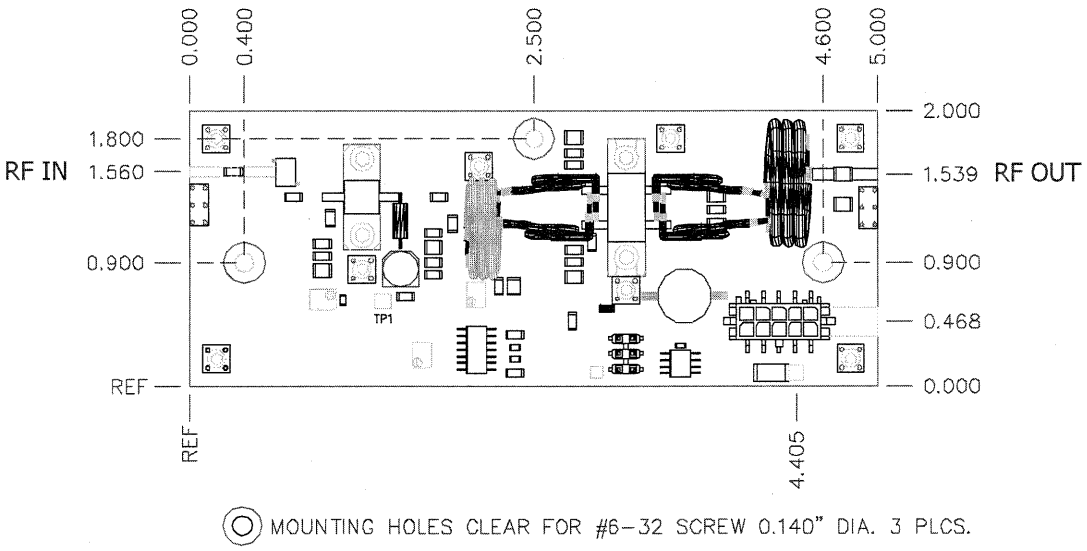
Delta RF Technology, Inc. • 801 East Glendale Ave • Sparks • NV • 89431 • U S A

PA25-VHF-H-34-A0

High Power RF Amplifiers and Accessories

25W VHF Band III TV Linear Pallet Amplifier



Tips for Mechanical Mounting:

1 All holes are clear for #6 Screw. Stainless Steel mounting hardware is recommended, grade 18-8 or better. A lock washer of same material should also be used.
2 Ensure mounting surface is flat to better than 0.003" / "
3 Use a thin layer of thermal compound on the backside of the PA - no more than 0.001" - 0.002" thickness!
4 Torque all screws to 10-12 in-lbs

Considerations for Mechanical Mounting:

- Considerations for proper thermal design include
- Total power dissipated = Total DC Power Consumed x (1-Efficiency)
- Ambient Airflow
- Thermal Resistance of Heat Sink

For this PA, typical DC efficiency is 30%. At 25W Pk power output, 15W Average, +28.0V DC operation, 84 total watts are consumed, which leaves 70W dissipated power. If we assume an input air temperature of +25°C, and a maximum desired baseplate temperature of 55°C, this leaves a temperature differential between baseplate and ambient air of 30°C. The desired thermal resistance for heatsink mounting surface to air is therefore 30°C/74W = 0.4°C/W.
Since the baseplate is aluminum, it is important to find a heat sink that it sized at least as big as the outline of the PA which can give this thermal resistance. For example, a 100mm x 54mm heat sink with serrated fins, 70mm in length, (20 fins across 127mm dimension) with an air velocity of 4 m / s exceeds this value.