8. OPERATIONAL DESCRIPTION - MODEL Axcera-CU50ATD

8.1 General Description

The CU50ATD is a complete 50-watt UHF solid-state, digital television transmitter. It operates at a nominal output power of 50 watts average.

8.2 Technical Specifications

Type of Emission 6M00K1D

Frequency Range.....470 MHz to 608 MHz and 614 to 806 MHz

Output Power.....50 watts average

8.3 Performance Specifications

Operating Frequency Range.....470 MHz to 608 MHz and 614 to 806 MHz

RF output - Nominal:
Power .....50 watts average
Impedance .....50 ohms
Connector ..... "N"

Regulation of Output..... 3%
Signal-to-Noise Ratio (SNR) ..... 27 dB or better
Carrier Frequency Stability.....±1 ppm

Out of Band:
Compliant with FCC Simple or Stringent Mask
(Measured in 30 KHz RBW, relative to total average power)

Data Interface:
Input Rate.....19.39 Mbps, 6 MHz Channel
Input Interface.....SMPTE 310M (ASI optional)

Electrical Requirements

Power Line Voltage .....117/230 volts, 50/60 Hz
Power Consumption ..... 1000 watts

Environmental

Maximum Altitude .....8,500 feet
Operational Temperature Range .....0°C to +50°C

Mechanical

Dimensions:
Width ..... 19" (Rack mount)
Height..... 3RU
Weight.....50 lbs

8.4. System Overview

The CU50ATD is made up of the trays/assemblies listed in Table 8-1.

Table 8-1. CU50ATD Major Trays and Assemblies

MAJOR ASSEMBLY DESIGNATOR	TRAY / ASSEMBLY NAME
A1	Digital Transmitter Tray

8.4.1 Transmitter Tray

The Transmitter accepts an RF On Channel signal (-79 to –8 dBm) and converts it to a DTV RF On Channel output signal at 50 Watts. The transmitter provides linear and nonlinear correction capability for the transmission path as well as internal test sources that are used during initial transmitter installation.

8.4.1.1 (A1) 8 VSB Demodulator Board (1308275)

The RF input to the Transmitter is connected to the J1 BNC connector located on the rear panel of the tray. This RF signal is wired to (A1) the 8 VSB demodulator board (1308275), which generates a SMPTE-310 output at J13. The (A1) 8 VSB demodulator assembly receives an off air 8 VSB signal on any VHF or UHF channel and demodulates this to an MPEG-2 transport stream that is per the SMPTE-310M standard. The input to the assembly is at an "F" style connector on the shielded tuner and can be at a level of –78 dBm to –8 dBm. The tuner (TU1) down converts the RF channel to a 44 MHz IF signal. This IF signal is the input to the digital receiver chip U1. The digital receiver chip subsequently decodes the IF and delivers an MPEG-2 transport stream, on a parallel data bus, to a programmable logic array, U8. U8 clocks the asynchronous MPEG data from the receiver chip and outputs a synchronous data stream at a 19.39 MHz rate to buffer/driver U11. U11 subsequently drives the output at J13 to a lower level that is AC coupled out of the board and is cabled to J42 on the 8 VSB Modulator Board.

8.4.1.2 (A2) 8 VSB Modulator Board (1304883)

The (A2) 8 VSB Modulator Board (1304883) accepts the SMPTE-310 MPEG data stream input at the SMA connector J42 and produces a 6 MHz wide IF output, at the IF Output Jack J38. The IF output is centered at 44 MHz using a pilot carrier of 46.69 MHz generated on the board.

This SMPTE-310 MPEG data stream input is applied to a high-speed window comparator U21 that adjusts the level to a low voltage TTL signal to be used by the Altera FPGA, U3. The SMPTE-310 signal is input to the FPGA to recover the clock and the data. A portion of the clock and recovery circuit is performed by a high-speed comparator, U17, which functions as an external delay circuit.

The FPGA subsequently uses the SMPTE-310 clock and data as the input to the channel coder contained inside the FPGA. The channel coder is a series of DSP blocks defined by the ATSC standard for 8 VSB data transmission. These blocks include the data randomizer, Reed Solomon Encoder, data interleaver, trellis coder, and sync inserter.

The channel coder portion, inside the FPGA, generates the 8 distinct levels in an 8 VSB transmitter. These levels are subsequently input to a linear equalizer that provides for frequency response correction in the transmission path. The linear equalizer is a 67-tap FIR filter that is loaded with tap values from the microcontroller, U1, located on this board. The output of the linear equalizer is then input to two pulse shaping filters, an in phase (I) and a quadrature (Q) filter that are also located inside the FPGA. The pulse shaping filters are FIR filters that have fixed tap values that are preset inside the FPGA. The output of the pulse shaping filters is then applied to a Pre-Distortion Linearizer chip, U4, which can be used to correct for nonlinearities in the data transmission path. The output of the Pre-Distortion chip is gain scaled and output to a dual D/A converter, which output a baseband I and Q analog signal.

The baseband I and Q signals from the D/A converter are applied to differential analog filters that remove some of digital artifacts from the D/A conversion process. The output of the I channel filter is then mixed with the pilot frequency, 46.69 MHz, using mixer U30. The output of the Q filter is mixed with the pilot frequency that is phase shifted 90 degrees using mixer U34. The mixers are current driven devices so that when the outputs of U30 and U34 are connected together, they provide a combined output. This combined output is subsequently input to a final differential output filter which provides the final IF output at the SMA connector, J38. To maintain signal integrity, the IF output is connected to the SMA connector J39 with a small semi-rigid cable assembly. The final IF output then appears at J1-2B.

The 46.69 MHz pilot, that is used in the mixing process is generated from a 46.69 MHz VCXO, U37, that is phase locked to a 10 MHz reference. The VCXO and the 10 MHz are divided down to a common frequency, which is then compared internal to the FPGA. The FPGA subsequently provides error signals to an analog phase locked implemented with op amp stages U45-A, B and C. The output of these compensation stages is used as the control voltage to the VCXO, U37. The phase locked output of U37 is applied to an analog filter to remove harmonics of the pilot and then input to the quadrature splitter Z1. The outputs of Z1 are used as the inputs to the mixers in the analog output section.

8.4.1.3 (A3) IF Pre-Corrector Board (1308796)

The IF output (0 dBm) of the 8 VSB Modulator connects to J2 on the (A3) IF Pre-Corrector Board (1308796), which provides response, in phase and quadrature pre-correction to the IF signal. The Pre-Corrected IF output at J1 is cabled to the IF In Jack on (A4) the Digital Agile Upconverter Board, which up converts the IF to the On Channel RF signal that is cabled to the RF Out Jack of the board. The RF out is connected to J1 the RF input jack on the ALC board. The (A5) ALC Board, (1308570), is used to control the RF drive power to the RF amplifier chain in the transmitter. The board accepts an 8-VSB RF input signal at J1, the RF input jack, at a nominal input level of -3 dBm average power and amplifies it to whatever drive level is necessary to drive the final RF amplifier in the tray to full power. The RF

output of the ALC board at J2, typically 0 to +10 dBm, is cabled to J1 on the Amplifier Assembly.

8.4.1.4 (A6) Amplifier Assembly (1308867)

The (A6) Amplifier Assembly (1308867) is made up of (A6-A1) the 2 Stage UHF Amplifier Board, (1308784) and (A6-A2) the RF Module Pallet w/Philips transistors (1300116). The assembly has approximately 36 dB of gain.

8.4.1.5 (A6-A1) 2 Stage UHF Amplifier Board, (1308784)

The 2 Stage UHF Amplifier Board, (1308784) consists of a driver stage and a parallel connected final amplifier stage, which have a total gain of approximately 23 dB. The working point settings for the 2 Stage Amplifier Board are factory set using the potentiometers R32 for Q2, R15 for Q1, and R24 for Q3 and should not be altered. The input RF connects to the first amplifier stage U2, which has a gain of approximately 14 dB. The output is split by U2 and connected to the final amps. The final amplification circuit consists of parallel-connected push-pull LDMOS amplifier circuits Q1 and Q3 operating in class AB each with approximately 14 dB of gain. The board uses a power supply voltage of 28-32V. The RF transistors are operated at a voltage of 24V generated by the voltage regulators U1 for Q1, U5 for Q3 and U6 for Q2, which provide a separate regulated voltage to each transistor. In order to match the LDMOS impedance to the characteristic impedance of the input and output sides, matching networks are located before and after the amplifier circuits. The hybrid coupler U2 splits the input to the parallel amplifiers and the hybrid coupler U4 combines the amplified outputs. The combined output connects through a directional coupler to J1, the RF output jack of the board. The directional coupler provides an RF sample at J3 that is used by an external overdrive protection circuit. The RF output of the board, when used as a driver, has an output power level of 3 Watts maximum 8-VSB with approximately 1.8 Amps total current draw from the power supply. The board can also be used as the final output stage in a transmitter with the amplifier generating 6 Watts maximum 8-VSB. In the transmitter, the output of the 2 Stage UHF Amplifier Board at J1 connects to the RF input of the RF Module Pallet.

8.4.1.6 (A6-A2) RF Module Pallet w/Philips Transistors (1300116)

The RF Module Pallet w/Philips Transistors (1300116) is made from a RF Module Pallet w/o Transistors (1152336). The amplifier is capable of delivering a maximum output power of 100-Watts peak, with an amplification factor of approximately 13 dB. The amplification circuit consists of push-pull amplifier blocks V1 and V2, connected in parallel and operating class AB. In order to match the impedance of the transistors to the characteristic impedance of the input and output sides, matching networks are placed ahead and behind the amplifier blocks. Transformers Z3 and Z4 at the input to V1 and V2 and Z5 and Z6 at the output of V1 and V2 serve to balance the input and output signals. The paralleling circuit is achieved using the 3-dB input coupler Z1 and the second part of Z1, which is the 3-dB output coupler. The working point settings of the amplifier circuits are factory implemented by means of the potentiometers R9, R11, and R12 and should not be altered. The combined output of Z1 connects to the RF output jack of the board, which is cabled to J2 the output jack of the assembly. The output of the amplifier assembly at J2 connects to the input jack J1 of the output detector board.

8.4.1.7 (A7) Output Detector Board (1308685)

The (A7) Output Detector Board (1308685) provides forward (2V=100%) and reflected (2V=100%) power samples to the transmitter's Control Board for metering and monitoring purposes. R7 is the reflected power calibration pot and R23 is the forward power calibration pot. A Forward power sample, -10 dBm, connects to J4 on the board, which is cabled to the front panel sample jack of the tray. The RF output of the board, typically +46 dBm, is at J2, which is cabled to J2 the RF Output Jack of the tray.

8.4.5 AC Input

The 110VAC or 220VAC, needed to operate the tray, connects through the AC power cord at J6, the power entry module located on the rear panel of the tray. An On/Off 10A/250VAC circuit breaker is part of the power entry module. With the circuit breaker switched On, the (L) line input is wired to F1 a 20 Amp fuse for over current protection. The AC lines are connected to terminal block TB1, which distributes the AC to (A9 and A10) the two DC power supplies. Voltages for the operation of the boards in the tray are generated by (A9) a +5VDC and ±12VDC power supply and (A10) a +32VDC power supply. There are two varistors, mounted on TB1, connected from the line input to neutral and to ground for surge protection. The AC also connects to the (A11) fan mounted on the rear panel of the tray. The fan will run when AC is applied to the tray. The +5VDC and ±12VDC outputs of the (A9) power supply connects to the terminal block (TB2) that distributes the DC to the boards in the tray. Some of the +5VDC and ±12VDC outputs connect directly to the 8 VSB Demodulator and 8 VSB Modulator boards while the other outputs connect through the transmitter's Control Board to the IF Pre-corrector, the Digital Upconverter, the ALC, the Amplifier Assembly and the Output Detector Boards. The +32VDC power supply outputs connect to the (A8) Control Board, which then supplies the switched +32VDC to the (A6) Amplifier Assembly.

8.4.6 Control & Status

Table 1: Transmitter LCD Display

DISPLAY	FUNCTION
LCD	Provides a two-line readout of the input received channel, internal functions, status, and fault conditions.

The front panel has seven pushbuttons for the two for the control of the transmitter and five for control of the displayed menus.

Table 2: Transmitter Control Pushbuttons

PUSHBUTTON	FUNCTION
OPR	When pushed switches the transmitter to Operate.
STBY	When pushed switches the transmitter to Standby.
ENTER	Selects the changes made in the menus and submenus.
Left & Right Arrow	Scrolls through the main menus
Up & Down Arrow	Scrolls through submenus of the main menu when they are present.

Table 3: Transmitter Status and Operate/Standby Indicators

LED	FUNCTION
OPERATE/STANDBY (Green/Amber)	A **Green** LED indicates that the system is in Operate. An **Amber** LED indicates that the system is in Standby.
STATUS (Green/Red/ Amber)	A **Green** LED indicates that the system is functioning normally. A flashing **Red** LED indicates a fault is occurring at this time. An **Amber** LED indicates a fault occurred in the past but the system is now operating normally.

8.4.7 Input and Output Connections

The input connections to the transmitter are made to the jacks mounted on the rear of the tray. The tray accepts an On Channel RF signal at J1, the RF input jack, and outputs a digital RF ON Channel signal at J2, the RF Output Jack. A 10 MHz reference input connects to J3 on the tray. Refer to Figure 2 and to Table 4 that follow for detailed information.

Figure 2: Rear View of the CU50ATD Transmitter.

Table 4: Rear Chassis Connections for the Transmitter.

Port	Type	Function	Impedance
J1	BNC	RF Input: On Channel RF Input	75Ω
J2	N	RF Output: On Channel RF Output	50Ω
J3	BNC	10 MHz Input: External 10 MHz Reference Input	50Ω
J4	25 Pos D	External Amplifier: Interface to external amplifier tray	N/A
J5	16 Pos D	Remote: Remote control and status indications	N/A
J6	IEC	AC Input: AC input connection and On/Off circuit breaker	N/A
J7		Ethernet: (Optional Ethernet connection)	N/A

8.4.8 Remote Connections

The remote connections for the transmitter are made to the Remote 16 Pos "D" connector Jack J5 located on the rear panel of the tray.

Table 5: Remote Connections to J5 for the transmitter.

Signal Name	J5 Pin Designations	Signal Type / Description
RMT Transmitter Operate	1	Discrete Open Collector Input - A pull down to ground on this line indicates that the transmitter is to be placed into the operate mode.
RMT Forward Power	2	Analog Output - 0 to 4.0 V- This is a buffered loop through of the calibrated "System Forward Power ". Indicates the transmitter's Forward power. Scale factor is 100 % / 3.2V.
RMT Transmitter Standby	3	Discrete Open Collector Input - A pull down to ground on this line indicates that the transmitter is to be placed into the standby mode.
Ground	4,8,9,10 & 14	Ground pins available for remote
RMT RF System Interlock	5	When this signal's circuit is completed to ground, the transmitter is allowed to operate. If this circuit is

Signal Name	J5 Pin Designations	Signal Type / Description
		opened, the transmitter switches to Standby.
RMT Reflected Power	6	Analog Output - 0 to 4.0 V- This is a buffered loop through of the calibrated "System Reflected Power ". Indicates the transmitter's Reflected power. Scale factor is 100 % / 3.2V.
RMT Fault Reset	7	Discrete Open Collector Input - A pull down to ground on this line indicates that any transmitter Faults are to be reset.
RMT Operate Status	11	Discrete Open Collector Output - A low indicates that the Transmitter is in Operate.
RMT Fault	13	Discrete Open Collector Output - A low indicates that the Transmitter has a Fault.
RMT Input Fault	15	Discrete Open Collector Output - A low indicates that the Transmitter has an Input Fault.
Not Used	16	N/A

8.4.9 Front Panel Screens

A LCD display located on the front of the transmitter displays the current operating status of the transmitter. The screens are scrolled through using the buttons to the right of the display. The Left & Right Arrows scroll through the Main Menus, which are shown below aligned on the left side. The Up & Down Arrows scroll through the Submenus of the Main Menus, when they are present, which are shown below indented under the Main Menu in which they are contained. The ENTER button selects the changes made. Please refer to the Users Manual for more information regarding front panel screens.