8. OPERATIONAL DESCRIPTION - MODEL Axcera-CHV400BTD

8.1 General Description

The CHV400BTD is a complete 400-watt VHF solid-state, digital television transmitter. It operates at a nominal output power of 400 watts average.

8.2 Technical Specifications

Type of Emission 6M00K1D

Frequency Range ..... 174 MHz to 216 MHz

Output Power..... 400 watts average

8.3 Performance Specifications

Operating Frequency Range ..... 174 MHz to 216 MHz

RF output - Nominal:
Power ..... 400 watts average
Impedance..... 50 ohms
Connector ..... "7/8" EIA

Regulation of Output 3%
Signal-to-Noise Ratio (SNR) ..... 30 dB or better
Carrier Frequency Stability .....±1000 Hz

Data Interface:
Input Rate..... 19.39 Mbps, 6 MHz Channel
Input Interface..... SMPTE 310M (ASI optional)

Electrical Requirements

Power Line Voltage .....230 volts, 50/60 Hz
Power Consumption .....2700 watts

Environmental

Maximum Altitude ..... 8,500 feet
Operational Temperature Range ..... 0°C to +50°C

Mechanical

Dimensions:
Width ..... 22.00”
Height ..... 55.00”
Depth ..... 34.00”
Weight..... 125 lbs

8.4. System Overview

The CHV400BTD is made up of the trays/assemblies listed in Table 8-1.

Table 8-1. CHV400BTD Major Trays and Assemblies

MAJOR ASSEMBLY DESIGNATOR	TRAY/ASSEMBLY NAME
A1	20W Driver Tray
A2	Power Amplifier Tray

8.4.1 Driver Tray

The Transmitter Driver provides an On Channel output signal at 400 Watts.

8.4.1.1 Digital Modulator Board, Part of the Digital Modulator w/Power Conditioner

The Digital Modulator w/Power Conditioner is made up of the Digital Modulator Board and the Power Conditioner Board.

SMPTE-310 Input

The digital modulator board accepts a SMPTE-310 input at the SMA connector J42 from the 8 VSB demodulator board in a BRD system or directly from the RF input jack on the rear panel of the tray in a BTD system. This input is applied to a high speed window comparator U21 that adjusts the level to a low voltage TTL signal to be used by the Altera FPGA, U3. The SMPTE-310 signal is input to the FPGA to recover the clock and the data. A portion of the clock and recovery circuit is performed by a high-speed comparator, U17, which functions as an external delay circuit.

Channel Coder

The FPGA subsequently uses the SMPTE-310 clock and data as the input to the channel coder contained inside the FPGA. The channel coder is a series of DSP blocks defined by the ATSC standard for 8 VSB data transmission. These blocks include the data randomizer, Reed Solomon Encoder, data interleaver, trellis coder, and sync inserter.

The channel coder portion inside the FPGA generates the 8 distinct levels in an 8 VSB system. These levels are subsequently input to a linear equalizer that provides for frequency response correction in the transmission path. The linear equalizer is a 67 tap FIR filter that is loaded with tap values from the microcontroller, U1, located on

this board. The output of the linear equalizer is then input to two pulse shaping filters, an in phase (I) and a quadrature (Q) filter that are also located inside the FPGA. The pulse shaping filters are FIR filters that have fixed tap values that are preset inside the FPGA. The output of the pulse shaping filters is then applied to a Pre-Distortion Linearizer chip, U4, which can be used to correct for nonlinearities in the data transmission path. The output of the Pre-Distortion chip is gain scaled and output to a dual D/A converter, which output a baseband I and Q analog signal.

Analog Output Section

The baseband I and Q signals from the D/A converter are applied to differential analog filters that remove some of digital artifacts from the D/A conversion process. The output of the I channel filter is then mixed with the pilot frequency, 46.69 MHz, using mixer U30. The output of the Q filter is mixed with the pilot frequency that is phase shifted 90 degrees using mixer U34. The mixers are current driven devices so that when the outputs of U30 and U34 are connected together, they provide a combined output. This combined output is subsequently input to a final differential output filter which provides the final IF output at the SMA connector, J38. To maintain signal integrity, this IF output is connected to the SMA connector J39 with a small semi-rigid cable assembly. The final IF output then appears at J1-2B.

Pilot *Frequency Generation*

The 46.69 MHz pilot, which is used in the mixing process, is generated from a 46.69 MHz VCXO, U37 that is phase locked to a 10 MHz reference. The VCXO and the 10 MHz are divided down to a common frequency, which is then compared internal to the FPGA

The FPGA subsequently provides error signals to an analog phase locked implemented with op amp stages U45-A, B and C. The output of these compensation stages is used as the control voltage to the VCXO, U37. The phase locked output of U37 is applied to an analog filter to remove harmonics of the pilot and then input to the quadrature splitter Z1. The outputs of Z1 are used as the inputs to the mixers in the analog output section.

Voltage Requirements

The ±12 VDC and +5VDC needed for operation of the board connect to J1 on the Power Conditioner Board (1309404) which delays the +5VDC so that the ±12 VDC to the 8 VSB Modulator Board is applied first. The voltage output of the power conditioner board is at J2 that is jumpered to J30 on the 8 VSB modulator board.

The ±12 VDC connect to the 8 VSB modulator board at J30-1. The +12V SYS connects to J18A, B & C and to regulator circuits. The +12V SYS is filtered by L2, L3, C105 and C106 before it is applied to the rest of the board as +12VQ and +12VI. The -12 VDC SYS connects to J19A, B & C and to regulator circuit. The -12V SYS is filtered by L6, L7, C111 and C112 before it is applied to the rest of the board as -12VI and –12VQ.

The +12V SYS also connects through the resistor R81 to provide +5V EXT to the rest of the board, and to the regulators U23 that provides +3.3V to the rest of the board and to U27 that provides +1.8V output. The +3.3V also connects to U24 that supplies +1.5V output. The +12V SYS connects to the regulator U25 and U26 to supply the +5VA output. The output of U25 also connects to U28, which provides the +5V output to the rest of the board. +12V SYS is filtered by L4 and C107 to provide the +12V

output to the board. The –12V SYS also connects to the regulator U22 that provides the –5V VA to the rest of the board. -12V SYS is filtered by L5 and C108 to provide the -12V output to the board.

8.4.1.2 IF Pre-Corrector Board

The IF Pre-Corrector Board provides ALC, automatic or manual, gain control of the IF level. The board also supplies pre-correction Response, In Phase and Quadrature Non-Linear adjustments. The board has the circuitry for ALC Fault, Input Fault and Modulation Fault monitoring and indications.

The input IF signal at J2, typically 0 dBm peak power centered at 36 or 44 MHz, is fed to a splitter circuit Z1 which produces two equal outputs, one at Port 1 and the other at Port 2. The output at Port 1 connects to the input and modulation fault circuitry. The output at Port 2 connects to the pin-diode attenuator circuit.

Pin-Diode Attenuator Circuit

The output of Z1 at Port 2 connects to a pin-diode attenuator circuit that consists of CR1, CR2 & CR3. Each of the pin diodes contains a wide intrinsic region; this makes the diodes function as voltage-variable resistors at this intermediate frequency. The value of the resistance is controlled by the DC bias supplied to the diode. The pin diodes are configured in a pi-type attenuator configuration where CR1 is the first shunt element, CR3 is the series element, and CR2 is the second shunt element. The control voltage, which can be measured at TP2, originates either from the ALC circuit when the switch S1 is in the ALC Auto position, between pins 2 and 3, or from pot R37, MAN GAIN, when S1 is in the Manual Gain position, between pins 1 and 2. In the pin diode attenuator circuit, changing the amount of current through the diodes by forward biasing them changes the IF output level of the board. By controlling the value of the voltage applied to the pin diodes, the IF signal level is maintained at the set level.

When the IF signal passes out of the pin-diode attenuator through C7, it is applied to the modular amplifier U1. This device contains the biasing and impedance-matching circuits that makes it operate as a wide-band IF amplifier. The output of U1 connects through C8, NON-LIN IN, to the Summing Port input of the splitter Z3. The splitter provides the outputs to the Non-Linear Pre-Corrector stages. The output at Port 1 connects to the Quadrature Pre-Corrector and the output at Port 2 connects to the In Phase Pre-Correctors.

In Phase and Quadrature Corrector Circuits

Two of the Pre-Corrector stages are in the In Phase Amplitude pre-correction path and one stage is in the Quadrature Phase pre-correction path. Each stage has a variable threshold control adjustment, R67 and R69, in the In Phase path, and R89 in the Quadrature path, which determine the point that the gain is changed in each of the stages.

The output of Z3 at Port 2 connects to J10, which is jumpered through W5 to J9. External In-Phase Corrector circuits may be connected between these jacks. The signal from J9 connects to the first corrector stage on the board. The first corrector stage in the In Phase path operates as follows. The In Phase IF signal is applied to the transformer T3, which doubles the voltage swing by means of a 1:4 impedance transformation. Resistors R75 and R78 form an L-pad that lowers the level of the

signal. The input signal level, when it reaches a set level, causes the diodes CR9 and CR11 to turn on, generating current flow that puts them in parallel with the L-pad. When the diodes are put in parallel with the resistors, the attenuation through the L-pad is lowered, causing stretch of the signal.

The signal is next applied to amplifier U8 to compensate for the loss through the L-pad. The breakpoint, or cut-in point, for the first corrector is set by controlling where CR9 and CR11 turn on. This is accomplished by adjusting the threshold cut-in resistor R67. R67 forms a voltage-divider network from +6.8 VDC to ground. The voltage at the wiper arm of R67 is buffered by the unity-gain amplifier U5A. This reference voltage is then applied to R68, R71, and C33 through L11 to the CR9 diode. C33 keeps the reference from sagging during the vertical interval. The .9 VDC reference voltage is applied to the unity-gain amplifier U5B. The reference voltage is then connected to diode CR11 through choke L12. The two chokes L11 and L12 form a high impedance for IF that serves to isolate the op-amp ICs from the IF.

After the signal is amplified by U8, it is applied to the second corrector stage in the In Phase path through T4. The second In Phase Stage and the stage in the Quadrature path operate in the same fashion as the first. All three corrector stages are independent and do not interact with each other. The In Phase Correctors can be disabled by moving the jumper W4 on J8 to the Disable position, between pins 1 & 2. This moves all of the breakpoints past the signal peaks so that they will have no affect. The pre-distorted IF signal, in the In Phase path, connects to the op amp U9 whose output level is controlled by R88, the in phase amplifier adjustment. The pre-distorted In Phase IF signal connects to Port 1 on the combiner Z4.

The Port 1 output of Z3 connects from J11 through the W6 jumper to J12. The IF is connected to T5, the 1:4 impedance transformer input to the Quadrature circuit. External Quadrature Corrector stages may be connected between jacks J11 and J12. The pre-distorted IF signal, in the Quadrature Phase path, connects to the op amp U11 whose output gain is set by R102, which provides a means of balancing the level of the Quad Phase pre-distorted IF signal that connects to Port 2 on the combiner Z4.

The Quadrature and In Phase pre-distorted IF signals are combined by Z4, amplified by U10 and connected through C57 to the S Port of the splitter Z2. Z2 provides two outputs of the combined Quadrature and In Phase pre-distorted IF signals.

Frequency Response Corrector Circuit

The output of Z2 at Port 2 connects to the first corrector stage of the three-stage frequency-response corrector circuit. The three stages are adjusted as needed to attain the best response across the bandwidth. The frequency-response corrector circuit operates as follows. Variable resistors R24, R25 and R26 are used to adjust the depth and gain of the notches and variable caps C14, C15 and C16 are used to adjust the frequency position of the notches. These are adjusted as needed to compensate for frequency response problems. The jumpers W1 on J4, W2 on J5 and W3 on J6 are moveable to set the frequency response of the circuits for 44 MHz, which is between pins 2 & 3 or between 1 & 2 for 36 MHz.

The Non-Linear and Frequency Response pre-corrected IF is connected to the op-amp U2. After amplification, the IF is split with one path connected through a divider

network to J1 the IF output jack on the board, -12 dBm. The other path is fed through a divider network to J3 the IF Sample Jack, –18dBm.

ALC Circuit

The other non-linear pre-corrector output of Z2 at Port 1 connects to the input of the ALC circuit. The IF signal is applied to the transformer T1, which doubles the voltage swing by means of a 1:4 impedance transformation. It is connected to the ALC detector circuit, consisting of C11, CR4 and R21. The detected ALC level output is amplified by U3A and wired to U3B, pin 6, where it is summed with the power control setting of R40 the ALC Adjust pot. The output of U3B connects through S1 pins 2 to 3, if it is in the ALC position, to the pin-diode attenuator circuit, CR1, CR2 & CR3. The high forward biases them more or less, that increases or decreases the IF level, therefore the output level. When the input signal level increases, the forward bias on the pin attenuator decreases, therefore the output power decreases, that maintains the output power as set by the customer.

The ALC voltage is set for 1.0 VDC at TP1 with a –12 dBm peak sync output as measured at J1 of the board. The ALC action starts with the ALC detector level monitored at TP1. The detector output at TP1 is nominally, 1.0 VDC, and is applied through resistor R33 to a summing point at op-amp U3B pin 6. The current available from the ALC detector is offset, or complemented, by current taken away from the summing junction. In normal operation, U3B pin 6, is at 0 VDC when the loop is satisfied. If the recovered or peak-detected IF signal level at the IF input to this board should drop, which normally indicates that the output power has decreased, the null condition no longer occurs at U3B pin 6. When the level drops, the output of U3B pin 7 goes more positive. If S1 is in the Automatic position, it will cause the ALC pin-diode attenuators CR1, CR2, and CR3 to have less attenuation and therefore increase the IF level that will compensate for the decrease in the output power level.

If the ALC cannot increase the input level enough to satisfy the ALC loop, due to the lack of range, an ALC fault will occur. The fault is generated because U3C pin 9, increases above the trip point set by R47 and R50 until it conducts. This makes U3C pin 8, high and causes Q3 to conduct, which lights the Red ALC Fault LED DS1.

Input Fault and Modulation Fault Circuitry

The input IF signal at Z1 Port 1 connects to the input and modulation fault circuitry at T2. T2 doubles the voltage swing by means of a 1:4 impedance transformation. The output is connected to a detector circuit, consisting of R54, CR6, R58 and C19. The detected IF level output is amplified by U4A and then split. There is a Test Point at TP3 for a voltage reference check of the input level.

One output of U4A is connected to the detector CR5 that produces a Peak Sync Voltage, which is applied to the Op-Amp U12A. The detector provides a reference that determines the IF signal level at the input to the Board. The operation of the Threshold Detector is as follows. The Minimum IF Input level at TP3 is fed through detector CR5 to the Op-Amp IC U12A Pin 2. The reference voltage for the Op-Amp is determined by the voltage divider consisting of R52 and R57 off the +12 VDC line. When the detected input signal level at U12A Pin 2 falls below this reference threshold, approximately 10 dB below the normal input level, the output of U12A at Pin 1, goes to the +12 VDC Rail. This High is connected to the Gate of Q4 which forward biases it and creates a current path from the +12 VDC line through the Red

LED DS2, the Input Level Fault Indicator which lights, and the Transistor Q4 to Ground. The High also connects through the diode CR7 to the Gate of Q6 that conducts and connects a low to J7-1, Input Loss, which is wired to the Control Board for control and monitoring.

The Video Input Level at TP3 is also fed to a modulation loss circuit consisting of the IC U4B, U12B and associated component. When the input signal level to the U4B falls below the reference set by R62 and R60, which acts as a loss of Modulation Detector, the output of U4B, goes high which is split. One part biases On the Transistor Q9. A current path is then established from the +12 VDC line, the resistors R63 and R64, the Red LED DS3, the Modulation Loss Indicator, which lights, through Q9 to ground. The other High output of U4B is connected to U12B pin 5 whose output at pin 7 goes High. This high connects to the gate of Q8 Biasing it On. With Q8 On, a low is connected to J7-2, Modulation Loss, which is wired to the Control Board for control and monitoring.

±12 VDC, +6.8 VDC, and VREF needed to operate the Board

The ±12 VDC connects to the board at jack J7. The +12 VDC connects to J7 pins 5 and 6 and is filtered by L10 and C25 before it is applied to the rest of the board. The -12 VDC connects to J7 pin 8 and is filtered by L9 and C23 before it is applied to the rest of the board.

Two reference voltages are needed for the operation of the pre-corrector circuits. One +12 VDC input is split by R103 and R104. The split +12 VDC output through R103 connects to the Zener diode VR1, which generates the +6.8 VDC output that is used in the pre-corrector stage. The split +12 VDC output through R104 connects to the diodes CR15 and CR16 that supply a .9 VDC reference output voltage, VREF, which provides temperature compensation for the two diodes in each of the in phase and quadrature pre-corrector stages.

8.4.1.3 Frequency Agile Upconverter Board (1309695)

The board takes a 44 MHz or 36 MHz IF signal and converts it to a TV channel in the range of 54-860 MHz. The IF input signal, (≈-8dBm level), is connected to J6 on the board. The IF first passes through a frequency response pre-corrector, consisting of R145, C188, R 146 and C189. The pre-corrector circuit compensates for any response variation in the ceramic filter used to pick the appropriate conversion sideband. The pre-corrected signal is then converted to a second IF centered at 1044 MHz using U16, U18 and associated components. The signal is next applied to a second mixer, U15, where it is converted to the final RF channel frequency. The signal is then sent to a low pass filter that removes unwanted conversion products above 1 GHz, amplified by U21 passed to another low pass filter that removes unwanted conversion products above 1 GHz, amplified by U20 and connected to J7 the RF output jack for the board (≈-3dBm level).

The upconverter has two local oscillators, LO1 and LO2. The LO1 oscillator consists of U1, U2, U5, U6 and amplifiers U3 and U4. The LO1 oscillator operates at 1 GHz for 44 MHz IF inputs and is used to convert the signal to 1044 MHz. In 36 MHz IF systems, this oscillator circuit operates at 1.008 GHz. The Red LED DS4 will light if the PLL for the LO1 oscillator is not locked.

The second LO, LO2, consists of two VCOs, U26 and U31, that are used to generate the second LO. One VCO operates from 1.1-1.5 GHz and the second from 1.5-1.9 GHz. The Red LED DS2 will light if the PLL for the LO2 oscillator is not locked.

Both of the LOs, LO1 and LO2, are locked to an on board 10 MHz VCXO. The 10 MHz VCXO circuit consists of U36, U39, the VCTCXO Y1 and associated components. When an external 10 MHz signal is applied to J10 on the board, the internal VCXO is locked to the external 10 MHz, otherwise, it is free-running. The Red LED DS6 will light if an

8.4.1.4 ALC Board, Innovator CX Series

The ALC Board, Innovator CX Series, is used to control the RF drive power to the RF amplifier chain in the CU30, CU50, CU100 and CU125 systems. The board accepts an 8-VSB RF input signal at a nominal input level of -3 dBm average power and amplifies it to whatever drive level is necessary to drive the final RF amplifier in the tray to full power. The input signal to the board at J1 is split by U4, with one half of the signal driving a PIN diode attenuator, DS1 and DS2, and the other half driving a detector, U13, that is used to mute the PIN attenuator when there is no input signal. The output of the PIN attenuator is sent to two cascaded amplifiers, U2 and U3, which are capable of generating +10 dBm average power from the board at J2.

The PIN attenuator is driven by an ALC circuit or by a manual fixed voltage bias, depending on the position of switch S1. When the switch is pointing to the left, looking from the front of the tray, the ALC circuit is enabled. When the switch is pointing to the right, the ALC circuit is disabled and the PIN attenuator is controlled through the Manual gain pot R62. When the switch is in either ALC or manual, the voltage in the unused circuit is preset low by the circuitry connected to pins 4-6 on SW1. This allows the RF power to ramp up slowly to full power when the switch changes positions. CR8, C33 and associated components control the ramp up speed of the manual gain circuit. CR9, C42 and their associated circuits do the same thing for the ALC circuit. The practical effect of this is to preset the RF drive power to near zero output power when enabling and disabling the ALC, followed by a slow controlled ramp up of power.

The ALC circuit normally attempts to hold the tray output power constant, but there are four faults that can override this. These faults are Input Fault, VSWR Cutback Fault, VSWR Shutdown Fault and Overdrive Fault.

The Input Fault is generated by comparator U7C and presets the PIN attenuator and ALC circuit to maximum attenuation whenever the input signal drops below about -7 dBm. Test point TP2 allows the user to measure the detected input voltage.

The VSWR cutback circuit is set so that the ALC circuit will start reducing RF drive once the Reflected power reaches a level of about 6% and will keep reducing the drive to maintain that level. U8A, U8B and their associated components, diode-or the metering voltages, which generates this cutback. The forward power is scaled to 2V = 100 % and the reflected power is scaled to 2V = 25%. The Reflected metering voltage is doubled again by U8B so that when the voltage of U8B exceeds the voltage at the output of U8A, the reflected power takes over the ALC circuit. Once the U8B voltage drops below the forward power at U8A, the forward power takes over again.

The VSWR shutdown circuit will shut the tray down if the Reflected power increases to 15% or higher, which can happen if the tray sees reflected power when the ALC is in manual.

The Overdrive protection looks at a sample of the RF signal that is applied to J1 of the board. The peak level of this signal is detected and can be measured on TP1. This voltage is applied to a comparator with the threshold set by R38. If this threshold is exceeded, the ALC circuit mutes then ramps up to try again. This circuit also works in manual gain as well.

8.4.1.5 Amplifier Assembly – Used in the CHV20B Tray

The (A6) Amplifier Assembly (1313959) is made up of (A6-A1) the VHF HB Pre-Driver Assembly (1313899) and (A6-A2) the 100 Watt Amplifier Pallet, Italmec (1313484). The ALC Board (1308570) is also part of this assembly. The assembly has approximately 36 dB of gain.

8.4.1.6 VHF HB Pre-Driver Assembly

The VHF HB Pre-Driver Assembly (1313899) consists of a driver stage and a parallel connected final amplifier stage, that have a total gain of approximately 23 dB.

The input RF at J1 connects through a matching network consisting of R11-R13 to a splitter IC Z1. The split outputs connect to parallel-connected push-pull 1 Watt high linearity amplifier ICs (U1& U4) operating in class AB each with approximately 17 dB of gain. The board uses a power supply voltage of +42VDC that connects to J6. The +42VDC is filtered on the board and connected to the step down transformer T1 which produces a +12VDC output that is used by the two amplifier ICs (U1 & U4). The two amplified outputs are connected to a combiner IC Z2. The combined output connects through a directional coupler U6 to J2, the RF output jack of the board. The directional coupler provides an RF sample at J4 that is used by an external overdrive protection circuit located on the (A6-A3) ALC Board. The output of the pre-driver amplifier assembly at J2 connects to the RF Input connection on the (A6-A2) 100W Amplifier Pallet, Italmec.

8.4.1.7 50 Watt Amplifier Pallet, Italmec

The 50 Watt Amplifier Pallet, Italmec is made by Italmec for Axcera's use. This broadband amplifier operates in the frequency range of 170 to 240 MHz. The amplifier is capable of delivering a maximum output power of 25 Watts digital, with an amplification factor of approximately 24 dB. The RF output of the pallet is wired to J2 the RF output jack of the 20W driver amplifier assembly. The output of the 20W driver amplifier assembly is cabled to the J1 on (A7) the output metering detector board (1313747).

8.4.1.8 Output Metering Detector Board

The (A7) Output Detector Board provides forward (2V=100%) and reflected (2V=25%) power samples to the CX Control Board for metering and monitoring purposes. R7 is the reflected power calibration pot and R23 is the forward power calibration pot. A Forward power sample, -10 dBm, connects to J4 (-10 dBm typical) on the board, which is cabled to the front panel sample jack of the tray. The RF

output of the board will vary depending in which system it is located, is at J2, which is cabled to J9 the RF Output Jack of the amplifier tray.

8.4.1.9 Control Card, Innovator CX

The Innovator CX control board provides the overall system control for the CXB system. There are two main elements of the board, U7 and U9. U7 is a programmable logic device that is loaded with firmware, which provides the overall system control. It decides whether or not to allow the system to generate RF output power, and turns the +32 VDC power supply on and off depending on whether or not it is receiving any faults, either faults generated on board, or faults generated externally. The second major component of the board is the microcontroller U9, which controls the front panel indications and drives the display. The U9 microcontroller is not involved in the decision making process, U7 does that. Rather, it is layered on top of U7 and is the EPLD's interface to the outside world. Information is passed between the microcontroller and the EPLD. The microcontroller communicates information to and from the front panel and sends the EPLD the information it needs to decide whether or not to allow the system to turn on. The front panel viewable LEDs DS3 for Operate/Standby and DS4 for Status indicate the current operating condition of the system are mounted on and controlled by this board. The U9 microcontroller can also communicate, using the Optional Ethernet Kit, with a daughter card that allows the user to view remote control parameters via a web Ethernet interface.

The ±12 VDC and +5 VDC from the (A9) power supply are routed to the other boards in the tray through this board. The (A10) +28/+42 VDC power supply connects the +28/+42 VDC to the board at J19-1 with 4 common. The ±12 VDC and +5 VDC input voltages to this board is connected through J21 and filtered before being connected to the rest of the board. +12 VDC connects through J21-1, +5VDC through J21-2 & 3, and -12 VDC through J21-6. Common connections for the input voltages are connected to J21-4 & 5. The ±12 VDC and +5 VDC are used on this board and also routed to the other boards in the tray through this board. The +3.3 VDC for the microcontroller and programmable logic array, mounted on the board, is provided by the voltage regulator IC U6 from the filtered +5 VDC input. The output of U6 can be adjusted to +3.3 VDC using R120.

8.4.1.10 Power Supplies used in CHV20B

Voltages for the operation of the boards in the tray are generated by (A9) a +5VDC and ±12VDC power supply and (A10) a +28/+42VDC power supply. The 230VAC input to the tray connects through the AC power cord at J10, the power entry module located on the rear panel of the tray.

An On/Off 10A/250VAC circuit breaker is part of the power entry module. With the circuit breaker switched On, the (L) line input is wired to F1 a 10 Amp fuse for over current protection. The AC lines are connected to terminal block TB1, which distributes the AC to (A9 and A10) the two DC power supplies. There are two varistors, mounted on TB1, connected from the line input to neutral and to ground for surge protection. The AC also connects to the (A11) fan mounted on the rear panel of the driver trays, but in the CHV20B system the fan is connected through the A10 power supply. In trays other than the CHV20B, the fan will run when AC is applied to the tray and the circuit breaker is switched On. The +5VDC and ±12VDC outputs of the (A9) power supply connects to the terminal block (TB2) that

distributes the DC to the boards in the tray. Some of the +5VDC and ±12VDC outputs connect directly to the 8 VSB Demodulator and 8 VSB Modulator boards while the other outputs connect through the CX Control Board to the IF Precorrector, the Digital Upconverter, the ALC, the Amplifier Assembly and the Output Metering Detector Boards.

The +28/+42VDC outputs of the (A10) power supply connect to the (A8) CX Control Board, which then supplies the switched +24/+42VDC to the (A6) Amplifier Assembly. In CHV20B trays the DC output of the (A10) power supply also connects to the (A11) fan mounted on the rear panel, which will operate when AC is applied to the tray, the On/Off circuit breaker is On and the (A10) power supply is operating.

AC Input

The 230VAC, needed to operate the tray, connects through the AC power cord at J6, the power entry module located on the rear panel of the tray. An On/Off 10A/250VAC circuit breaker is part of the power entry module. With the circuit breaker switched On, the (L) line input is wired to F1 a 20 Amp fuse for over current protection. The AC lines are connected to terminal block TB1, which distributes the AC to (A9 and A10) the two DC power supplies. Voltages for the operation of the boards in the tray are generated by (A9) a +5VDC and ±12VDC power supply and (A10) a +32VDC power supply. There are two varistors, mounted on TB1, connected from the line input to neutral and to ground for surge protection. The AC also connects to the (A11) fan mounted on the rear panel of the tray. The fan will run when AC is applied to the tray. The +5VDC and ±12VDC outputs of the (A9) power supply connects to the terminal block (TB2) that distributes the DC to the boards in the tray. Some of the +5VDC and ±12VDC outputs connect directly to the 8 VSB Demodulator and 8 VSB Modulator boards while the other outputs connect through the transmitter's Control Board to the IF Pre-corrector, the Digital Upconverter, the ALC, the Amplifier Assembly and the Output Detector Boards. The +32VDC power supply outputs connect to the (A8) Control Board, which then supplies the switched +32VDC to the (A6) Amplifier Assembly.

8.4.6 Control & Status

Table 1: Transmitter LCD Display

DISPLAY	FUNCTION
LCD	Provides a two-line readout of the input received channel, internal functions, status, and fault conditions.

The front panel has seven pushbuttons for the two for the control of the transmitter and five for control of the displayed menus.

Table 2: Transmitter Control Pushbuttons

PUSHBUTTON	FUNCTION
OPR	When pushed switches the transmitter to Operate.
STBY	When pushed switches the transmitter to Standby.
ENTER	Selects the changes made in the menus and submenus.
Left & Right Arrow	Scrolls through the main menus
Up & Down Arrow	Scrolls through submenus of the main menu when they are present.

Table 3: Transmitter Status and Operate/Standby Indicators

LED	FUNCTION
OPERATE/STANDBY (Green/Amber)	A **Green** LED indicates that the system is in Operate. An **Amber** LED indicates that the system is in Standby.
STATUS (Green/Red/ Amber)	A **Green** LED indicates that the system is functioning normally. A flashing **Red** LED indicates a fault is occurring at this time. An **Amber** LED indicates a fault occurred in the past but the system is now operating normally.

8.4.7 Input and Output Connections

The input connections to the transmitter are made to the jacks mounted on the rear of the tray. The tray accepts an On Channel RF signal at J1, the RF input jack, and outputs a digital RF ON Channel signal at J9, the RF Output Jack. A 10 MHz reference input connects to J3 on the tray. Refer to Figure 2 and to Table 4 that follow for detailed information.

Table 4: Rear Chassis Connections for the Driver.

Port	Type	Function	Impedance
J1	BNC	Input A: On Channel RF Input (BRD) –78 to –8 dBm or SMPTE-310 Input (BTD)	50 Ohms
J2	BNC	Input B: On Channel RF Input (BRD) –78 to –8 dBm or SMPTE-310 Input (BTD)	50 Ohms
J6	BNC	10 MHz Input: Optional External 10 MHz Reference Input	50 Ohms
J7	BNC	1 PPS Input: Optional External 1 PPS Reference Input	50 Ohms
J9	N	RF Output: On Channel RF Output	50 Ohms
J10	IEC	AC Input: AC input connection to 85-264VAC Source and On/Off circuit breaker	N/A
J11	9 Pos Male D	External Amplifier: Interface to System and external amplifier trays, if present. Also provides two interlocks, one for RF System and one for Reject Load. If the interlocks are not used, jumpers from J11-5 to J11-9, ground, for RF system Interlock and from J11-6 to J11-9 are needed to allow the transmitter to go to operate.	N/A
J12	15 Pos Female D	Remote: Remote control and status indications	N/A
J13	RJ-45	Serial: Provides communication to System and to external amplifier trays, if present.	N/A
J14	RJ-45	Ethernet: Optional Ethernet connection. May not be present in your tray.	N/A
J15 Front Panel	BNC	RF Sample: Output Sample from Output Detector Board. In a CU50, the sample level at J15 is approximately 60dB down from the output power level of the tray.	50 Ohms
J16 Front Panel	9 Pos Female D	Serial: Used to load equalizer taps into the modulator.	N/A

Table 5: Rear Chassis Connections for the Power Amplifier.

Port	Type	Function	Impedance
J1	N	RF Input: On Channel RF from CU driver tray	50Ω
J2	7/16" (1.1cm) Din	RF Output: On Channel RF Output	50Ω
J3	IEC	AC Input: AC input connection to 230VAC Source	N/A
J4	9 Pos D	Remote: Amplifier Control Interface (Connects to J11 on the driver tray)	N/A
J5	RJ-45	Serial data	N/A
J8 Front Panel	BNC	RF Sample: Output Sample from Combiner thru Control Board. In a CU500, the sample level is approximately 70dB down from the output power level of the tray.	50Ω

8.4.8 Remote Connections

The remote connections for the transmitter are made to the Remote 16 Pos "D" connector Jack J5 located on the rear panel of the tray.

Table 6: Remote Connections to J5 for the transmitter.

Signal Name	J5 Pin Designations	Signal Type/Description
RMT Transmitter Operate	1	Discrete Open Collector Input - A pull down to ground on this line indicates that the transmitter is to be placed into the operate mode.
RMT Forward Power	2	Analog Output - 0 to 4.0 V- This is a buffered loop through of the calibrated "System Forward Power ". Indicates the transmitter's Forward power. Scale factor is 100 % / 3.2V.
RMT Transmitter Standby	3	Discrete Open Collector Input - A pull down to ground on this line indicates that the transmitter is to be placed into the standby mode.
Ground	4,8,9,10 & 14	Ground pins available for remote
RMT RF System Interlock	5	When this signal's circuit is completed to ground, the transmitter is allowed to operate. If this circuit is opened, the transmitter switches to Standby.
RMT Reflected Power	6	Analog Output - 0 to 4.0 V- This is a buffered loop through of the calibrated "System Reflected Power ". Indicates the transmitter's Reflected power. Scale factor is 100 % / 3.2V.
RMT Fault Reset	7	Discrete Open Collector Input - A pull down to ground on this line indicates that any transmitter Faults are to be reset.
RMT Operate Status	11	Discrete Open Collector Output - A low indicates that the Transmitter is in Operate.
RMT Fault	13	Discrete Open Collector Output - A low indicates that the Transmitter has a Fault.
RMT Input Fault	15	Discrete Open Collector Output - A low indicates that the Transmitter has an Input Fault.

Signal Name	J5 Pin Designations	Signal Type/Description
Not Used	16	N/A

8.4.9 Front Panel Screens

A LCD display located on the front of the transmitter displays the current operating status of the transmitter. The screens are scrolled through using the buttons to the right of the display. The Left & Right Arrows scroll through the Main Menus, which are shown below aligned on the left side. The Up & Down Arrows scroll through the Submenus of the Main Menus, when they are present, which are shown below indented under the Main Menu in which they are contained. The ENTER button selects the changes made. Please refer to the Users Manual for more information regarding front panel screens.

8.5.1 Power Amplifier Tray

8.5.1.1 System Metering Board

The function of the System Metering Board is to detect forward and reflected output power samples and generate output voltages that are proportional to the power levels of the sampled signals for use by the control monitoring assembly in the exciter/driver tray.

There are two identical signal paths on the board: one for forward power and one for reflected power. A sample of the forward output power, from the external (A11) output coupler, enters the board at the SMA jack J3. The signal is filtered and connected to resistors R5, R3 and R6 that form an input impedance-matching network to Pin 3 on U1. The forward power signal is detected by the RF detector IC U1. The detected output at pin 7 is split with one half connected to the forward average calibration pot R7, digital, which adjusts the level of the signal connected to Pin 11 on U2. The other half of the split is connected to the peak calibration pot R18, analog, which adjusts the level of the signal connected to Pin 8 on U2. U2 is a Bilateral Switch IC whose output, digital or analog, is controlled by the selection of the modulation type in the exciter/driver tray. In this BTC transmitter the average, digital, output connects to the amplifier IC U3A that is wired to the SYS_FWD and RMT_FWD Power Metering Outputs. A reading of 2 VDC measured at TP1 is equal to a 100% Forward Power reading on the meter. The SYS_FWD level connects to J9 on the board that is cabled to J11 on the exciter/driver tray for use in the control monitoring assembly. The RMT_FWD level connects to J10 on the board for use by remote control and monitoring.

A sample of the reflected output power, from the external (A11) output coupler, enters the board at the SMA jack J8. The signal is filtered and connected to resistors R26, R22 and R27 that form an input impedance-matching network to Pin 3 on U6. The reflected power signal is detected by the RF detector IC U6. The detected output at pin 7 is connected to the reflected calibration pot R25, which adjusts the level of the signal connected to the amplifier IC U3B that is wired to the SYS_RFLD and RMT_RFLD Power Metering Outputs. A reading of 2 VDC measured at TP2 is equal to a 25% Reflected Power reading on the meter. The SYS_RFLD level connects to J9 on the board that is cabled to J11 on the exciter/driver tray for use in the control monitoring

assembly. The RMT_RFLD level connects to J10 on the board for use by remote control and monitoring.

+12 VDC enters the board at J9-1, from the exciter/driver tray and is connected through a filter and isolation circuit consisting of C31, C14 and L5 before it is connected to the regulator IC U5. U5 supplies the +5 VDC needed for operation of the ICs on the board. The +5 VDC is connected through a filter circuit consisting of C15, C19 and C21 before it is connected to the rest of the board.

8.5.1.2 Amplifier Control Board

The Amplifier Control Board uses a Programmable logic device to control the amplifier tray. It takes an enable signal from an external driver tray, and turns the power supplies on whenever the driver has told it to turn on, unless it detects faults internal to the tray. The board monitors the forward and reflected power, the heatsink temperature, the pallet currents, and the power supply voltage and will generate alarm signals if any of those parameters exceed safe limits. The amplifier tray has no front panel display other than a two LEDs, one for Status and one for Enable. The board sends all its output information, including the forward and reflected levels, back to the driver tray, through J4, so the information can be displayed on that tray's LCD Display. The board will generate a Red Blinking Status LED if it detects an alarm, fault, prompting the operator to look at the LCD display on the driver tray to see what fault has occurred.

The +5 VDC inputs to this board are routed through J4 and J5. The +5 VDC inputs are diode Or connected so that either the +5VDC from the (A8) power supply or the +5VDC from the (A9) power supply will operate the board. The +5VDC is split with one output connected to U1 a voltage regulator IC, which provides +5V and +5V_ANALOG as outputs. The +5 VDC is filtered before being connected to the rest of the board. The other +5 VDC output is connected to the regulator IC U2 that supplies +3.3 V to the microcontroller and programmable logic array.

8.5.1.3 Current Metering Board

The current metering board measures the current into the RF output amplifier pallets and supplies this value to the control board. In the CU500 amplifier tray, there are four sensing circuits which are used. Each circuit has two parallel .01Ω series current sensing resistors and a differential input IC that supplies a voltage output that is proportional to the current for metering purposes. The +42VDC from the (A8) power supply connects to TB2 and TB4 on the board. The +42VDC from the (A9) power supply connects to TB8 and TB10 on the board. The +42VDC input at the TB2 input senses the current to the (A1) 878 output amplifier pallet through TB1 on the board. The +42VDC input at the TB4 input senses the current to the (A2) 878 output amplifier pallet through TB3 on the board. The +42VDC input at the TB8 input senses the current to the (A3) 878 output amplifier pallet through TB7 on the board. The +42VDC input at the TB10 input senses the current to the (A4) 878 output amplifier pallet through TB9 on the board.

The four sensing circuits are identical only one will be described. For the (A1) 878 amplifier pallet, the +42VDC from the (A8) switching power supply connects to TB2. R1 and R2 are the parallel .01Ω current sensing resistors which supplies the voltage values to the U1 current sense amplifier IC. R11 is a gain adjust, which is adjusted to eliminate any rSense Error and to place the OpAmp output at 2.61V for 40Amps

sense as measured at TP3. The current sense output at J1-1 connects to the (A7) control board for metering purposes.

8.5.1.4 2-Way Splitter Board

The 2 way splitter board takes the RF Input at J1 (≈12.5 Watts ATSC) on the board and splits it into two equal outputs (≈5Watts ATSC) that connect to the inputs of the two amplifier pallets at J1.

8.5.1.5 500 Watt Amplifier Pallets

There are two 500 Watt Amplifier Pallets mounted on the Amplifier Heatsink Assembly. Each of the amplifier pallets has approximately +25dB of gain for the VHF HB frequency range of 170 to 230 MHz. The pallets operate Class AB and generate 200 Watts ATSC with an input of 1 Watt ATSC.

8.5.1.6 2-Way Combiner Board

The 2 way combiner board takes the two RF Inputs at J4 & J5 (≈200Watts ATSC) on the board and combines them to a single output (≈400Watts) at J1 that connects to J2 the 7/16" (1.1cm) Din RF output jack of the tray.

8.5.1.7 CHV400B, 500 Watt, 750 Watt and 1000 Watt Amplifier Tray Power Supplies

The 230VAC, needed to operate the tray, connects through the AC power cord at J3, the power entry module located on the rear panel of the tray. The AC lines are connected to a terminal block TB1 to which the circuit breaker(s) connect. There are two On/Off 20A/250VAC circuit breakers that are mounted on the back panel of the tray on either side of J3 the AC input jack**. NOTE**: In CHV400B Amplifier tray there is one circuit breaker. With the circuit breaker(s) switched On, the AC is distributed to the one (A8) or two (A8 and A9) DC power supplies. In a standard CHV400B amplifier tray one 20 Amp circuit breaker CB1 connects the AC to the (A8) DC power supply. In all power amplifier trays, TB1 has three varistors (VR1-VR3) connected across the AC input lines for surge and over voltage protection. The AC input connected to TB1 is wired to 2 amp fuses that is connected to the two fans (A11 & A12) mounted on the rear panel of the tray. Both fans will run immediately when AC is applied to the tray.

The +5VDC for the operation of the amplifier control board in the tray is generated by the (A8) or both the (A8 & A9) power supplies at J1-9 on each power supply. The +5VDC from the (A8) power supply connects to J4-8 and the +5VDC from the (A9) power supply connects to J5-8 on the control board. The +5VDC is produced when AC is connected to the tray and the CB1 and/or the CB2 circuit breakers are turned On. Either or both power supplies provides the +5VDC for use by the control board.

The +42VDC needed by the amplifier modules on the heatsink assembly is generated by the (A8 & A9) power supplies in a 750 and 1000W amplifier trays. In a standard CHV400 amp tray there is only the (A8) power supply. The power supplies will operate when AC is connected to the tray, the CB1 circuit breaker for the (A8) power supply and the CB2 circuit breaker for the (A9) power supply, are turned On and a Low is provided on the Inhibit Line that connects to J1-6 on the power supplies from

the control board. The CB1 circuit breaker supplies the AC to the (A8) power supply which provides the +42VDC to the (A2) and (A3) amplifier pallets. The CB2 circuit breaker supplies the AC to the (A9) power supply which provides the +42VDC to the (A4) and (A5) amplifier pallets.