Chapter 3
Circuit Descriptions

3.1 (A4) High-Band VHF Exciter (1070901; Appendix C)

3.1.1 (A4) Aural IF Synthesizer Board, 4.5 MHz (1265-1303; Appendix D)

The aural IF synthesizer board amplifies each of the three possible audio inputs and the amplifier circuits that supply the single audio output. The balanced audio or the composite audio input is connected to the board while the subcarrier audio (SCA) input can be connected at the same time as either of the other two inputs. The board has the 4.5-MHz voltage-controlled oscillator (VCO) and the aural modulation circuitry that produces the modulated 4.5-MHz output. The board also contains a phase lock loop (PLL) circuit that maintains the precise 4.5-MHz separation between the aural (41.25 MHz) and the visual (45.75 MHz) IF frequencies.

3.1.1.1 Balanced Audio Input

The first of the three possible baseband inputs to the board is a 600Ω-balanced audio input (+10 dBm) that enters through jack J2, pins 1 (+), 2 (GND), and 3 (-), and is buffered by U1B and U1C. Diodes CR1 to CR4 protect the input stages of U1B and U1C if an excessive signal level is present on the input leads of jack J2. The outputs of U1B and U1C are applied to differential amplifier U1A; U1A eliminates the common mode signals (hum) on its input leads. A pre-emphasis of 75 ms is provided by R11, C11, and R10 and can be eliminated by removing jumper W5 on J5. The signal is then applied to amplifier U1D whose gain is controlled by jumper W3 on J11. Jumper W3 on jack J11 is positioned according to the input level of the audio signal (0 or +10 dBm). If the input level is approximately 0 dBm, the mini-jumper should be in the high gain position between pins 1 and 2 of jack J11. If the input level is approximately +10 dBm, the mini-jumper should be in low gain position between pins 2 and 3 of jack J11. The balanced audio is then connected to buffer amplifier U2A whose input level is determined by the setting of balanced audio gain pot R13. The output of the amplifier stage is wired to the summing point at U2D, pin 13.

3.1.1.2 Composite Audio Input

The second possible audio input to the board is the composite audio (stereo) input at BNC jacks J3 and J13. The two jacks are loop-through connected; as a result, the audio can be used in another application by connecting the unused jack and removing W4 from J12. Jumper W4 on jack J12 provides a 75Ω-input impedance when the jumper is between pins 1 and 2 of jack J12 and a high impedance when it is between pins 2 and 3. Diodes CR9 to CR12 protect the input stages of U6A and U6B if an excessive signal level is applied to the board. The outputs of U6A and U6B are applied to differential amplifier U2C, which eliminates common mode signals (hum) on its input leads. The composite input signal is then applied to amplifier U2B; the gain of this amplifier is controlled by composite audio gain pot R17. The composite audio signal is connected to the summing point at U2D, pin 13.

3.1.1.3 Subcarrier Audio Input

The third possible input to the board is the SCA input at BNC jack J4. The SCA input has an input impedance of 75Ω that can be eliminated by removing jumper W2 from pins 1 and 2 of J14. The SCA input is bandpass filtered by C66, C14, R22, C15, C67, and R23 and is fed to buffer amplifier U3A. The amplified signal is then applied though SCA gain pot R24 to the summing point at pin 13 of U2D.

3.1.1.4 Audio Modulation of the VCO

The balanced audio, or the composite audio and/or the SCA-buffered audio signals, are fed to the common junction of resistors R14, R20, and R27 that connect to pin 13 of amplifier U2D. The output audio signal at pin 14 of U2D is typically .8 Vpk-pk at a ±25-kHz deviation for balanced or .8 Vpk-pk at ±75-kHz deviation for composite as measured at TP1. This signal is applied to VCO U10. A sample of the deviation level is amplified, detected by U7A and U7B, and connected to J10 on the board. This audio-deviation level is connected to the front panel meter through the transmitter control board.

The audio is connected to CR13 to CR16; these are varactor diodes that frequency modulate the audio signal onto the generated 4.5-MHz signal in U10. U10 is the 4.5-MHz VCO that generates the 4.5-MHz continuous wave (CW) signal. The output frequency of this signal is maintained and controlled by the correction voltage output of U5 PLL IC. The audio-modulated, 4.5-MHz signal is fed to amplifiers U11A and U11B. The output of U11B is connected to the 4.5-MHz output jacks at J7 and J8.

3.1.1.5 Phase Lock Loop (PLL) Circuit

A sample of the signal from the 4.5-MHz aural VCO at the output of U11A is applied to PLL IC U5 at the F_{in} connection. In U5, the signal is divided down to 50 kHz and is compared to a 50-kHz reference signal. The reference signal is a divided-down sample of the visual IF, 45.75-MHz signal that is applied to the oscillator-in connection on the PLL chip through jack J6 on the board. These two 50-kHz signals are compared in the IC and the fV, and fR is applied to the differential amplifier U3B. The output of U3B is fed back through CR17 to the 4.5-MHz VCO IC U10; this sets up a PLL circuit. The 4.5-MHz VCO will maintain the extremely accurate 4.5-MHz separation between the visual and aural IF signals; any change in frequency will be corrected by the AFC error voltage.

PLL chip U5 also contains an internal lock detector that indicates the status of the PLL circuit. When U5 is in a "locked" state, pin 28 goes high and causes the green LED DS1 to illuminate. If the 4.5-MHz VCO and the 45.75-MHz oscillator become "unlocked," out of the capture range of the PLL circuit, pin 28 of U5 will go to a logic low and cause the red LED DS2 to light. A mute output signal from Q3 (unlock mute) will be applied to jack J9. This mute is connected to the transmitter control board.

3.1.1.6 Voltage Requirements

The ±12 VDC needed for the operation of the board enters through jack J1. The +12 VDC is connected to J1-3 and filtered by L2, C3, and C4 before it is connected to the rest of the board. The -12 VDC is connected to J1-5 and filtered by L1, C1, and C2 before it is connected to the rest of the board. +12 VDC is connected to U8 and U9; these are 5-volt regulator ICs that provide the voltage to the U10 and U5 ICs.

3.1.2 (A5) Sync Tip Clamp/ Modulator Board (1265-1302; Appendix D)

The sync tip clamp/modulator board can be divided into five circuits: the main video circuit, the sync tip clamp circuit, the visual modulator circuit, the aural IF mixer circuit, and the diplexer circuit.

The sync tip clamp/modulator board takes the baseband video or 4.5-MHz composite input that is connected to the video input jack (either J1 or J2, which are loop-through connected), and produces a modulated visual IF + aural IF output at output jack J20 on the board. The clamp portion of the board maintains a constant peak of sync level over varying average picture levels (APL). The modulator portion of the

board contains the circuitry that generates an amplitude-modulated vestigial sideband visual IF signal output that is made up of the baseband video input signal (1 Vpk-pk) modulated onto an externally generated 45.75-MHz IF carrier frequency. The visual IF signal and the aural IF signal are then combined in the diplexer circuit to produce the visual IF + aural IF output that is connected to J20, the IF output jack of the board.

3.1.2.1 Main Video Signal Path (Part 1 of 2)

The baseband video or the 4.5-MHz composite input connects to the board at J2. J2 is loop-through connected to J1 and terminated to 75 watts if jumper W4 is on jack J3. With jumper W4 removed, the input can be connected to another transmitter through J1; J1 is loop-through connected to J2.

Test point TP1 is provided to monitor the level of the input. The input is fed to the non-inverting and inverting inputs of U1A, a differential amplifier that minimizes any common-mode hum that may be present on the incoming signal. Diodes CR1 to CR4 form a voltage-limiter network in which, if the input voltages exceed the supply voltages for U1A, the diodes conduct, preventing damage to U1A. CR1 and CR3 conduct if the input voltage exceeds the negative supply and CR2 and CR4 conduct if the input voltage exceeds the positive supply voltage.

The video output of U1A is connected to J22 on the board. Normally, the video at J22 is jumpered to J27 on the board. If the 4.5-MHz composite input kit is purchased, the 4.5-MHz composite signal at J22 connects to the external composite 4.5-MHz filter board and the 4.5-MHz bandpass filter board. These two boards provide the video-only signal to J27 and the 4.5-MHz intercarrier signal to J28 from the 4.5-MHz composite input. The video through the video gain pot R12 (adjusted for 1 Vpk-pk at TP2) connects to amplifier U1B.

The output of U1B, if the delay equalizer board is present in the tray, connects the video from J6, pin 2, to the external delay equalizer board and back to the sync tip clamp/modulator board at J6, pin 4. If the delay equalizer is not present, the video connects through jumper W1 on J5, pins 1 and 2. The delay equalizer board plugs directly to J6 on the sync tip clamp/modulator board. The video from J6, pin 4, is then connected through jumper W1 on J5, pins 2 and 3, to the amplifier Q1. The output of Q1 connects to Q2; the base voltage of Q2 is set by the DC offset voltage output of the sync tip clamp circuit.

3.1.2.2 Sync Tip Clamp Circuit

The automatic sync tip clamp circuit is made up of U4A, Q7, U3B, and associated components. The circuit begins with a sample of the clamped video that is split off from the main video path at the emitter of Q3. The video sample is buffered by U3A and connected to U4A. The level at which the tip of sync is clamped, approximately -1.04 VDC as measured at TP2, is set by the voltage-divider network connected to U4A. If the video level changes, the sample applied to U4A changes. If jumper W7 on J4 is in the Clamp-On position, the voltage from the clamp circuit that is applied to the summing circuit at the base of Q2 will change; this will bring the sync tip level back to approximately -1.04 VDC. Q7 will be turned off and on according to the peak of sync voltage level that is applied to U4A. The capacitors C14, C51, C77, and C41 will charge or discharge to the new voltage level, which biases U3B more or less, through jumper W7 on J4 in the Auto Clamp-On position. U3 will increase or decrease its output, as needed, to bring the peak of sync back to the correct level as set by R152 and R12. This voltage level is applied through U3B to Q2. In the Manual position, jumper W7

on J4 is in the Clamp-Off position, between pins 1 and 2, and adjustable resistor R41 provides the manual clamp bias adjustment for the video that connects to Q2.

Jumper W6 on jack J35 must be in the Normal position, between pins 2 and 3, for the clamp circuit to operate with a normal non-scrambled signal. If a scrambled signal is used, the tray is operated with jumper W6 in the Encoded position, connected between pins 1 and 2. The clamp circuit is set by adjusting depth of modulation pot R152 for the correct depth of modulation as measured at TP2.

Depending on the input video level, the waveform as measured at TP2 may not be 1 Vpk-pk. If W7 on J4 is moved to the Clamp-Off (Manual) position, between pins 1 and 2, the clamp level is adjusted by R41 and will not automatically be clamped to the set level. The output of buffer amplifier U3A drives the sync tip clamp circuit consisting of differential amplifier U4A, FET Q7, and buffer amplifier U3B. U4A is biased by R124, R125, R184, R152, and R126 so that the clamped voltage level at peak of sync is approximately -1.04 VDC as measured at TP2.

3.1.2.3 Main Video Signal Path (Part 2 of 2)

The clamped video from Q2 is connected to white clipper circuit Q3. Q3 is adjusted with R20 and set to prevent video transients from overmodulating the video carrier. The clamped video is connected to sync clipper circuit Q4 (adjusted by R24); Q4 limits the sync to -40 IRE units. The corrected video connects to emitter follower Q4 whose output is wired to unity gain amplifier U2A and provides a low-impedance, clamped video output at pin 1.

3.1.2.4 Visual Modulator Circuit

The clamped video signal from U2A is split. One part connects to a metering circuit, consisting of U20 and associated components, that produces a video output sample at J8-6 and connects through the transmitter control board to the front panel meter for monitoring. The other clamped video path from U2A is through a sync-stretch circuit that consists of Q5 and Q6. The sync-stretch circuit contains R48; R48 adjusts the sync stretch magnitude (amount) and R45 adjusts the cut-in. This sync-stretch adjustment should not be used to correct for output sync problems, but it can be used for video input sync problems. The output of the sync-stretch circuit connects to pin 5, the I input of mixer Z1.

The video signal is heterodyned in mixer Z1 with the visual IF CW signal (45.75 MHz). The visual IF CW signal enters the board at jack J15 and is connected to U9, where it is amplified and wired to pin 1, the L input of mixer Z1. The adjustable capacitor C78 and resistor R53 are set up to add a small amount of incidental carrier phase modulation (ICPM) correction to the output of the mixer stage to compensate for any non-linearities generated by the mixer.

The modulated 45.75-MHz RF output of mixer Z1 is amplified by U5 and is fed to double-sideband visual IF output jack J18. The level of this output jack is adjusted by R70. J18 is the visual IF loop-through output jack that is normally jumpered to J19 on the board. If the optional visual IF loop-through kit is purchased, the visual is connected out of the board to any external IF processor trays.

After any external processing, the modulated visual IF, double-sideband signal re-enters the board through J19. The visual IF from J19 is amplified by U10 and U11 and routed through the vestigial sideband filter network,

consisting of T1, FL1, and T2, and produces a vestigial sideband visual IF signal output. The filtered vestigial sideband visual IF is amplified by U7 and connected to a T-type attenuator. R62 can be adjusted to set the visual IF gain; this is the amount of visual IF signal that is coupled to amplifier IC U8. R63 and C30 are adjusted for the best VSBF frequency response. The amplified IF signal is fed to the input of the diplexer circuit that consists of R76, L13, and L12. A detected voltage sample of the visual IF is available at test point TP5.

3.1.2.5 41.25-MHz Aural IF Circuit

On this board, the 41.25-MHz aural IF is created by mixing the modulated 4.5-MHz aural intercarrier signal, produced by the aural IF synthesizer board or from the composite 4.5-MHz filter board, with the 45.75-MHz CW signal produced by the 45.75-MHz IF carrier oven oscillator board. The modulated 4.5-MHz aural intercarrier signal enters the board at J14 or J28 and is connected to IF relay K1. Jumper W3 on J7 determines whether the 4.5-MHz used by the board is internally generated or from an external source. With jumper W3 connected between pins 2 and 3, the 4.5 MHz from the aural IF synthesizer board or from the 4.5-MHz composite input is connected to mixer Z2. If an external 4.5-MHz signal is used, it enters the board at J12 and is fed through gain pot R88 to amplifier IC U13A. The amplified 4.5 MHz is then connected to J7 and, if jumper W3 is between pins 1 and 2, the 4.5-MHz signal from the external source is connected to the mixer. Mixer Z2 heterodynes the aural-modulated, 4.5-MHz signal with the 45.75-MHz CW signal to produce the modulated 41.25-MHz aural IF signal.

The output of the mixer is fed to a bandpass filter that is tuned to pass only the modulated 41.25-MHz aural IF signal that is fed to jack J16, the 41.25-MHz loop-through out jack of the board.

For normal operation, the 41.25-MHz signal is jumpered by a coaxial cable from J16 to J17 on the board. If the (optional) aural IF loop-through kit is purchased, the 41.25-MHz signal is connected to the rear of the tray, to which any processing trays can be connected, and then back to jack J17 on the board. The modulated 41.25-MHz aural IF signal from J17 is connected through amplifier ICs U15 and U16. The amplified output is connected to the attenuator-matching circuit that is adjusted by R85. R85 increases or decreases the level of the 41.25 MHz that sets the A/V ratio for the diplexer circuit. The diplexer circuit takes the modulated 45.75-MHz visual IF and the modulated aural IF and combines them to produce the 45.75-MHz + 41.25-MHz IF output. The combined 45.75-MHz + 41.25-MHz IF signal is amplified by U12 and connected to combined IF output jack J20 on the board. A sample of the combined IF output is provided at J21 on the board. If a NICAM input is used, it connects to J36 on the board. The level of the NICAM signal is set by R109 before it is fed to the diplexer circuit consisting of L28, L29, and R115. This circuit combines the NICAM signal with the 45.75-MHz visual IF + 41.25-MHz aural IF signal.

3.1.2.6 Operational Voltages

The +12 VDC needed to operate the transmitter control board enters the board at J23, pin 3, and is filtered by L26, L33, and C73 before it is fed to the rest of the board.

The -12 VDC needed to operate the board enters the board at J23, pin 5, and is filtered by L27 and C74 before being fed to the rest of the board.

3.1.3 (A6) Delay Equalizer Board (1227-1204; Appendix D)

The delay equalizer board provides a delay to the video signal, correction to

the frequency response, and amplification of the video signal.

The video signal enters the board at J1-2 and is connected to a pi-type, low-pass filter consisting of C16, L7, and C17. This filter eliminates any unwanted higher frequencies from entering the board. The output of the filter is connected to amplifier stage U1; the gain is controlled by R29. The video output of the amplifier stage is wired to the first of four delay-equalizing circuits that shape the video signal to the FCC specification for delay equalization or to the desired shape needed for the system. The board has been factory-adjusted to this FCC specification and should not be readjusted without the proper equipment.

Resistors R7, R12, R17, and R22 adjust the sharpness of the response curve while inductors L1, L2, L3, and L4 adjust the position of the curve. With a delay equalizer test generator signal or a sine x/x video test pattern input, the resistors and inductors can be adjusted, while monitoring a Tektronix VM700 test measurement set, until the desired FCC delay equalization curve or system curve is attained. The delay-equalized video signal is connected to J1-4, the video output of the board. A sample of the delayed video signal is connected to J2 on the board and can be used for testing purposes.

The ±12 VDC needed to operate the board enters the board at J1. The +12 VDC connects to J1-9, which is filtered by L5 and C11 before it is directed to the rest of the board. The -12 VDC connects to J1-6, which is filtered by L6 and C12 before it is directed to the rest of the board.

3.1.4 (A7) IF Carrier Oven Oscillator Board (1191-1404; Appendix D)

The IF carrier oven oscillator board generates the visual IF CW signal at 45.75 MHz for NTSC system "M" usage. The +12 VDC is applied through jack J10 to crystal oven HR1, which is preset to operate at 60° C. The oven encloses crystal Y1 and stabilizes the crystal temperature. The crystal is the principal device that determines the operating frequency and is the most sensitive in terms of temperature stability.

Crystal Y1 operates in an oscillator circuit consisting of transistor Q1 and its associated components. Feedback is provided through a capacitor-voltage divider, consisting of C5 and C6, that operates the crystal in a common-base amplifier configuration using Q1. The operating frequency of the oscillator can be adjusted by variable capacitor C17. The oscillator circuit around Q1 has a separate regulated voltage, 6.8 VDC, which is produced by a combination of dropping resistor R4 and zener diode VR1. The output of the oscillator at the collector of Q1 is capacitively coupled through C8 to the base of Q2. The small value of C8, 10 pF, keeps the oscillator from being loaded down by Q2.

Q2 is operated as a common-emitter amplifier stage whose bias is provided through R8 from the +12 VDC line. The output of Q2, at its collector, is split between two emitter-follower transistor stages, Q3 and Q4. The output of Q3 is taken from its emitter through R11 to establish an approximate 50-ohm source impedance through C11 to J3, the main output jack. This 45.75-MHz signal is at about the +5 dBm power level. In most systems, this output is either directed to a visual modulator board or to some splitting and amplifying arrangement that distributes the visual IF carrier for other needs. The second output from the collector of Q2 is fed to the base of Q4, the emitter follower transistor.

Q4 drives two different output circuits. One output is directed through voltage dividers R14 and R15 to jack J2 and is meant to be fed to a frequency counter. While monitoring J2 the oscillator can be set exactly on the operating frequency

(45.75 MHz) by adjusting C17. The output at J2 is at a power level of approximately -2 dBm, which is sufficient to drive most frequency counters. The other output of Q4 connects to prescaler chip U1, which divides the signal by 15. The output of U1 is applied to U2, a programmable divider IC. U2 is programmed through pins 11 to 20 to divide by 61. This results in a 50-kHz signal at pin 9 that is available as an output at J1. The output of 50 kHz is generally used in systems where the visual IF carrier oven oscillator is used as the reference for a PLL circuit; an example of this is when the PLL circuit uses the aural IF synthesizer board and the aural VCO. The 50-kHz CMOS output at jack J1 is not capable of achieving enough drive level for a long coaxial cable length. As a result, when a long coaxial cable is needed, the output at jack J5 is utilized. The push-pull transistor stage Q5 and Q6, along with emitter resistor R18, provide a large-load output capability at J5.

The stages U1, U2, Q5, and Q6 are powered by +5.1 VDC, which is obtained by using the +12 VDC line voltage, and voltage-dropping resistor R16 and zener diode VR2.

The +12 VDC power is applied to the board through jack J4, pin 3, and is isolated from the RF signals which may occur in the +12 VDC line through the use of RF choke L2 and filter capacitor C10.

3.1.5 (A8) ALC Board, NTSC (1265-1305; Appendix D)

The automatic level control (ALC) board provides the ALC and amplitude linearity correction of the IF signal. The ALC adjusts the level of the IF signal through the board to control the output power of the transmitter.

The visual + aural IF input (0 dBm) signal from the modulator enters the board at modulator IF input jack J32. If the (optional) receiver tray is present, the visual + aural IF input (0 dBm) from the receiver tray connects to receiver IF input jack J1. The modulator IF input connects to relay K3 and the receiver IF input connects to relay K4. The two relays are controlled by the Modulator Select command that is connected to J30 on the board. Modulator select enable/disable jumper W11 on J29 controls whether the Modulator Select command at J30 controls the operation of the relays or not. With jumper W11 on J29, pins 1 and 2, the Modulator Select command at J30 controls the operation of the relays; with jumper W11 on J29, pins 2 and 3, the modulator is selected all of the time.

3.1.5.1 Modulator Selected

With the modulator selected, J11-10 and J11-28 on the rear of the UHF exciter tray are connected together; this makes J30 low and causes relays K3 and K4 to de-energize. When K4 is de-energized, it connects the receiver IF input at J1, if present, to 50 watts. When K3 is de-energized, it connects the modulator IF input at J32 to the rest of the board; Modulator Enable LED DS5 will be illuminated.

3.1.5.2 Receiver Selected

With the receiver selected, which is J11-10 and J11-28 on the rear of the UHF exciter tray (connected to J30 on the board) not connected together, relays K3 and K4 are energized. When K4 is energized, it connects the receiver IF input at J1, if present, to the rest of the board. When K3 is energized, it connects to the modulator IF input at J32 to 50 watts; Modulator Enable LED DS5 will be illuminated.

3.1.5.3 Main IF Signal Path (Part 1 of 3)

The selected visual + aural IF input (0 dBm) signal is split, with one half of the signal entering a bandpass filter that consists of L3, L4, C4, L5, and L6. This

bandpass filter can be tuned with C4 and is substantially broader than the IF signal bandwidth. It is used to slightly steer the frequency response of the IF to make up for any small discrepancies in the frequency response in the stages that precede this point. The filter also serves the additional function of rejecting unwanted frequencies that may occur if the tray cover is off and the tray is in a high RF environment (if this is the case, the transmitter will have to be serviced with the tray cover off in spite of the presence of other RF signals). The filtered IF signal is fed through a pi-type matching pad consisting of R2, R3, and R4 to the pin-diode attenuator circuit consisting of CR1, CR2, and CR3.

3.1.5.4 Input Level Detector Circuit

The other part of the split IF input is connected through L2 and C44 to U7; U7 is an IC amplifier that is the input to the input level detector circuit. The amplified IF is fed to T4; T4 is a step-up transformer that feeds diode detector CR14. The positive-going detected signal is then low-pass filtered by C49, L18, and C50. This allows only the video with positive sync to be applied through emitter follower Q1. The signal is then connected to detector CR15 to produce a peak-sync voltage that is applied to op-amp U9A. There is a test point at TP3 that provides a voltage reference check of the input level. The detector serves the dual function of providing a reference that determines the input IF signal level to the board and also serves as an input threshold detector.

The input threshold detector prevents the automatic level control from reducing the attenuation of the pin-diode attenuator to minimum (the maximum signal) if the IF input to the board is removed. The ALC, video loss cutback, and the threshold detector circuits will only operate when jumper W3 on jack J6 is in the Auto position, between pins 1 and 2. Without the threshold detector, and with the pin-diode attenuator at minimum, when the signal is restored it will overdrive the stages following this board.

As part of the threshold detector operation, the minimum IF input level at TP3 is fed through detector CR15 to op-amp IC U9A, pin 2. The reference voltage for the op-amp is determined by the voltage divider that consists of R50 and R51 (off the +12 VDC line). When the detected-input signal level at U9A, pin 2, falls below this reference threshold (approximately 10 dB below the normal input level), the output of U9A at pin 1 goes to the +12 VDC rail. This high is connected to the base of Q2. At this point, Q2 is forward biased and creates a current path from the -12 VDC line and through red LED DS1, the input level fault indicator, which becomes lit, resistor R54, and transistor Q2 to +12 VDC. The high from U9A also connects through diode CR16 to U9B, pin 5, whose output at pin 7 goes high. The high connects through range adjust pot R74 to J20, which connects to the front panel-mounted power adjust pot. This high connects to U10A, pin 2, and causes it to go low at output U10A, pin 1. The low is applied through jumper W3 on J6 to the pin-diode attenuator circuit that cuts back the IF level and, therefore, the output power level, to 0. When the input signal level increases above the threshold level, the output power will raise, as the input level increases, until normal output power is reached.

The video input level at TP3 is also fed to a sync-separator circuit, consisting of IC U8, CR17, Q3, and associated components, and then to a comparator circuit made up of U9C and U9D. The reference voltage for the comparators is determined by a voltage divider consisting of R129, R64, R65, R66, and R130 (off the -12 VDC line). When the input signal level to the detector at TP3 falls below this reference threshold, which acts as a loss of sync detector circuit, the output of U9C and U9D goes towards the -12 VDC rail and is split, with one part biasing on transistor Q5. A

current path is then established from the +12 VDC line through Q5, the resistors R69, R137, and the red LED DS3 (video loss indicator), which becomes lit. When Q5 is on, it applies a high to the gates of Q6 and Q7. This causes them to conduct and apply video loss fault pull-down outputs to J18, pins 5 and 2.

The other low output of U9C and U9D is connected through CR20 to jack J5. Jumper W2 on J5, in the Cutback Enable position (between pins 2 and 3), connects the low to the base of the forward-biased Q4. If jumper W2 is in the Disable position, between pins 1 and 2, the auto cutback will not operate. With Q4 biased on, a level determined by the setting of cutback level pot R71, which is set at the factory to cut back the output to approximately 25%, is applied to U9B, pin 5. The output of U9B at pin 7 goes low and is applied through the power adjust pot to U10A, pin 2, whose output goes low. This low is applied to the pin-diode attenuator to cut back the level of the output to approximately 25%.

3.1.5.5 Pin-Diode Attenuator Circuit

The input IF signal is fed to a pin-diode attenuator circuit that consists of CR1 to CR3. Each of the pin diodes contain a wide intrinsic region; this makes the diodes function as voltage-variable resistors at this intermediate frequency. The value of the resistance is controlled by the DC bias supplied to the diode. The pin diodes are configured in a pi-type attenuator configuration where CR1 is the first shunt element, CR3 is the series element, and CR2 is the second shunt element. The control voltage, which can be measured at TP1, originates either from the ALC circuit when jumper W3 on J6 is in the ALC Auto position, between pins 1 and 2, or from pot R87 when the jumper is in the Manual Gain position.

On the pin-diode attenuator circuit, a current path exists from J6 through R6 and then through the diodes of the pin attenuator. Changing the amount of current through the diodes by forward biasing them changes the IF output level of the board. There are two extremes of attenuation ranges for the pin-diode attenuators. In the minimum attenuation case, the voltage, measured at TP1, approaches the +12 VDC line. There is a current path created through R6, through series diode CR3, and finally through R9 to ground. This path forward biases CR3 and causes it to act as a relatively low-value resistor. In addition, the larger current flow increases the voltage drop across R9 that tends to turn off diodes CR1 and CR2 and causes them to act as high-value resistors. In this case, the shunt elements act as a high resistance and the series element acts as a low resistance to represent the minimum loss condition of the attenuator (maximum signal output). The other extreme case occurs as the voltage at TP1 is reduced and goes towards ground or even slightly negative. This tends to turn off (reverse bias) diode CR3, the series element, causing it to act as a high-value resistor. An existing fixed current path from the +12 VDC line, and through R5, CR1, CR2, and R9, biases series element CR3 off and shunt elements, diodes CR1 and CR2 on, causing them to act as relatively low-value resistors. This represents the maximum attenuation case of the pin attenuator (minimum signal output). By controlling the value of the voltage applied to the pin diodes, the IF signal level is maintained at the set level.

3.1.5.6 Main IF Signal Path (Part 2 of 3)

When the IF signal passes out of the pin-diode attenuator through C11, it is applied to modular amplifier U1. This device includes within it the biasing and impedance matching circuits that makes it operate as a wide-band IF amplifier. The output of U1 is available, as a sample of the pre-correction IF for troubleshooting purposes and system setup, at jack J2. The IF signal is then connected to the linearity corrector portion of the board.

3.1.5.7 Linearity Corrector Circuits

The linearity corrector circuits use three stages of correction to correct for any amplitude non-linearities of the IF signal. Each stage has a variable threshold control adjustment, R34, R37, or R40, and a variable magnitude control adjustment, R13, R18, or R23. The threshold control determines the point at which the gain is changed and the magnitude control determines the amount of gain change that occurs once the breakpoint is reached. Two reference voltages are needed for the operation of the corrector circuits. Zener diode VR1, with R33 and R135, provides a +6.8 VDC reference and the diodes CR11 and CR12 provide a .9 VDC reference that temperature compensates for the two diodes in each corrector stage.

For the linearity correctors to operate, an IF signal is applied to transformer T1, which doubles the voltage swing by means of a 1:4 impedance transformation. Resistors R14, R15, and R16 form an L-pad that lowers the level of the signal. The amount that the level is lowered is adjusted by adding more or less resistance, using R13, in parallel with the L-pad resistors. R13 is only in parallel when the signal reaches a level large enough to turn on the diodes CR4 and CR5. When the diodes turn on, current flows through R13, putting it in parallel with the L-pad.

When R13 is put in parallel with the resistors, the attenuation through the L-pad is lowered, causing signal stretch (the amount determined by the adjustment of R13). The signal is next applied to amplifier U2 to compensate for the loss through the L-pad. The breakpoint, or cut-in point, for the first corrector is set by controlling where CR4 and CR5 turn on. This is accomplished by adjusting cut-in resistor R34; R34 forms a voltage-divider network from +6.8 VDC to ground. The voltage at the wiper arm of R34 is buffered by unity-gain amplifier U5D. This reference voltage is then applied to R35, R36, and C39 through L12 to the CR4 diode. C39 keeps the reference from sagging during the vertical interval. The .9 VDC reference created by CR11 and CR12 is applied to unity-gain amplifier U5B. The reference voltage is then connected to diode CR5 through choke L11. The two chokes L11 and L12 form a high impedance for RF that serves to isolate the op-amp ICs from the IF.

After the signal is amplified by U2, it is applied to the second corrector stage through T2. This corrector and the third corrector operate in the same fashion as the first. All three corrector stages are independent and do not interact with each other.

The correctors can be disabled by moving jumper W1 on J4 to the Disable position, between pins 2 and 3; this moves all of the breakpoints past the tip of sync so that they will have no affect. The IF signal exits the board at IF output jack J3 after passing through the three corrector stages and is normally connected to an external IF phase corrector board.

3.1.5.8 Main IF Signal Path (Part 3 of 3)

After the IF signal passes through the external IF phase corrector board, it returns to the ALC board at IF input jack J7. The IF then passes through a bandpass filter consisting of L20, C97, C62, L21, C63, L22, L23, C64, and C99. This bandpass filter is identical in both form and function to the one described in Section 3.3 of this chapter. In this case, the filter is intended to make up for small errors in frequency response that are incurred by the signal while being processed through the linearity and incidental phase correction circuits.

Following the bandpass filter, the signal is split using L24, L25, and R89. The signal passing through L24 is the main IF path through the board. A sample of the corrected IF signal is split off and connected to J10, the IF sample jack.

The IF connects to jacks J27 and J28. These jacks control whether a 6-dB pad is included in the circuit by the positioning of jumpers W9 and W10. The 6-dB pad-in is when jumpers W9 and W10 are connected between pins 2 and 3 on J27 and J28. The 6-dB pad-out is when jumpers W9 and W10 are connected between pins 1 and 2 on J27 and J28. Normally, the pad is out. The IF signal is then applied to a two-stage, frequency-response corrector circuit that is adjusted as needed.

Variable resistors R103 and R106 adjust the depth and gain of the notches and variable caps C71 and C72 adjust the frequency position of the notches. The IF signal is amplified by U13 and U14 before it is connected to J12, the IF output jack of the board. R99 is an output level adjustment that is set to provide approximately 0 dBm of IF output at J12. A sample of the IF is fed to J11 to provide an IF sample point that can be monitored without breaking the signal path and gives an indication of the IF signal after the linearity and the frequency-response correction takes place.

3.1.5.9 ALC Circuit

The other path of the corrected IF signal is used in the ALC circuit. The IF is wired out of the splitter through L25 and connects to op-amp U12. The output of U12 is wired to jacks J8 and J9 on which jumpers W4 and W8 control the normal or encoded operation of the ALC circuitry. For normal operation, jumper W4 on J8 is between pins 1 and 2 and jumper W8 on J9 is between pins 1 and 2. The IF signal is applied to transformer T5; T5 doubles the voltage swing by means of a 1:4 impedance transformation before it is connected to the ALC detector circuit on the board and amplified by U10B.

For normal operation, jumper W7 on J26 is between pins 1 and 2 and jumper W5 on J21 is between pins 1 and 2. The detected ALC voltage is wired to U10A, pin 2, where it is summed with the front panel power control setting. The output power adjustment for the transmitter is achieved, if the (optional) remote power raise/lower kit (1227-1039) is purchased, by R75, a motor-driven pot controlled by switch S1 on the board, or screwdriver adjust pot R1 on the front panel of the UHF exciter tray. An external power raise/lower switch can be used by connecting it to jack J10, at J10-11 power raise, J10-13 power raise/lower return, and J10-12 power lower, on the rear of the UHF exciter tray. S1, or the remote switch, controls relays K1 and K2, which control motor M1 that moves variable resistor R75. If the (optional) remote power raise/lower kit is not purchased, the ALC voltage is controlled only by screwdriver adjust pot R1 on the front panel of the UHF exciter tray. The ALC voltage is set for .8 VDC at TP4 with a 0 dBm output at J12 of the board. A sample of the ALC at J19, pin 2, is wired to the transmitter control board where it is used on the front panel meter and in the AGC circuits.

This ALC voltage, and the DC level corresponding to the IF level after signal correction, are fed to U10A, pin 2, whose output at pin 1 connects to the ALC pin-diode attenuator circuit. If there is a loss of gain somewhere in an IF circuit, the output power of the transmitter will drop. The ALC circuit senses this drop at U10A and automatically lowers the loss of the pin-diode attenuator circuit to compensate by increasing the gain.

The ALC action starts with the ALC detector level that is monitored at TP4. The detector output at TP4 is nominally +.8 VDC and is applied through resistor R77 to a summing point at op-amp U10A, pin 2. The current available from the ALC detector is offset, or complemented, by current taken away from the summing junction. In normal operation, U10A, pin 2, is at 0 VDC when the loop is satisfied. If the recovered or peak-detected IF signal at IF input jack J7 of this board should drop in level,

which normally means that the output power is decreasing, the null condition would no longer occur at U10A, pin 2. When the level drops, the output of U10A, pin 1, will go more positive. If jumper W3 on J6 is in the Automatic position, it will cause the ALC pin-diode attenuators CR1, CR2, and CR3 to have less attenuation and increase the IF level; this will act to compensate for the decrease in level. If the ALC cannot increase the input level enough to satisfy the ALC loop, due to there not being enough range, an ALC fault will occur. The fault is generated because U10D, pin 12, increases above the trip point set by R84 and R83 until it conducts. This makes U10D, pin 14, high and causes the red ALC Fault LED DS2 to light.

3.1.5.10 Scrambled Operation with Encoding

For encoded, scrambled operation, jumper W4 on J8 must be connected between pins 2 and 3, jumper W8 on J9 must be between pins 3 and 2, jumper W7 on J26 must be between pins 2 and 3, and jumper W5 on J21 must be between pins 2 and 3. The IF is connected through W4 on J8 to the sync regeneration circuits.

If this board is operated with scrambling, using suppressed sync, the ALC circuit operates differently than described above because there is no peak of sync present on the IF input. A timing pulse from the scrambling encoder connects to the board at J24. This timing pulse is converted to sync pulses by U17A and U17B, which control the operation of Q8. The sync amplitude is controlled by R149 and is then applied to U15A, where it is added to the detected IF signal to produce a peak of sync level. The output of U15A is peak detected by CR26 and fed to U15B. If necessary, intercarrier notch L39 can be placed in the circuit by placing W6 on J22. The intercarrier notch is adjusted to filter any aural and 4.5-MHz intercarrier frequencies. The peak of sync signal is fed through R162, the ALC calibration control, to amplifier U15C. The amplified peak of sync output is connected through J21, pins 2 and 3, to U10A, where it is used as the reference for the ALC circuit and the AGC reference to the transmitter control board. Voltage TP4 should be the same in either the normal or the encoded video mode. Monitor J9, pins 3 and 4, with a spectrum analyzer, check that the board is in the AGC mode, and tune C103 to notch-out the aural IF carrier.

3.1.5.11 Fault Command

The ALC board also has circuitry for an external mute fault input at J19, pin 6. This is a Mute command and, in most systems, it is involved in the protection of the circuits of high-gain output amplifier devices. The Mute command is intended to protect the amplifier devices against VSWR faults. In this case, the action should occur faster than just pulling the ALC reference down. Two different mechanisms are employed: one is a very fast-acting circuit to increase the attenuation of the pin-diode attenuator, CR3, CR1, and CR2, and the second is the reference voltage being pulled away from the ALC amplifier device. An external Mute is a pull-down applied to J19, pin 6, to provide a current path from the +12 VDC line through R78 and R139, the LED DS4 (Mute indicator), and the LED section of opto-isolator U11.

These actions turn on the transistor section of U11 that applies -12 VDC through CR21 to U10A, pin 3, and pulls down the reference voltage. This is a fairly slow action that is kept at this pace by the low-pass filter function of R81 and C61. When the transistor section of U11 is on, -12 VDC is also connected through CR22 to the pin-diode attenuator circuit. This establishes a very fast muting action, by reverse biasing CR3, in the event of an external VSWR fault.

3.1.5.12 ±12 VDC Needed to Operate the Board

The ±12 VDC connects to the board at J14. The +12 VDC connects to J14-3 and is filtered by L30, L41, and C80 before it is applied to the rest of the board. The -12 VDC connects to J14-5 and is filtered by L31 and C81 before it is applied to the rest of the board.

The +12 VDC also connects to U16, a 5-VDC regulator IC, that produces the +5 VDC needed to operate timing IC U17.

3.1.6 (A9) IF Phase Corrector Board (1227-1250; Appendix D)

The IF phase corrector board has adjustments that pre-correct for any IF phase modulation distortion that may occur in output amplifier devices such as Klystron power tubes and solid-state amplifiers. Two separate, adjustable IF paths are on the board: a quadrature IF path and an in-phase IF path. The quadrature IF is 90° out of phase and much larger in amplitude than the in-phase IF. When they are combined in Z1, it provides the required adjustable phase correction to the IF signal.

The IF input signal enters at J1 and is AC coupled to U1. U1 amplifies the IF before it is connected to Z1, a splitter that creates two equal IF outputs: IF output 1 is connected to J2 and IF output 2 is connected to J3. The IF output 1 at J2 is jumpered through coaxial cable W4 to jack J6, the quadrature input, on the board. The IF output 2 at J3 is jumpered through coaxial cable W5 to jack J7, the in-phase input, on the board.

3.1.6.1 Phase Corrector Circuit

The phase corrector circuit corrects for any amplitude nonlinearities of the IF signal. It is designed to work at IF and has three stages of correction. Each stage has a variable threshold and magnitude control. The threshold control determines the point at which the gain is changed and the magnitude control determines the gain change once the breakpoint is reached. The second stage has a jumper that determines the direction of correction, so that the gain can increased either above or below the threshold, and either black or white stretch can be achieved.

In the phase corrector circuit, the IF signal from J6 is applied to transformer T1; T1 doubles the voltage swing using a 1:4 impedance transformation. Resistors R8, R61, R9, and R48 form an L-pad that attenuates the signal. This attenuation is adjusted by adding R7, a variable resistor, in parallel with the L-pad. R7 is only in parallel when the signal reaches a level large enough to bias on CR1 and CR2 and allow current to flow through R7. When R7 is put in parallel with the L-pad, the attenuation through the L-pad is lowered, causing black stretch.

Two reference voltages are utilized in the corrector stages and both are derived from the +12 VDC line. Zener diode VR1, with R46 as a dropping resistor, provides +6.8 VDC from the +12 VDC line. Diodes CR11 and CR12 provide a .9 VDC reference to temperature compensate the corrector circuits from the effects of the two diodes in each corrector stage.

The threshold for the first corrector stage is set by controlling where CR1 and CR2 turn on. This is accomplished by adjusting R3 to form a voltage divider from +6.8 VDC to ground. The voltage at the wiper of R3 is buffered by U9C, a unity-gain amplifier, and applied to CR1. The .9 VDC reference is connected to U9D, a unity-gain amplifier, whose output is wired to CR2. These two references are connected to diodes CR1 and CR2 through chokes L2 and L3. The two chokes form a high impedance for RF to isolate the op-amps from the RF. The adjusted signal is next applied to amplifier U2 to compensate for the loss through the L-pad. U2 is powered through L4 and R10 from the +12 VDC line. After the signal is amplified by U2, it

is applied to the second corrector stage through T2 and then to a third corrector stage through T3. The other two corrector stages operate in the same manner as the first; they are independent and do not interact with each other.

When jumper W1 on J8 is connected from center to ground, R15 is put in series with ground. In this configuration, black stretch (white compression) is applied to the IF signal by controlling the attenuation through the path. When W1 is connected from the center pin to the end that connects to T2, R15 is put in parallel with the L-pad. In this configuration, black compression (white stretch) is applied to the IF signal by controlling the attenuation through the path.

The phase correctors can be bypassed by moving jumper W2 on J9 to the Disable position. This action will move all of the threshold points past sync tip so that they will have no effect. R68 can be adjusted and set for the correction range that is needed. TP2 is a test point that gives the operator a place to measure the level of the quadrature IF signal that is connected to pin 6 on combiner Z2.

3.1.6.2 Amplitude Corrector Circuit

The amplitude corrector circuit uses one stage of correction to correct for any amplitude nonlinearities of the IF signal. The stage has a variable threshold control, R31, and a variable magnitude control, R35. The threshold control determines the point at which the gain is changed and the magnitude control determines the amount of gain change once the breakpoint is reached.

Two reference voltages are needed for the operation of the corrector circuit. Zener diode VR1 with R46 provides +6.8 VDC and the diodes CR11 and CR12 provide a .9 VDC reference voltage to temperature compensate for the two diodes in the corrector stage. In the amplitude corrector circuit, the IF signal from J7 is applied to transformer T4 to double the voltage swing by means of a 1:4 impedance transformation. Resistors R36, R55, R56, and R37 form an L-pad that lowers the level of the signal. The amount that the level is lowered is adjusted by adding more, or less, resistance, using R35 in parallel with the L-pad resistors. R35 is only in parallel when the signal reaches a level large enough to turn on diodes CR8 and CR9. When the diodes turn on, current flows through R35 and puts it in parallel with the L-pad. When R35 is in parallel with the resistors, the attenuation through the L-pad is lowered, causing signal stretch (the amount of stretch determined by the adjustment of R35).

The signal is next applied to amplifier U5 to compensate for the loss in level through the L-pad. The breakpoint, or cut-in point, for the corrector stage is set by controlling where CR8 and CR9 turn on. This is achieved by adjusting cut-in resistor R31 to form a voltage divider from +6.8 VDC to ground. The voltage at the wiper arm of R31 is buffered by unity-gain amplifier U8B. This voltage is then applied to R34 through L11 to the CR9 diode. The .9 VDC reference created by CR11 and CR12 is applied to unity-gain amplifier U8A. C36 keeps the reference from sagging during the vertical interval. The reference voltage is then connected to diode CR8 through choke L12. The two chokes L11 and L12 form a high impedance for RF to isolate the op-amp ICs from the IF.

After the signal is amplified by U5, it is applied to a second stage through T5. The transformer doubles the voltage swing by means of a 1:4 impedance transformation. Resistors R39, R57, R58, and R40 form an L-pad that lowers the level of the signal. The signal is applied to amplifier U6 to compensate for the loss in level through the L-pad. After the signal is amplified by U6, it is applied to a third stage through T6. The transformer doubles the voltage swing by means of a

1:4 impedance transformation. Resistors R42, R59, R60, and R43 form an L-pad to lower the level of the signal. The signal is applied to amplifier U7 to compensate for the loss in level through the L-pad. TP1 is a test point that gives the operator a place to measure the level of the in-phase IF signal that is connected to mixer stage Z2. The amplitude corrector can be disabled by moving jumper W3 on J10 to the Disable position; this will move the breakpoint past sync tip and will have no effect on the signal.

3.1.6.3 Output Circuit

The phase-corrected signal from pin 1 on combiner Z2 exits the board at IF output jack J4 after passing through a matching network consisting of six resistors.

3.1.7 (A11) VHF Mixer/Amplifier Enclosure Assembly (1088067; Appendix C)

The VHF mixer/amplifier enclosure assembly is made up of the x4 multiplier board, the VHF filter/mixer board, and the high-band VHF filter/amplifier board.

3.1.7.1 (A1) x4 Multiplier Board (1174-1112; Appendix D)

The x4 multiplier board multiplies the frequency of an RF input signal by a factor of four. The board is made up of two identical x2 broadband frequency doublers.

The input signal (+5 dBm) at the fundamental frequency enters through SMA jack J1 and is fed through a 3-dB matching pad, consisting of R1, R2, and R3, to amplifier IC U1. The output of the amplifier stage is directed through a bandpass filter, consisting of L2 and C4, that is tuned to the fundamental frequency. The voltage measured at TP1 is typically +0.6 VDC. The first doubler stage consists of Z1 with bandpass filter L3 and C6 tuned to the second harmonic. The harmonic is amplified by U2 and fed through a bandpass filter, consisting of C10 and L5, also tuned to the second harmonic frequency. The voltage measured at TP2 is typically +1.2 VDC. The next doubler stage consists of Z2 with bandpass filter C12 and L6 tuned to the fourth harmonic of the fundamental frequency. The fourth harmonic is then amplified by U3 and fed to the SMA output jack of the board at J2. The typical LO signal output level is a nominal +15 dBm.

The +12 VDC for the board enters through jack J3-3 and is filtered by L7 and C16 before being distributed to the circuits on the board.

3.1.7.2 (A2) VHF Filter/Mixer Board (1150-1102; Appendix D)

The VHF filter/mixer board is made up of three separate circuits: a filter and amplifier circuit for the LO input, a mixer stage, and a filter and amplifier for the RF output of the mixer. The board is mounted inside of (A11) the VHF mixer/amplifier enclosure assembly (1088067), an aluminum enclosure that provides RFI protection. The filter/amplifier board (1064252) is also mounted inside the enclosure.

The LO input (+5 dBm) connects to the board at J3 and is fed to a filter circuit. The input to the filter consists of C11, C12, and L5, with C12 adjusted for the best input loading. C13 and C17 are adjusted for the best frequency response and C18 is adjusted for the best output loading of the LO signal. Capacitor C15 is adjusted for the best coupling. The filtered LO is amplified by U2 and connected to LO output jack J4. Typically, the output at jack J4 is jumpered by a coaxial jumper to jack J5 on the board. The LO at J5 connects to mixer Z1 at pin 1 (+14 dBm).

The IF input connects to the board at J7 and is fed to mixer Z1 at pin 3 (-3 dBm).

Mixer Z1 takes the LO input at pin 1 and the IF input at pin 3 to produce an RF output at pin 8. The RF output at pin 8 (-14 dBm) connects through a pi-type attenuator, made up of R3, R4, and R5, before it is connected to RF output jack J6. Normally, jack J6 is connected by a coaxial jumper to J1 on the board. J1 connects to the input of a filter circuit, consisting of C25, C1, C23, C2, and L1, with C2 adjusted for the best input loading. C3 and C6 are adjusted for the best center frequency, C4 is adjusted for the best coupling, and C7 is adjusted for the best output loading of the RF signal. The filtered RF is amplified by U1 and connected to the RF output jack for the board at J2 (-2 dBm).

The +12 VDC needed for the operation of the board is supplied by an external power supply in the tray. The +12 VDC enters the board at J8, pin 3, and is filtered and isolated from the rest of the tray by L7 and C22 before being applied to the board.

3.1.7.3 (A3) High-Band VHF Filter/ Amplifier Board (1064252; Appendix D)

The VHF high-band filter/amplifier board is made up of two separate circuits: a filter circuit and an amplifier with a gain control circuit.

The RF input connects to the board at J7 and is fed through a channel filter circuit. The input to the filter consists of C27, C28, and C29, with C29 adjusted for the best input loading. C23 and C26 are adjusted for center frequency, with C24 adjusted for the best coupling, and C20 is adjusted for the best output loading of the RF signal. The filtered RF is connected to RF output jack J6; J6 is usually jumpered to jack J1 on the board.

The filtered RF at J1 connects through a 7-dB pi-type attenuator, consisting of R1, R2, and R3, before it is wired to a pin-diode attenuator circuit. The pin-diode attenuator circuit is made up of CR1, CR2, and CR3 and is controlled by the bias current applied through R5. The diodes CR1, CR2, and CR3 are pin-type diodes with a broad intrinsic region sandwiched inside the diode. This broad intrinsic region causes the pin diodes to act as variable resistors instead of as detecting devices at the RF frequencies. The resistance values of the pin diodes are determined by the relative amount of forward bias that is applied to the diodes. Jumper W1 on J5 is set for manual gain or auto gain by its position on the jack. Between 1 and 2 is manual gain, which uses pot R9 to set the output level; between 2 and 3 is auto gain, which uses the external control voltage input to jack J4 as the level control (this arrangement is not used in this configuration).

The level-controlled RF is pre-amplified by U1 and connected to Q1, the output amplifier for the board. C17 is used to maximize the RF signal. The RF output is amplified by Q1 and applied to the RF output jack for the board at J2.

The output from Q1 is first fed through direction coupler Z1 before exiting the board at J2, the RF output. The RF sample derived from Z1 has two functions. The first function is to provide an RF sample at J8 on the board which is fed to the front panel of the exciter tray through a voltage divider consisting of R19 and R18. The second function is to provide a peak-detected voltage that is used by the exciter tray for metering purposes. The sample provided by Z1, pin 3, is first fed through a dB pad consisting of R20, R21, and R22. The voltage is stepped up by 1-to-4 transformer T1. The signal is then peak detected by C32 and C14 before being buffered and amplified by U2. The peak-detected voltage that is used for metering purposes is controlled by pot R28 on the board.

The +12 VDC needed for the operation of the board is supplied by an external power supply in the tray. The +12 VDC enters the board at J3, pin 3, and is filtered and isolated from the rest of the

tray by L5 and C19 before being applied to the entire board. The –12 VDC enters the board at J3, pin 5, and is filtered and isolated from the rest of the tray by L6 and C35 before being applied to the entire board.

3.1.8 (A17) Transmitter Control Board (1265-1311; Appendix D)

The transmitter control board provides information on system control functions and the operational LED indications; these can be viewed on the front panel of the transmitter. The main control functions are for the Operate/Standby and Auto/Manual selections. When the transmitter is switched to Operate, the board supplies the enables to any external amplifier trays. The board also performs the automatic switching of the transmitter to Standby upon the loss of the video input when the transmitter is in Auto.

The transmitter control board contains a VSWR cutback circuit. If the VSWR of the transmitter increases above 20%, the VSWR cutback circuit will become active and cut back the output level of the transmitter, as needed, to maintain a maximum of 20% VSWR. An interlock (low) must be present at J8-24 for the transmitter to be switched to Operate and, when the interlock is present, the green Interlock LED DS5 will be lit.

3.1.8.1 Operate/Standby Switch S1

K1 is a magnetic latching relay that controls the switching of the transmitter from Operate and Standby. When the Operate/Standby switch S1, on the front panel of the tray, is moved to Operate, one coil of relay K1 energizes and causes the contacts to close and apply a low to U4B-9. If the transmitter interlock is present, and there is no overtemperature fault, lows will also be applied to U4B-10, U4B-11, and U4B-12.

With all the low inputs to U4B, the output at U4B-13 will be low. The low biases off Q1 and this turns off the amber Standby LED DS1 on the front panel. In addition, this action applies a high to Q2 and turns on and lights the green Operate LED DS2 (also on the front panel). When Q2 is biased on, it connects a low to Q12 and biases it off; this allows the ALC to be applied to J1 and connect to any external amplifier trays. The low from U4B-13 is also applied to Q4 and Q24, which are biased off, and removes the disables from J1-4 and J18-1. The low from U4B-13 also connects to Q10, which is biased on, and connects a high to Q6, Q7, Q8, and Q9; these are biased on and apply -12 VDC enables to J8-2, J8-3, J8-4, and J8-5, which connect to any external amplifier trays. The high applied to Q2 is also connected to Q5 and Q26, which are biased on, and apply a low enable to J1-3, which connects to a remote operate indicator. The transmitter is now in the Operate mode.

When the Operate/Standby switch S1 is moved to Standby, the other coil of relay K1 energizes, causing the contacts to open and a high (+12 VDC) to be applied to U4B-9. The high at the input causes the output at U4B-13 to go high. The high biases on Q1 and applies a low to the amber Standby LED DS1, on the front panel, and turns on and applies a low to Q2. This causes Q2 to turn off and extinguishes the green Operate LED DS2. When Q12 is biased on, the output from U2C goes low and pulls the ALC voltages at J1 low; this lowers the gain of the external amplifier trays. The high from U4B-13 is applied to Q4 and Q24, which are biased on, and applies disables at J1-4 and J18-1. The high from U4B-13 connects to Q10, which is biased off. The Q10 bias off removes the high from Q6, Q7, Q8, and Q9, which are biased off, and removes the -12 VDC enables at J8-2, J8-3, J8-4, and J8-5, which connect to the external amplifier trays. The low applied to Q2 is also connected to Q5 and Q26, which are biased off, and removes the remote enable at J1-3. The transmitter is now in the Standby mode.

3.1.8.2 Automatic/Manual Switch S2

K2 is a magnetic latching relay that switches the operation of the transmitter to Automatic or Manual using Auto/ Manual switch S2 on the front panel of the tray.

When S2 is set to the Auto position, the operation of the transmitter is controlled by the fault circuits and will stay in Operate even if Operate/Standby switch S1 is moved to Standby. With S2 in Auto, a low is applied to one coil in the relay and this energizes and closes the contacts. The closed contacts apply a low to the green Automatic LED DS3; as a result, DS3 is illuminated. The low from the relay connects to U5A, pin 2; U5D, pin 13; Q21; and Q23. When Q21 and Q23 are biased off, this causes their outputs to go high. The high from Q21 connects to the amber Manual LED DS4, on the front panel, biasing it off, and to Q22, biasing it on. The drain of Q22 goes low and is applied to J8-7; this enables any remote auto indicator connected to J8-7. The low to Q23 biases it off and removes the enable to any remote manual indicator connected to J8-6.

When S2 is set to the Manual position, the operation of the transmitter is no longer controlled by the fault circuits; it is controlled by Operate/Standby switch S1. With S2 in Manual, a low is applied to the other coil in the relay and this energizes and opens the contacts. The open contacts remove the low from the green Automatic LED DS3 on the front panel and causes it to not light. The high connects to U5A, pin 2; U5D, pin 13; Q21; and Q23. Q21 and Q23 are biased on; this causes their outputs to go low. The low from Q21 connects to the amber Manual LED DS4 on the front panel, biasing it on, and to Q22, biasing it off. The drain of Q22 goes high and is applied to J8-7; this will disable any remote auto indicators connected to it J8-7. Q23 is biased on and applies a low enable to any remote manual indicator connected to J8-6.

3.1.8.3 Automatic Turning On and Off of the Transmitter Using the Presence of Video

The transmitter control board also allows the transmitter to be turned on and off by the presence of video at the transmitter when the transmitter is in Auto. When a video fault occurs due to the loss of video, J7-5 goes low. The low is applied through W1, on J10, to Q16, which is biased off, and to the red Video Loss Fault LED DS9, on the front panel, which will light. The drain of Q16 goes high and connects to U5B, pin 5, causing the output at pin 4 to go low. The low connects to Q18, which is biased off, and causes the drain of Q18 to go high. The high connects to U3D, pin 12, whose output at pin 14 goes high. The high connects to U5C, pins 8 and 9, causing its output at pin 10 to go low, and to U5A, pin 1, causing its output at pin 3 to go low.

With S2 set to Automatic, a low is applied to U5A, pin 2, and to U5D, pin 13. When U5A, pin 1, is high and U5A, pin 2, is low, it causes the output at pin 3 to go low. When U5D, pin 12, is low and U5D, pin 13, is low, it causes its output to go high. When U5A, pin 3, is low, it biases off Q20 and removes any pull down to the Operate switch. A high at U5D, pin 11, biases on Q19 and applies a low enable to the Standby switch that places the transmitter in the Standby mode.

When the video signal is returned, J7-5 goes high. The high is applied to Q16, which is biased on, and to the red Video Fault LED DS9, which is extinguished. The output of Q16 goes low and connects to U5B, pin 5. If there is no receiver ALC fault, U5B, pin 6, is also low; this causes the output at pin 4 to go high. The high connects to Q18, which is biased on, and causes the drain of Q18 to go low. The low connects to U3D, pin 12, whose output at pin 14 goes low. The low connects to U5C, pins 8 and 9, which causes its output at pin 10 to go high, and to U5A, pin 1. With Auto/Manual

switch S2 in Auto, a low is applied to U5A, pin 2, and to U5D, pin 13. When U5A, pins 1 and 2, is low, its output at pin 3 goes high. When pin 12 of U5D is high, the output of U5D at pin 11 goes low. When U5A, pin 3, is high, it biases on Q20 and applies a pull-down enable to the Operate switch. A low at U5D, pin 11, biases off Q19 and removes any pull down to the Standby switch. As a result of these actions, the transmitter is switched to Operate.

3.1.8.4 Faults

There are four possible faults, video loss fault, VSWR cutback fault, overtemperature fault, and ALC fault, which may occur in the transmitter and are applied to the transmitter control board. During normal operation, no faults are sent to the board. The receiver ALC fault circuit will only function if a receiver tray is part of the system. The overtemperature fault is only used with 2-kW transmitters and is controlled by the temperature of the reject load.

3.1.8.5 Video Loss Fault

If a video loss occurs while the transmitter is in Auto, the system will change to the Standby mode until the video is returned; at that point, it will immediately revert to Operate. A video loss fault applies a low from the ALC board to the video fault input at J7-5 on the board.

With jumper W1 in place on J10, the video fault is connected to LED DS9 and to Q16. The red Video Loss Fault LED DS9 on the front panel will light. Q16 is biased off and causes its drain to go high. The high is wired to U5B, pin 5, whose output at U5B, pin 4, goes low. The low is wired to Q18, which is biased off, and causes the drain to go high. The high is connected to U3D, pin 12, which causes its output at U3D, pin 14, to go high. The high connects to U5A, pin 1, and, if the transmitter is in Auto, pin 2 of U5A is low. When pin 1 is high and pin 2 is low, the output of U5A goes low and reverse biases Q20, shutting it off. The high at U5C, pins 8 and 9, causes its output at pin 10 to go low. This low is connected to U5D, pin 12, and, if the transmitter is in Auto, pin 13 of U5D is also low. The lows on pins 12 and 13 cause the output to go high and forward bias Q19. The drain of Q19 goes low and connects the coil in relay K1, causing it to switch to Standby.

When the video returns, the video loss fault is removed from the video fault input at J7-5. With jumper W1 in place on J10, the base of Q16 goes high. The red Video Loss Fault LED DS9 on the front panel will be extinguished. Q16 is biased on, which causes its drain to go low. The low is wired to U5B, pin 5; U5B, pin 6, will be low if no ALC fault occurs. The two lows at the inputs make the output at U5B, pin 4, go high. The high is wired to Q18, which is biased on, causing the drain to go low. The low is connected to U3D, pin 12, which causes its output at U3D, pin 14, to go low. The low connects to U5A, pin 1, and, if the transmitter is in Auto, pin 2 of U5A is also low. With both inputs low, the output of U5A at pin 3 goes high. The high forward biases Q20 and causes its drain to go low. The low connects to the operate coil on relay K1 that switches the transmitter to Operate. The low at U5C, pins 8 and 9, causes its output at pin 10 to go high. This high is connected to U5D, pin 12, and, if the transmitter is in Auto, pin 13 of U5D is low. The high on pin 12 causes the output of U5D to go low and reverse bias Q19. The drain of Q19 goes high and this removes the low from the standby coil in relay K1.

3.1.8.6 Overtemperature Fault

In the 1-kW transmitter, there is no connection to the overtemperature circuit on the transmitter control board. In the 2-kW transmitter, the thermal switch on the output dummy load connects to J8-1 on the board. In the 100-watt transmitter, the (A6) thermal switch on (A23) the 100-watt amplifier heatsink

assembly connects to J12 on the board. If the temperature of the thermal switch raises above 170° F, it closes and applies a low to J8-1 or to J12. The low connects to Q3, which is biased off, and to the red Overtemperature LED DS6, which is biased on. The drain of Q3 goes high and connects to pins 11 and 12 of U4B. The high at the input to U4B causes it to go high and switches the system to Standby; this removes the Operate Enable commands to any external amplifier trays.

3.1.8.7 VSWR Cutback Fault

The reflected power sample of the RF output of the transmitter is connected to J2, pin 9, of the transmitter control board. The sample connects to op-amp U1B, pin 5, which buffers the signal before it is split. One of the split-reflected samples connects to J1-5 on the board; J1-5 is wired to J10-5 on the rear of the tray for remote monitoring. Another split-reflected sample connects to position 3 on the front panel meter for the tray. The final split remote-reflected sample connects to U2B, pin 5.

If the reflected sample level increases above the level set by R22, the VSWR cutback pot, the output of U2B at pin 7, goes high. The high is connected to Q11 through CR11, which is biased on, making U2C, pin 10, low and causing U2C, pin 8, to go low. This low is split and fed out of the tray at J1-6, J1-7, J1-8, and J1-9. These are ALC outputs to the amplifier trays that cut back the output power of the amplifier trays. The low from U2C, pin 8, is also fed through coaxial jumper W2 on J13 and J14 to R73. R73 is a bias-adjust pot that sets the level of the pin attenuator bias available as an output at J16. The high at U2B, pin 7, is also fed to the base of Q14 and Q13, which are forward biased. This produces a low at the drains that connect to the front panel amber VSWR Cutback LED DS7, causing it to light and indicate that the tray is in cutback, and to output jack J8-37 for the connection to a remote VSWR cutback indicator.

3.1.8.8 Receiver ALC Fault

If a receiver tray is part of the system, a sample of the ALC voltage from this tray is connected to J8-11 on the transmitter control board. If the receiver is operating normally, the ALC level that is applied to U3C, pin 9, remains below the trip level set by R35; as a result, the output at pin 13 stays high. The high is applied to the red ALC Fault LED DS8, which is off. The high also connects to U3A, pin 2, and to Q15. Q15 is biased on and the drain goes low. The low connects to U5B, pin 6. In addition, U5B normally has a low that is connected to U5B, pin 5, and produces a high at output pin 4. The high is wired to Q18, which is biased on, and makes its drain low. The low connects to U3D, pin 12, which, because the level is below the preset, the output at U3D, pin 14, goes low. A low at this point indicates a no-fault condition. The high that is connected to U3A, pin 2, causes its output to go low. The low is connected to Q25, which is biased off. The low is removed from J8-12, which will not light any remote receiver fault indicator that is connected to it.

If the receiver malfunctions, the ALC level applied to U3C, pin 9, goes high. This is above the level set by R35 and causes the output at pin 13 to go low. The low is applied to the red ALC Fault LED DS8, which lights. The low also connects to U3A, pin 2, and to Q15. Q15 is biased off and the drain goes high. The high connects to U5B, pin 6, and produces a low at output pin 4. The low is wired to Q18, which is biased off, and this makes its drain go high. The high connects to U3D, pin 12 and, because the level is above the preset, the output at U3D, pin 14, goes high. A high at this point indicates a fault condition that switches the transmitter to Standby. The low connected to U3A, pin 2, causes its output to go high. The high is connected to Q25, which is biased on, and causes

the drain to go low. The low is connected to J8-12, which can light any remote receiver fault indicator that is connected to it.

3.1.8.9 Metering

The front panel meter connects to J3-1 (-) and J3-2 (+), the output of switch S3, on the transmitter control board. The front panel meter has seven metering positions which are controlled by S3: Audio, Video, % Aural Power, % Visual Power, % Reflected Power, % Exciter, and ALC. The video sample connects to the board at J5-4 and is connected through video calibration pot R20 to position 6 on front panel meter switch S3. The audio sample enters the board at J5-6 and is connected through audio calibration pot R19 to position 7 on front panel meter switch S3.

The reflected sample connects to the board at J2-9 and is connected through buffer amplifier U1B and 100Ω resistor R84 to position 3 on front panel meter switch S3. The visual sample connects to the board at J2-5 and is connected through buffer amplifier U1D and 100Ω resistor R86 to position 4 on front panel meter switch S3. The aural sample connects to the board at J2-7 and is connected through buffer amplifier U1C and 100-watt resistor R85 to position 5 on front panel meter switch S3. The exciter sample connects to the board at J2-3 and is connected through buffer amplifier U1A and 100Ω resistor R87 to position 2 on front panel meter switch S3. The ALC sample connects to the board at J6-1 and is connected through buffer amplifier U2C and ALC calibration pot R15 (which adjusts the output of U2A, pin 1) and through 100Ω resistor R18 to position 1 on front panel meter switch S3. Typical readings on the meter are:

- Video = 1 Vpk-pk at white
- % Reflected = < 5%
- % Visual power = 100%
- % Aural power = 100%
- % Exciter = The level on the meter needed to attain 100% output power from the transmitter

Refer to the test specifications sheet for the transmitter for the actual reading:

- ALC = .8 VDC
- Audio = ±25 kHz with a balanced audio input or ±75 kHz with a composite audio input

Samples are provided for the remote metering of the exciter at J1-10, the visual at J8-26, the aural at J8-27, and the reflected at J1-5.

U6 is a temperature-sensor IC that gives the operator the ability to measure the temperature inside the tray by measuring the voltage at TP1. The sensor is set up for +10 mV equals 1° F (for example, 750 mV equals 75° F).

3.1.8.10 Operational Voltages

The +12 VDC needed for the operation of the transmitter control board enters the board at jack J4, pin 3. C28, L1, and L3 are for the filtering and isolation of the +12 VDC before it is split and applied to the rest of the board. The -12 VDC needed for the operation of the board enters the board at jack J4, pin 5. C29 and L2 are for the filtering and isolation of the -12 VDC before it is split and applied to the rest of the board.

The +12 VDC is split when it is connected to the board. Four of the +12 VDC outputs are fed out of the board at J8-16, J8-17, J8-18, and J8-19 through diodes CR7, CR8, CR9, or CR10 and resistors R50, R51, R52, or R53 are fed to any external amplifier trays for use in their logic circuits. The resistors are for current limiting and the diodes are to prevent voltage feedback from the external amplifier trays.

3.1.9 (A19) Visual/Aural Metering Board (1265-1309; Appendix D)

The visual/aural metering board provides detected outputs of the visual, aural, and reflected output samples that are used for monitoring on the front panel meter. The board also provides adjustments for the calibration of the readings on the meter. These readings are attained from samples of the forward power and reflected power outputs of the tray.

A forward power sample, visual + aural, is applied to SMA jack J1 on the board. The input signal is split, with one path connected to forward power sample SMA jack J2 for monitoring purposes. The other path is connected through C1 to CR2, R4, R5, R6, C4, and CR1, which make up a detector circuit. The detected visual + aural signal is amplified by U6B and its output is split. One amplified output of U6B connects to the aural level circuit and the other output connects to the visual level circuit.

3.1.9.1 Aural Level Circuit

One of the detected visual + aural level outputs of U6B connects through C6 to the intercarrier filter circuit that consists of R13, R14, L1, C7, and C8; C8 and L1, the intercarrier filter, can be adjusted for a maximum aural reading. The filter notches out the video + aural and only leaves the 4.5-MHz difference frequency between the visual and aural, which is a good representation of the aural level. The 4.5-MHz signal is fed to buffer amplifier U6A. The output of U6A is detected by diode detector CR3 and U1A and then fed through aural calibration control R20 to amplifier U2D. The amplified output of U2D is split, with the main output connected through R21 to J6, pin 1, which supplies the aural level output to the front panel meter for monitoring. The other output of U2D is connected to aural null adjust R51 and offset null adjust R48, which are adjusted to set up the visual power calibration.

3.1.9.2 Visual Level Circuit

The other detected visual + aural level output from U6B is connected to U1C and, if there is no scrambling, connects directly to intercarrier notch L3, which is adjusted to filter out the aural and the 4.5-MHz intercarrier frequencies, leaving only a visual-with-sync output. The visual-with-sync output is fed to a peak-detector circuit consisting of CR5 and U2A. The signal is then fed through visual calibration control R28, which is adjusted for a 100% visual reading with no aural, to amplifier U2B. The amplified visual peak of sync output is connected to comparator U2C. The other input to U2C is the level set by aural null adjust R51, which is adjusted for 100% visual power after the aural is added and the peak power is adjusted back to the reference level. Inputs to U2C also come from offset null adjust R48, which is adjusted for 0% visual power with the transmitter in Standby. The adjusted output is amplified by U3D and connected to the other input of U2C. The output of U2C connects to J6, pins 2 and 3, which supply the peak of sync visual level output to the front panel meter for monitoring.

If this board is operated with scrambling, using suppressed sync, the visual level circuit operates differently than described above because there is no peak of sync present on the forward sample input. For the board to operate properly, a timing pulse from the scrambling encoder must connect to the board at J4. This timing pulse is converted to sync pulses by U4A and U4B, which control the operation of Q2. Intercarrier notch L2 is tuned to remove any visual + aural signal that may remain.

The sync amplitude is controlled by gate amplitude adjust R25 and then applied to the minus input of U1C. At this point, it is inserted into the visual + aural signal that is connected to the plus input of U1C, producing a peak of sync in the signal. The output of U1C is connected to

intercarrier notch L3, which is adjusted to filter out the aural and the 4.5-MHz intercarrier frequencies. The visual-with-sync output is fed to a peak-detector circuit, consisting of CR5 and U2A, and then fed through visual calibration control R28 to amplifier U2B. The amplified visual peak of sync output is connected to J6, pins 2 and 3, that supply the peak of sync visual level output to the front panel meter for monitoring. R32 moves the pulse to where the sync should be and R25 sets the visual metering calibration with no sync present.

3.1.9.3 Reflected Level Circuit

A reflected-power sample is applied to J3 of the visual/aural metering board and is detected by diode detector CR7 and U3B. The detected output is fed through reflected calibration pot R39, which can be adjusted to control the gain of U3C. The output of U3C connects to J6, pin 7, which supplies a reflected-power level output to the front panel meter.

3.1.9.4 Voltages for Circuit Operation

The ±12 VDC is applied to the board at J5. The +12 VDC is connected to J5, pin 3, and is isolated and filtered by L4 and C34 before it is connected to the rest of the board. The +12 VDC also connects to U5, a 5-VDC regulator that provides the voltage needed to operate U4. The -12 VDC is applied to J5, pin 1, and is isolated and filtered by L5 and C35 before it is connected to the rest of the board.

3.1.10 (A4-A14) Channel Oscillator Assembly, Dual Oven (1145-1202; Appendix D)

The channel oscillator assembly contains the channel oscillator board (1145-1201) that generates a stable frequency-reference signal of approximately 100 MHz. The channel oscillator assembly is an enclosure that provides temperature stability for the crystal oscillator. An SMA output at jack J1 and an RF sample at BNC connector jack J2 are also part of the assembly.

Adjustments can be made through access holes in the top cover of the assembly. These adjustments are set at the factory and should not be tampered with unless it is absolutely necessary and the proper, calibrated equipment is available. R1 is the temperature adjustment; C11 is the course-frequency adjustment; C9 is the fine-frequency adjustment; and C6, C18, L2, and L4 are adjusted for the maximum output of the frequency as measured at jack J1.

The +12 VDC for the assembly enters through FL1 and the circuit-ground connection is made at E1.

3.1.11 (A4-A13) EEPROM FSK Identifier Board (1265-1308; Appendix D)

The FSK identifier board, with EEPROM, generates a morse code identification call sign by frequency-shift keying the VCXO oscillator in the upconverter or by sending a bias voltage to the IF attenuator board to amplitude modulate the aural carrier. This gives the station a means of automatically repeating its identification call sign, at a given time interval, to meet FCC requirements.

The starting circuit is made up of U1B and U1D, which are connected as a flip-flop, with gate U1A used as the set flip-flop. U1A automatically starts the flip-flop each time U3 completes its timing cycle. At the start of a cycle, U1B enables clock U2. U2 applies the clock pulses that set the speed, which is adjusted by R2, for when the identification code is sent to 12-bit binary counter U4. R2, fully clockwise (CW), is the fastest pulse train and R2, fully counter-clockwise (CCW), is the slowest pulse train. U4 provides binary outputs that address EEPROM U5.

The scans in U4 will continue until field effect transistor (FET) Q1 is gated on.

The gate of Q1 is connected to pin 13 on U4, which is the maximum count used in the EEPROM, and will provide a reset pulse each time the binary counter goes high on pin 13. The reset pulse, when the drain of Q1 goes low, is applied to the flip-flop and the timer U3, which determines the length of time between the sending of the identification code. R14 is adjusted to set this time interval. R14, fully CW, is the longest interval between identification calls, approximately eight minutes. R14, fully CCW, is the shortest interval between the sending of the code (approximately 10 seconds).

U6B is an amplifier connected to the output of U5, which turns the LED DS1 on and off at the rate set by R2. This gives the operator a visual indication that the FSK identifier board is operating and at the rate at which it is operating.

The data output of U5, which is serial, is connected to U6A, whose output shifts low and high, and is applied to the VCXO board, which shifts the frequency according to the programming of U5. The deviation of the shift is adjusted by R4 and is typically set at 1 kHz. Once R4 is set, R9 is re-adjusted to -1.5 VDC at J3-2.

The +12 VDC from an external power supply enters the board at J1, pin 3. The voltage is fed through RF choke L1 and is filtered by C1 before being applied to the rest of the tray. The +12 VDC is also applied to U7, which is a voltage regulator that regulates its output at +5 VDC. The +5 VDC is fed to the ICs on the board. The -12 VDC from an external power supply enters the board at J1, pin 5. The voltage is fed through RF choke L2 and filtered by C2 before being applied to the rest of the tray.

3.1.12 (A4-A12) IF Attenuator Board (1150-1201; Appendix D)

The IF attenuator board is operated with the FSK identifier board to produce an amplitude-modulated aural IF signal for broadcasting the required FCC station identification call sign at the proper time intervals.

The board contains a pin-diode attenuation circuit that consists of CR1 and the two resistors R2 and R3. The bias output of the FSK identifier board is applied to J3 of the IF attenuator board. As the bias applied to J3 increases and decreases, the amplitude of the aural IF signal, which enters the board at J1 and exits the board at J2, will increase and decrease. This produces an amplitude-modulated IF signal at J2, the aural IF output jack of the board.

3.2 (A6 and A7) 600-Watt High-Band VHF Amplifier Trays (1219-1100; Appendix C)

The 600-watt high-band VHF amplifier tray (1219-1100) can be adjusted at the factory for use as either a visual, a visual + aural, or an aural RF amplifier tray. As a visual amplifier, the tray has approximately 55 dB of gain at the frequency of the VHF high-band channel and will take the typical +3 dBm input and amplify it to an output level of approximately +58 dBm, 100%=600 watts peak of sync. As an aural amplifier, the tray is calibrated for 400 watts equals 100% output. As a visual + aural amplifier, the tray is calibrated for 300 watts peak of sync visual plus –10 dB or –13 dB aural power (30 watts or 15 watts).

The tray is made up of the boards and assemblies listed in Table 3-1.

Table 3-1. 600-Watt Amplifier Tray Boards and Assemblies

MAJOR ASSEMBLY DESIGNATOR	BOARD / ASSEMBLY NAME	DRAWING NUMBER
A1-A1	Phase shifter board (mounted in [A1] an RF enclosure assembly)	1198-1602
A2-A1	Filter/amplifier board (mounted in [A2] an RF enclosure assembly)	1218-1104
A2-A2	High band driver board (mounted in [A2] an RF enclosure assembly)	1219-1103
A3-A1	Overdrive protection board (mounted in [A3] an RF enclosure assembly)	1198-1601
A3-A2	High band VHF amplifier board (mounted in [A3] an RF enclosure assembly)	1219-1114
A3-A3	4-way splitter board (mounted in [A3] an RF enclosure assembly)	1219-1101
A4-A1, A4-A2, A4-A3, and A4-A4	Four high band VHF amplifier boards (mounted in [A4] an RF enclosure assembly)	1218-1201
A5-A1	4-way combiner board	1219-1102
A13	AGC control board	1142-1601
A8	Current metering board	1198-1609
A10	+48 VDC switching power supply assembly	

The on-channel visual RF or aural RF input signal (+3 dBm) enters the rear of the tray at BNC jack J1 and is fed through J1 of the (A1) enclosure assembly to J1 of (A1-A1) the phase shifter board (1198-1602). The board provides a phase shifter adjustment of the RF signal that is needed to provide maximum output during the combining of multiple 600-watt amplifier trays in an amplifier array. Front panel-mounted phase shift potentiometer R2 connects to J3 on the board and controls the phase of the RF signal.

If the input signal level to the phase shifter board falls below a preset level, a high, which is an input fault, connects from J5 of the board to J14 on the AGC control board. When an input fault occurs, the AGC control board generates a fault output at J1, which is connected to J4 on the filter/amplifier board. The fault cuts back the RF signal level using the pin-diode attenuator circuit on the filter/amplifier board.

The phase-controlled output at J2 of the phase shifter board (+2 dBm) is directed to J7, the input jack of (A2-A1) the filter amplifier board (1218-1104) that is made up of two circuits. The first circuit is a channel filter that is adjusted for the desired channel frequency and bandwidth. The filtered output (+1 dBm) is connected to the second circuit; this circuit contains two amplifiers. The RF connects through a pin-diode circuit to amplifier IC U1. The amplitude of the RF signal through the pin-diode attenuator

circuit is controlled by the voltage applied to J4, the external control jack of the board. Jumper W1 on J5 should be between pins 2 and 3; these pins provide external control, through J4, of the gain of the board as well as the output level of the tray.

The front panel-mounted gain pot R3 connects to the AGC control board and is used to adjust the AGC pin-attenuator bias voltage that connects to J4 on the filter/amplifier board. The RF signal, after the pin-attenuator circuit, is amplified by the second amplifier stage Q1 to about +14 dBm; this signal is connected to the output of the board at J2. The RF output of the filter/amplifier board connects to J1 on (A2-A2) the high-band VHF driver board (1219-1103). The board contains an RF power FET that has a gain of 20 dB.

The RF output of the board at J2 (+34 dBm) connects to J2 of (A3) an RF enclosure that contains the overdrive protection board, the high-band amplifier board, and the 4-way splitter board. The signal is connected to J4 of (A3-A1) the overdrive protection board (1198-1601). The RF signal is through-connected directly to J5, the RF output jack of the board. A sample of the RF on the board is applied to a diode-detector circuit that consists of CR1 and U1A. The gain of amplifier U1D is controlled by detector gain pot R11, which is set to +.4 VDC as measured at TP1.

The set output of U1D is connected to comparator IC U1B. The trip point for the comparator is adjusted by R12, typically to 110% output power, sync only. When the signal reaches that level, the overdrive protection board will cut back the output power of the tray and the red Overdrive LED DS1 on the board and the red Overdrive LED DS1 mounted on the front panel will be illuminated. Typically, the output power level will bounce down and then up and continue bouncing until the output level is lowered to the normal operating level (100%). The red Overdrive LED DS1, the green Module LED DS3, and the Enable LED DS2 may blink on and off during the bouncing of the output level; this is a normal occurrence. The greater the output level is above 110%, the larger the bounce will be.

The RF output of the overdrive protection board at J5 connects to J1 on (A3-A2) the high-band amplifier board (1219-1114) that amplifies the RF before it is connected to J1 on (A3-A3) the 4-way splitter board (1219-1101). The splitter board takes the +34 dBm input and provides four +30 dBm outputs at J1, J2, J3, and J4 of the (A3) amplifier enclosure.

The four RF outputs connect to (A4) the final amplifier enclosure. This enclosure contains four (A4-A1, A4-A2, A4-A3, and A4-A4) high-band amplifier boards (1218-1201). The RF signals connect to J1 on each of the high-band amplifier boards. Each amplifier board provides approximately 20 dB of gain.

The RF signal inputs to the amplifier boards (+30 dBm) are amplified to +49.5 dBm outputs at J2. These outputs are connected to J1, J2, J3, and J4 on (A5-A1) a 4-way combiner board (1219-1102). The 4-way combiner takes the four +49.5 dB inputs and combines them to form the 300-watt RF output at J5 of the combiner that connects to J2, the RF output jack of the tray.

The 4-way combiner board provides a forward power sample at J9 and a reflected output power sample at J11. The forward output power sample connects to J4 on (A13) the AGC control board (1142-1601). The reflected output power sample connects to J5 on (A13) the AGC control board (1142-1601). The AGC control board contains two peak-detector networks that provide detected outputs that are used for front panel and remote meter indications of forward and reflected output power levels, the AGC detector voltage level, and the VSWR

cutback protection if the reflected power level increases above the preset level.

Two voltages, +48 VDC from the internal switching power supply and +12 VDC from the exciter control panel, are needed for the operation of the tray. The +12 VDC connects to J3-7 and J3-8 on the rear of the tray; these are wired to J8, pins 4 and 1, on (A13) the AGC control board. The +12 VDC is connected to U8, a +5 VDC regulator IC that supplies the +5 VDC needed for the operation of the front panel-mounted LEDs.

The (A10) +48 VDC switching power supply provides the +48 VDC to (A8) the current metering board (1198-1609). The current metering board distributes the voltages through fuses to the amplifier devices on the filter/amplifier, the high-band driver board, the high-band amplifier board, and the four final high-band amplifier boards. The fuses F1, F2, F3, and F4 are 10-amp fuses; F5 is a 5-amp fuse; and F6 and F7 are 1-amp fuses. There are two spare fuses, one 1 amp and one 10 amp, on the top, right-hand side of the tray. Fuse F1 protects (A4-A1) the high-band amplifier board; fuse F2 protects (A4-A2) the high-band amplifier board; fuse F3 protects (A4-A3) the high-band amplifier board; fuse F4 protects (A4-A4) the high-band amplifier board; fuse F5 protects (A3-A2) the high-band amplifier board; and fuse F6 protects (A2-A1) the filter/amplifier board. Fuse F7 supplies +48 VDC to J8, pin 2, on the AGC control board. The +48 VDC is connected to regulator IC U7 that takes the +48 VDC and provides a +12 VDC output. The +12 VDC is used for the operation of the AGC control board. The +12 VDC is also connected through the current metering board, jumpered from TB1-5 to TB1-6, to the phase shifter board, the filter/amplifier board, and the overdrive protection board.

The current metering board also supplies sample outputs of the operating currents of the amplifier devices in the tray to the front panel current meter. The meter in the (I_1) position reads the current for the (A4-A1) high-band amplifier board; the meter in the (I_2) position reads the current for (A4-A2) the high-band amplifier board; the meter in the (I_3) position reads the current for the (A4-A3) high-band amplifier board; and the meter in the (I_4) position reads the current for the (A4-A4) high-band amplifier board. To read the desired current, place switch S2 in the proper position, checking that S1 is in the Current position. These current readings can be used when setting up the idling currents, no RF drive applied, for the devices. (I_1, I_2, I_3, and I_4) are each set for 2 amps when the tray is a visual amplifier, or a visual + aural amplifier, and they are set for 1 amp when the tray is an aural amplifier.

230 VAC is applied through jack J4 to terminal block TB1 in the tray. When CB1, the 15-amp, front panel-mounted circuit breaker, is switched on, the 230 VAC is distributed from TB1 to (A11 and A12) two cooling fans, which will begin to operate, and to (A10) the switching power supply. There are two surge suppressors, VR1 and VR2, mounted on TB1 that provide protection from transients or surges on the input AC line. There are two other surge suppressors, VR3 and VR4, mounted at the input to the switching power supply from each AC line to ground, that provide protection from transients or surges on the AC line.

The switching power supply only operates when the power supply enable control line, jack J3, pins 9 and 10, on the rear of the tray, is shorted. The enable is generated by the control panel when the amplifier array is switched to Operate. The enable is applied to (A13) the AGC control board (1142-1601) which, if there is no thermal fault, connects the enable from J10, pins 6 and 7, to J1-6 and J1-8 on the switching power supply assembly. The green Enable LED DS2 on the front panel will light, indicating that an enable is present. If the amplifier array is in Standby, or if a

thermal fault occurs, the AGC control board will not enable the switching power supply. As a result, the +48 VDC will be removed from the amplifier modules and the front panel Enable and Module Status LEDs will not be lit.

The front panel meter (A9) uses the front panel Selector switch S1 to monitor the AGC Voltage, % Output Reflected Power, % Forward Power, and the Switching Power Supply Voltage (+48 VDC). The meter in the AGC position will read anywhere from .5 volts to 3 volts. The meter is calibrated in the Power Supply position using R86 on the AGC control board. The % Output Power is calibrated using R44 and the % Reflected Power is calibrated using R53 on the AGC control board. With S1 in the Current position, S2 can be switched to read the idling currents, no RF drive applied, of the high-band amplifier boards. Typical readings are an idling current of 2 amps visual, or visual + aural, or 1 amp aural in the amplifier assembly I_1, I_2, I_3, and I_4 positions.

The reflected power sample from the 4-way combiner board is fed back to the AGC control board at J5. On the board, the reflected sample is connected through the detector circuit to VSWR cutback circuit U13C. If the reflected power increases above 20%, the output power of the tray, as set by R60 (the VSWR cutback on the AGC control board), will be cut back to maintain a 20% reflected output level.

The red VSWR Cutback LED DS4 on the front panel will remain lit until the reflected level drops below 20%.

There are three thermal switches in the tray for overtemperature protection. Two of the thermal switches (A4-A5 and A4-A6) are mounted on the rear of (A4) the heatsink for the high-band amplifier boards and the third thermal switch (A5-A2) is mounted on the heatsink for (A5-A1) the 4-way combiner board. The thermal switches close when the heatsink on which they are mounted reach a temperature of 175° F. The closed thermal switch causes the AGC control board to remove the enable to the switching power supply. This eliminates the +48 VDC and lights the red Overtemperature LED DS5 on the front panel. The AGC control board will extinguish the Module Status LED DS3.

3.3 (A9) Bandpass Filter Assembly (1067297; Appendix C)

The RF input connects to the (A9) constant impedance bandpass filter assembly (1067318) at jack J1 of (A1) a splitter/combiner board (1092-1092). The splitter/combiner board divides the combined RF signal into two signals before feeding it to jack J1 of (A2 and A3) two 5-section bandpass filters with traps. These filters screen the 6 MHz-wide signal and attenuate the –4.5-MHz and +9-MHz out-of-band products. These signals connect to jacks J2 and J3 on (A4) the other splitter/combiner board (1092-1092), that recombines the two signals before sending them on to jack J1 of (A5) the directional coupler module (1092-1308). The directional coupler module provides forward and reflected samples to the exciter tray for metering purposes.