QC101100

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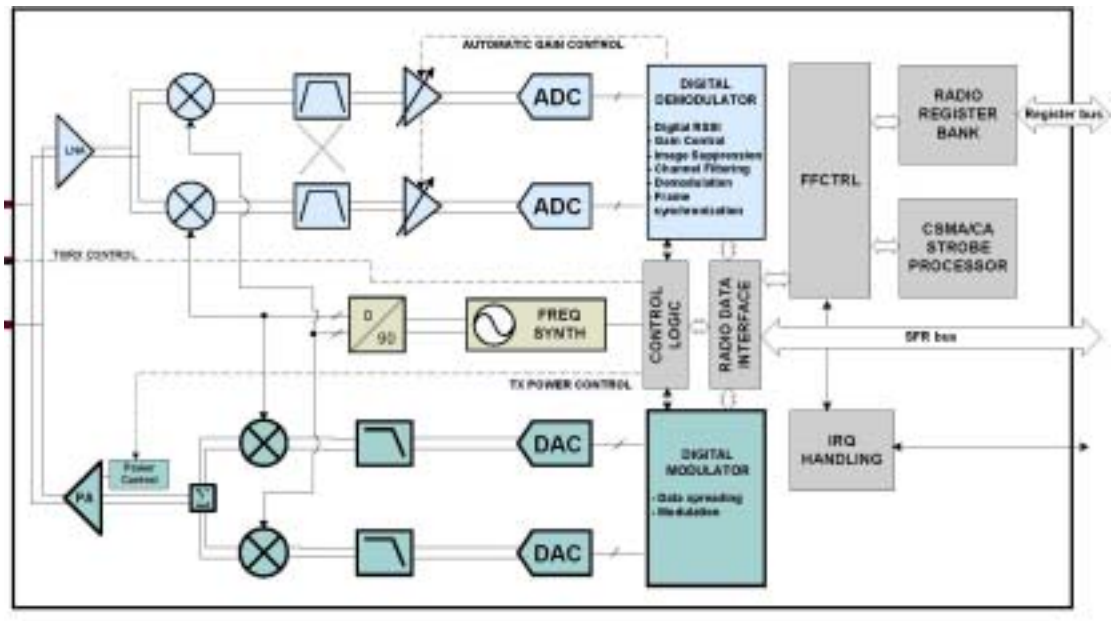
Architecture

The Zigbee Power Module **QC101100** provides the Zigbee routing services needed to form a full Zigbee Mesh Network. It also functions as a power switch, and can sense when a load is applied (teapot function). It has a battery backup providing at least 2 hours of standby power, to allow the Zigbee network to continue to operate during power outages.

The hardware architecture is shown in Figure 1.

The hardware is base on the CC2430, it is a true System-on-chip (SoC) solution specifically tailored for IEEE 802.15.4 and Zigbee application. The CC2430 combines the RF transceiver and industry-standard enhanced 8051 MCU, suit for systems where ultra low power consumption is required. The CC2430 monitors the status of low battery, temperature, current and buttons, and send these information to other Zigbee units via 2.4G RF.

Figure 2 : CC2430 Radio Module



A simplified block diagram of the IEEE 802.15.4 compliant radio inside CC2430 is shown in Figure 2. The radio core is based on the industry leading CC2420 RF transceiver.

CC2430 features a low-IF receiver. The received RF signal is amplified by the lownoise amplifier (LNA) and down-converted in quadrature (I and Q) to the intermediate frequency (IF). At IF (2 MHz), the complex I/Q signal is filtered and amplified, and then digitized by the ADCs. Automatic gain control, final channel filtering, despreading, symbol correlation and byte synchronization are performed digitally.

An interrupt indicates that a start of frame delimiter has been detected. CC2430 buffers the received data in a 128 byte receive FIFO. The user may read the FIFO through an SFR interface. It is recommended to use direct memory access (DMA) to move data between memory and the FIFO.

CRC is verified in hardware. RSSI and correlation values are appended to the frame. Clear channel assessment, CCA, is available through an interrupt in receive mode.

The CC2430 transmitter is based on direct up-conversion. The data is buffered in a 128 byte transmit FIFO (separate from the receive FIFO). The preamble and start of frame delimiter are generated in hardware. Each symbol (4 bits) is spread using the IEEE 802.15.4 spreading sequence to 32 chips and output to the digital-to-analog converters (DACs).

An analog low pass filter passes the signal to the quadrature (I and Q) up-conversion mixers. The RF signal is amplified in the power amplifier (PA) and fed to the antenna.

The internal T/R switch circuitry makes the antenna interface and matching easy. The RF connection is differential. A balun may be used for single-ended antennas. The biasing of the PA and LNA is done by connecting TXRX_SWITCH to RF_P and RF_N through an external DC path.

The frequency synthesizer includes a completely on-chip LC VCO and a 90 degrees phase splitter for generating the I and Q LO signals to the down-conversion mixers in receive mode and up-conversion mixers in transmit mode. The VCO operates in the frequency range 4800-4966 MHz, and the frequency is divided by two when split into I and Q signals.

The digital baseband includes support for frame handling, address recognition, data buffering, CSMA-CA strobe processor and MAC security