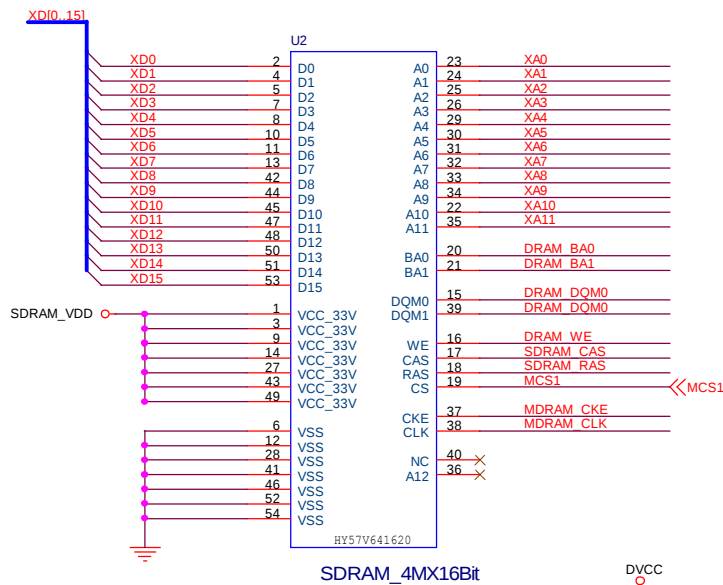
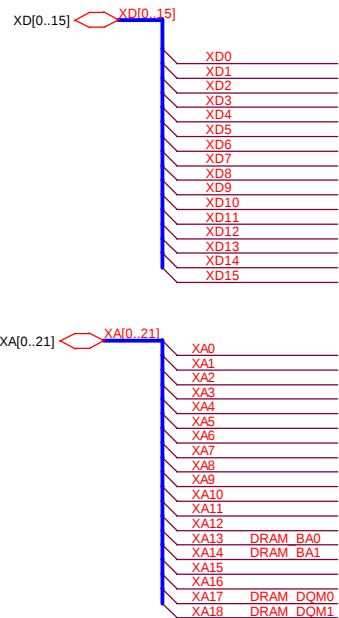
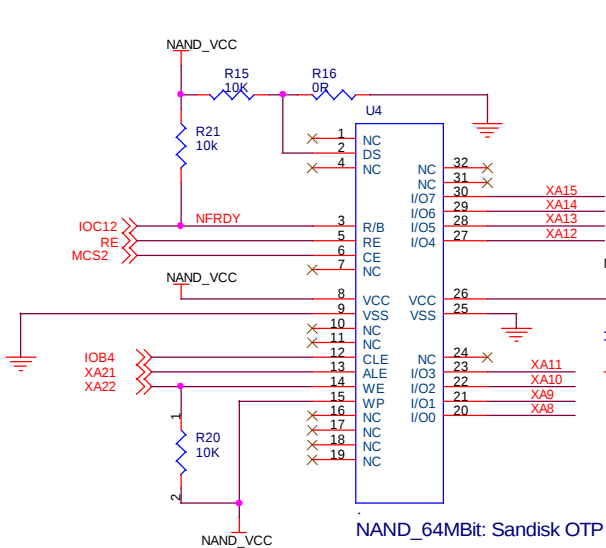
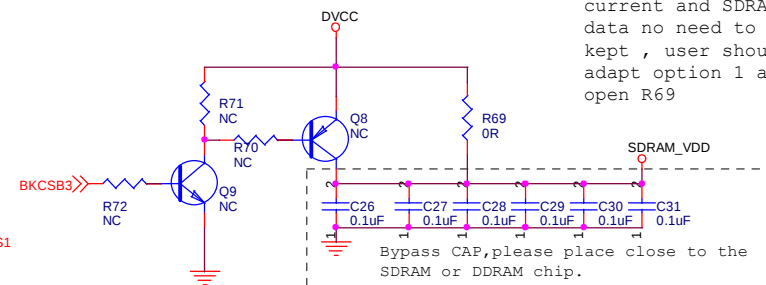
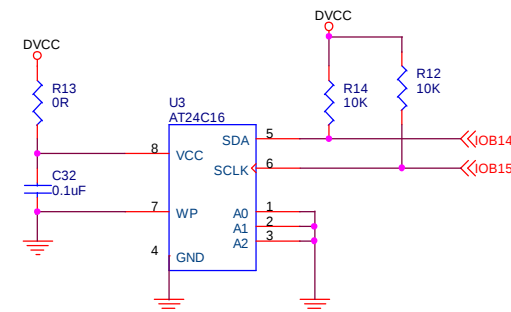
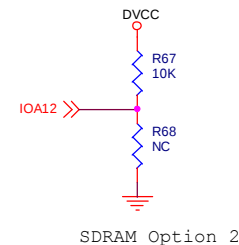
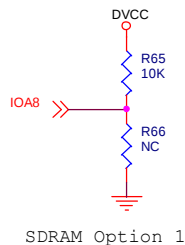


Option 2: if SDRAM should keep data, DVCC & SDRAM_DVCC should be wired by R69 (0-ohm)

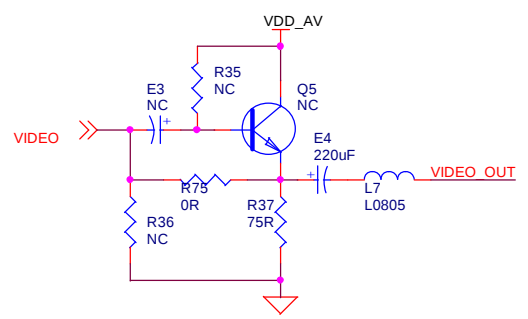
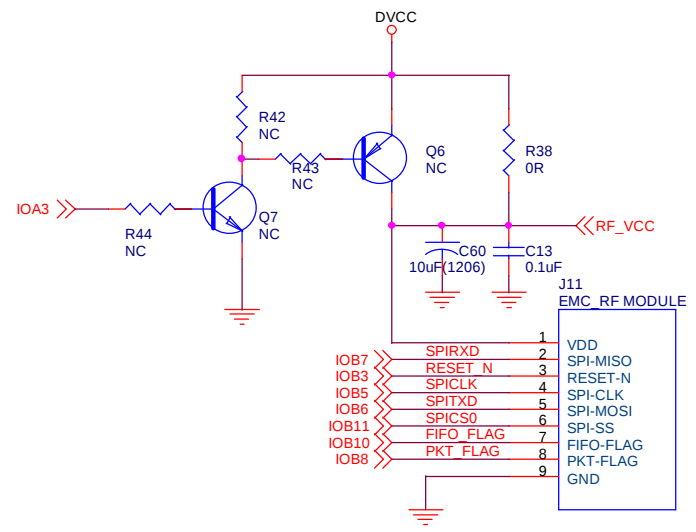
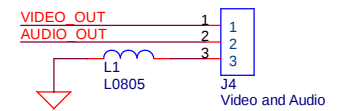
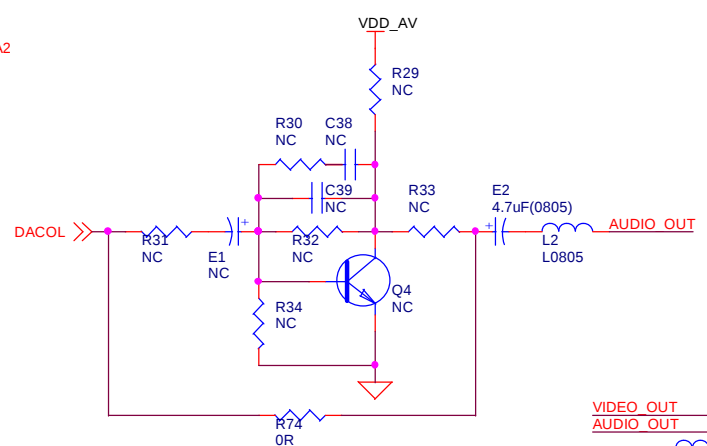
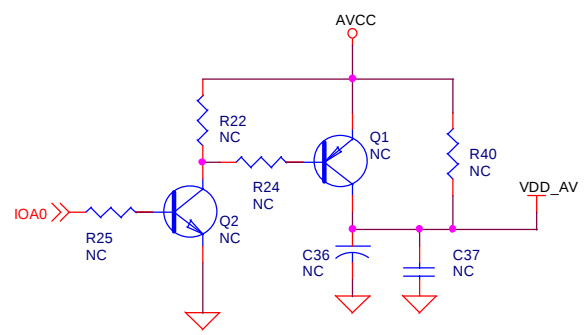
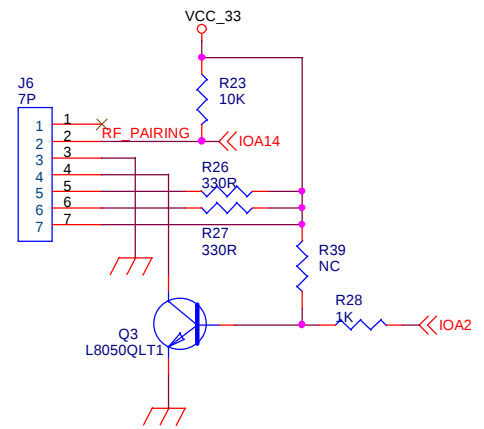
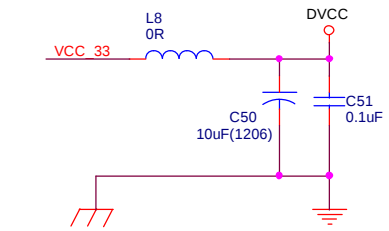
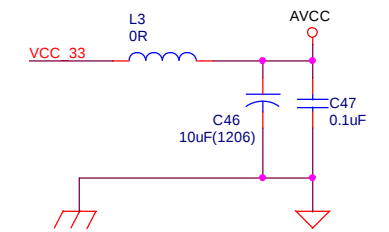
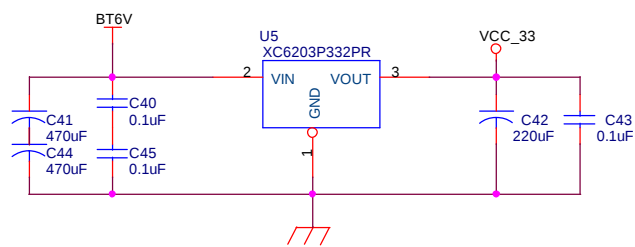
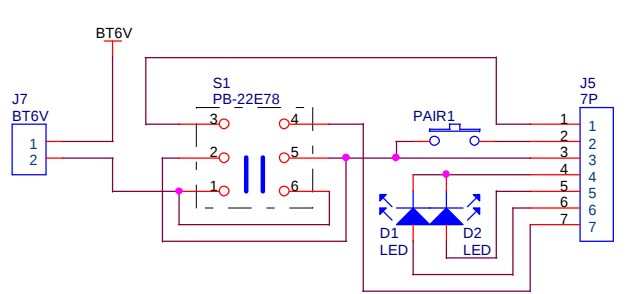
Option 1: To reduce sleep current and SDRAM data no need to be kept, user should adapt option 1 and open R69



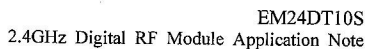
Nandflash: R17:0R, R18:NC
ROM & OTP: R17:NC, R18:0R



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Size	Document Number	Rev		
Custom	<Doc>	<RevCode>		
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C8/C9: depend on the Y1 load capacitance. Note:
CL=18P When 0, SPI_MOSI data clocked in on rising edge of SPI_CLK.
When 1, SPI_MOSI data clocked in on falling edge of SPI_CLK.

