Addendum 01 to
FCC Processing Gain report of:

Description:	**2.4 GHz USB WLAN**
Brand name:	**Intersil**
Model number:	**ISL37300XU**

FCC ID: OSZ37300XU

for
-channel 1 at 11 Mbps
-channel 6 at 1, 2, 5.5 and 11 Mbps
-channel 11 at 11 Mbps

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Testing for compliance with FCC rules 15-247e

Scope

This report presents the test procedure, test configuration and test data associated with a FCC Part 15.247 (e) Jamming Margin test for the indirect measurement of processing gain.

Applicable Reference Documents.

1. "Operation within the bands 902-928 MHz, 2400-2483.5, and 5725-5850 MHz" ***Title 47 Part 15 section 247 (e) Code of Federal Regulations***. **(47 CFR 15.247).**

2. "Report and Order: Amendment of Parts 2 and 15 of the Commission's Rules Regarding Spread Spectrum Transmitters. Appendix C: 'Guidance on Measurements for Direct Sequence Spread Spectrum Systems" ***FCC 97-114. ET Docket No. 96-8, RM-8435, RM-8608, RM-8609.***

3. "ISL3873B WLAN MAC controller with Direct Sequence Spread Spectrum Baseband Processor" ***Intersil Corporation Preliminary Data Sheet***, Melbourne FL, September 2001.

4. " M-ary Orthogonal Keying BER Curve",

Test Background and Procedure.

According to FCC regulations [1], a direct sequence spread spectrum system must have a processing gain, G_p of at least 10 dB. Compliance to this requirement can be shown by demonstrating a relative bit-error-ratio (BER) performance improvement (and corresponding signal to noise ratio per symbol improvement of at least 10 dB) between the case where spread spectrum processes (coding, modulation) are engaged relative to the processes being bypassed. In some practical systems, the spread spectrum processing cannot simply be bypassed. In these cases, the processing gain can be indirectly measured by a jamming margin test [2]. In accordance with the new NPRM 99-231, if the vendor has a system with less than 10 chips per symbol, the CW jamming results must be supported by a theoretical explanation of the system processing gain.

Theoretical calculations

The processing gain is related to the jamming margin as follows [2]:

$$G_p = \left(\frac{S}{N}\right)_{output} + \left(\frac{J}{S}\right) + L_{system}$$

Where $BER_{REFERENCE}$ is the reference bit error ratio with its corresponding, theoretical output signal to noise ratio per symbol, $(S/N)_{output}$, (J/S) is the jamming margin (jamming signal power relative to desired signal power), and L_{system} are the system implementation losses.

The maximum allowed total system implementation loss is 2 dB.

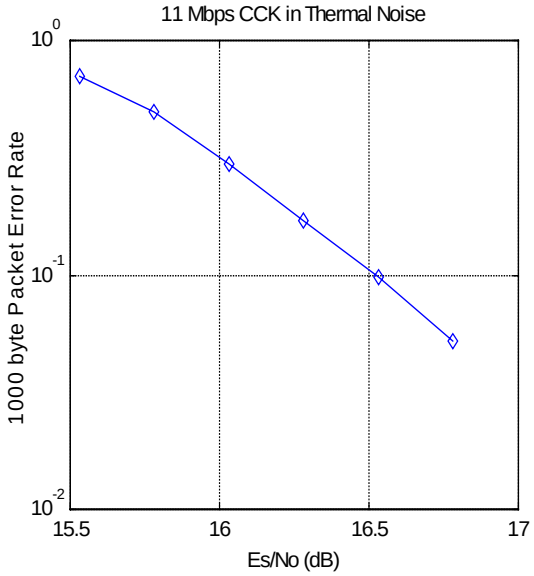
The ISL3873B direct sequence spread spectrum baseband processor uses CCK modulation which is a form of M-ary Orthogonal Keying. The BER performance curve is given by [5]:

" The probability of error for generalized M-ary Orthogonal signaling using coherent demodulation is given by:

$$P_e = 1 - P_{c1} = 1 - \frac{1}{\sqrt{2\pi}} \int_{-\frac{S_{01}}{N_0}}^{\infty} \left[2\left(1 - Q\left\{ z + \sqrt{2\,\frac{E_b}{\eta}} \right\}\right) \right]^{\frac{M}{2}-1} \exp\left\{ -\frac{z^2}{2} \right\} dz$$

This integral cannot be solved in closed form, and numerical integration must be used. This is done in a MATHCAD environment and is displayed in graphical format.

1000 byte PER vs. Es/No



The reference PER is specified as 8% . The corresponding Es/No (signal to noise ratio per symbol) is 16.4 dB. The Es/No required to achieve the desired BER with maximum system implementation losses is 18.4 dB. The minimum processing gain is again, 10 dB, therefore:

$$G_p = \left(\frac{E_s}{N_o}\right)_{output} + \left(\frac{J}{S}\right) + L_{system} = 16.4dB + 2.0dB + \left(\frac{J}{S}\right) \geq 10dB$$

$$G_p = 18.4dB + \left(\frac{J}{S}\right) \geq 10dB$$

The minimum jammer to signal ratio is as follows:

$$\left(\frac{J}{S}\right) \geq -8.4dB$$

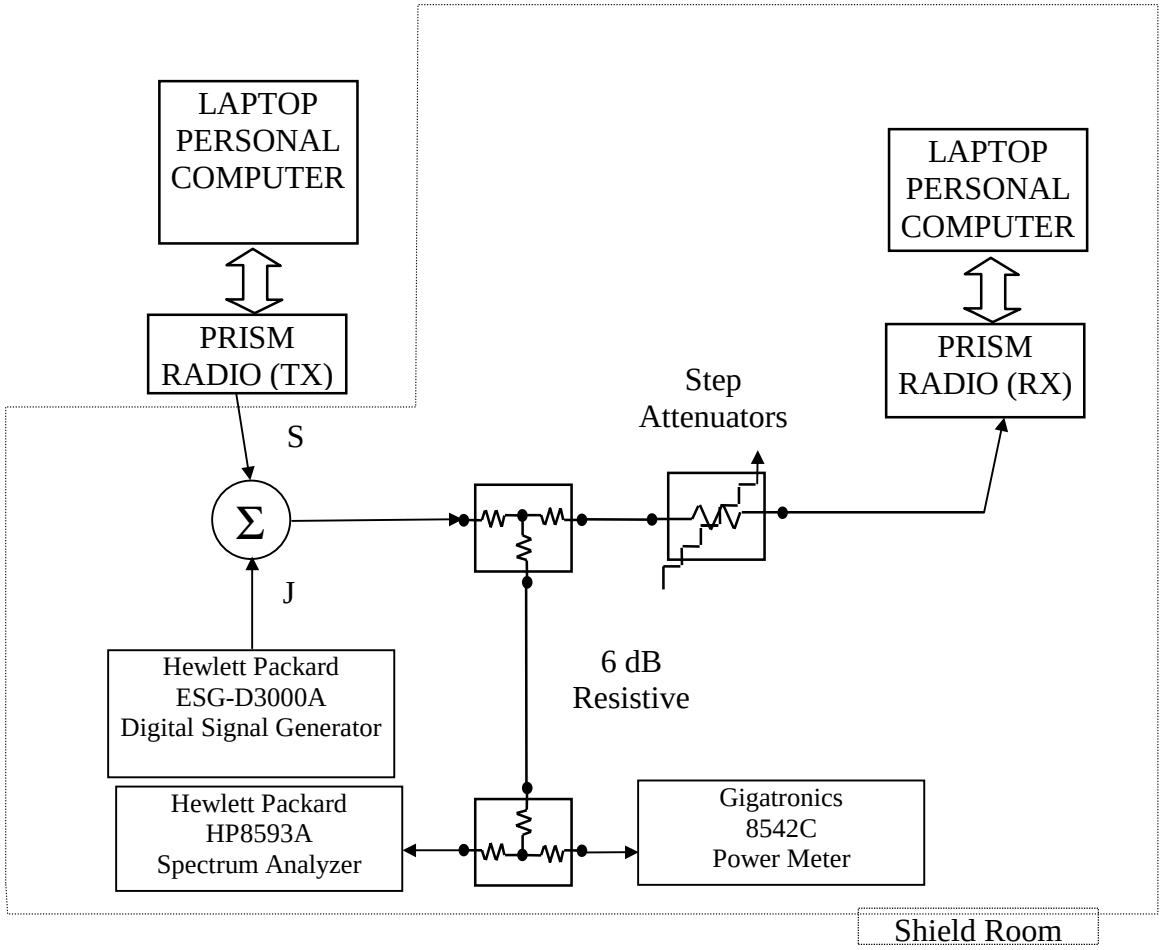
For the case of the ISL3873B, the bit rates are 1, 2, 5.5, and 11 Mbps. The corresponding symbol rates are 1, 1, 1.375, and 1.375 MSps. The chip rate is always 11 MCps, so the ratio of chip rate to symbol rate is 11:1 for the 1 and 2 Mbps rates and 8:1 for the 5.5 and 11 Mbps rates. Since the symbol rate to bit rate is less than 10 for the higher rates, we supply the theoretical processing gain calculation for these cases where both spread spectrum processing gain and coding gain are utilized. This is reasonable in that they cannot be separated in the demodulation process. If a separable FEC coding scheme were used, we would not be comfortable making this assertion.

As can be seen from the curve of figure 1, the Es/N0 is 16.4 dB at the PER of 8%. This PER can be related to a BER of 1e-5 on 1000 byte packets. With 8 bits per symbol, the Eb/N0 is then 7.4 dB or 9 dB less than the Es/N0. It is well known that the Eb/N0 of BPSK is 9.6 dB for 1e-5 BER, so therefore the coding gain of CCK over BPSK is 2.2 dB. We add this to the processing gain of 9 dB to get 11.2 dB overall processing gain for the CW jammer test.

Taking the calculations above, if the $\left(\frac{J}{S}\right) \geq -8.4\,dB$ then the equipment passes the CW jamming test.

Test Configuration: CW Jamming Margin (15.247) (e)

Basic Test Block Diagram



Test Procedure

Obtain the simplex link shown. Perform all independent instrumentation calibrations prior to this procedure. Set operating power levels using fixed and variable attenuators in system to meet the following objectives:

1. Signal Power at receiver approximately -60 dBm (above thermal sensitivity such that thermal noise does not cause bit errors).

2. Signal Power at power meter between -20 and -30 dBm for optimal linearity.

3. Use spectrum analyzer to monitor test.

4. Ensure that CW Jammer generator RF output is disabled and measure the power at the power meter port using the power meter. This is the relative signal power, Sr .

5. Disable Transmitter, and set CW Jammer generator RF output frequency equal to the carrier frequency and enable generator output. Set reference CW Jammer power level at power meter port 8.4 dB below Sr (minimum J/S, or 10 dB processing gain reference level). Note the power level setting on the generator, this is the reference CW Jammer power setting, Jr.

6. Disable CW Jammer, re-establish link. PER test should be operating essentially error-free.

7. Enable CW Jammer at the reference power level and verify that the PER test indicates a PER of less than 8%.

8. Alternatively, adjust the CW Jammer level to that which causes 8% PER and verify that the S/J is less than 8.4 dB.

9. Repeat step 7 for uniform steps in frequency increments of 50 kHz across the receiver passband with the CW Jammer. In this case the receiver passband is +8.5 MHz.

The number of points where the PER fails to achieve 8% (is higher than 8%) is determined and if this is above 20% of the total, the test is failed otherwise it is passed.