# Product Specification

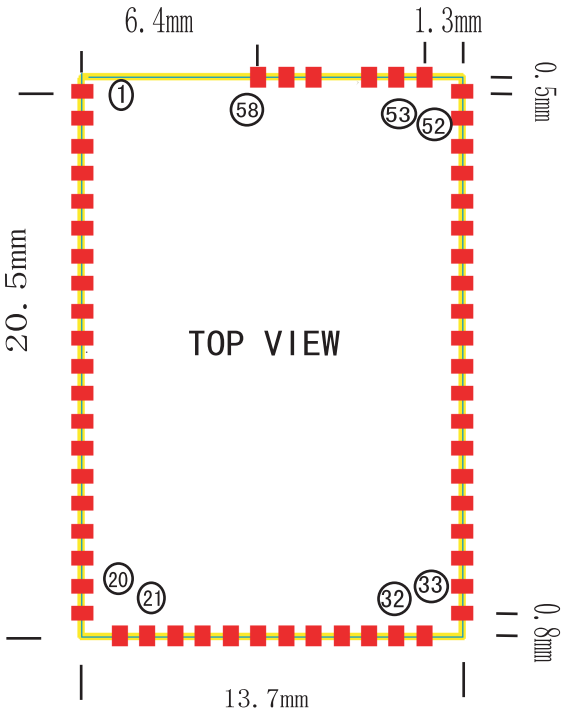
## CLASS Ⅱ

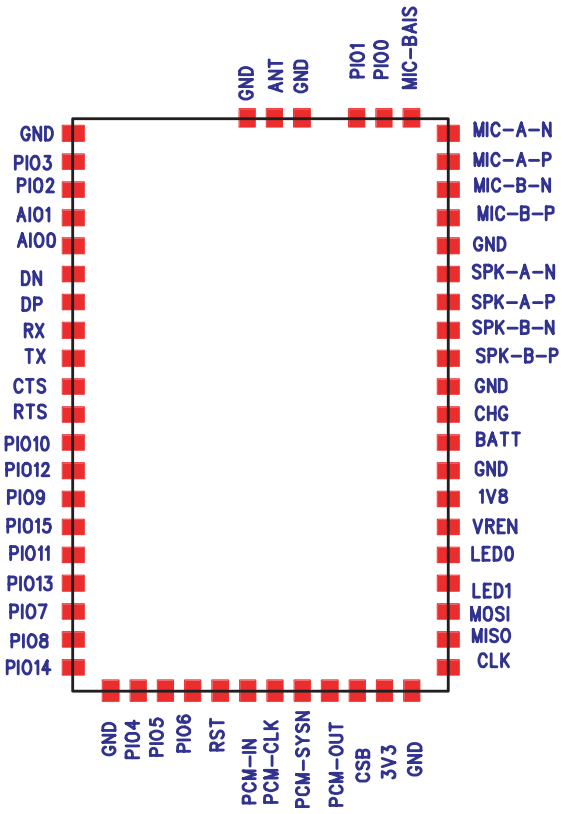
## BC05 Flash MODULE

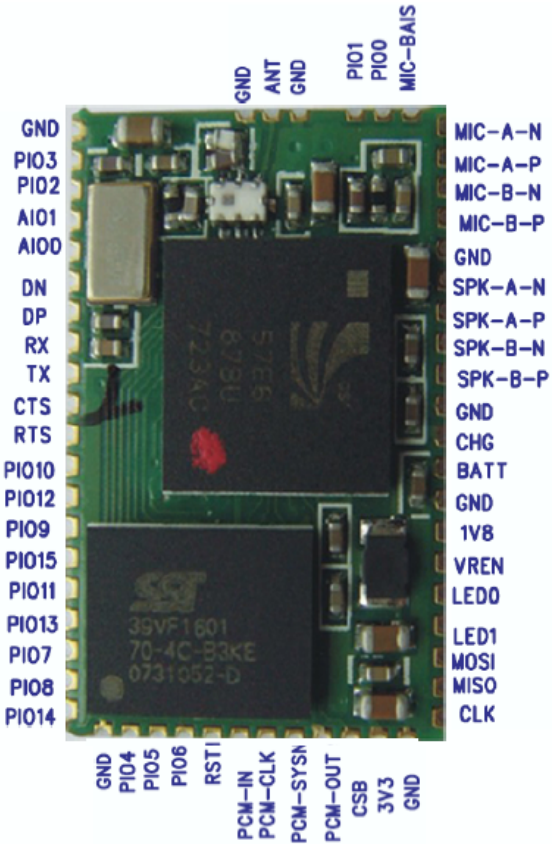
| | | | |
|---|---|---|---|
| **DRAWN BY ：** | FuLiQuan | | **MODEL :** YG-209M |
| **CHECKED BY ：** | Raymond Mok | | **DESCRIPTION :** BC05+16M Flash Module |
| **APPD. BY：** | HuangZhiMing | | **REV ：** 1.0 |

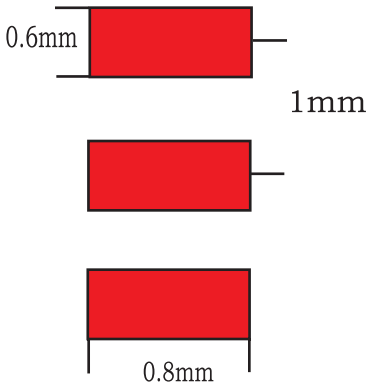
## Contents

## 1. Product Photo



## 2. Feature

- Radio Transceiver
  - Typical –82dBm sensitivity
  - Up to +2dBm RF transmit power with power level control
- Baseband
  - Fully Qualified Bluetooth V2.0+EDR
  - Integrated Audio CODEC in one chip
  - Built-in link controller, link manager protocol and flash
  - Low Power 3.3V Operation
  - Full speed USB interface, compliant with USB 1.1
  - Integrated Battery Charger With Programmable Current
  - PIO control
  - Standard HCI(UART or USB)l
  - UART interface with programmable baud rate
  - Basic module without antenna
  - Basic module as SMD type
  - With Audio Out & Audio in
- Package option
  - Edge connector

## 3. Summary of Benefit

- Complete Bluetooth Solution
  - Complete 2.4GHz radio transceiver and baseband
  - CSR Bluecore 05- BT MultiMedia, single chip bluetooth system with CMOS technology
  - Adaptive frequency hopping feature (AFH)
  - Smallest footprint, 21mmX13.7mm
  - Simplify overall design/development cycle
  - Full speed Class 2 bluetooth operation
  - Class I support using external power amplifier
- Low power standby modes to enable high efficient power management
- High performance radio transceiver
- Low overall system cost

- Application
  - Stereo Headphone
  - Automotive Hands-Free Kits
  - Handsfree headset
  - Stereo (AV) Transmitter
  - Bluetooth Sound Box

- Software
  - Support CSR bluetooth stack
  - Design for Client

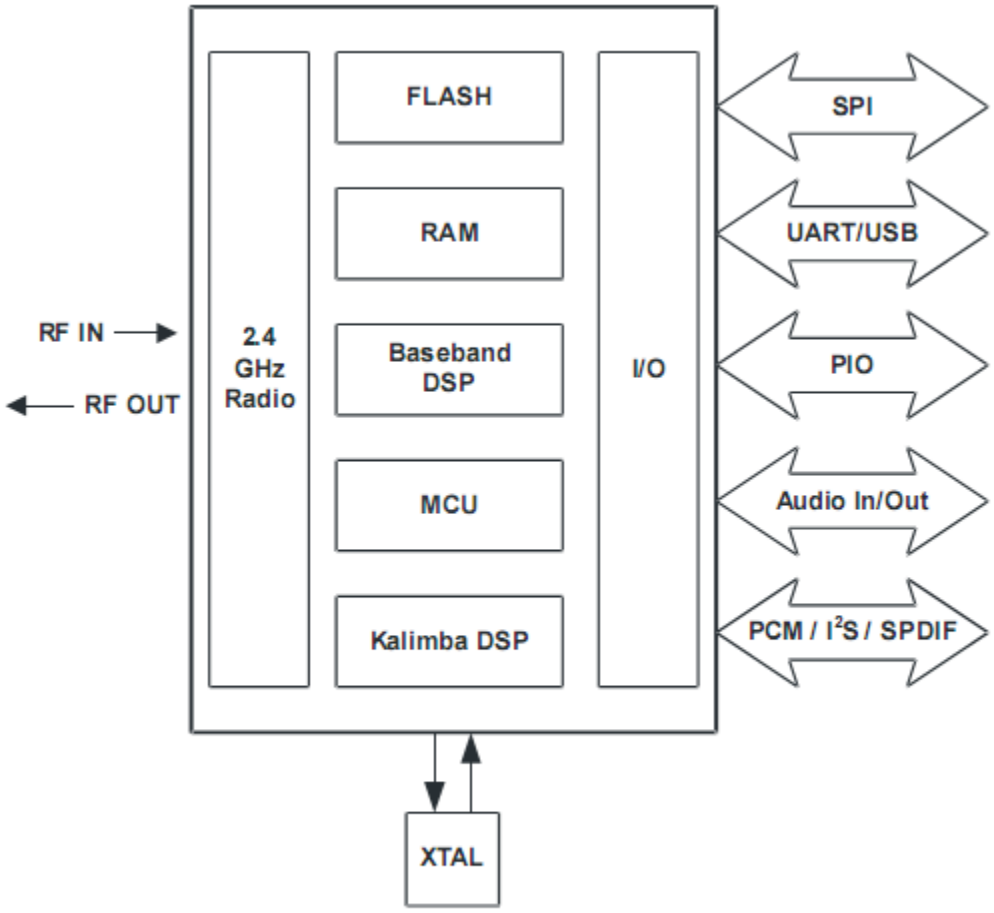
## 4. Device Terminal Function

| PIN Name | PIN # | Pad type | Description | Note |
|---|---|---|---|---|
| GND | 1.21.32.40 43.4856.58 | VSS | Ground pot | |
| 1.8V | 39 | VDD1.8V | Integrated 1.8V (+) supply with On-chip output within 1.7-1.9V | |
| 3.3V | 31 | VDD3.0V | Integrated 3.3V (+) supply with On-chip l output within 3.0.-3.3V | |
| BATT | 41 | Battery terminal+ve | Lithium ion/polymer battery positiveterminal. | |
| CHG | 42 | Charger input | Lithium ion/polymer battery charger input | |
| VREN | 38 | Analogue | High-voltage linear regulator and switch-moderegulator | |
| AIO0 | 5 | Bi-Directional | Programmable input/output line | |
| AIO1 | 4 | Bi-Directional | Programmable input/output line | |
| PIO0 | 54 | Bi-Directional RX EN | Programmable input/output line, control output for LNA(if fitted) | |
| PIO1 | 55 | Bi-Directional TX EN | Programmable input/output line, control output for PA(if fitted) | |

| | | | | |
|---|---|---|---|---|
| **PIO2** | **3** | **Bi-Directional** | **Programmable input/output line** | |
| **PIO3** | **2** | **Bi-Directional** | **Programmable input/output line** | |
| **PIO4** | **22** | **Bi-Directional** | **Programmable input/output line** | |
| **PIO5** | **23** | **Bi-Directional** | **Programmable input/output line** | |
| **PIO6** | **24** | **Bi-Directional** | **Programmable input/output line** | |
| **PIO7** | **18** | **Bi-Directional** | **Programmable input/output line** | |
| **PIO8** | **19** | **Bi-Directional** | **Programmable input/output line** | |
| **PIO9** | **14** | **Bi-Directional** | **Programmable input/output line** | |
| **PIO10** | **12** | **Bi-Directional** | **Programmable input/output line** | |
| **PIO11** | **16** | **Bi-Directional** | **Programmable input/output line** | |
| **RET** | **25** | **CMOS Input with weak intemal pull-down** | **RESET** | |
| **UART_RTS** | **11** | **CMOS output, tri-stable with weak internal pull-up** | **UART request to send, active low** | |
| **UART_CTS** | **10** | **CMOS input with weak internal pull-down** | **UART clear to send, active low** | |
| **UART_RX** | **8** | **CMOS input with weak internal pull-down** | **UART Data input** | |
| **UART_TX** | **9** | **CMOS output, Tri-stable with weak internal pull-up** | **UART Data output** | |
| **SPI_MOSI** | **35** | **CMOS input with weak internal pull-down** | **Serial peripheral interface data input** | |
| **SPI_CSB** | **30** | **CMOS input with weak internal pull-up** | **Chip select for serial peripheral interface, active low** | |
| **SPI_CLK** | **33** | **CMOS input with weak internal pull-down** | **Serial peripheral interface clock** | |
| **SPI_MISO** | **34** | **CMOS input with weak internal pull-down** | **Serial peripheral interface data Output** | |

| | | | | |
|---|---|---|---|---|
| **USB_DN** | **6** | **Bi-Directional** | **USB** | |
| **USB_DP** | **7** | **Bi-Directional** | **USB** | |
| **MIC_A_P** | **51** | **Analogue input** | **Microphone input L positive pot** | **Microphone Left Positive** |
| **MIC_A-N** | **52** | **Analogue input** | **Microphone input L negative pot** | **Microphone Left Negative** |
| **MIC_B_P** | **49** | **Analogue input** | **Microphone input R positive pot** | **Microphone Right Positive** |
| **MIC_B_N** | **50** | **Analogue input** | **Microphone input R negative pot** | **Microphone Right Negative** |
| **SPK_A_P** | **46** | **Analogue output** | **Speaker output L negative** | **Left Negative** |
| **SPK_A_N** | **47** | **Analogue output** | **Speaker output L positive** | **Left Positive** |
| **SPK_B_P** | **44** | **Analogue output** | **Speaker output R negative** | **Right Negative** |
| **SPK_B_N** | **45** | **Analogue output** | **Speaker output R positive** | **Right Positive** |
| **PCM_IN** | **26** | | **Synchronous PCM data input** | |
| **PCM_SYNC** | **28** | | **Synchronous PCM data strobe** | |
| **PCM_CLK** | **27** | | **Synchronous PCM data clock** | |
| **PCM_OUT** | **29** | | **Synchronous PCM data output** | |
| **ANT** | **57** | **Analogue** | **RF In/Out** | |
| **LED0** | **37** | **Open drain output** | **LED driver** | |
| **LED1** | **36** | **Open drain output** | **LED driver** | |
| **MIC_BAIS** | **53** | **Analogue** | **Microphone bia** | |

## 5. Block Diagram




System Architecture

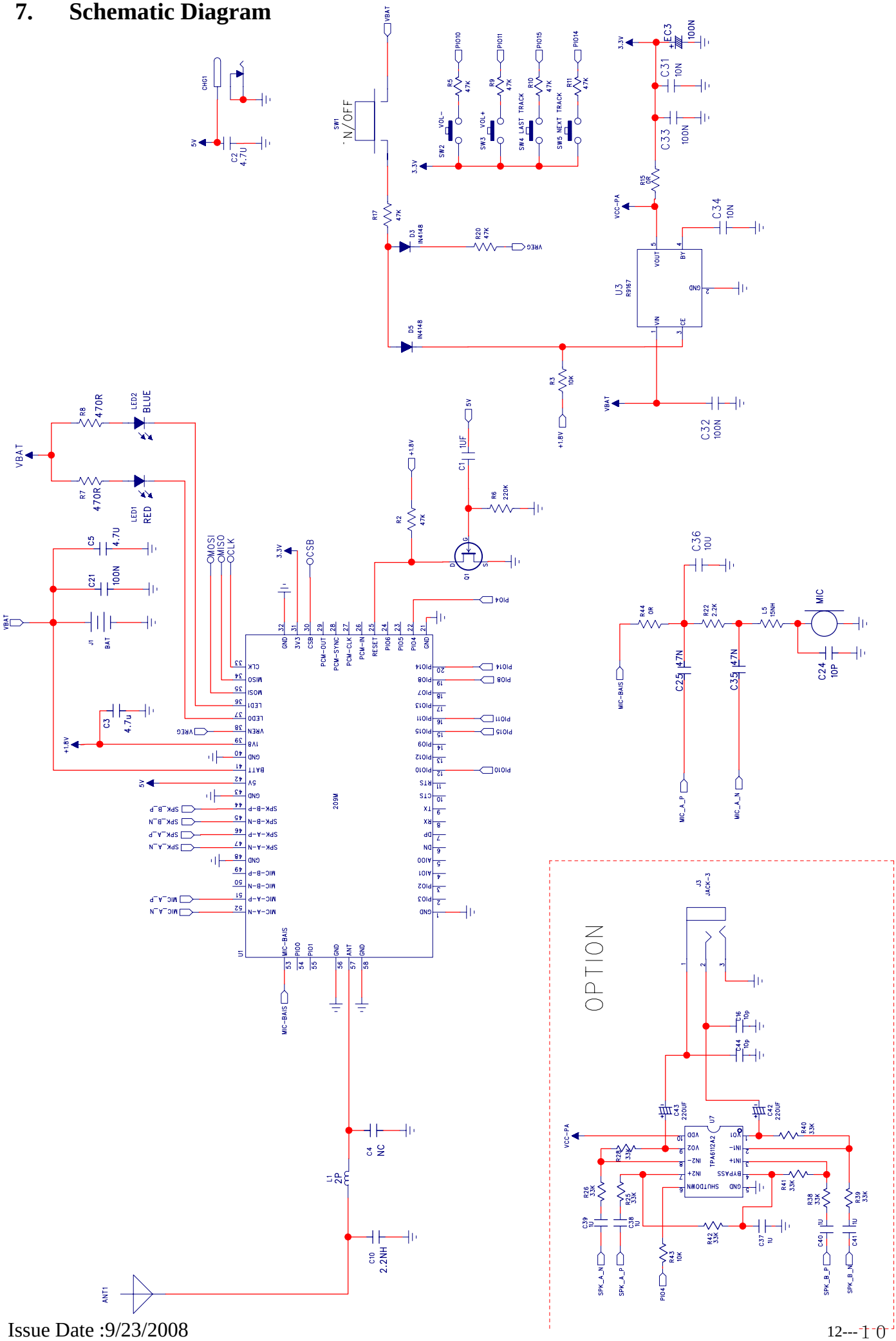
## 6. Electrical Specification:

- **Eecommended Operating condition**

| Operating Condition | Min | Max |
|---|---|---|
| Operating temperature range | -20℃ | +75℃ |
| Guaranteed RF performance range(a) | -20℃ | +75℃ |
| Supply voltage: VDD_RADIO, VDD_VCO, VDD_ANA and VDD_CORE | 1.7V | 1.9V |
| Supply voltage: VDD_PADS, VDD_PIO, VDD_MEM and VDD_USB | 1.7V | 3.6V |
| Supply voltage: VREG_IN | 3.0v | 4.2V(b) |
| Supply voltage: BAT_P | 3.0v | 4.2V |
| Supply voltage: V_CHG | 4.35V | 6.5V |

| Radio Characteristics | VDD = 1.8V | | Temperature = +20°C | | |
|---|---|---|---|---|---|
| | Min | Typ | Max | Bluetooth Specification | Unit |
| Maximum RF transmit power[a] [b] | - | 2.5 | - | -6 to +4[c] | dBm |
| RF power variation over temperature range with compensation enabled(±)[d] | - | 1.5 | - | - | dB |
| RF power variation over temperature range with compensation disabled(±) | - | 2 | - | - | dB |
| RF power control range | - | 35 | - | ≥16 | dB |
| RF power range control resolution[e] | - | 0.5 | - | - | dB |
| 20dB bandwidth for modulated carrier | - | 780 | - | ≤1000 | kHz |
| Adjacent channel transmit power $F = F_0 \pm 2MHz$[f] [g] | - | -40 | - | ≤-20 | dBm |
| Adjacent channel transmit power $F = F_0 \pm 3MHz$ | - | -45 | - | ≤-40 | dBm |
| Adjacent channel transmit power $F = F_0 \pm > 3MHz$ | - | -50 | - | ≤-40 | dBm |
| $\Delta f1_{avg}$ Maximum Modulation | - | 165 | - | $140<f1_{avg}<175$ | kHz |
| $\Delta f2_{max}$ Minimum Modulation | - | 150 | - | ≥115 | kHz |
| $\Delta f1_{avg}/\Delta f2_{avg}$ | - | 0.97 | - | ≥0.80 | - |
| Initial carrier frequency tolerance | - | 6 | - | ±75 | kHz |
| Drift Rate | - | 8 | - | ≤20 | kHz/50μs |
| Drift (single slot packet) | - | 7 | - | ≤25 | kHz |
| Drift (five slot packet) | - | 9 | - | ≤40 | kHz |
| 2nd Harmonic Content | - | -65 | - | ≤-30 | dBm |
| 3rd Harmonic Content | - | -45 | - | ≤-30 | dBm |

## 7. Schematic Diagram



## 8. Testing Block Diagram

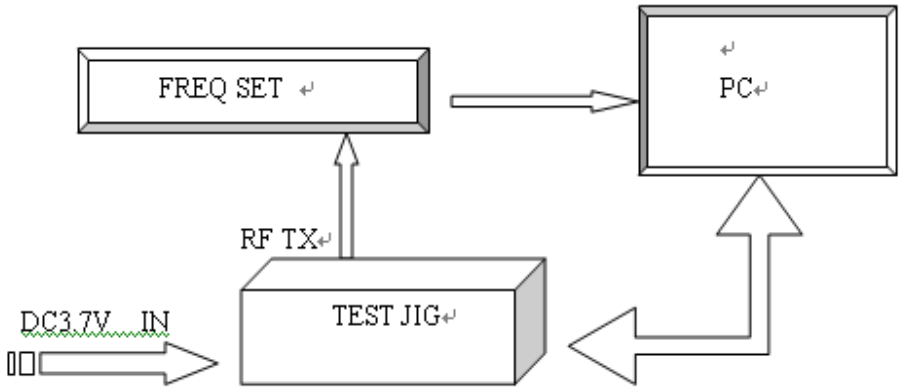



Fig 1 Programming and Freq. Alignment Test Procedure

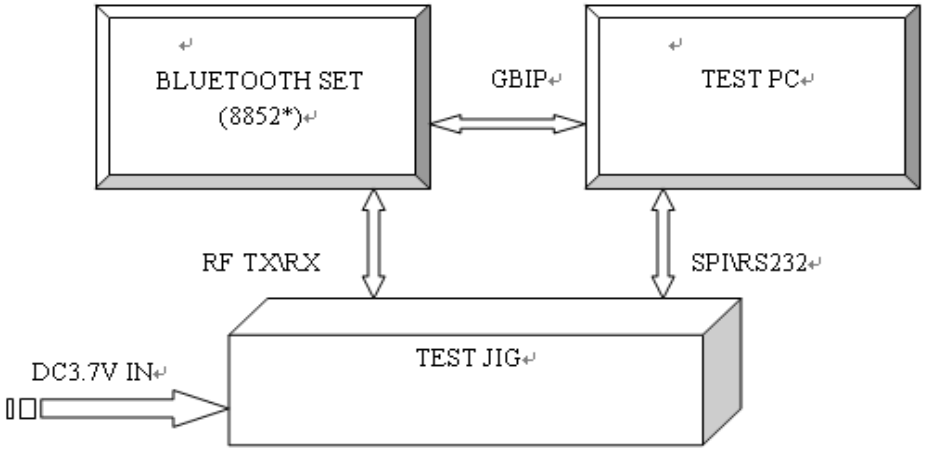



Fig 2 RF Parameter Test procedure

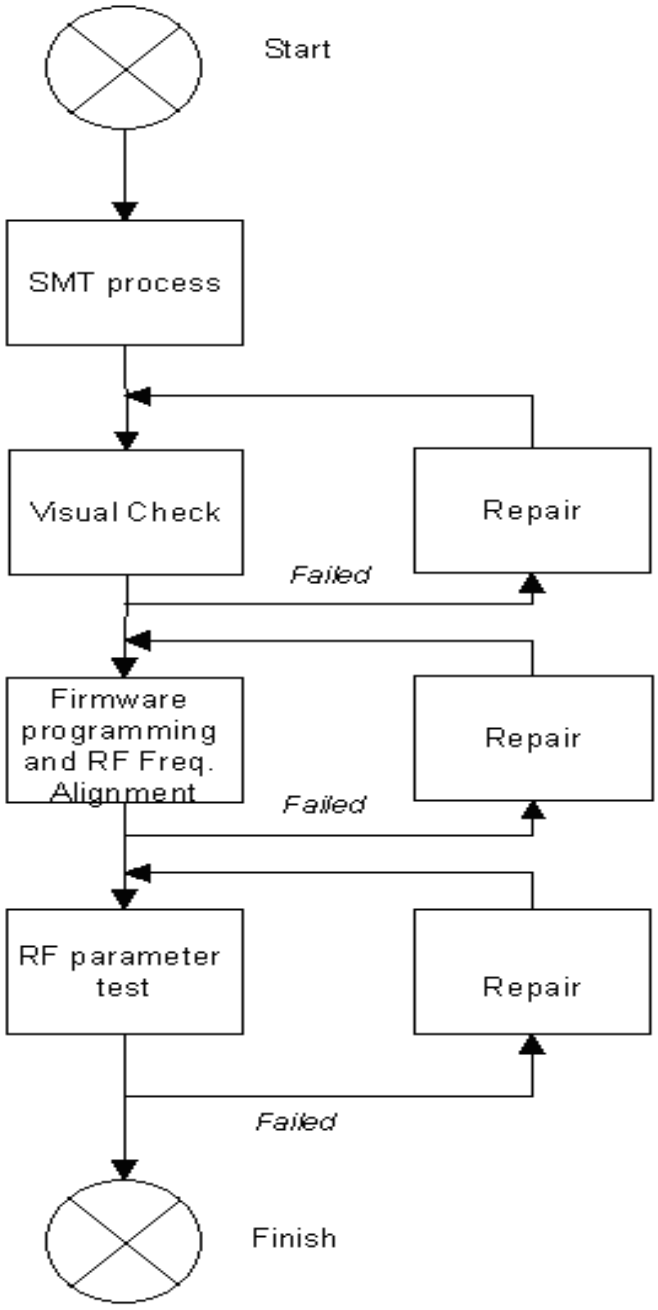



**Fig 3 Assemble/Alignment/Testing Flow Chart**