OCCUPIED BANDWIDTH

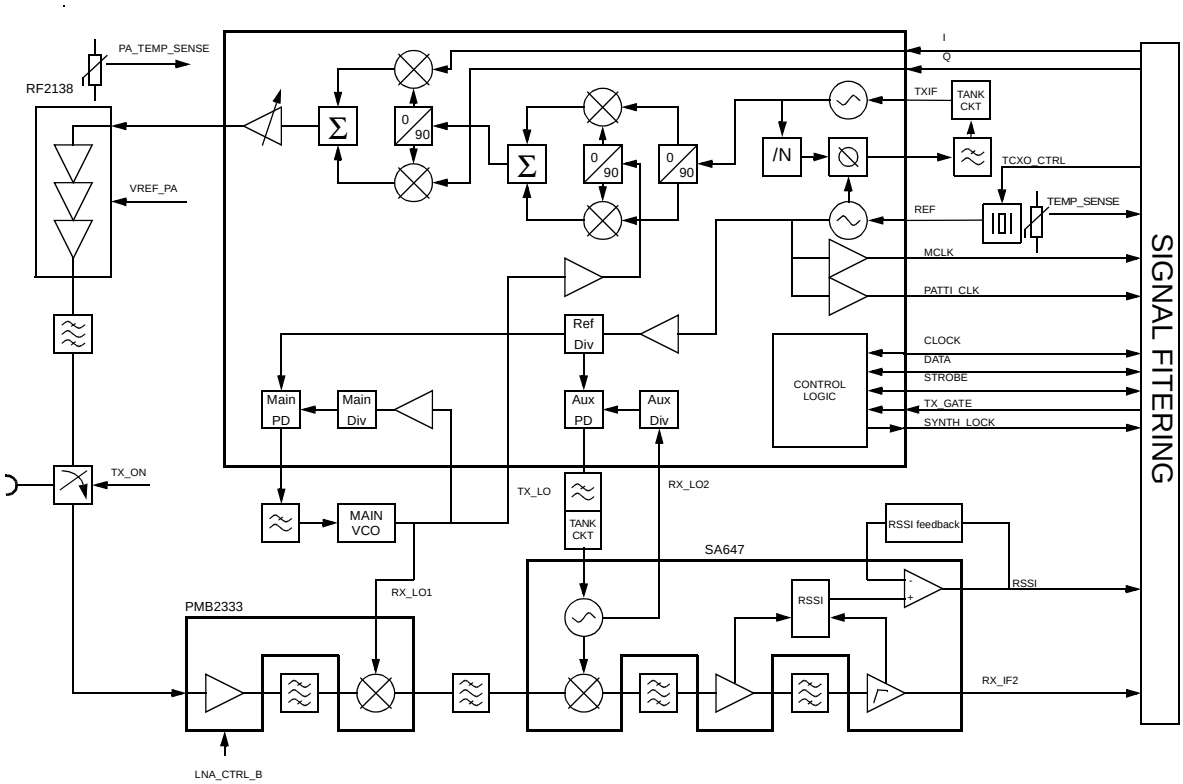
Method of Measurement Per 2.989 (c,1) Data on Occupied Bandwidth is presented in the form of a spectrum analyzer plot which illustrates the transmitter sidebands. A plot is taken of the carrier sideband modulated with a 2500 Hz tone at a level 16 dB greater than that required to produce 50 percent modulation. (The spectrum analyzer grid indicates the reference level of the carrier unmodulated in all exhibits.)

Data, Digital Voice Bn = 2(B/2) + 2DK where B = 8000 Hz
D = 2100 Hz
K=1(assumed)

Bn=12200
Therefore, Emission Designators are,
12K2F1D

3 RADIO FUNCTIONAL DESCRIPTION

Radio parts in detail:



3.1 Reference frequency

The reference frequency **19.2 MHz** is generated by a crystal unit combined with a buffer amplifier. It is tuned by varying the voltage over a varactor diode, VCTCXO_CTRL. This signal is generated by the 10-bit DAC in the circuit PATTI. The tuning sensitivity is approximately 0.05 ppm/step in the middle range.

VCTCXO_CTRL shall initially be set to a nominal value, which is compensated for temperature variations detected by TEMP_SENSE according to a table stored in the modems nonvolatile memory.

The frequency is adjusted according to the estimated received frequency error. The latest used value is stored. If the modem has not yet detected a base station, VTCXO_CTRL is set to stored nominal value + temperature compensation. These values are calibrated and stored during production.

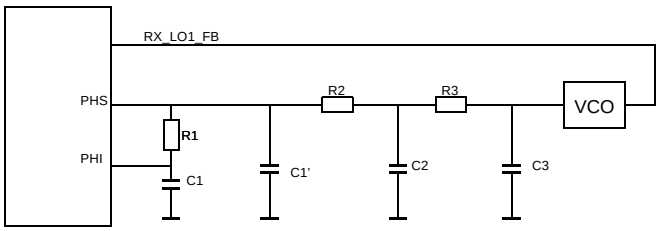
3.2 JACE: SYNTHESIZERS AND PLLS

The JACE ASIC implements the PLLs and synthesizers for the main VCO and auxiliary VCO. In TX mode it also includes the TX IF VCO. It is controlled

by a 3-wire serial interface from the Pepper ASIC. It also serves as a buffer amplifier for the reference clocks MCLK and PATTI_CLK.

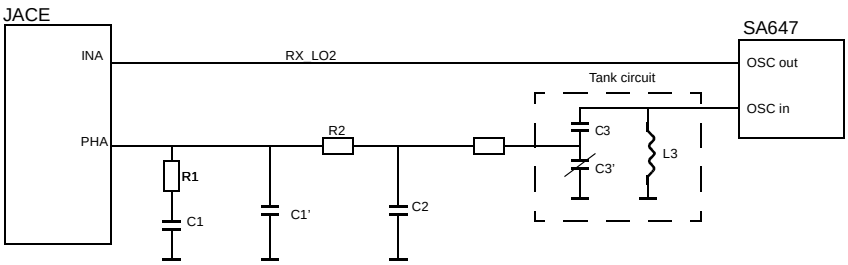
The main synthesizer locks the main VCO to either the RX LO1 or the TX frequency according to the respective mode RX or TX.

The picture below shows the main VCO loop filter:



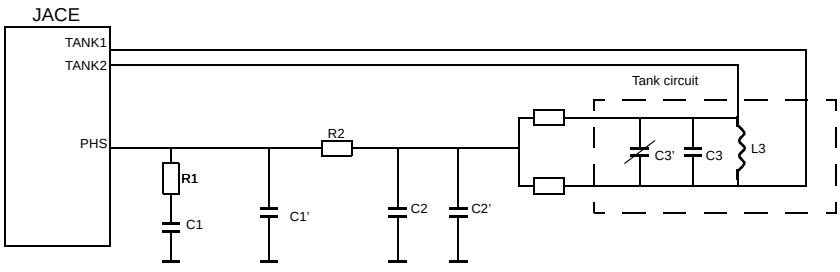
R1, C1 and C1' sets loop performance, R2 and C2 attenuates spuriouses caused by channel spacing fractional counters, and R3 and C3 attenuates the spuriouses at the phase detector frequency.

In RX mode the auxiliary synth locks the VCO in SA647 to the RX_LO2. RX LO2 is generated by the auxiliary loop in ASIC JACE together with the oscillator in the receiver IF circuit. The frequency is **94.95 MHz**.



Loop filter and tank: R1, C1 and C1' sets loop performance, R2 and C2 attenuates the phase detector frequency and L3, C3 and C3' is the resonant tank circuit. C3' is a varactor diode, which is the tuning element in the tank.

In TX mode an internal TX IF VCO is locked to 7x the reference frequency. The **TX IF is 134.4 MHz**. The oscillator is integrated in ASIC JACE. A tank resonance circuitry is tuned to this frequency with a varicap diode:



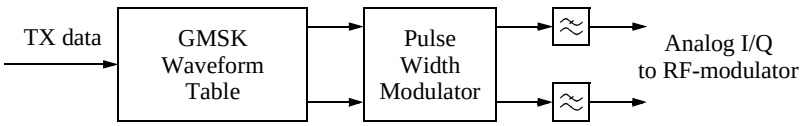
R1, C1 and C1' sets loop performance, R2, C2 and C2' attenuates the reference frequency spuriouses and L3, C3 and C3' is the resonant tank circuit. C3' is a varactor diode, which is the tuning element in the tank.

3.3 MODULATION GENERATION

Only digital modulation is used. Pepper sends TX data to the DSP. The DSP performs channel coding and then uses stored sets of tabbelized values to generate streams of samples for I & Q signals.

The samples are returned to PEPPER, which converts them via PWM and subsequent lowpassfilters to analogue I & Q signals. These signals modulate the RF carrier as described in the block schematics above.

I/Q Generation



The RF signal characteristics follow the Mobitex Interface Specification, which defines GMSK with a B*T of 0.3, +2 kHz deviation for a series of ones and -2 kHz deviation for a series of zeros.

3.4 TRANSMITTER FRONTEND

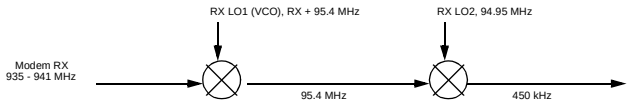
The transmitter front end consists of a filter and a power amplifier (PA).

The PA is a RF2173 from RF Micro-Devices. This circuit can transmit a 3 W peak power bursted signal, which reads as maximal 2 W at the modem's RF connector. The board temperature is supervised in order to prevent overheating in high temperature and during high duty cycle situations. Outside a set temperature range the TX will be disabled. The PA output matching is done with a combination of microstrip and discrete components.

The filter is a wide SAW bandpass filter. The main purpose of this filter is to attenuate spuriouses and harmonics. Since the modem operates with semi-duplex, the noise in the receiver band does not need to be considered when the transmitter is turned off.

3.5 RECEIVER

Frequency conversion blocks:



The 450 kHz signal is then filtered and processed in the digital section by the circuit PEPPER.

1st stage:

The receiver front-end PMB2333 contains a LNA and a mixer, with external SAW RF filter between the LNA and the mixer.

The LNA has single-ended input/outputs, all mixer ports are balanced. A balun is used on the LO input, while the IF and RF port matching is done with discrete components.

The RF filter has three major functions; reducing sideband noise, attenuating spuriouses (first image and 2x2 spurious), and preventing blocking.

The **1st RX IF is at 95.4 MHz** and the IF filter at this frequency is a crystal filter with external matching. This filter serves for second image rejection and adjacent channel attenuation.

2nd stage:

The **2nd RX IF is at 450 kHz** and is processed in an SA647. This circuit contains a second mixer, an oscillator for the second RX LO and a limiting amplifier. External filters are required for noise reduction and channel selectivity. The SA647 also produces an RSSI voltage proportional to the received power in dB.

The IF filters determine channel bandwidth and receiver selectivity. They also have the task to prevent the limiter from being saturated by out-of-band noise, and reduce the risk of oscillation due to feedback loops.

For the second RX IF two filters are used, one between mixer and IF amplifier, and one between IF amplifier and limiter. This way problems associated with cascading filters are avoided.

4 POWER SUPPLY

The supply voltage from the host system should be **7.2 V DC nominal**, in battery powered applications **minimal 6 V and maximal 9 V DC**. This voltage is downconverted by a number of regulators to the voltages used on board.

Name	Voltage V	Current mA	Usage
VRX	3.8	30	Receiver
VTX1	3.8	120	ASIC
V5_GESSICA	5	TBD	GESSICA
CVDD	1.8	TBD	ASIC
V_VCO	3.8	10	VCO
V_PA	3.3	2000 (peak)	PA
VTCXO	3.8	10	Reference oscillator

The external supply is enabled by a WAKE signal on the system interface connector. The regulator supplying the PA voltage is not affected by the WAKE-switch, since it is fed directly by the external voltage supplied from the host system.

The power amplifier supply is controlled by the signal TX_GATE.

The receiver supply voltage is enabled with signal VRX_ON.

To ensure that the modem has time enough to store away relevant parameters at power down, the signal HOSTPOW_B is used to delay the WAKE-switch turn-off.

5 CONNECTORS

5.1 SYSTEM CONNECTOR

The system connector P1 is a 30 pin surface mount connector:

Pin	Symbol	I/O	Description
1	SUPPLY	I	DC power supply input
2	SUPPLY	I	DC power supply input
3	TX_GATE	O	Transmit enable signal
4	RESET	I	System reset
5			
6	RD	O	UART:Serial port receive data line
7	TD	I	UART:Serial port transmit data line
8	RTS	I/O	UART:Request To Send
9	CTS	I/O	UART:Clear To Send
10	DTR	I/O	UART:Data Terminal Ready
11	DCD	O	UART:Data Carrier Detect
12	REF_CLK	I/O	Reference clock. Nominal 19.2 MHz
13	GND		Ground
14	GND		Ground
15			
16			
17	SCL	I/O	I^2C serial clock
18	SDA	I/O	I^2C serial data
19	VDD	I	JTAG VCC
20	BIN1_IN_OUT	I/O	User defined binary input or output
21	BIN2_IN_OUT	I/O	User defined binary input or output
22	BIN3_OUT	O	User defined binary output
23	BIN4_OUT	O	User defined binary output
24	WAKE/SYSTEMSTART	I	Modem power-up
25	GND		Ground
26	DOWNLOAD	I	FLASH programming enable
27	AD_OUT	O	User defined analog output, D/A
28	GND		Ground
29	GND		Ground
30	AD_IN	I	User defined analog input, A/D

5.2 ACCESSORY CONNECTORS

At the edges of the baseband side of the board two lines of twelve holes each are introduced as a preparation for connection of external accessories. P2 is used for I^2C communication with external devices and P3 for the JTAG and the DSP emulator.

5.2.1 Pin description P2

Pin	Symbol	I/O	Description
1	SUPPLY	I	Supply voltage
2	GND		Ground
3	SDA	I/O	I^2C serial data
4	SCL	I/O	I^2C serial clock
5			
6			
7			
8			
9	REF_CLK	I/O	Reference clock, nominal 19.2 MHz
10	AWAKE	O	Accessory wake
11			
12			

5.2.2 Pin description P3

Pin	Symbol	I/O	Description
1	ARESET	I/O	Accessory reset
2			
3	EMU0	I/O	DSP emulator interrupt
4	EMU1	I/O	DSP emulator interrupt
5	VCCS	I	JTAG: VCC
6	TDI	I	JTAG: Test Data In
7	TDO	O	JTAG: Test Data Out
8	TMS	I	JTAG: Test Mode Select
9	TCK	I	JTAG: Test Clock
10	TRST	I	JTAG: Test Reset
11	RESET	I	System reset
12	GND		Ground

5.3 ANTENNA CONNECTOR

The antenna RF connector is of type M/A-COM OSMT, a surface mount miniature snap-on connector with 50 ohm impedance. For adapter cables and order codes refer to the M3090 integrators manual for OEMs.

5.4 INTERFACING M3090 FOR EVALUATION

For M3090 testing during type approval or OEM evaluation an interface adapter is used to supply power and allow communication from any standard PC RS232 interface. The adapter follows the instructions and specifications stated in the OEM integrator's manual, which Ericsson provides for M3090 system integration. From the M3090 RF contact adapter cables to standard SMA RF connectors are available. For order codes refer to the OEM manual.

6 TERMINOLOGY

ARM	Advanced RISC Machine
DSP	Digital Signal Processor
HAL	Hardware Abstraction Layer
IF	Intermediate Frequency
I & Q	Inphase and Quadrature phase, advanced modulation scheme
LO	Local Oscillator
MIS	Mobitex Interface Specification
PA	Power Amplifier
PLL	Phase Locked Loop
RF	Radio Frequency
RISC	Reduced Instruction Set Computer

7 REFERENCES

[1] MIS, Mobitex Interface Specification,
Ericsson Document 1551-CNH160 013 Uen, Rev A

[2] M3090 Mobitex Radio Modem Integration Manual,
Ericsson Document 19817-DPY 101 2327 Uen, Rev A

[3] M3090 IWD
Ericsson Document 1/155 19-CNH 119 466 Uen, **PA3**

[4] M3090 HW description
Ericsson Document **?????, Draft**