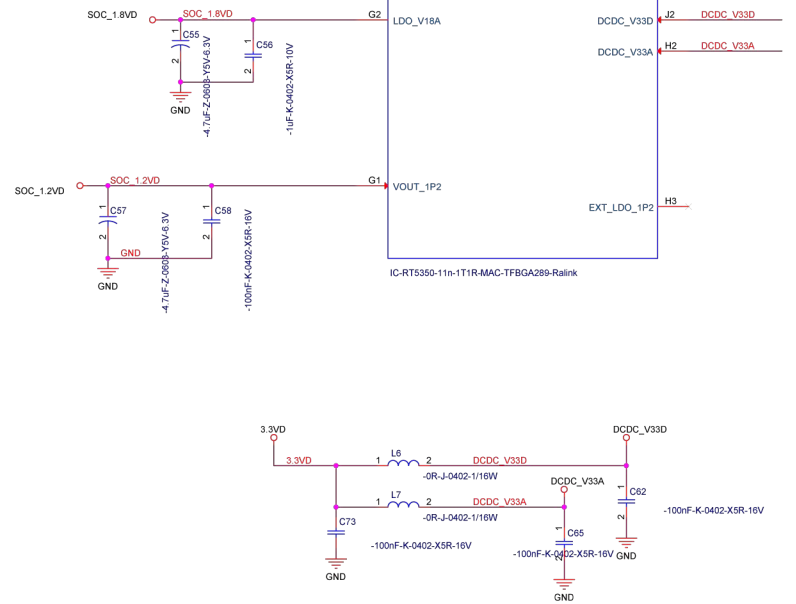
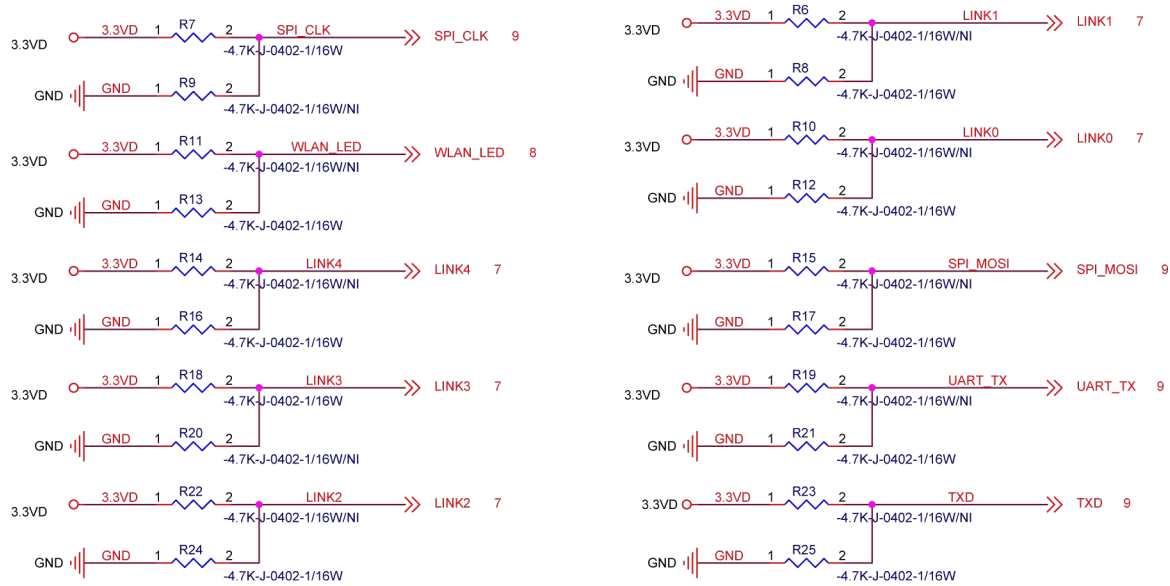


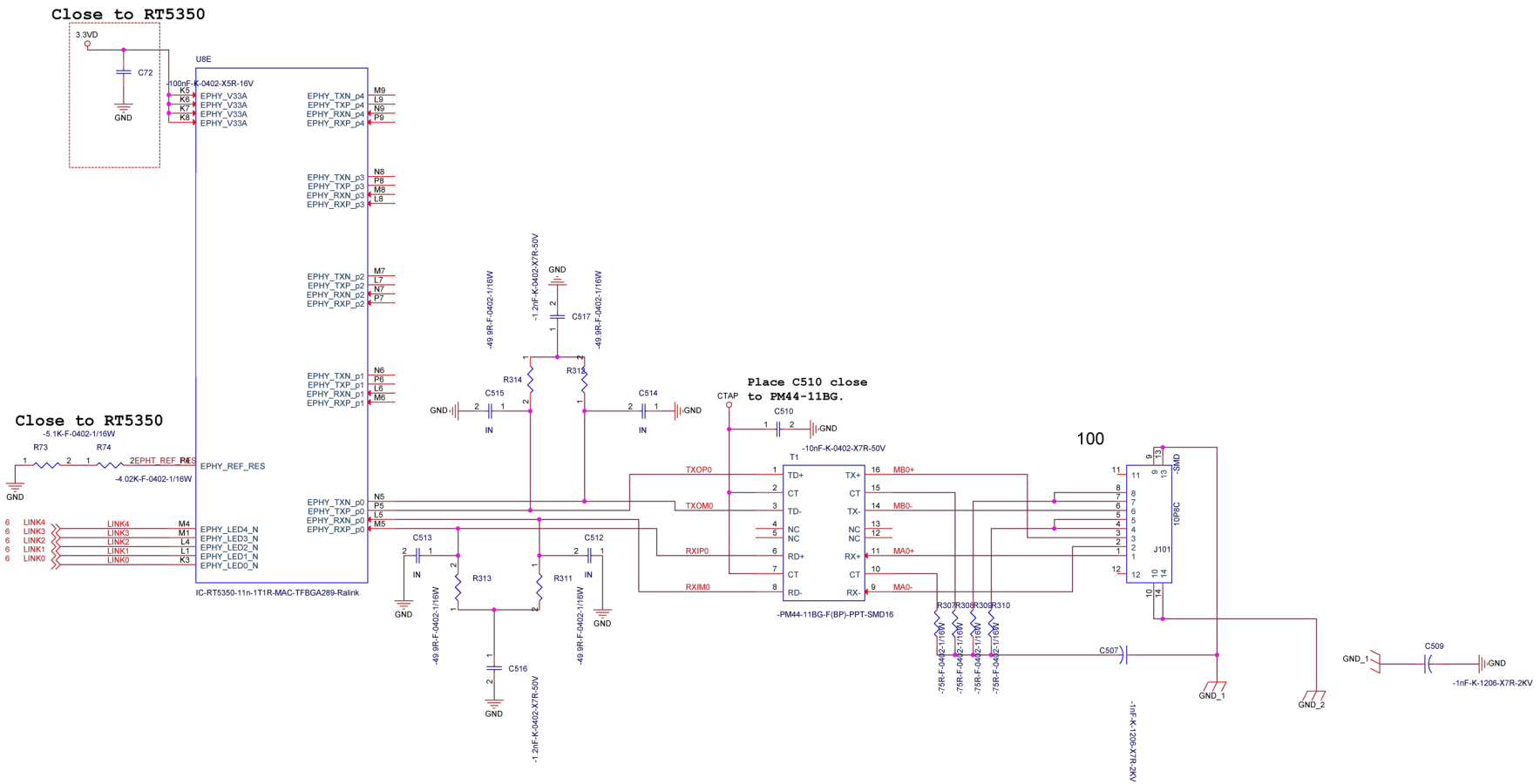
5V->3.3V 5V->1.8V



## RT5350 Boot Up Strapping

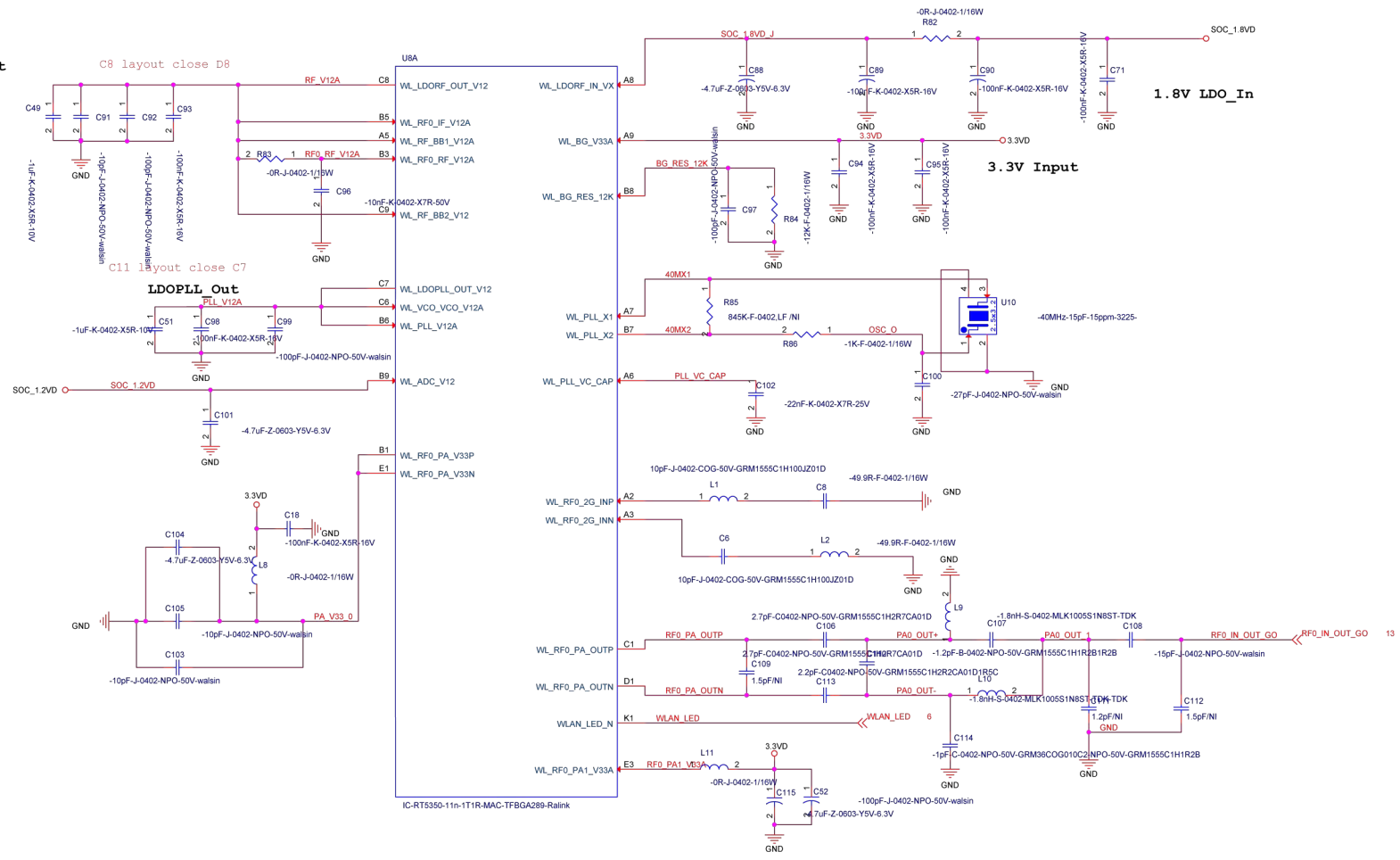
Pin Name	Description	Value=0	Value=1
SPI_CLK	XTAL_FREQ_HI	20MHz	40MHz
WLAN_LED_N	Big Endian	Little Endian	Big Endian
EPHY_LED4_N	DRAM_FROM_EE	from boot strapping	from EEPROM
{EPHY_LED3_N, EPHT_LED2_N}	DRAM_SIZE	INIC/AP(SDR) 0: 2MB/8MB 1: 8MB/16MB 2: 16MB/32MB 3: 32MB/64MB	
{EPHY_LED1_N, EPHT_LED0_N}	CPU_CLK_SEL	CPU clock select 0: 360MHz 1: Reserved 2: 320MHz 3: 300MHz	
{SPI_MOSI, TXD2, TXD}	CHIP_MODE[2:0]	A vector to set chip function/test/debug modes 0 : Normal mode(boot fromSPI serial flash) 1 : iNIC-USB mode 2 : Reserved 3 : Reserved 4 : Reserved 5 : iNIC-PHY mode 6 : SCAN mode 7 : TEST/DEBUG mode	

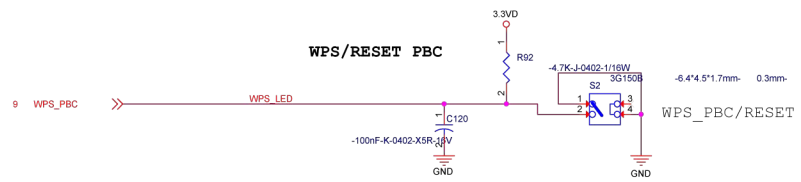
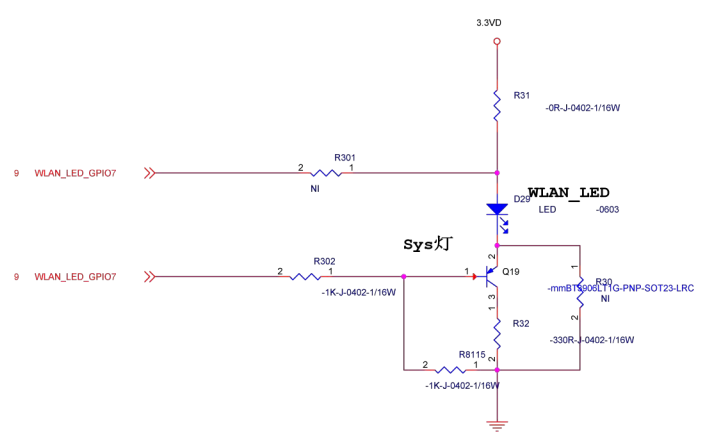
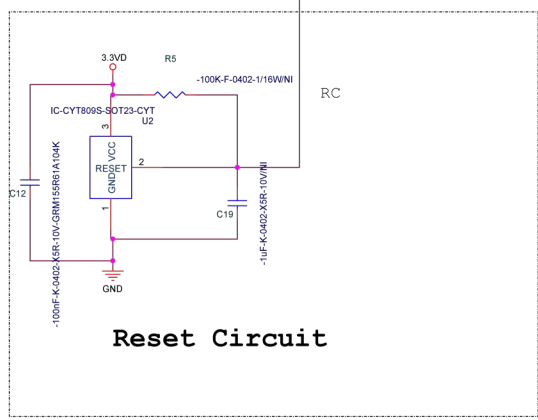
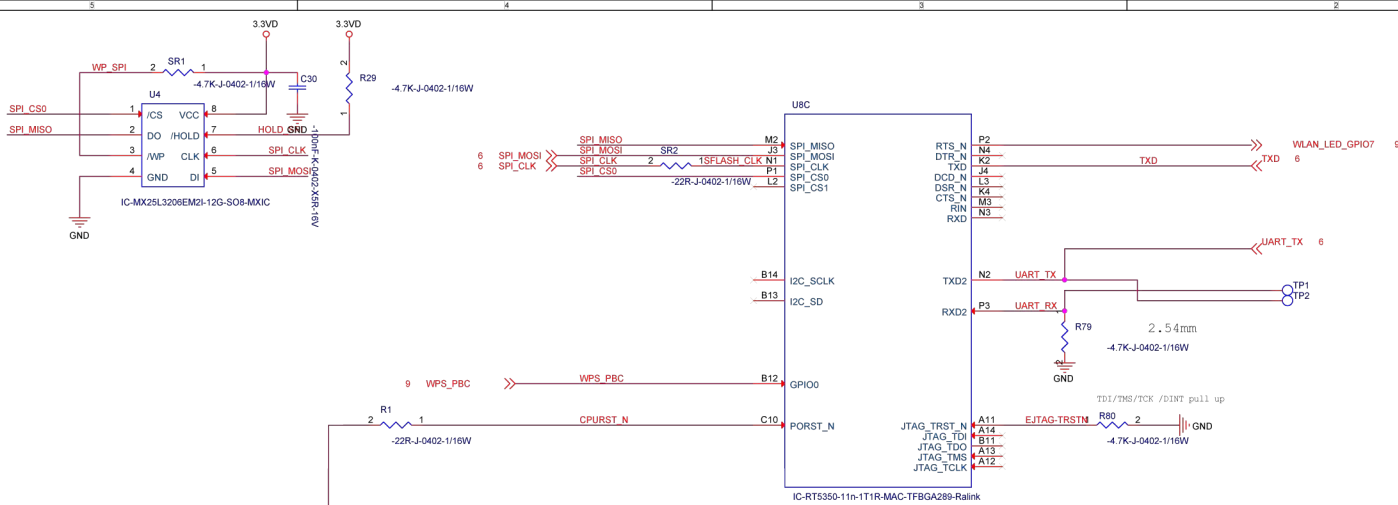


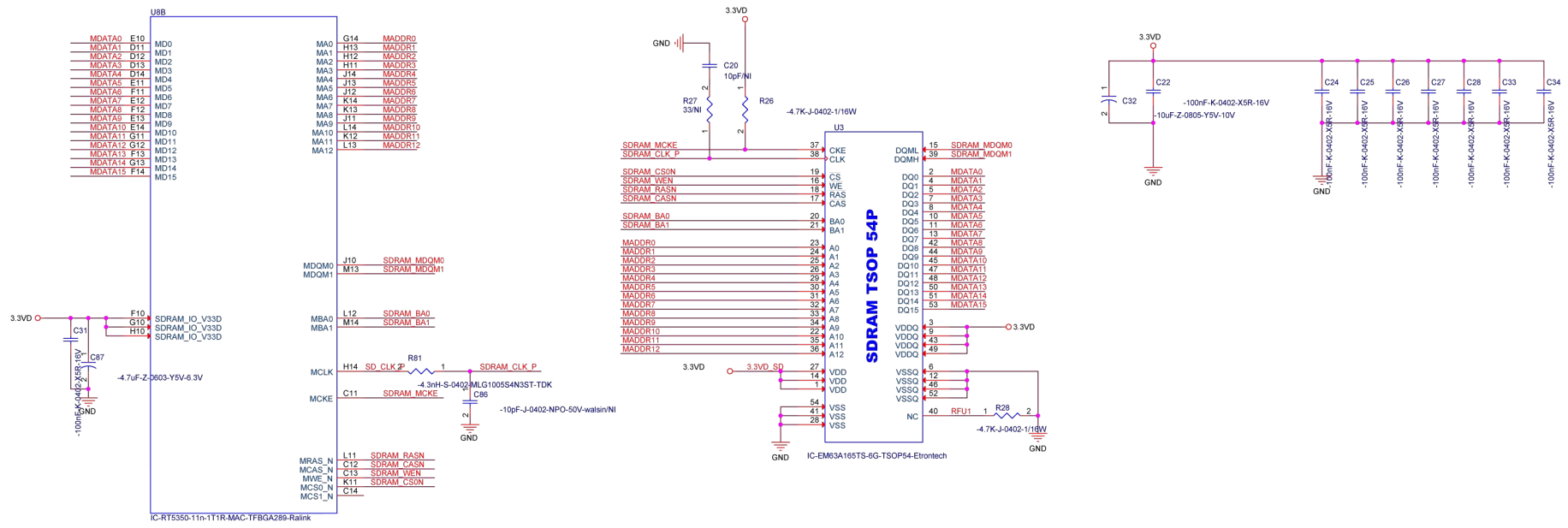


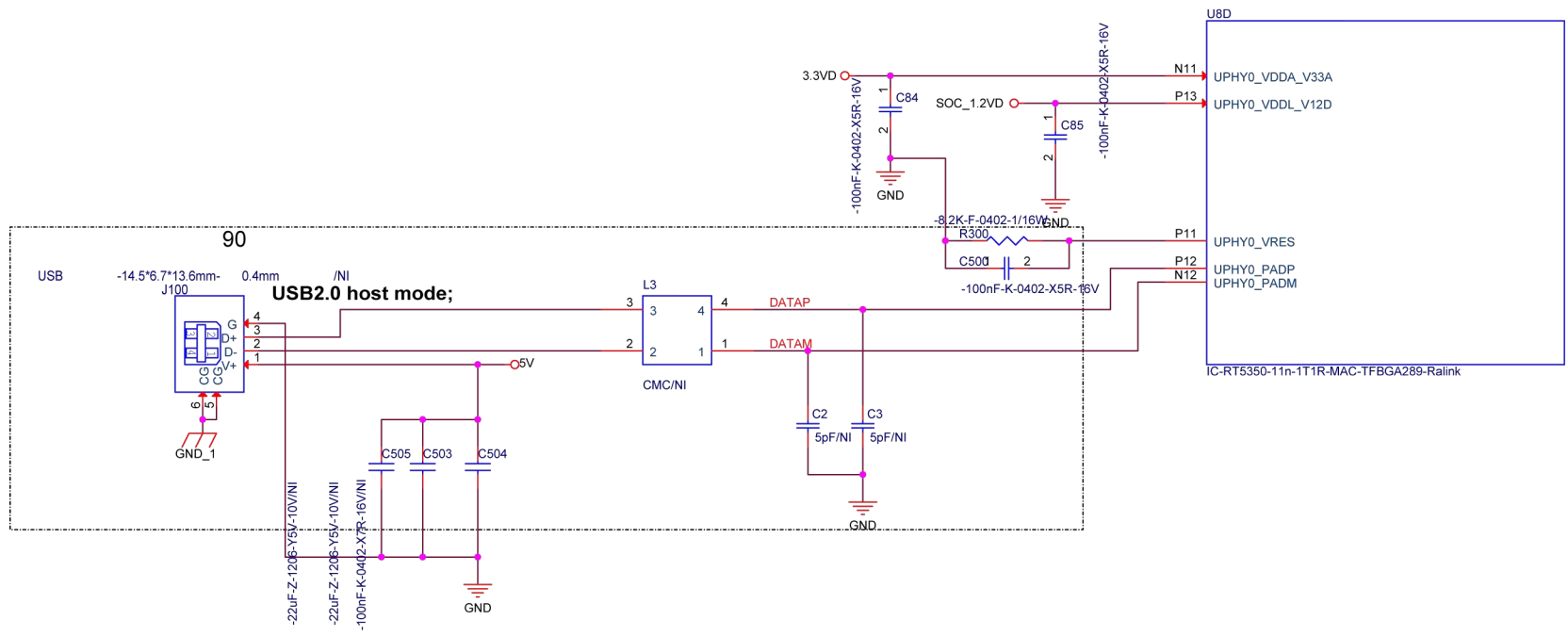
PHY address 5~d0	-> Internal PHY for port 0
PHY address 5~d1	-> Internal PHY for port 1
PHY address 5~d2	-> Internal PHY for port 2
PHY address 5~d3	-> Internal PHY for port 3
PHY address 5~d4	-> Internal PHY for port 4
PHY address 5~d5	-> default for the external Port 5
PHY address 5~d5 ~ 5~d31	are free for the external PHY.

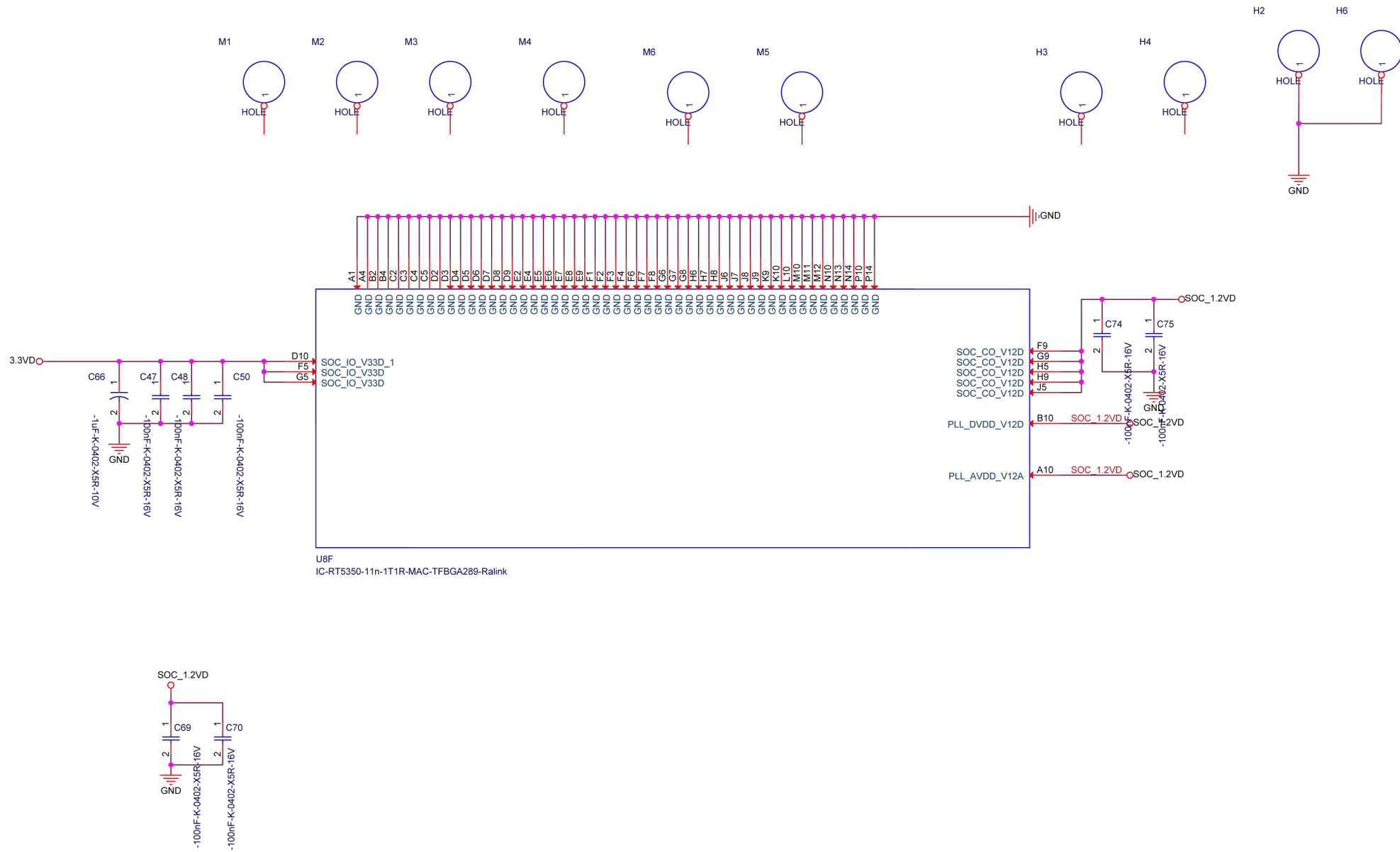
LDORF\_Out













(ANTENNA0)  
(TX0/RX0)

