L.S. RESEARCH Inc.

HIGH TECHNOLOGY ELECTRONIC CONSULTANTS

TEST REPORT:

Harris HFA3860 Processor

FCC 15.247(e) Jamming Margin Test

prepared for

Harris Corporation
Semiconductor Sector

November 15, 1999

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PROJECT INFORMATION

PROJECT: Harris PRISM HFA3860 Jamming Margin Test
                                  Margin Test

COMPANY CONTACTS: Carl Andren, Wireless Products Engineering
                                  John Fakatselis, Wireless Products Engineering
                                  2401 Palm Bay Road, N.E.
                                  MS:62A-024
                                  Palm Bay, FL 32905
                                  Phone (407)-724-7535
                                  FAX: (407)-724-7886

L.S. RESEARCH CONTACTS: Brian Petted, Vice President,.Engineering
                                  Bill Steinike, Business Manager
                                  Phone: (414) 375-4400
                                  FAX: (414) 375-4248
                                  R&D FAX: (414)-375-6731

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Signature Page:

Prepared By: ___Mr. Brian Petted___
               Vice-President of Engineering

Technical Approval By: ___Mr. Kenneth Boston, PE___
                        EMC laboratory manager

Special Note:

This report has been updated with revised measurement data. The original measurements showed that the processing gain for Channel 11 failed, due to excessive gain slope in the receiver. The problem had been corrected later and re-measured by the Harris Corporation, Semiconductor Sector with similar techniques. The measurement data in this report was supplied by Harris Corporation, Semiconductor Sector and is a measurement of the corrected RF assembly. An identical RF assembly is inserted as a subassembly in the product under test for type certification. The test data herein, reflects the performance of the RF assembly contained within the product under test.

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1.0 Scope

This report presents the test procedure, test configuration and test data associated with a FCC Part 15.247 (e) Jamming Margin test for the indirect measurement of processing gain. The report also outlines a modified test using a simulated frequency hopped interferer, as well as a broadband jamming test.

2.0 Applicable Reference Documents.

[1] "Operation within the bands 902-928 MHz, 2400-2483.5, and 5725-5850 MHz" *Title 47 Part 15 section 247 (e) Code of Federal Regulations*. **(47 CFR 15.247).**

[2] "Report and Order: Amendment of Parts 2 and 15 of the Commission's Rules Regarding Spread Spectrum Transmitters. Appendix C: 'Guidance on Measurements for Direct Sequence Spread Spectrum Systems" *FCC 97-114. ET Docket No. 96-8, RM-8435, RM-8608, RM-8609.*

[3] *"*The Treatment of Uncertainty in EMC Measurements" *NAMAS, NIS 81 Edition 1, May 1994. NAMAS Executive, National Physical Laboratory, Teddington Middlesex, TW11 0LW, England.*

[4] " HFA3860 Direct Sequence Spread Spectrum Baseband Processor" *Harris Corporation Semiconductor Sector Preliminary Data Sheet*, Melbourne FL, June 1997.

[5] " M-ary Orthogonal Keying BER Curve", *Communication from Harris Corporation to L.S. Research, Inc.*

[6] " Harris HFA3860 Processor FCC 15.247(e) Jamming Margin Test", *L.S. Research, Inc.,* January 14, 1998

3.0 Test Background and Procedure.

According to FCC regulations [1], a direct sequence spread spectrum system must have a processing gain, G_p of at least 10 dB. Compliance to this requirement can be shown by demonstrating a relative bit-error-ratio (BER) performance improvement (and corresponding signal to noise ratio per symbol improvement of at least 10 dB) between the case where spread spectrum processes (coding, modulation) are engaged relative to the processes being bypassed. In some practical systems, the spread spectrum processing cannot simply be bypassed. In these cases, the processing gain can be indirectly measured by a jamming margin test [2].

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The processing gain is related to the jamming margin as follows [2]:

$$G_p = BER_{REFERENCE} \leftrightarrow \left| \frac{S}{N} \right|_{output} + \left(\frac{J}{S} \right) + L_{system}$$

Where $BER_{REFERENCE}$ is the reference bit error ratio with its corresponding, theoretical output signal to noise ratio per symbol, $(S/N)_{output}$, (J/S) is the jamming margin (jamming signal power relative to desired signal power), and L_{system} are the system implementation losses.

The maximum allowed total system implementation loss is 2 dB.

The HFA3860 direct sequence spread spectrum baseband processor uses M-ary Bi-Orthogonal Keying. The BER performance curve is given by [5]:

" The probability of error for generalized M-ary Orthogonal signaling using coherent demodulation is given by:

$$P_e = 1 - P_{c1} = 1 - \frac{1}{\sqrt{2\pi}} \int_{-\frac{S_{01}}{N_0}}^{\infty} \left[2 \left(1 - Q \left(z + \sqrt{2 \frac{E_b}{\eta}} \right) \right) \right]^{\frac{M}{2} - 1} \exp \left\{ -\frac{z^2}{2} \right\} dz$$

This integral cannot be solved in closed form, and numerical integration must be used. This is done in a MATHCAD environment and is displayed in graphical format for M=2, 4, 8, and 16." (Shown on next page for M=16).

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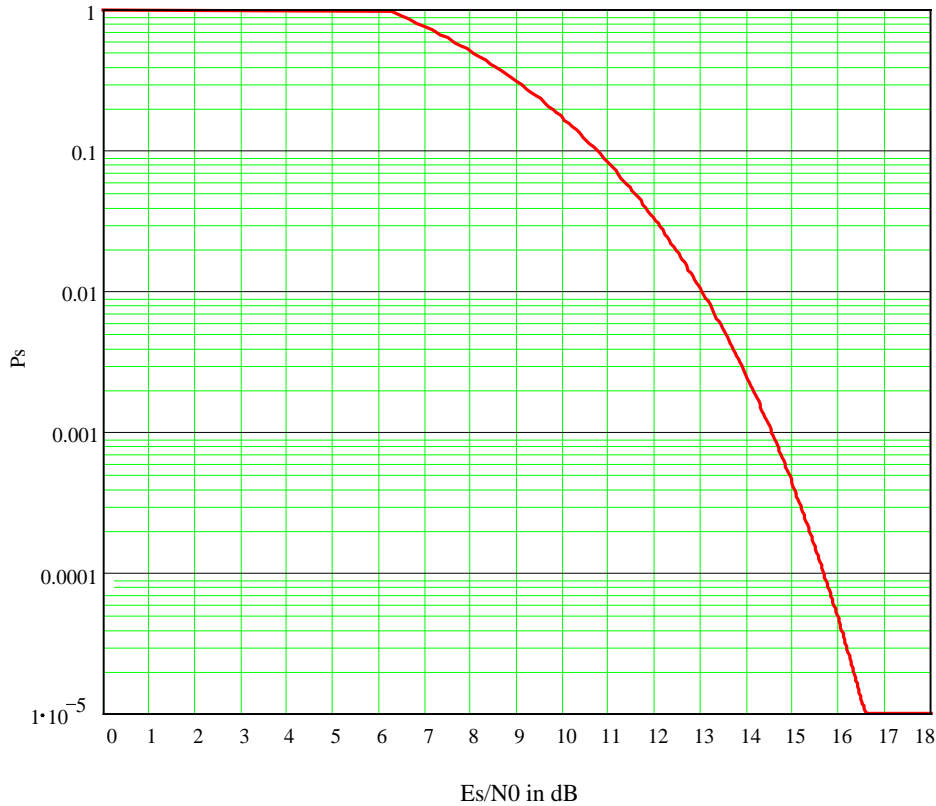
M=16 QMBOK Es/No

The reference BER is specified as $1 \cdot 10^{-5}$. The corresponding Es/No (signal to noise ratio per symbol) is 16.6 dB. The Es/No required to achieve the desired BER with maximum system implementation losses is 18.6 dB. The minimum processing gain is again, 10 dB, therefore:

$$G_p = \left|\frac{E_s}{N_o}\right|_{output} + \left(\frac{J}{S}\right) + L_{system} = 16.6\ dB + 2.0\ dB + \left(\frac{J}{S}\right) \geq 10 dB$$
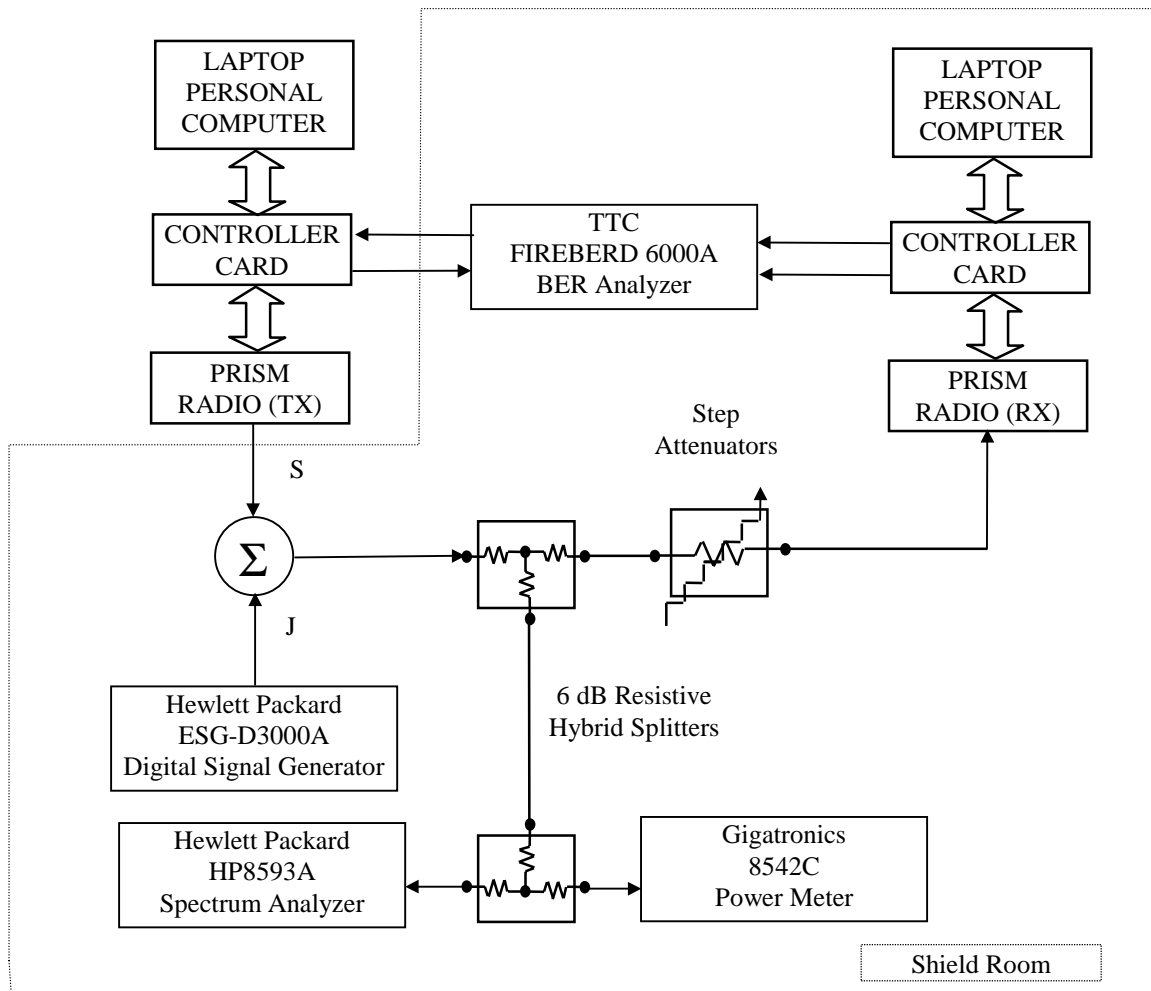
$$G_p = 18.6\ dB + \left|\frac{J}{S}\right| \geq 10 dB$$

The minimum jammer to signal ratio is as follows:

$$\left|\frac{J}{S}\right| \geq -8.6\ dB$$

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4.0 Test Configuration: CW Jamming Margin (15.247) (e)

4.1 Basic Test Block Diagram

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4.2 Test Procedure

4.2.1 Obtain the simplex link shown. Perform all independent instrumentation calibrations prior to this procedure. Set operating power levels using fixed and variable attenuators in system to meet the following objectives:

1. Signal Power at receiver approximately -60 dBm (above thermal sensitivity such that thermal noise does not cause bit errors).

2. Signal Power at power meter between -20 and -40 dBm for optimal linearity.

3. Use spectrum analyzer to monitor test.

4. Ensure that CW Jammer generator RF output is disabled and measure the power at the power meter port using the power meter. This is the relative signal power, S_r.

5. Disable Transmitter, and set CW Jammer generator RF output frequency equal to the carrier frequency and enable generator output. Set reference CW Jammer power level at power meter port 8.6 dB below S_r (minimum J/S, or 10 dB processing gain reference level). Note the power level setting on the generator, this is the reference CW Jammer power setting, J_r.

6. Disable CW Jammer, re-establish link. BER test set should be operating error-free.

7. Enable CW Jammer at a low power level and gradually increase the CW Jammer power until the BER test set indicates the reference BER level ($1 \bullet 10^{-5}$). Note nominal Jammer power setting, J_n.

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4.2.2 This test is repeated for a fixed signal carrier frequency and for uniform steps in frequency increments of 50 kHz across the receiver passband with the CW Jammer. In this case the receiver passband is ±8.5 MHz. The procedure can be illustrated as follows:

For offset frequency - 8.5 MHz to carrier frequency + 8.5 MHz , Step 50 kHz.
  Do:
  Adjust Nominal Jammer Level setting.
  Until:
  Average BER is equal to reference BER.
  Record Indicated Nominal Jammer Level setting.
Next offset frequency.

4.2.3 The nominal Jammer Level settings are tabulated versus offset frequency. The J/S ratio and the processing gain are then calculated as follows:

$$| \frac{J}{S} | = -\left[(S_r - J_n) - (S_r - 8.6 dB - J_r)\right]$$

If $J_n = J_r$ then:

$$| \frac{J}{S} | = -\left[8.6 dB\right]$$

is the J/S ratio associated with 10 dB processing gain.

4.2.4 The processing gain then is determined using the J/S ratio:

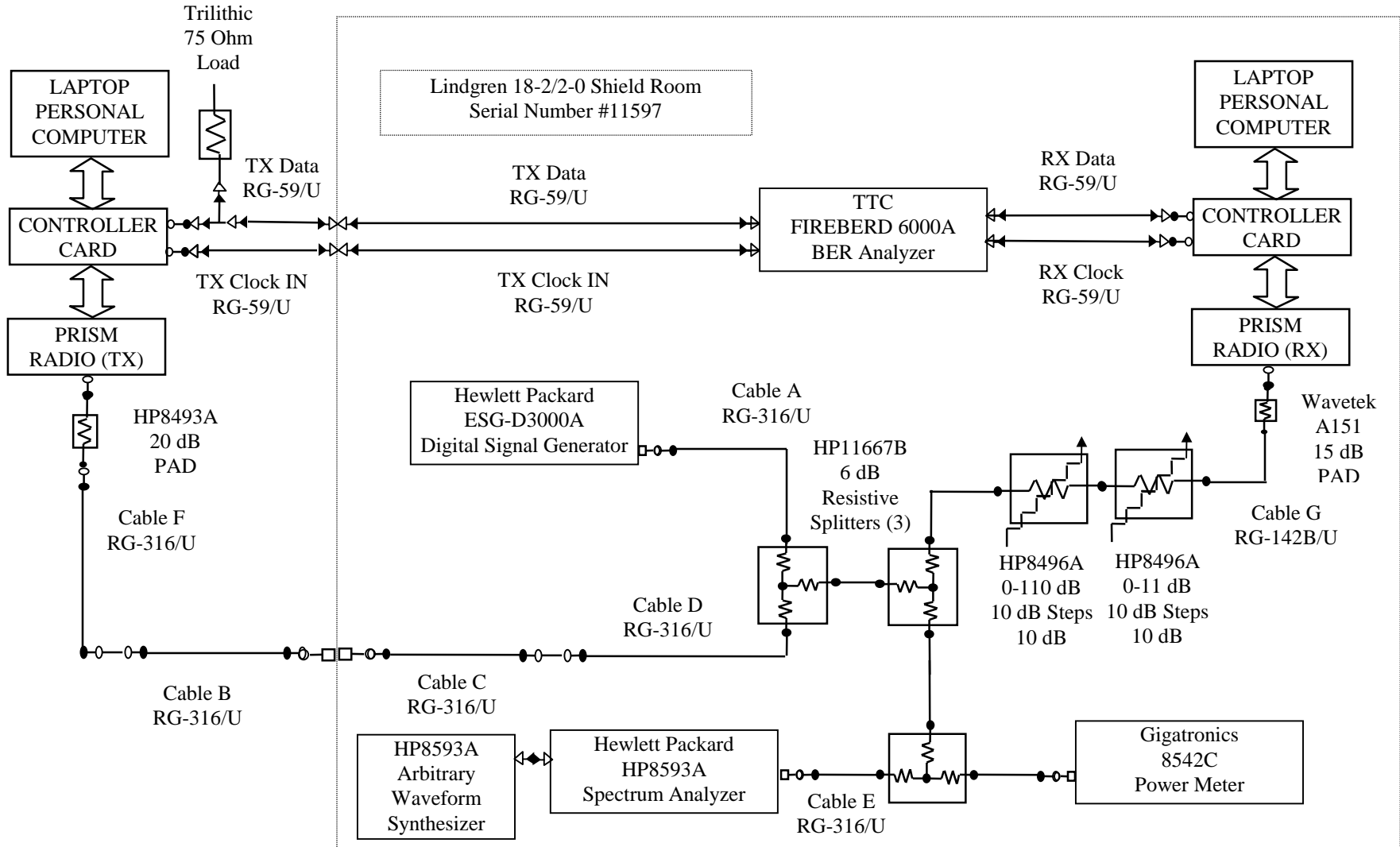$$G_p = 18.6\ dB\ +\ | \frac{J}{S} |$$

4.2.4 The numerical data associated with the following radio channels is tabulated and presented in Appendix A:

Channel 1: 2412 MHz   Table entries: Δf ,S_r,J_n,(J/S),G_p
Channel 6: 2437 MHz   Table entries: Δf ,S_r,J_n,(J/S),G_p
Channel 11: 2462 MHz   Table entries: Δf ,S_r,J_n,(J/S),G_p

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4.3 Test Electrical Configuration:

4.4   Measurement Equipment List

Equipment	LSR Serial No.	Serial Number	Calibration
HP8592E Spectrum Analyzer	CC00130C	3205A00103	Initial Only
Gigatronics 8542C Power Meter	EE960005	1831450	2/14/97
Gigatronics 86301A Sensor	-	1830164	2/5/97
TTC Fireberd 6000 BER Test Set Test Interval 10^7 Pattern: 2^23-1 External TX input	CC00164C	10016	11/29/96
HP ESG-D3000A (E4432) Signal Gen.	CC00162	US36260452	6/1/97
HP8496A Step Atten. 0-110 dB, 10 dB	-	-	CFE
HP8494A Step Atten. 0-11 dB, 1 dB	-	-	CFE
HP11667 Power Splitters (3)	-	08596,0627,09716	CFE
HP8493A Fixed Attenuator 20 dB	-	2708A	CFE
HP33120A Arbitrary Waveform Synthesizer	-	US34005826	Initial Only
Fixed Noise Source	CC00104C	-	NC

4.5 Measurement Uncertainties for Absolute Measurements

The measurement uncertainties are determined by the methods specified in NAMAS NIS 81, Edition 1, May 1994, "The Treatment of Uncertainty in EMC Measurements". Relanvant equipment specifications found in Appendix B.

Equipment	Specified Characteristic	Probability Density	Specified Uncertainty
HP8592E Spectrum Analyzer	Reference Level	Uniform	± 0.3 dB $+0.01 \bullet$ dB from -20 dBm
HP8592E Spectrum Analyzer	Calibrator Output	Uniform	± 0.4 dB
HP8592E Spectrum Analyzer	Absolute Amplitude Calibration Uncertainty	Uniform	± 0.15 dB
Gigatronics 86301A Sensor	Power Calibration Factor	Uniform	1.33 %
HP ESG-D3000A (E4432) Signal Gen.	Output Power	Uniform	± 0.9 dB

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HP Spectrum Analyzer Total Uncertainty (-60 dBm level):

Perform Root-Sum-Square of three uncertainties to find total uncertainty for a 95% confidence level:

Uniform uncertainties specify the probability density interval ±a. The variance of the uniform density is a/3.

Sum the uncorrelated variances to find the total variance:

Total variance = [(0.3 dB +0.01 • 40 dB)/3 +(0.4)/3+(0.15)/3] = 1.25/3 = 0.416

The uncertainty for a 95% confidence interval is 1.96 times the standard deviation:

Total Uncertainty = ±1.96 • √0.416 = 1.96 • 0.644 = ±1.26 dB

Gigatronics Power Sensor Power Calibration Factor Uncertainty:

Probable error in Power sensor: ±1.33% , ±10 log10 (1.0133) = ±0.0574 dB
Variance = 0.0574/3 =0.01913
Total uncertainty = ±1.96 • √0.01913 = ±0.27 dB

Signal Generator Output Power Uncertainty:

Level Accuracy = ±0.9 dB
Variance = 0.9/3 =0.3
Total uncertainty = ±1.96 • √0.3 = ±1.1 dB

5.0 CW Jamming Margin Test Data

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The tabulated numerical test data is presented in Appendix A. The numerical data is presented in graphical form here. Processing gain versus CW frequency Offset for Channels 1, 6, and 11 are presented. The measured relative signal power, reference jamming level, and reference jamming level setting are shown below for each channel:

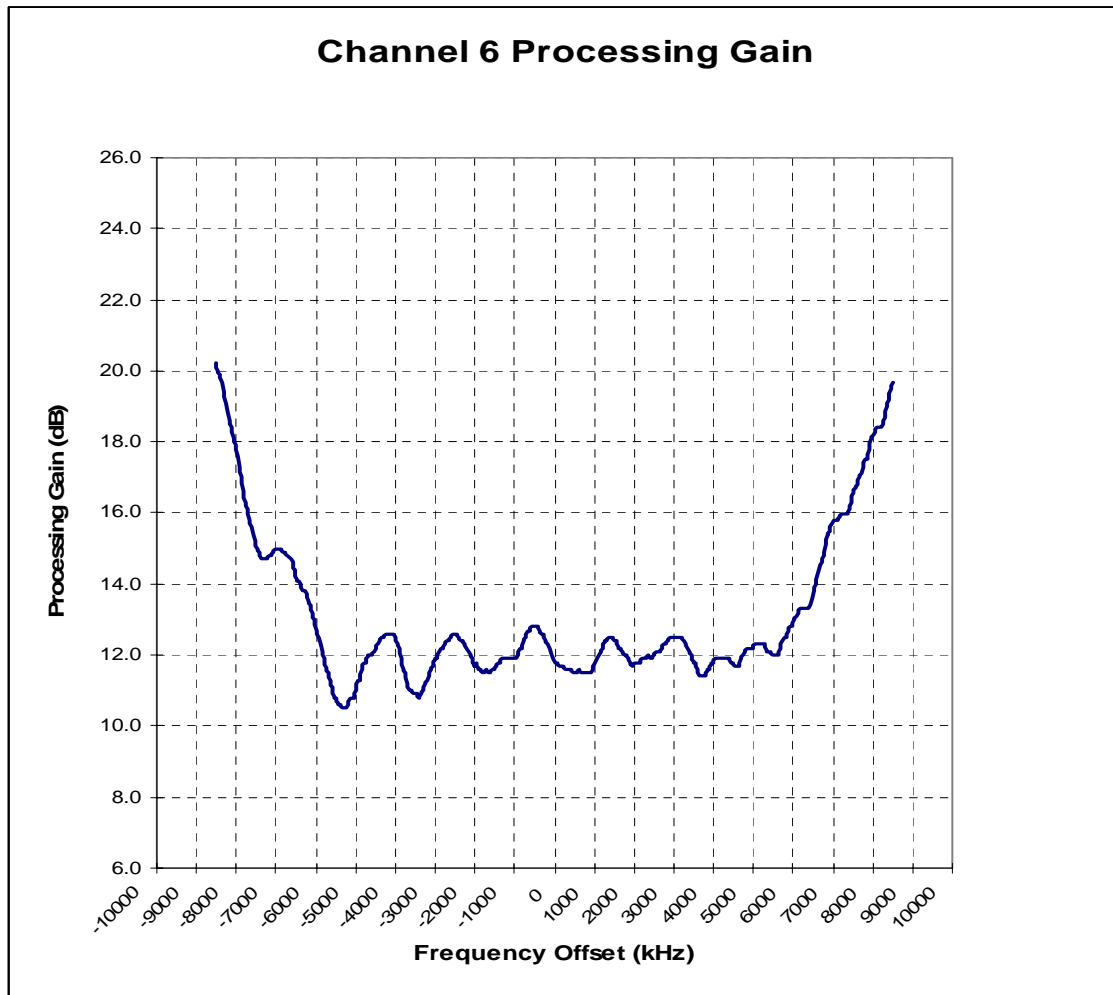|	Channel 1	Channel 6	Channel 11
Relative Signal Power , Sr	-28.1 dBm	-26.5 dBm	-28.7 dBm
Reference Jamming Level	-36.7 dBm	-35.1 dBm	-37.3 dBm
Reference Jamming Level Setting, Jr	-16.0 dBm	-14.5 dBm	-15.9 dBm

5.1 CW Jamming Test Data for Channel 1 (dB)

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The processing gain versus frequency offset from the carrier is presented below. The Jamming Margin test procedure [3] allows the worst 20% of the points to be discarded. The minimum processing gain is the minimum of the remaining points. The minimum of remaining points can be determined by calculating the upper bound of the 20% percentile of processing gain data. This number will be listed with the data and it represents the final compliance quantity.
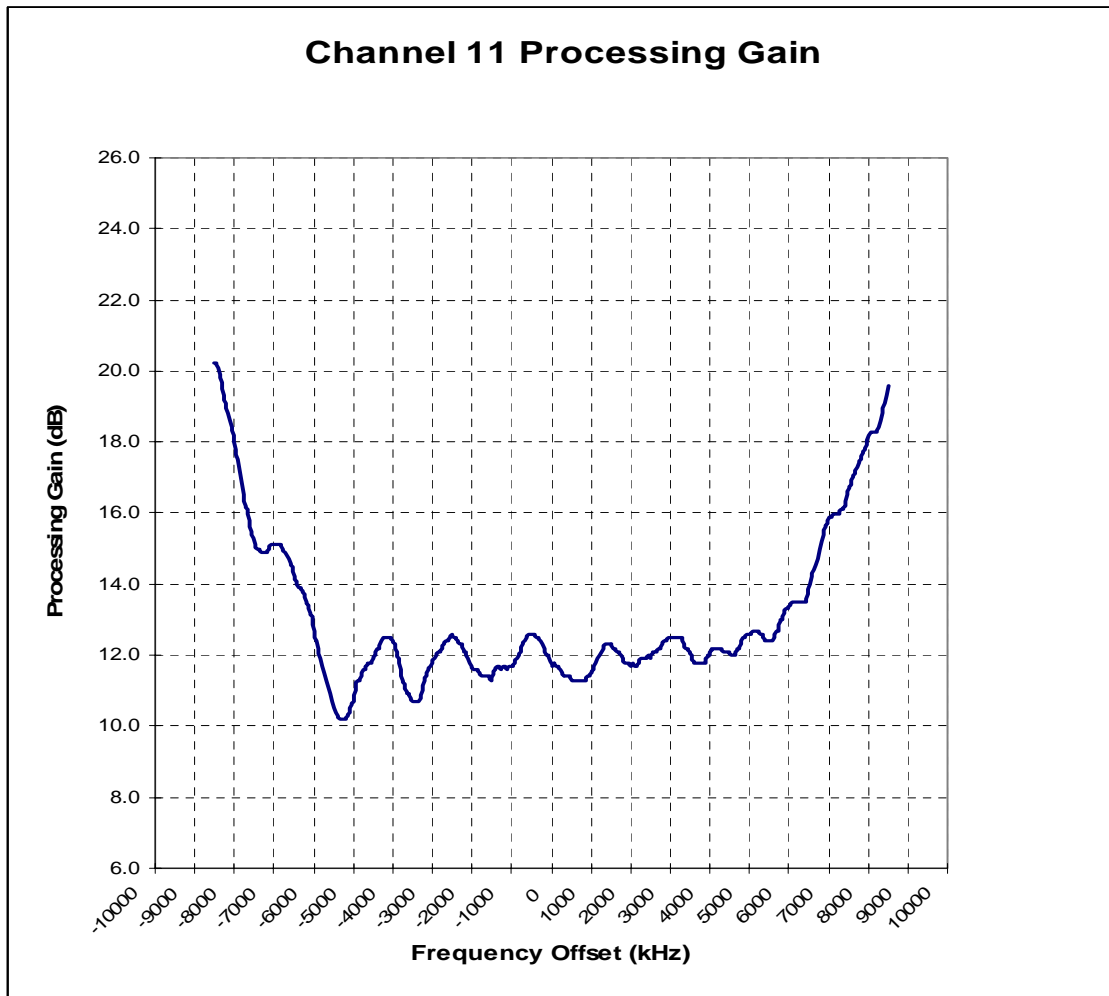

Channel 1 Processing Gain
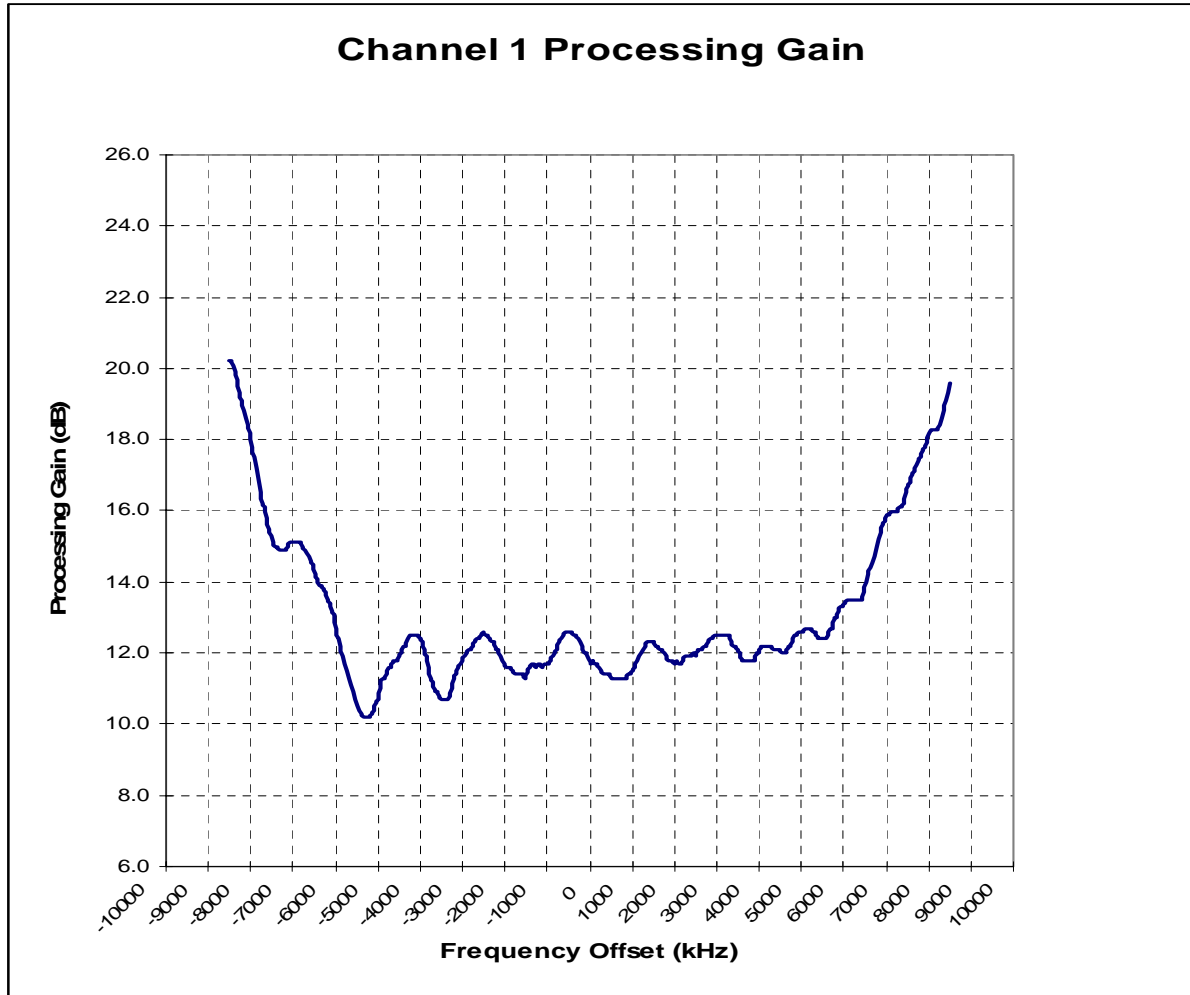
__The minimum processing gain with 20% worst points removed is 11.6 dB.__

5.2 CW Jamming Test Data for Channel 6 (dB)

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Channel 6 Processing Gain

The minimum processing gain with 20% worst points removed is 11.7 dB.

5.3 CW Jamming Test Data for Channel 11 (dB) :

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Channel 11 Processing Gain

The minimum processing gain with 20% worst points removed is 11.6 dB.

6.0 Analysis of Test Data

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The main conclusions associated with this set of tests are as follows:

1. The system passes the CW jamming margin test on Channel 1.
2. The system passes the CW jamming margin test on Channel 6.
3. The system passes the CW jamming margin test on Channel 11.

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