K&A WIRELESS, LLC

A subsidiary of ASSA Industries, LLC

VTRAN-2500 THEORY OF OPERATION

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Theory of Operation

The VTRAN-2500 is a digital, direct-sequence spread-spectrum (DS-SS) video transmission system. The system includes a transmitter and a receiver. The system is designed around the Harris PRISM chip set. The proprietary designs are the analog to digital and digital to analog converters that are used in the system. These boards are then integrated with the Harris PRISM chip set.

On the transmitter side, a standard video signal is obtained from a signal source. In our case, the source is a thermal imager in the shape of a camcorder. This video signal is digitized into an eight-bit parallel signal. In order to maintain the correct timing, this signal is sent to a frame buffer, which stores the information until the proper time. Once the correct timing is achieved, the signal is sent to a parallel to serial converter. This converts the parallel data stream into a single data stream. This data stream is formatted to be compatible with the Harris PRISM chip set.

Once the analog video is in the proper format, the signal is sent to the RF transmitter board. This board is based on the Harris PRISM chip set. During transmission, the data is sent to the baseband processor on the TX line (the PRISM chip set is a fully duplex solution). The data is then modulated into the differential quadrature phase shift keying (DQPSK) format. This provides a data rate of 2 MBPS. The data is then spread using the programmable PN code. There are two signals that are generated at this point (I and Q).

The I and Q signals are sent to the modulator, where the signal is filtered and then modulated with an IF frequency of 280 MHz. The two signals are then combined and sent to the up-converter. The up-converter shifts the IF frequency to one of the four channels that are programmed in the synthesizer. These frequencies are located within the 2.4-2.483 GHZ (ISM) band.

This signal is then passed through a power amplifier. The power amplifier produces an output power of ???mW, measured at the antenna.

On the receive side, the signal is obtained from the antenna and passed through a low-noise amplifier (LNA), which amplifies the low level signal. The signal is then passed through the down-converter and through the demodulator. Here there are two signals that have to be maintained, the I and Q. These signals are then passed through the baseband processor and demodulator, from the DQPSK format. The signal is then passed as a serial data stream to the Digital to Analog Converter board.

The analog converter converts the serial data to a parallel stream of data. This data is then triple buffered and converted to a standard analog signal using a D/A converter. From there the signal is displayed on a standard monitor.

The entire system is powered by two power supplies. The first is a linear regulator circuit that takes a given input voltage and outputs a regulated voltage. The second regulator circuit is used for the negative voltage required to bias the amplifier gate. This negative voltage is obtained using a voltage inverter.