4.6. *Processing Gain of A Direct Sequence Spread Spectrum, FCC CFR 47, Para. 15.247(e)*

PRODUCT NAME: OEM WLAN PC CARD 13316C, Model No.: GERSHWIN3

FCC REQUIREMENTS:

The processing gain of a direct sequence system shall be at least 10 dB. The processing gain shall be determined from the ratio in dB of the signal-to-noise ratio with the system spreading code turned off to the signal-to-noise ratio with the system spreading code turned on, as measured at the demodulated output of the receiver.

CLIMATE CONDITION:

Standard Temperature and Humidity: 21°C and 34%

POWER INPUT:

Using DC Power from a laptop computer.

TEST EQUIPMENT:

- Advantest Spectrum Analyzer, Model R3271, S/N: 15050203
- 3dB & 40 dB Attenuators, 50 Ohm IN/OUT
- Fluke RF Signal Generator, Model 6061A, Freq. range: 10 KHz - 1050 MHz.
- HP 8900 RF Peak Power Meter, Measuring Frequency Range: 100 MHz - 18 GHz.
- Bert Fireberd 4000 Communication Analyzer

METHOD OF MEASUREMENT:- **Jamming Margin Method**

The processing gain may be measured using the CW jamming margin method. Figure 1 shows the test configuration. The test consists of stepping a signal generator in 50 KHZ increments across the passband of the system. At each point, the generator level required to produce the recommended Bit Error Rate (BER) is recorded. This level is jammer level. The output power of the transmitting unit is measured at the same point. The Jammer to Signal (J/S) ratio is then calculated. Discard the worst 20% of the J/S data points. The lowest remaining J/S ratio is used when calculating the Process Gain.

The signal to noise ratio for an ideal differentially coherent detetion of a differentially encoded DPSK receiver can be derived from the Bit Error Probability (Pb) versus Signal-to-Noise ratio. See attached plot for detailed information.

For measurement of the $(S/N)_o$ we use the Pb of $1.0x10^{-5}$ minimum.

Ref.: Viterbi, A.J. Principles of Coherent Communications (New York: McGraw-HILL 1966), Pg. 207

Using equation (1) shown above, calculate the signal to noise ratio required for your chosen BER. This value and the measured J/S ratio are used in the following equation to calculate the Process Gain (Gp) of the system.

$$Gp = (S/N)o+Mj+Lsys$$

Where:

(S/N)o: Theoretical signal to noise ratio required to maintain the normal operation just before the BER appears. In real measurements the maximum error of 0.001 is allowed in an ideal system using their modulation scheme with all codes turned off (i.e. no spreading or processing gain).

Mj: Maximum jammer to Signal Ratio that recorded at the detected BER.

Lsys: System losses such as non-ideal synchronization, tracking circuitry, non-optimal baseband receiver filtering and etc... These losses can be in excess of 3 dB for each transmitter and receiver pair. For the purpose of this processing gain calculation we assume a Lsys at its minimum value of 3 dB.

Ref.: Dixon, R. Spread Spectrum Systems. (New York: Wiley, 1984), Chapter 1.

TEST RESULTS:

Conforms.

TEST PERSONNEL:

Tri M. Luu, P.Eng.

DATE:

Oct. 17, 1997

MEASUREMENT DATA:

Test Method Employed: Jamming Margin

SIG. GEN. FREQ. (MHz)	BER	(S/N)o (dB)	Lsys (dB)	Sig. Gen. Total Peak Power @ Rx (dBm)	Transmitter Total Peak Power @ Rx (dBm)	Jammer to Signal Ratio Mj (dB)	Processing Gain (dB)
Fc - 1.00	0.000020	9.6	2.0	-24.5	-27.9	3.4	15.0
Fc - 0.90	0.000013	9.8	2.0	-24.4	-27.9	3.5	15.3
Fc - 0.70	0.000010	9.9	2.0	-25.9	-27.9	2.0	13.9
Fc - 0.50	0.000015	9.8	2.0	-26.7	-27.9	1.2	13.0
Fc - 0.45	0.000018	9.7	2.0	-26.0	-27.9	1.9	13.6
Fc - 0.40	0.000015	9.8	2.0	-26.2	-27.9	1.7	13.5
Fc - 0.35	0.000012	9.9	2.0	-26.6	-27.9	1.3	13.2
Fc - 0.30	0.000015	9.8	2.0	-26.9	-27.9	1.0	12.8
Fc - 0.25	0.000018	9.7	2.0	-27.6	-27.9	0.3	12.0
Fc - 0.20	0.000011	9.9	2.0	-27.7	-27.9	0.2	12.1
Fc - 0.15	0.000016	9.8	2.0	-28.0	-27.9	-0.1	11.7
Fc - 0.10	0.000020	9.6	2.0	-28.4	-27.9	-0.5	11.1
Fc - 0.05	**0.000010**	**9.9**	**2.0**	**-29.2**	**-27.9**	**-1.3**	**10.6**
Fc	0.000020	9.6	2.0	-27.8	-27.9	0.1	11.7
Fc + 0.05	0.000010	9.9	2.0	-27.9	-27.9	0.0	11.9
Fc + 0.10	0.000020	9.6	2.0	-27.8	-27.9	0.1	11.7
Fc + 0.15	0.000017	9.7	2.0	-27.9	-27.9	0.0	11.7
Fc + 0.20	0.000015	9.8	2.0	-26.9	-27.9	1.0	12.8
Fc + 0.25	0.000010	9.9	2.0	-26.2	-27.9	1.7	13.6
Fc + 0.30	0.000010	9.9	2.0	-25.8	-27.9	2.1	14.0
Fc + 0.35	0.000012	9.9	2.0	-25.0	-27.9	2.9	14.8
Fc + 0.40	0.000013	9.8	2.0	-24.7	-27.9	3.2	15.0
Fc + 0.45	0.000014	9.8	2.0	-25.3	-27.9	2.6	14.4
Fc + 0.50	0.000020	9.6	2.0	-25.5	-27.9	2.4	14.0
Fc + 0.70	0.000015	9.8	2.0	-25.2	-27.9	2.7	14.5
Fc + 0.90	0.000016	9.7	2.0	-24.6	-27.9	3.4	15.1
Fc + 1.00	0.000013	9.8	2.0	-24.9	-27.9	3.0	14.8
MINIMUM PROCESSING GAIN: 10.6 dB							

- (S/N)o: Refer to attached curves, BER versus (S/N)o for Differiential Coherent Detection of Differientially Encoded DPSK
- Processing gain Gp = (S/N)o + Lsys + Mj = (S/N)o + 2 Mj

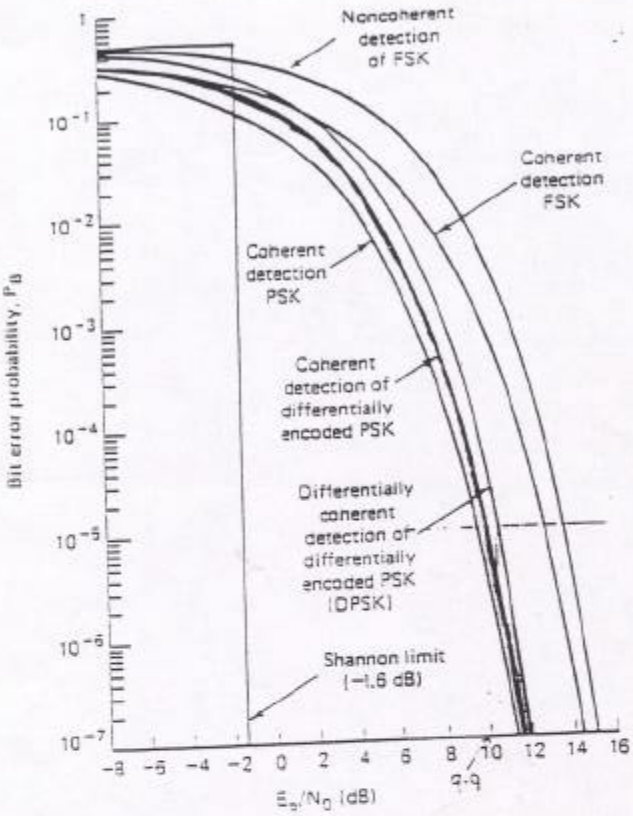


Figure 3.22 Bit error probability for several types of binary systems.

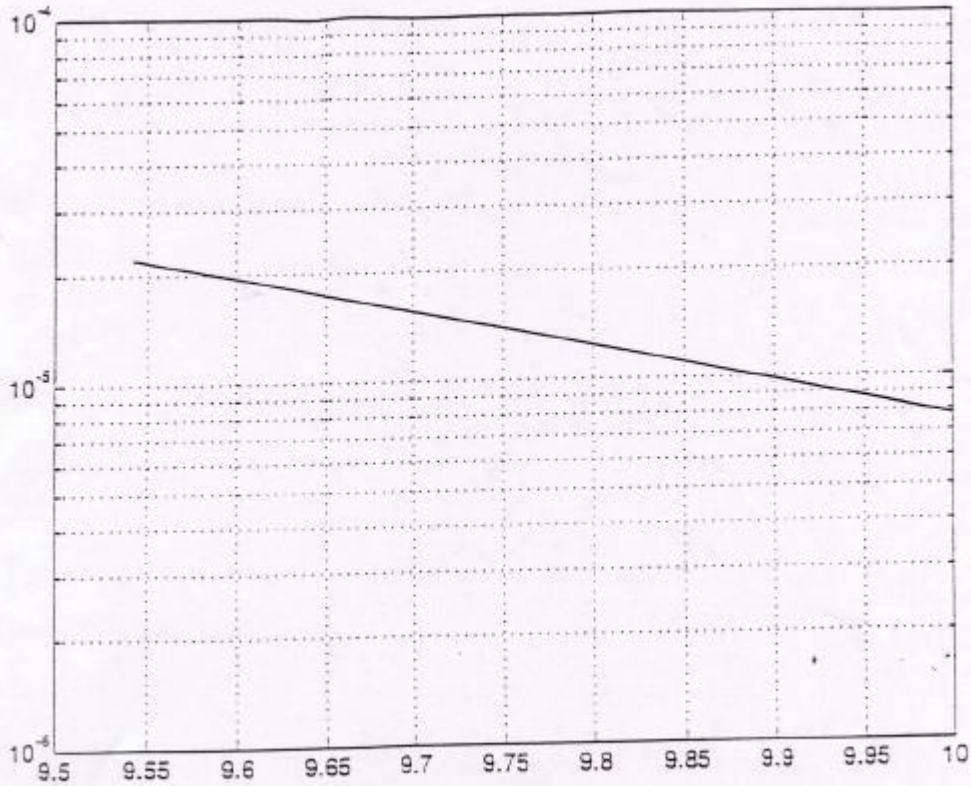
3.7.2 Probability of Bit Error for Coherently Detected Differentially Encoded PSK

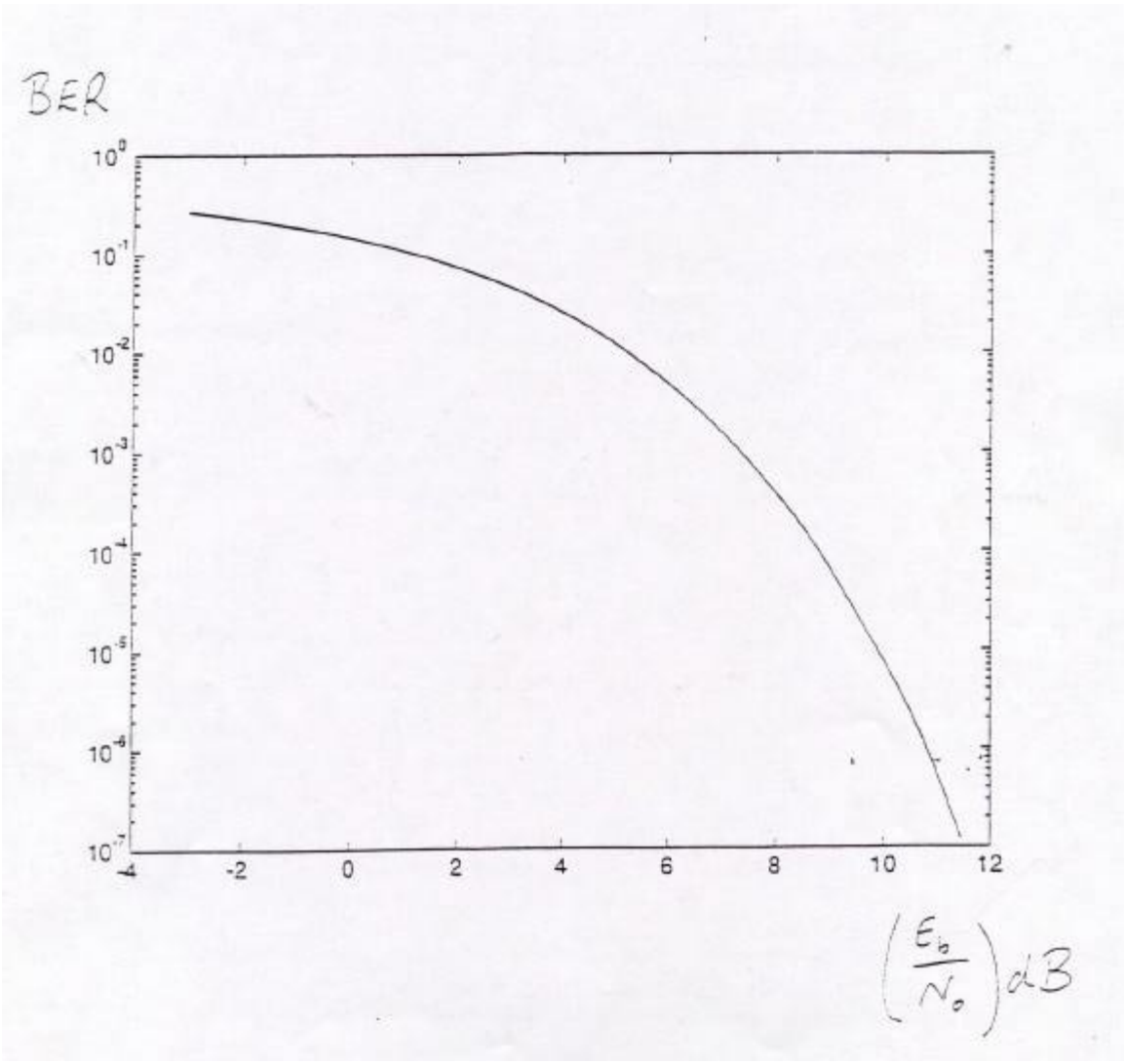
Channel waveforms sometimes experience inversion; for example, when using a coherent reference generated by a phase-locked loop (see Chapter 8), one may have phase ambiguity. If the carrier phase were reversed in a DPSK modulation application, what would be the effect on the message? The only effect would be an error in the bit during which inversion occurred or the bit just after inversion, since the message information is encoded in the similarity or difference between adjacent symbols. The similarity or difference quality remains unchanged if the carrier is inverted. Sometimes, systems are *differentially encoded* and *coherently detected*, simply to avoid these phase ambiguities.

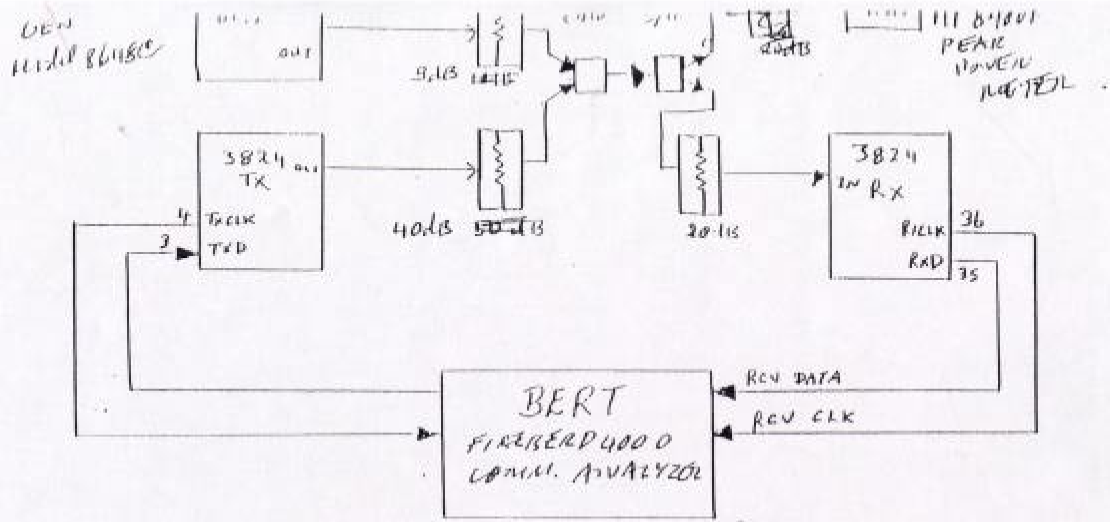
The probability of bit error for coherently detected, differentially encoded PSK is given by [7]

$$P_B = 2Q\left(\sqrt{\frac{2E_b}{N_0}}\right)\left[1 - Q\left(\sqrt{\frac{2E_b}{N_0}}\right)\right]$$

BER


10^{-4}
10^{-5}
10^{-6}
9.5
9.55
9.6
9.65
9.7
9.75
9.8
9.85
9.9
9.95
10
$\left(\frac{E_b}{N_o}\right)$ dB


BER
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
-4
-2
0
2
4
6
8
10
12
$\left(\frac{E_b}{N_o}\right)$ dB



1) Set MAC chip to continuous transmit in the transmit end. This guarantees that TX_PE (Pin 2 on 3824 TX) is set active and DATA will be clocked in from BERT.

2) Set MAC chip to continuous Receive at the Receive end. This guarantees that RX_PE is enabled and the receiver is operational.

1) Set up BERT to work with UNIPOLAR UNBALANCED sign (use the MODE switch)

2) Set Input Impedance to 8K (check with oscilloscope to make sure the wrong reflections are not degrading BER)

3) CLK PHASING switch: Use both (A) TX ↑ RCV ↑

4) PATTERN TO USE: Pseudorandom $2^{20}-1$ or $2^{23}-1$

Synchronization declared when 30+n consecutive error free bits received = 50 or 53

THEORETICAL PROCESSING GAIN

The table below represents the symbol rate, chip rate, and theoretical processing gain for the aforementioned EUT.

Data Rate (Mbps)	Symbol Rate (MSps)	Chip Rate (MCps)	Chip/Symbol Rate	Es/No (dB)	J/S (dB)
1	1	11	11:1	10.3	-2.3
2	1	11	11:1	13.3	-5.3
5.5	1.375	11	8:1	13.4	-5.4
11	1.375	11	8:1	16.4	-8.4