Block Diagram STARGATE RF910MHz BASE STATION

Author: Datalogic

STARGATE RF910MHz: FUNCTIONAL DESCRIPTION AND BLOCK DIAGRAMS

Functional blocks description with reference to page 3/4/5 block diagrams:

Main Processor
It's a 16 bits embeeded Microprocessor (Mitsubishi 37733) with internal Flash and Ram memories. Static Ram: 128 kB. Flash memory: 128kB
It runs at 12 Mhz. This processor moves data between other blocks and controls block funtionality.

Radio Transceiver
Receives and transmit data packets at 36864 baud Manchester encoded.
Tx Power out (50 Ohm) + 0 dBm typ.
Tx FM deviation = 45 KHz typ.

State Indicators
One led using red, orange and green colors.

Antenna
StarGate has an external antenna not removable.

UART
Two external UART (16550) which drives respectively the Radio Transceiver and the 232/485 input-output interface. It's frequency work is 3.6864 MHz.

PIC
Programmable OTP microcontroller which converts uart NRZ (start+data+stop) bits into radio output Manchester RZ data bits. It works at 3.6864 MHz.

Power Supply (Step Down)
No batteries.
Supplies 9-30 Vdc. It sources 70 mA.
An interface reset button is included.

Multiinterface
Transmit and received the data via RS232 and RS485 interface.

Clock sources description

12.00 MHz Quartz Crystal	Main Microprocessor Clock	(onto GEL-4734)
3.6864 MHz Ceramic Resonator	Microcontroller + UART	(onto GEL-4734)
3.6864 MHz Ceramic Resonator	UART	(onto GEL-2372)

Radio transmitter/ receiver:

X1: 14.21875MHz	XTAL TX
X2: 14.05160MHz	XTAL RX

RF suppression devices:

On dc power input:

N.2 inductor 1uH	TDK NCL453232T-1R0K
N.2 ferrite bead	TDK ZBFS5101

N.2 capacitors X7R C=220nF
N.1 capacitors 2F4 C=100nF

On 232 interface port:
N.4 ferrite bead MURATA BLM21A601S

On 485 interface port:
N.2 ferrite beads MURATA BLM21A601S

STARGATE BLOCK DIAGRAMS

Fig. 1 - Block Diagram of the Connections inside STARGATE RF910MHz BASE STATION and Printed Circuit Boards.

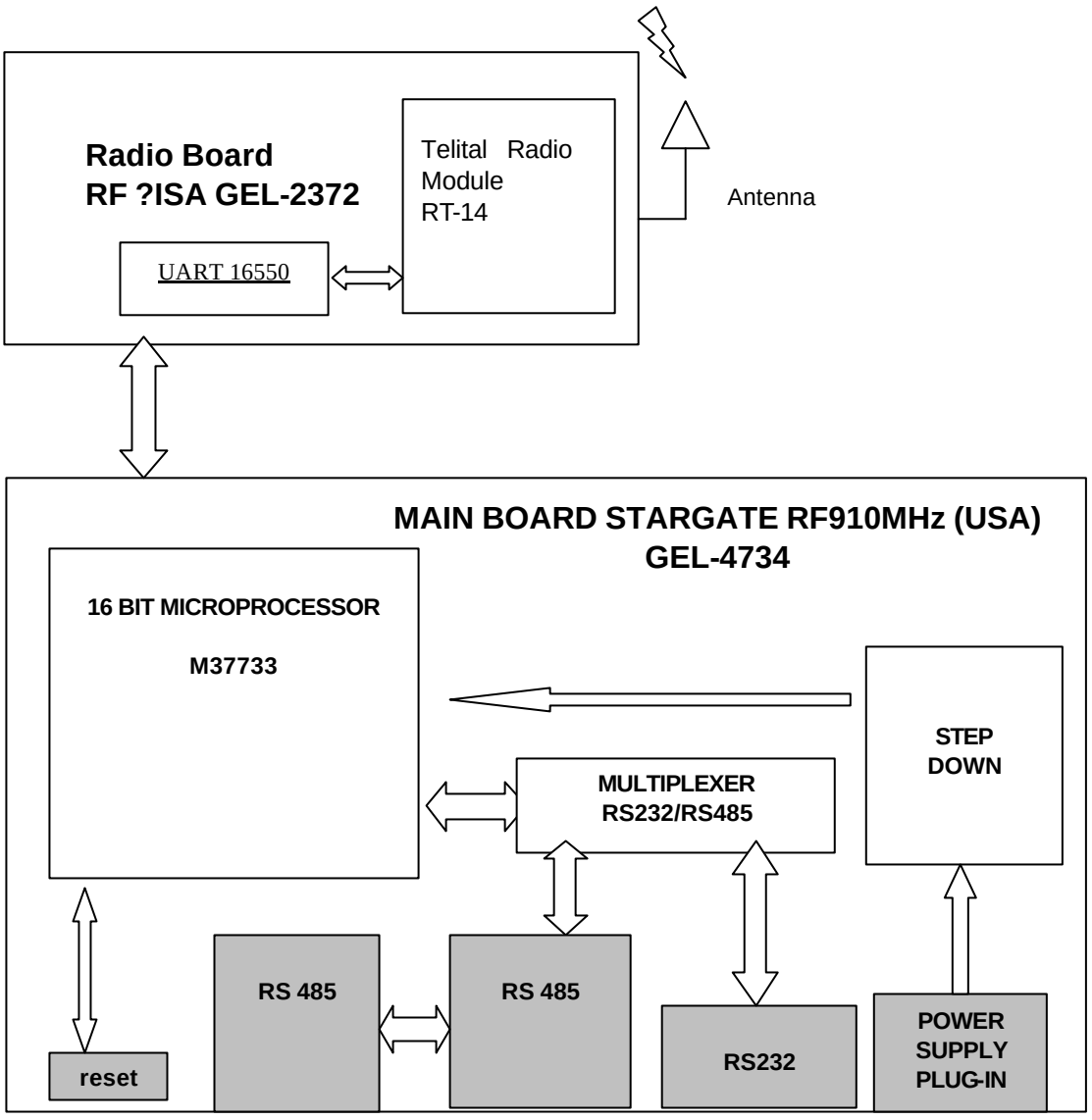

Fig. 2 - Block Diagram of the EUT

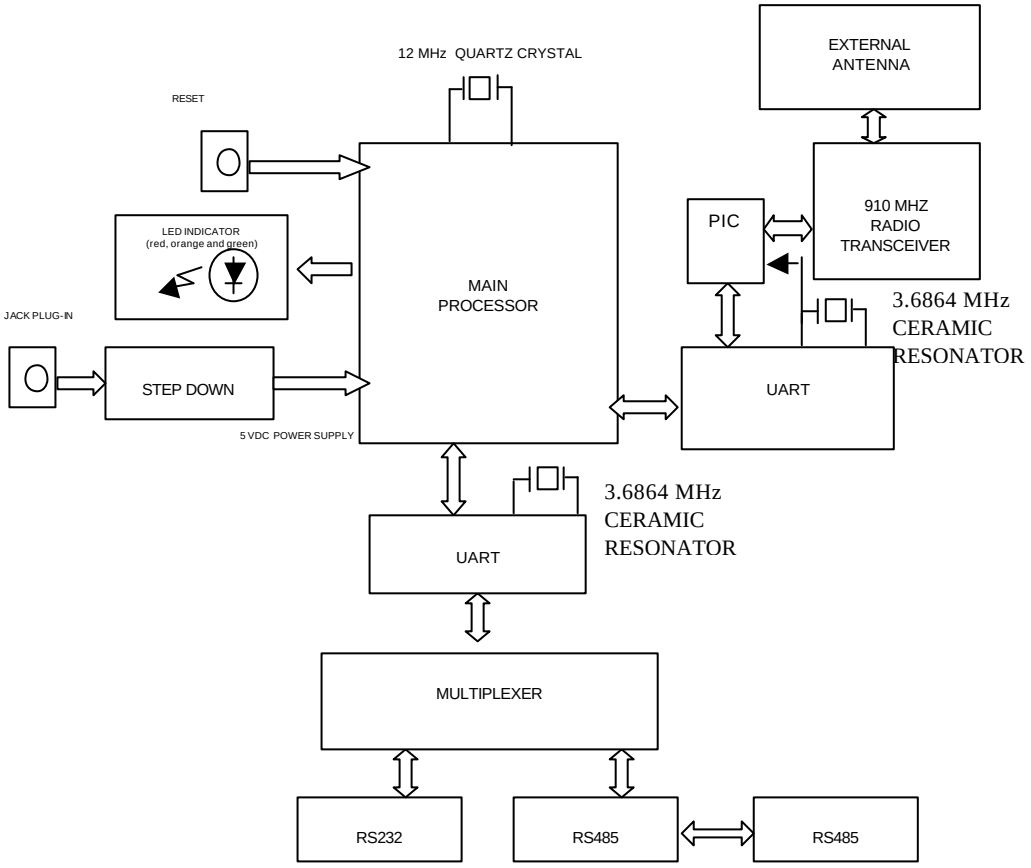

Fig. 3 - Block Diagram of Transceiver