Theory of Operation: Quick Pitch Interface Control:

Interface Control - Parent Circuit:

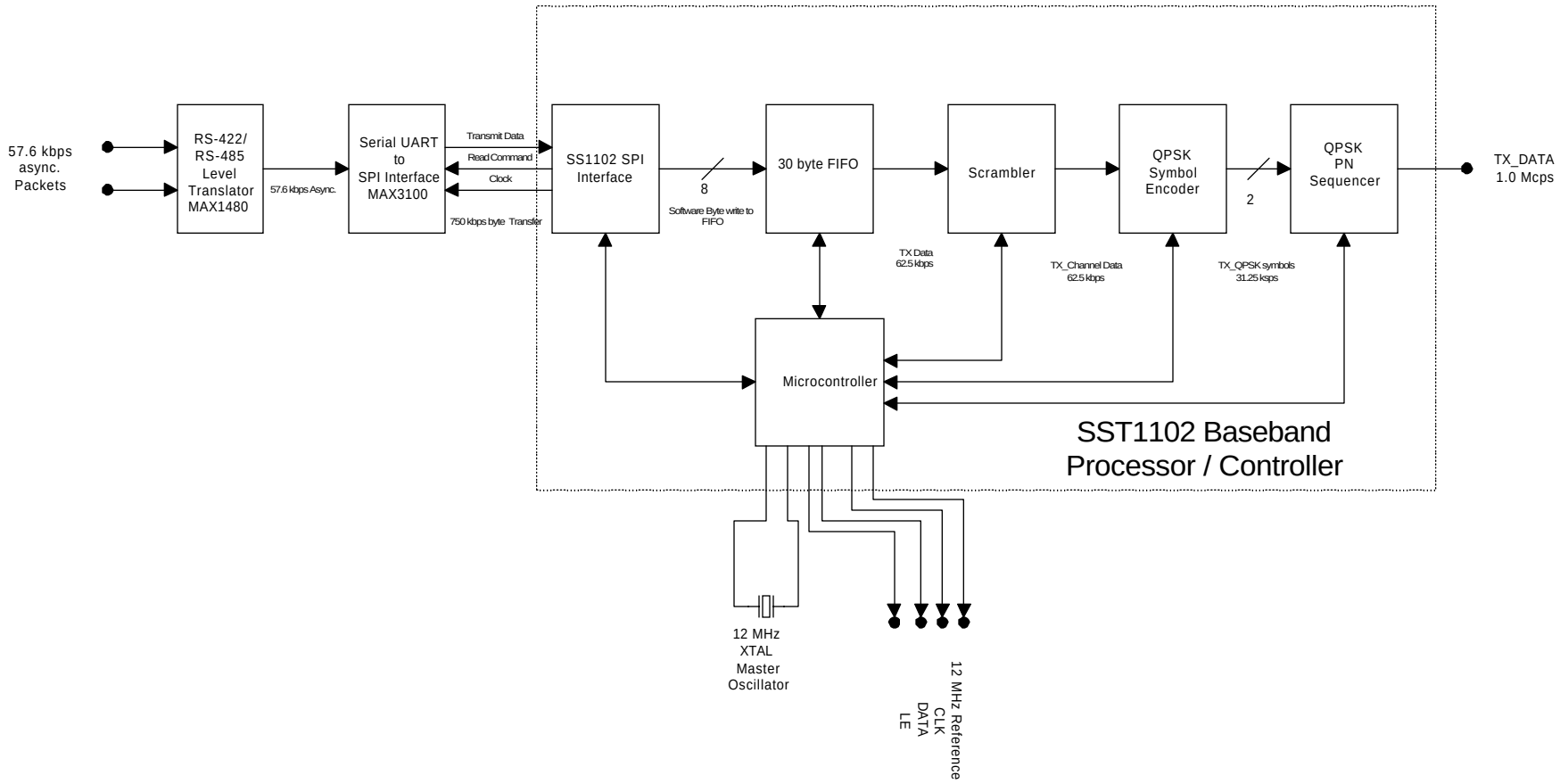
The interface control accepts data supplied by an array of third party external devices, makes logical decisions about the data, and outputs the data in a format compatible to a large area display. Data is received from the external devices as a TTL level signal or as a RS232 serial signal. The interface control includes a microcontroller that inspects the data for validity. If the data is determined to be valid, the data is then output in a proprietary RS422/RS485 format to the large area display. Data is sent to the display in one or two forms: 1) Data is output directly via shielded control cable, or 2) Data is communicated to the optional RF transmitter which subsequently outputs this "payload" data.

Optional RF Transmitter:

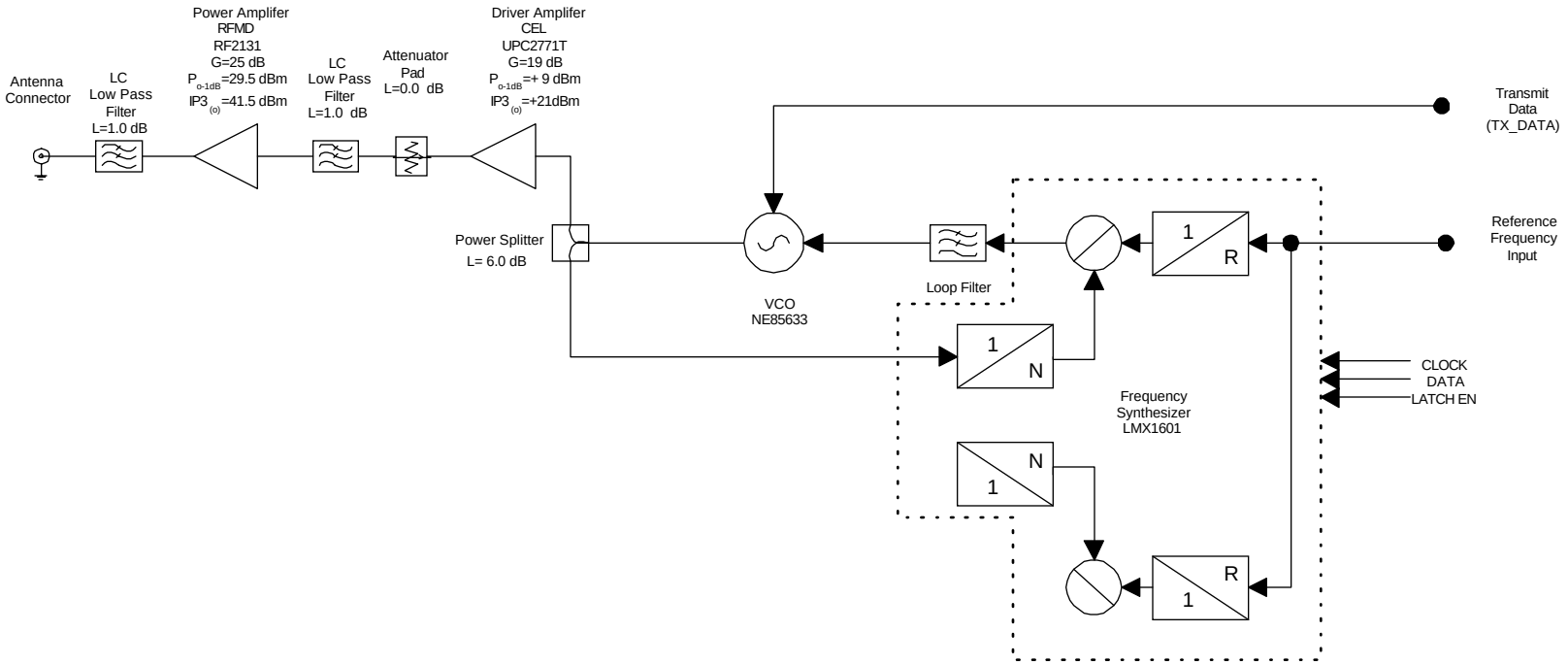
The transmitter baseband processor accepts the proprietary interface control payload data packets which vary from 14 to 126 bytes in length. The data is transmitted asynchronously at 56.7 kilobits per second and uses 20 millisecond idle periods for packet frame delimiting. The baseband subsystem performs level translation from RS-422/RS-485 differential levels to CMOS logic levels. The data is presented to a UART/ Serial Peripheral Interface (SPI). Bytes are transferred synchronously in a bursty fashion at a 750 kbps rate to the baseband processor SPI. The data byte is then transferred via a software register write to a 30 X 1 byte FIFO. The fill level of the FIFO is controlled by the microcontroller. The FIFO is emptied by shifting out each byte serially at a rate of 62.5 kbps. The payload is framed by a 32 byte preamble and 3 byte unique word.

The data is then scrambled for security and spectral whiteness (ensures that output spectrum is not dependent on input data, in the case of longs strings of ones and zeros). The data bits are paired into even and odd paired 2-bit symbols. These symbols serve as selectors for initiating the transmission of one-of-four 32 chip pseudorandom sequences (Gold Codes) at a symbol rate of 31.25 ksps. This results in a physical channel output data (chipping) rate of 1 Mcps.

A block diagram of the RF transmitter subsystem is presented below. The transmitter is a direct modulation with a phase-locked agile (tunable) local source. The VCO is directly modulated with the PN encoded Transmit data. The VCO output is amplified and filtered to produce the desired transmit signal.



Transmitter Baseband Block Diagram



Transmitter RF Block Diagram