NOTE ON THE SCHEMATICS

 The RF Module is normally shown on the schematic itself as an IC with the input and output pins being shown on the Module going to other circuitry and/or components.

For this Module, the pins are as follows (pin 1 is the upper left corner and pin 11 is the lower right corner)

Left hand side of the Module:
1. GND
2. DATA OUT
3. AUDIO
4. RSSI
5. PDN
6. LD
7. RX-TX SEL
8. GND
9. TXDATA
10. VIN

For the right hand side of the Module:
11. (pin for the output connector)
12. (pin for the output connector)
13. (pin for the output connector)
14. LEV ADJ
15. GND
16. CH SEL 0/UDATA
17. CH SEL 1/UCLOCK
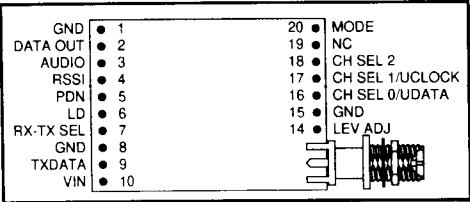18. CH SEL 2
19. NC
20. MODE

PIN DESCRIPTION


```
GND      ● 1        20 ●  MODE
DATA OUT ● 2        19 ●  NC
AUDIO    ● 3        18 ●  CH SEL 2
RSSI     ● 4        17 ●  CH SEL 1/UCLOCK
PDN      ● 5        16 ●  CH SEL 0/UDATA
LD       ● 6        15 ●  GND
RX-TX SEL● 7        14 ●  LEV ADJ
GND      ● 8
TXDATA   ● 9
VIN      ● 10
```

Figure 5: MC Series Pinouts (viewed looking down on top cover)

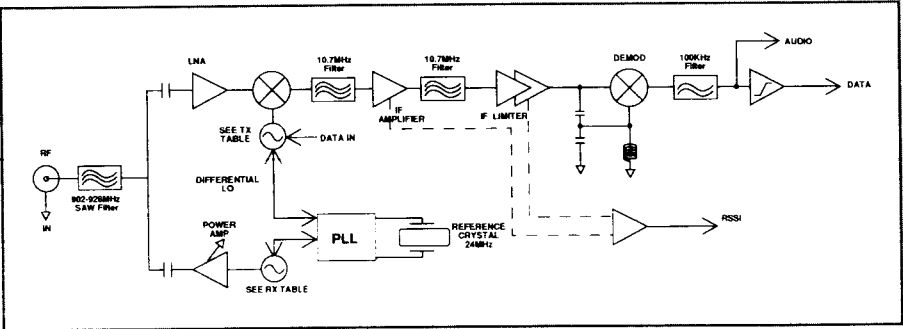| PIN#	PIN TITLE	EQUIVALENT CIRCUIT	DESCRIPTION
1, 8, 11, 13, 15	Ground		MODULE GROUNDS Tie to common groundplane
2	RXDATA		RECOVERED DATA OUTPUT
3, 19	N/C		NO CONNECTION
4	RSSI		RECEIVED SIGNAL STRENGTH INDICATOR
5	PDN		POWER DOWN Logic low powers down the transceiver
6	LOCKDET		LOCK DETECT Indicates PLL lock Use as CTS in TX
7	RX/TX SELECT		RX/TX SWITCH Open, or internally pulled high for RX pull low for TX
9	DATA IN		SERIAL DATA INPUT
10	VIN		SUPPLY VOLTAGE 2.7-12VDC
12	ANT		50Ω ANTENNA PORT TX/RX switched inside module
14	LEV ADJ		LEVEL ADJUST Open for maximum power Insert resistor to lower over 20db range
16	CH SEL0/UDATA		CHANNEL SELECT 0 / USER DATA Binary channel select 0 in parallel mode User data in serial mode
17	CH SEL1/UCLOCK		CHANNEL SELECT 1 / USER CLOCK Binary channel select 1 in parallel mode User clock in serial mode
18	CH SEL 2		CHANNEL SELECT 2 Binary channel select 2 in parallel mode Not used in serial mode
20	MODE		MODE SELECT Internally pulled up Leave open or high for serial channel mode Ground for parallel selection

Figure 6: MC Series Block Diagram

DESCRIPTION

The TC-900-MC-PA module is a multi-channel, half-duplex transceiver designed for the transmission of digital data wirelessly at distances of <500 feet outside and <200 feet inside. No external components (excluding an antenna) are required. The module incorporates on-board switch allowing the use of a single antenna. Linx offers a wide selection of antennas designed for use with the transceiver module. The PA version has been pre-certified by the FCC which greatly reduces the time to market and cost of product introduction.

The transceiver is half-duplex. Therefore, it can only be operated in one mode at a time: either transmit mode or receive mode. When transmitting, the receiver is powered down. Likewise, the transmitter is powered down in receive mode.

The TC-900-MC-PA incorporates a precision Low-Dropout Regulator on-board which allows the module to operate over an input voltage range of 2.7 to 16 volts DC. An on-board micro-controller reads the channel-selection lines and programs the PLL to the desired channel frequency. The MC-PA allows parallel selection from eight channels. For greater flexibility the MC-PA features a serial mode for selection from 250 channels. In this mode the desired channel is programmed via a single eight-bit word. The micro-controller also monitors the status of the PLL and indicates when the transmitter is stable and ready to transmit data by raising the Lock Detect (LD) line high.

TRANSMITTER OPERATION

The transmit section of the transceiver is capable of producing up to 1mW of output power while maintaining harmonics and spurious emissions within legal limits.

The transmitter is comprised of an LO and crystal-controlled frequency synthesizer. The frequency synthesizer phase locks the LO to a precision crystal to achieve a high-Q, low phase-noise oscillator. An accurate 24.00MHz VCXO (voltage-controlled crystal oscillator) serves as the frequency reference for the transmitter. The modulated 24.00MHz reference frequency is applied to the Phase-Locked Loop (PLL). The PLL, combined with a 902-928MHz VCO, forms a stable frequency synthesizer that can be programmed to oscillate at the desired transmit frequency.

An on-board micro-controller reads the channel-selection lines and programs the