NoWiresNeeded

Processing Gain - Theoretical calculations

The processing gain is related to the jamming margin as follows [2]:

$$G_p = \left(\frac{S}{N}\right)_{output} + \left(\frac{J}{S}\right) + L_{system}$$

Where $BER_{REFERENCE}$ is the reference bit error ratio with its corresponding, theoretical output signal to noise ratio per symbol, $(S/N)_{output}$, (J/S) is the jamming margin (jamming signal power relative to desired signal power), and L_{system} are the system implementation losses.

The maximum allowed total system implementation loss is 2 dB.

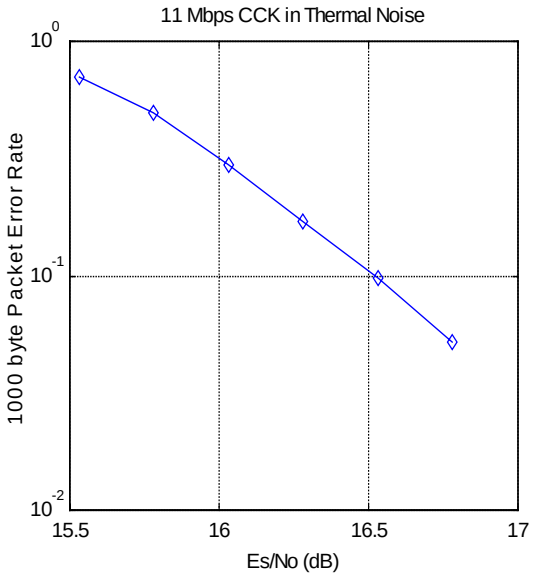
The HFA3861A direct sequence spread spectrum baseband processor uses CCK modulation which is a form of M-ary Orthogonal Keying. The BER performance curve is given by [5]:

" The probability of error for generalized M-ary Orthogonal signaling using coherent demodulation is given by:

$$P_e = 1 - P_{c1} = 1 - \frac{1}{\sqrt{2\pi}} \int_{-\frac{S_{01}}{N_0}}^{\infty} \left[2\left(1 - Q\left\{ z + \sqrt{2\,\frac{E_b}{\eta}} \right\}\right) \right]^{\frac{M}{2}-1} \exp\left\{ -\frac{z^2}{2} \right\} dz$$

This integral cannot be solved in closed form, and numerical integration must be used. There are error rate extensions for differential decoding and descrambling that are also to be accounted for. This is done in a MATHCAD environment and is displayed in graphical format below.

1.1 1000 byte PER vs. Es/No



The reference PER is specified as 8% . The corresponding Es/No (signal to noise ratio per symbol) is 16.4 dB. The Es/No required to achieve the desired BER with maximum system implementation losses is 18.4 dB. The minimum processing gain is again, 10 dB, therefore:

$$G_p = \left(\frac{E_s}{N_o}\right)_{output} + \left(\frac{J}{S}\right) + L_{system} = 16.4dB + 2.0dB + \left(\frac{J}{S}\right) \geq 10dB$$

$$G_p = 18.4\,dB + \left(\frac{J}{S}\right) \geq 10dB$$

The minimum jammer to signal ratio is as follows:

$$\left(\frac{J}{S}\right) \geq -8.4\,dB$$

For the case of the HFA3861A, the bit rates are 1, 2, 5.5, and 11 Mbps. The corresponding symbol rates are 1, 1, 1.375, and 1.375 MSps. The chip rate is always 11 MCps, so the ratio of chip rate to symbol rate is 11:1 for the 1 and 2 Mbps rates and 8:1 for the 5.5 and 11 Mbps rates. Since the symbol rate to bit rate is less than 10 for the higher rates, we supply the theoretical processing gain calculation for these cases where spread spectrum processing gain with embedded coding gain is utilized. This is reasonable in that they cannot be separated in the demodulation process. If a separable FEC coding scheme were used, we would not be comfortable making this assertion.

As can be seen from the curve of figure 1, the Es/N0 is 16.4 dB at the PER of 8%. This PER can be related to a BER of 1e-5 on 1000 byte packets. With 8 bits per symbol, the Eb/N0 is then 7.4 dB or 9 dB less than the Es/N0. It is well known that the Eb/N0 of BPSK is 9.6 dB for 1e-5 BER, so therefore the coding gain of CCK over BPSK is 2.2 dB. We add this to the processing gain of 9 dB to get 11.2 dB overall processing gain for the CW jammer test.

Taking the calculations above, if the $\left(\frac{J}{S}\right) \geq -8.4\,dB$ then the equipment passes the CW jamming test.