STI – Lock Module

Theory of Operations

The RF Lock Module consists of two separate transmission methods that are user-selected by pressing buttons on the device.
The first method of transmission (PRU Reset) is frequency agile circuitry that dynamically selects one of two possible fixed channels for data transmission in the 433.92MHz amateur band at 433.28MHz and 434.56MHz. It has a directly modulated UHF oscillator, utilizing FSK transmission at data rates of approximately 25kbaud with +/-100kHz FM deviation. It has a very low power output (using only emission from the PCB components themselves) and is only meant to be used at a very short range. The "on-time" for this transmission is less than 7ms.
The second method of transmission (PID Reset) is fixed frequency circuit that uses a ferrite core element to emanate an 800kHz non-modulated carrier. It has a very low power output, and is only meant to be used at a very short range. The "on-time" for this transmission is less than 50ms.

The module uses a 9VDC alkaline style battery as a power source, which is internally regulated to +5VDC and +18VDC for device operation.

The sections below briefly detail the operations of major block components.

Local Oscillators:
X1 and X3 form a pair of switched CMOS NAND gate (U9) oscillators. U9A-1 and U9C-9 are the control pins to the individual oscillators. The base frequencies of operation (TP14) are 6.77MHz and 6.79MHz.
U1 is an RF oscillator with a built-in times-64 PLL functionality. The base frequencies of oscillation are used as references to lock the RF oscillation. U1 uses a resonant inductive tank (L4, L5) to produce a times-32 RF oscillation that is then doubled and amplified (TP1) to approx. -2dBm. The final output frequencies from U1 are 433.28MHz and 434.56MHz.
Components C34, C99 and R1 are the PLL loop filter components. This loop is "turbo-charged" under microprocessor control to greatly increase its lock time. Components Q11, R96, R93 and R104 form a "charge-pump" arrangement to quickly boost the PLL loop filter voltage up to its proper operating point. This saves on total "up-time", thus increasing battery life expectancy. Op-amp U15 buffers the PLL loop voltage and amplifies a three-stage, windowed view of it to allow the microprocessor increased resolution in setting the operating point.
Components C3 and L1 match the RF oscillator output to 50ohms.

+5VDC Supply:
U7 is a linear low-dropout regulator that provides a regulated +5VDC for system operation.

Ref Oscillator, RF Oscillator, & 800kHz Osc Power:
There are three switch-able power subsystems operating on the module to provide power to separate stages only when needed, thus conserving battery life.
The "Ref Oscillator" switch (R91, R71, C105 and Q1) enables the local oscillators upon power-up, and provides a turn-off delay upon "power-down", insuring that they are stable for microprocessor operation. This also provides power for U15 in the RF Oscillator.
The "RF Oscillator" power is controlled by a low-dropout linear regulator (U2) and components: C101, C125, C10 and R3. This provides a stable +3.5VDC to the RF Oscillator circuitry, providing it immunity to momentary dips or noise in the system's +5VDC power supply.
The "800 kHz Osc" switch uses U8 to provide a stepped-up +18VDC supply for the ferritre core element.

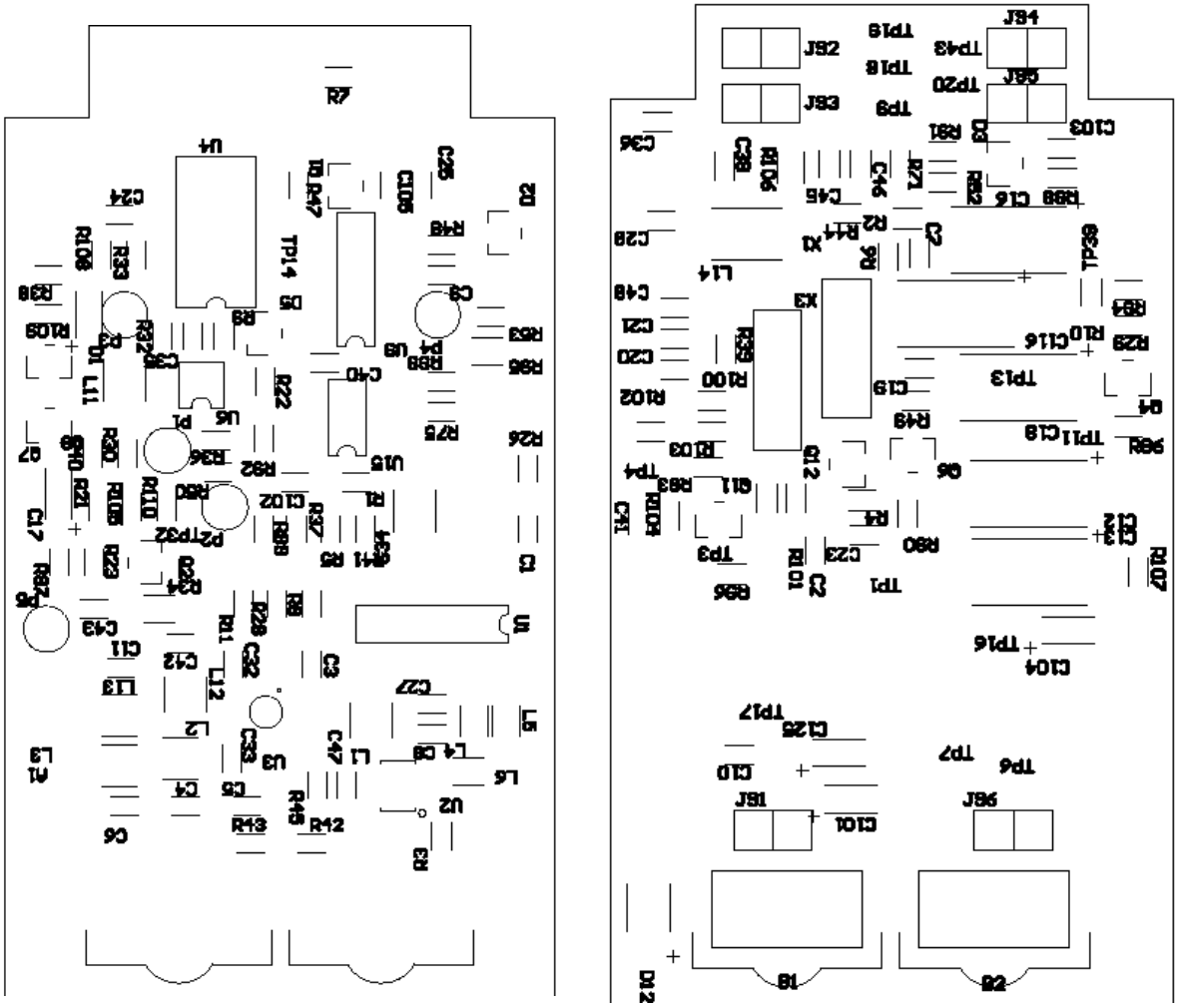
Wake-Up & Go to Sleep Circuitry:
User operated switches (SW1, SW2) enable the unit by turning on a p-channel MOSFET device for a pre-determined period of time, after which the unit goes to sleep to conserve battery life.

Microprocessor:
U4 is the controlling microprocessor that selects the operating channel and generates the data packets for transmission to the PRU. The local oscillators provide the operating frequency for U4.

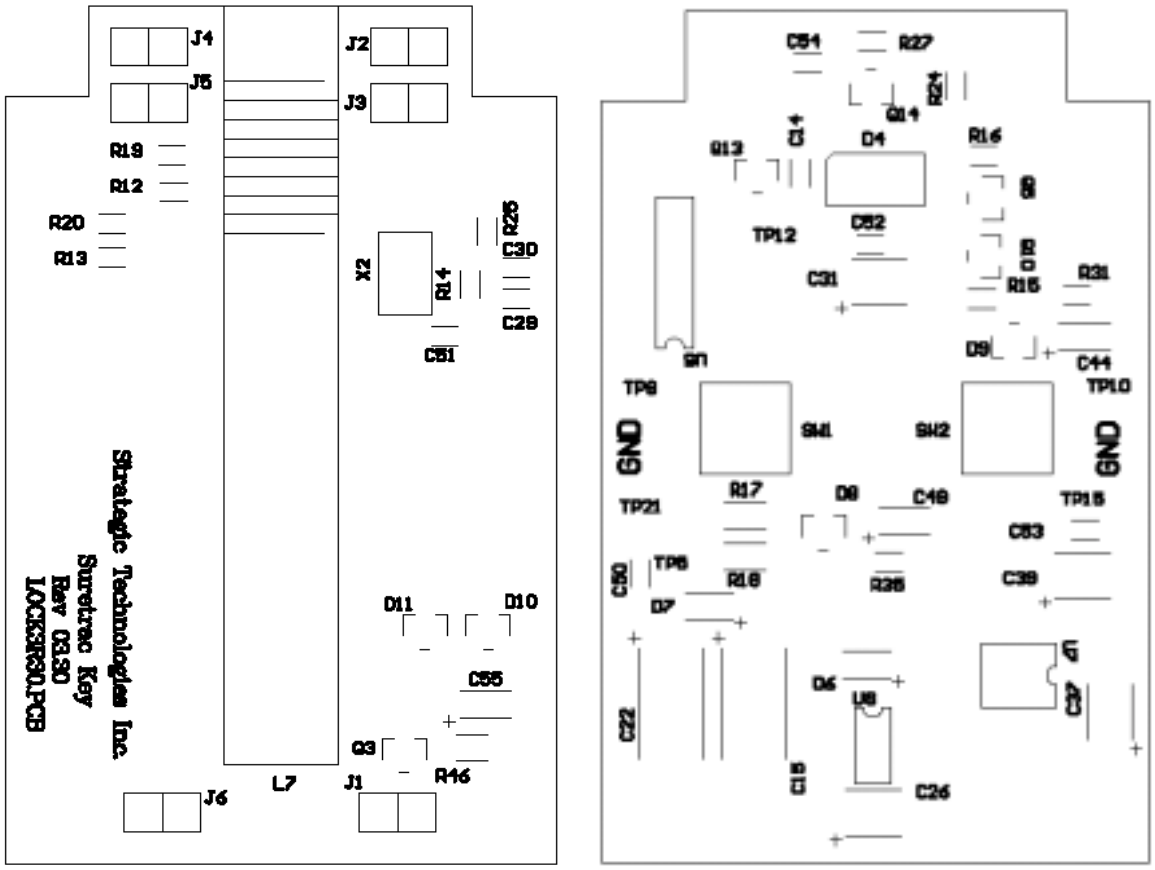
800kHz Oscillator:
X2is a cermaic resonator which forms a switched CMOS NAND gate (U5) oscillators. This oscillator drives the gate of n-channel MOSFET (Q13)

Ferrite Element:
L7 is a wire-wound ferrite element which is used to switch +18VDC at 800kHz frequency. This element provides the transmission means for this signal.

Lock Lower PCB – Bottom & Top Sides



Lock Upper PCB – Bottom & Top Sides



Lock Block Diagram